Power Supply Decoupling Capacitor Selection

nWP-030

White Paper

v1.1

Contents

Revision history

Date	Version	Description
September 2018	1.1	Updated nRF52840 capacitor selection on page 12
December 2017	1.0	First release (for nRF52840)

1 Introduction

The purpose of decoupling is to provide clean, noise-free power supplies for SoC-internal power rails. Internal regulators are stabilized for a given capacitance and interaction between regulator modes relies on decoupling capacitors.

Power supply decoupling capacitors must be selected with care to ensure sufficient effective capacitance for the nRF power system, because insufficient capacitance can cause instability and malfunction in power system operation mode engine. The effective capacitance of chip capacitors may only be a small fraction of the marked nominal value. There are several factors that may reduce effective capacitance beyond the specified tolerance in operation conditions, the most common ones being temperature coefficient, DC bias, and AC bias.

Nonideal characteristics are most pronounced in small, low-profile, and therefore high-density multilayer ceramic capasitors (MLCC). In small footprint designs, where the area is restricted, extra care must be taken to attain proper decoupling for nRF power supplies.

2 Selecting a decoupling capacitor

This is a summary of the issues to consider when looking for a decoupling capacitor to suit your application.

1. Choose your initial decoupling capacitor parameters to fit your application.

   Consider the following:

   - Preferred capacitor physical size – 0402, 0603
   - Ceramic material – X5R, X7R, or similar
   - Tolerance – Preferably ±10 %
   - Voltage rating appropriate to the supply
2. Study the intended capacitor datasheets, ask vendors, or download a tool to extract capacitor characteristics, paying attention to capacitance stability.
   a) Ensure sufficient rejection to DC bias.
   b) Attain effective capacitance at a low AC voltage value.
      - <50 mV AC rms
   c) Check temperature curve together with AC and DC bias in the application temperature range.
3. Extract minimum and maximum effective capacitance.
4. Iterate to find the capacitor that best suits your application.

3 Capacitor characteristics

Monolithic multilayer ceramic capacitors (MLCC) are commonly used for decoupling purposes because they are polarity-free, have low impedance, and are compact in various capacitance and package sizes.

The capacity density of ceramic capacitors has been improved to provide the smallest packages with a sufficient level of decoupling capacitance. In recent years, manufacturers have developed dielectrics so that even 10 µF capacitors can be found in 0402 packages up to 6.3 V in rated voltage.

However, the increased density means complications in capacitor characteristics. There are several factors that can have a significant impact on the effective capacitance of a decoupling capacitor in an application, the most significant ones being DC bias, AC bias, and temperature.

3.1 DC bias

The effective capacitance of ceramic capacitors typically decreases with added DC bias.

DC bias dependency is quite well-known and documented in capacitor datasheets. It has a clear relationship with capacitor density. There is a tendency for small packages with high marked nominal capacitance to degrade quickly when DC bias is applied. It might not become a significant problem in low-voltage supplies such as 1.3 V, but it can have a remarkable impact at 3.3 V.

The following graph shows the DC bias curves for the capacitors. The graph is created using the free Murata SimSurfing tool.

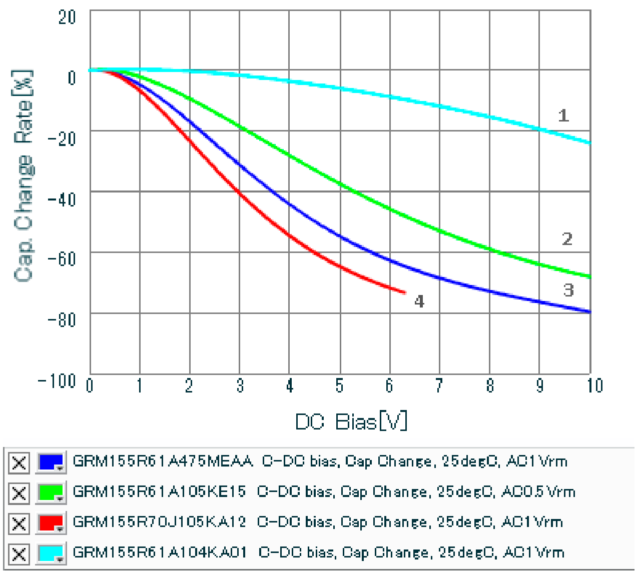

Figure 1: Typical capacitance changes vs. DC bias

The following table lists the Murata general purpose capacitors that are evaluated in terms of DC bias:

Line nr	Part number (graph color)	Value	Type/Size	Voltage	Capacitance change at 3 V
1	GRM155R61A104KA01 (cyan)	100 nF	X5R/0402	10 V	−3%
2	GRM155R61A105KE15 (green)	1.0 µF	X5R/0402	10 V	−20%
3	GRM155R61A475MEAA (blue)	4.7 µF	X5R/0402	10 V	−30%
4	GRM155R70J105KA12 (red)	1.0 µF	X7R/0402	6.3 V	−40%

- The density of the X5R 100 nF capacitor is fair compared to that of the 1 µF and 4.7 µF capacitors, and therefore DC bias does not influence effective capacitance on the low end of the voltage range.
- The X5R 1 µF capacitor has a moderate effect on DC bias and would present almost all of the capacitance at 1.3 V but degrades to −20 % at 3 V bias.
- The X5R 4.7 µF capacitor could be considered for decoupling higher voltage pins. However, the tool reveals that effective capacitance is reduced by 30 % because of the DC bias dependency at 3 V.
- The X7R 1.0 µF capacitor has the highest DC bias dependency. It could still be considered a capacitor to decouple lower voltage pins operating at 1.3 V, for instance, as the degradation is less than 10 % at this low voltage.

3.2 AC bias

A very pronounced unideal characteristic in high-density ceramic capacitors is AC voltage dependency. As the effect is inherited by high dielectric materials, all high-density ceramic capacitors suffer from it to some extent.

This phenomenon is based on the fact that in dielectric material, all the ions may not change polarity uniformly in a weak alternating electric field, as if the AC signal were small. With higher excitation they turn polarity concentrically, inducing effective capacitance to the nominal capacity of the capacitor.

Section 4.7 in the *JIS C 5101-1, 1998* standard defines 1 kHz 1 V_{rms} AC signal for measuring nominal capacitance. However, from the decoupling point of view, 1 V_{rms} is too high for the application, as the voltage ripple is typically intended to be below 10 mV RMS in supply rails. Therefore, it is more valid to evaluate capacitance at a low AC test signal. Unfortunately, AC voltage dependency is poorly documented among manufacturers, but Murata and Samsung, for example, have tools which can be used to evaluate the effect.

Murata SimSurfing was used to plot the four capacitors listed in DC bias on page 6 over AC voltage. See the figure below for the resulting plot.

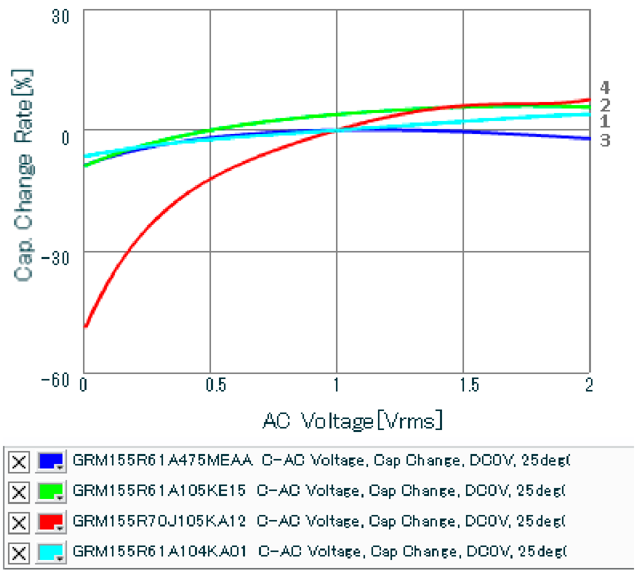

Figure 2: Capacitance change over applied AC voltage

The following table lists the Murata general purpose capacitors that are evaluated in terms of AC bias:

Line nr	Part number (graph color)	Value	Type/Size	Voltage	Capacitance change at 10 mV_{rms} AC
1	GRM155R61A104KA01 (cyan)	100 nF	X5R/0402	10 V	−7%
2	GRM155R61A105KE15 (green)	1.0 µF	X5R/0402	10 V	−10%
3	GRM155R61A475MEAA (blue)	4.7 µF	X5R/0402	10 V	−10%
4	GRM155R70J105KA12 (red)	1.0 µF	X7R/0402	6.3 V	−50%

The X7R 1 µF (red line, nr 4) performs very poorly with the small AC signal. The effective capacitance has dropped to almost half of the nominal value. Even if this capacitor is considered for REG1 decoupling when examining DC bias dependency in DC bias on page 6, the AC bias dependency clearly rules it out as insufficient.

The three other capacitors shown in the graph have a moderate effect on AC bias and they are also relatively stable in DC bias. They could be regarded as acceptable in decoupling but there is still the temperature coefficient to be examined. For more information, see Temperature on page 8.

The temperature coefficient, defined by a standard measurement setup, can differ substantially from a coefficient extracted with both AC and DC bias included in a temperature sweep.

3.3 Temperature

Ceramic capacitors are classified based on their temperature range.

The X5R capacitor, for example, is intended for temperatures ranging from −55 to +85°C, while in the X7R capacitor, the range is extended to temperatures between −55 and +125°C. These capacitors are temperature-compensated meaning that their capacitance is within ±15 % of the full temperature range.

However, this specification does not guarantee that effective capacitance falls within the range when operating outside standard AC and DC bias measuring conditions. As already discussed, application-defined operating conditions, supply decoupling denoted DC, and AC bias conditions in particular, are well outside the standard measurement setup.

Below, the general-purpose Murata GRM155R70J105KA12 1 µF X7R 0402 6.3 V capacitor is illustrated with respect to temperature as plotted by the Murata SimSurfing tool.

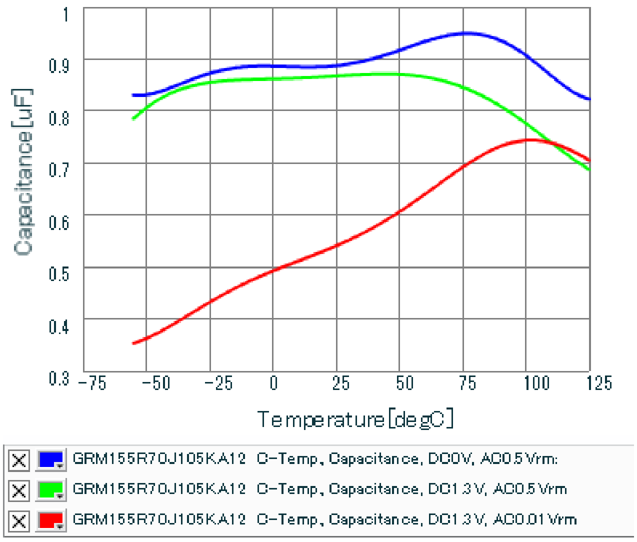

Figure 3: GRM155R70J105KA12: Capacitance over temperature in different operating conditions

In the figure above, the top line (in blue) denotes capacitance over temperature with a high AC signal without DC bias. It is fairly stable.

The middle line (in green) indicates an added DC bias of 1.3 V. The degradation in capacitance correlates with what was found in the DC bias study, and it has no significant second order effect. See DC bias on page 6.

The lower line (in red) uses the test signal of 10 mV AC RMS and, as indicated in the graph, the minimum capacitance has dropped by 60 % at −40°C. Eventually, this capacitor would be insufficient for decoupling purposes.

The same practice was carried out for GRM155R61A105KE15 1 µF X5R 0402 10 V for comparison. See the following figure.

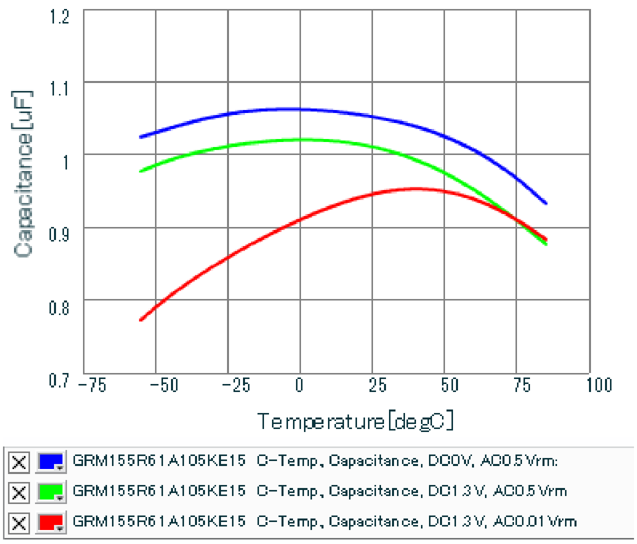

Figure 4: GRM155R61A105KE15: Capacitance over temperature in different operating conditions

In this case, the X5R performs much better over temperature if set to the operation point of 10 mV AC RMS and 1.3 V DC bias. The minimum capacitance of 0.82 µF can be seen from the red curve, including all three dependency aspects.

4 nRF52840

The guidelines and examples presented here help in evaluating the optimal decoupling capacitors for the nRF52840 SoC power supplies.

4.1 nRF52840 decoupling

The nRF52840 SoC includes integrated regulators that depend on off-chip decoupling capacitors.

These internal regulators and the cooperation between them and external regulators are designed for a given capacitance value. Insufficient or vulnerable capacitance can impact system stability and functionality.

The nRF52840 SoC features two battery inputs. It can be supplied either from the **VDDH** supply in high voltage (HV) mode, or from the **VDD** supply in normal voltage mode.

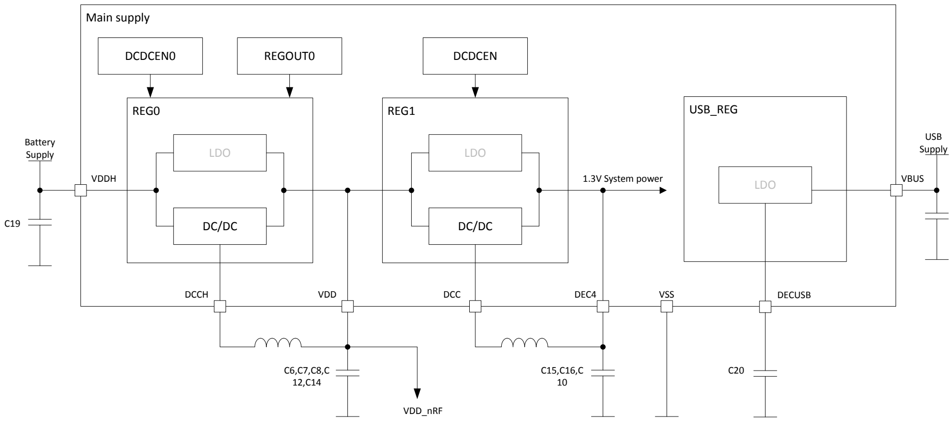

Figure 5: nRF52840 power system, high voltage mode

If supplied from the **VDDH** supply, there are two power stages in series down from the battery to 1.3 V system power. The **VDD** supply is internally regulated in REG0, and the decoupling capacitors are **C6**, **C7**, **C8**, **C12**, and **C14**. **DEC4** is output from REG1, and the decoupling capacitors are **C15** and **C16**. See reference design in nRF52840 capacitor selection on page 12.

For USB use there is an internal regulator, USB_REG, which is decoupled by capacitor **C20**.

In normal voltage mode, the **DEC4** pin is a regulator output while **VDD** is the input supply pin. Both must be decoupled, and **DEC4** must be according to the regulator requirement.

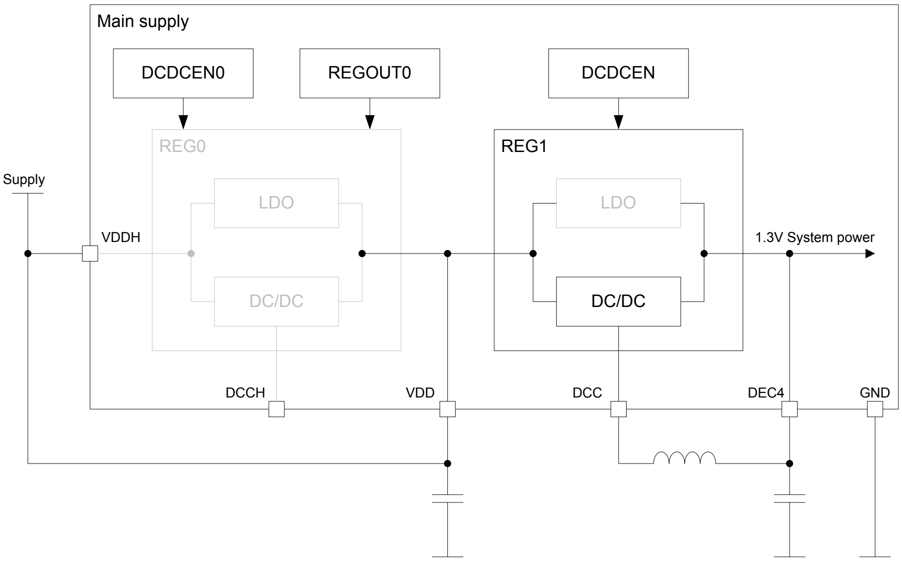

Figure 6: nRF52840 power system, normal voltage mode

For more information, see nRF52840 Product Specification.

4.2 nRF52840 capacitor selection

In the schematic design for the application, it is important to select decoupling capacitors with sufficient efficient capacitance for decoupling.

When designing the decoupling of the nRF52840 device, the following must be considered.

- Low voltage (LV) mode – DEC4 decoupling
- High voltage (HV) mode – VDD and DEC4 decoupling
- USB regulator – DECUSB decoupling

where:

- DEC4 operates at 1.3 V.
- VDD operates between 1.8 V and 3.3 V depending on voltage programming.
- DECUSB operates at 3.3 V.

The capacitor characteristics should be evaluated with respect to the dependencies examined in Capacitor characteristics on page 6.

The nRF52840 SoC can be used in various configurations depending on which power inputs are in use. The most comprehensive configuration is the one in which the REG0 stage is used to down-regulate VDDH voltage to VDD. The USB regulator feature is enabled as the **DECUSB** pin is decoupled and **VBUS** is connected.

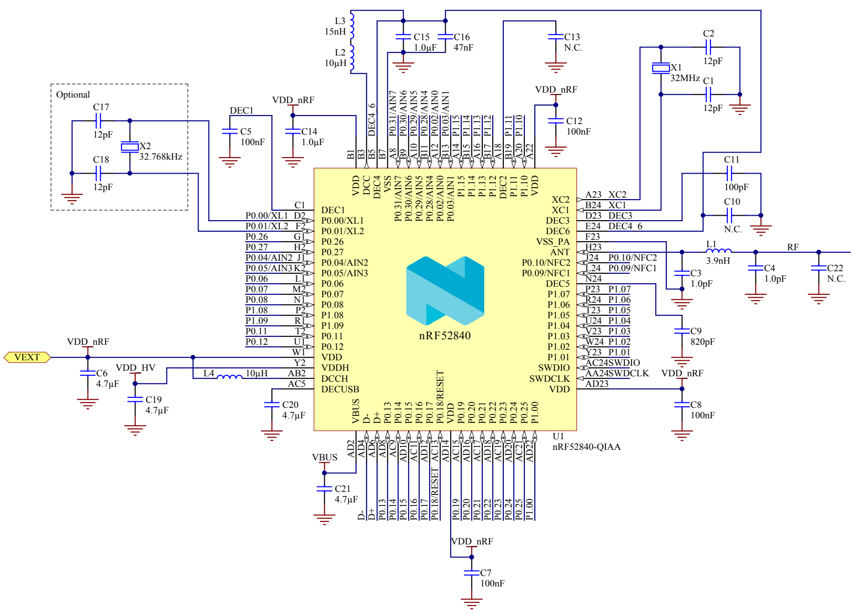

Figure 7: nRF52840 circuit configuration

For more information on nRF52840 reference circuitry, see nRF52840 Product Specification.

4.2.1 VDD

VDD is the global supply for the chip and it is decoupled on each corner to provide a clean, common power supply into the nRF52840 SoC.

In the nRF52840 reference design schematic, the SoC is supplied from **VDDH**, and **VDD** is the output for REG0 regulators connected to the net referred to as VDD_nRF in the schematic. There are five placeholders, **C6**, **C7**, **C8**, **C12**, and **C14** for decoupling the VDD_nRF. The nominal capacitance value is 4.7 µF. For the minimum and maximum effective capacitance specification, see nRF52840 effective capacitance specification on page 16.

As decoupling is distributed around the SoC, the total capacitance can consist of several combinations. The following are some examples of these:

- 2 × 2.2 µF + 3 × 100 nF
- 4 × 1 µF + 1 × 100 nF
- 5 × 1 µF
- 1 × 4.7 µF + 1 × 1 µF + 3 × 100 nF

4.2.2 DECUSB

DECUSB is an output for the internal USB regulator that regulates the VBUS down to 3.3 V to provide a power supply for the USB peripheral.

The supply is decoupled by **C20** in nRF52840 circuit configuration on page 13. The nominal capacitance value is 4.7 µF. For the minimum and maximum effective capacitance specification, see nRF52840 effective capacitance specification on page 16.

4.2.3 DEC4

DEC4 in the nRF52840 SoC is the 1.3 V output for REG1 regulators.

See nRF52840 circuit configuration on page 13.

It has three placeholders, **C15**, **C16**, and **C10**. **C15** shall be 1 µF and **C16** 47 nF. **C10** is a placeholder for a small radio decoupling capacitor, and it is not taken into account in regulator decoupling. For the minimum and maximum effective capacitance specification, see nRF52840 effective capacitance specification on page 16.

4.2.4 Example: Decoupling REG0 with 0603

If the application can fit a 0603 package which is up to 0.9 mm in height, the starting point for the VDD_nRF decoupling could be 2 × 2.2 µF + 3 × 100 nF.

The following are some 2.2 µF capacitors from the SimSurfing listing that appear to be suitable for development. Capacitance has been plotted over temperature with applied DC bias 3 V and AC bias 10 mV. The tool provides insight into details as illustrated below.

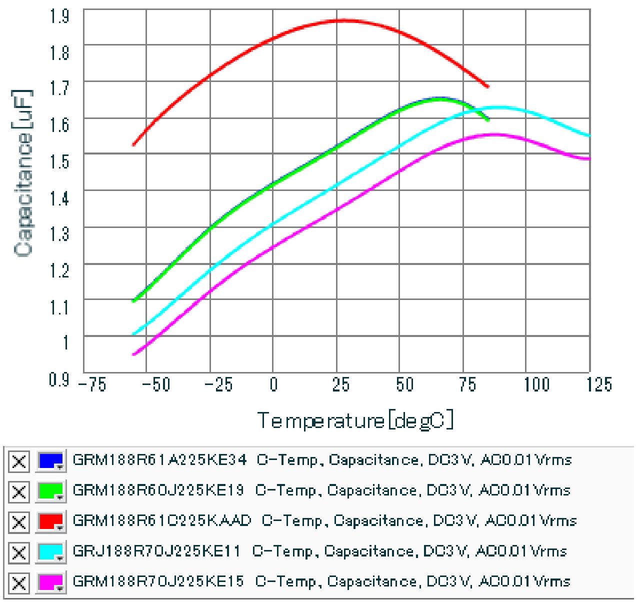

Figure 8: Temperature sweep of various 0603 2.2 µF capacitors in operating condition

The results show that, in terms of variation, the GRM188R61C225KAAD capacitor (red, top line) in the 0603 2.2 µF category is the best choice. Effective capacitance is approximately the minimum 1.65 µF between −40 and +85°C. The result is 3.3 µF when connecting two capacitors in parallel. With the assumption that 100 nF capacitors are ideal, the range can be deduced to attain 3.6 µF, whereas the nominal is exactly 4.7 µF. By multiplying the nominal value by a 10% tolerance, the maximum capacitance can be roughly estimated to be 5.2 µF. This would be a sufficient combination for VDD_nRF decoupling.

4.2.5 Example: Decoupling REG0 with 0402

In this example, the area available in the application is restricted, and therefore the 0402 package has been used.

Some initally suitable 2.2 µF capacitors were selected from the SimSurfer listing, and plotted capacitance over temperature with applied DC bias 3 V and AC bias 10 mV. The SimSurfer promptly indicates that, in general, 2.2 µF capacitors in 0402 are very unstable, and therefore not suitable for decoupling VDD in the nRF52840 SoC.

The capacitor GRM155R61A105KE15 1 µF X5R 0402 10 V in GRM155R61A105KE15: Capacitance over temperature in different operating conditions on page 10 showed an approximate minimum of 0.73 µF for temperatures between −40°C and +85°C with added DC and AC bias. In the following figure, the capacitor is examined with 3 V DC bias appropriate for VDD decoupling:

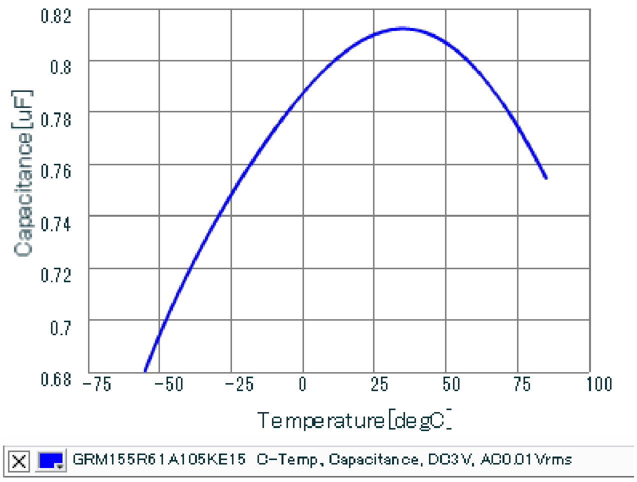

Figure 9: Temperature sweep of a GRM155R61A105KE15 1 µF capacitor 3 V DC bias and 10 mV AC bias

The effective capacitance in this capacitor is not reduced by the increased DC bias to a significant extent, as it remains over 0.71 µF with temperatures ranging from −40°C to +85°C. It is possible to use all five decoupling capacitor placeholders for this capacitor to attain a minimum effective capacitance of 0.71 µF × 5 = 3.65 µF with a nominal value of 5 µF. The same GRM155R61A105KE15 capacitor would also fit the REG1 decoupling.

4.2.6 Example: Decoupling USB regulator with 0603

This example shows how to find a single 0603 capacitor that is suitable for decoupling **DECUSB**. The nominal capacitance specified for **DECUSB** is 4.7 µF and the operating voltage in the supply is 3.3 V.

Some initally suitable 4.7 µF capacitors have been selected from the SimSurfer listing, and then capacitance has been plotted over temperature with applied DC bias 3.3 V and AC bias 10 mV.

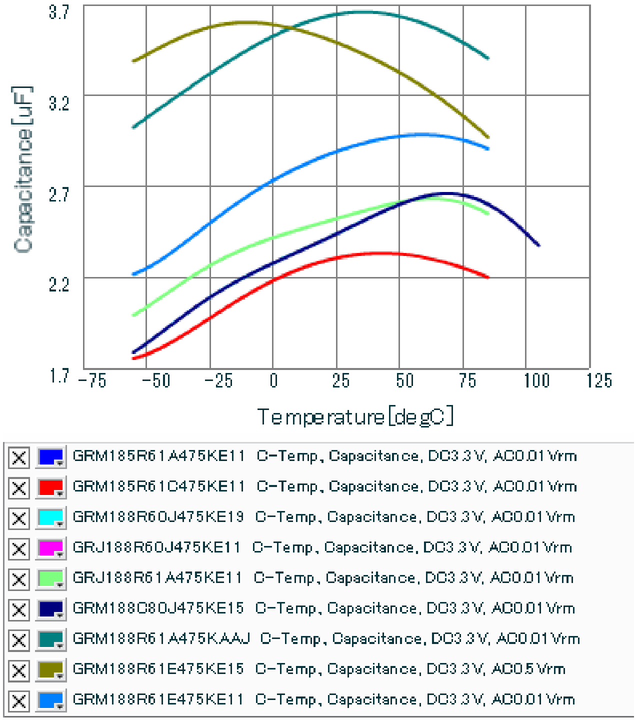

Figure 10: Various 0603 4.7 uF capacitors over temperature in operation point for USB regulator

A majority of capacitors would not have fulfilled the minimum capacitance specification of 2.35 µF but GRM188R61A475KAAJ, GRM188R61E475KE15, and GRM188R61E475KE11 were found to possess decent characteristics for the purpose. The thickness of these capacitors is 0.95 mm–1.0 mm while the others were 0.55 mm–0.9 mm.

If the thickness, or even the size 0603, is unfeasible in the application, **DECUSB** can also be decoupled by instantiating multiple smaller capacitors in parallel.

4.3 nRF52840 effective capacitance specification

The effective capacitance specification for nRF52840 consists of minimum, typical, and maximum values per each supply. Typical value is the target for nominal capacitance to be assembled on an application schematic. The minimum and maximum values denote the range in which the total effective capacitance must stay under all operating conditions as addressed in this white paper.

Symbol	Description	Effective capacitance			
		Min	Typ	Max	Unit
C_{VDD}	Effective capacitance in VDD	2.7	4.7	5.5	µF
C_{DEC4}	Effective capacitance in DEC4	0.7	1	1.3	µF
C_{DECUSB}	Effective capacitance in DECUSB	2.35	4.7	5.5	µF

Table 1: nRF52840 effective capacitance specification

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