nRF9160

Revision 2

Errata

v1.0

NORDIC® SEMICONDUCTOR

Contents

1 nRF9160 Revision 2 Errata

This Errata document contains anomalies for the nRF9160 chip, revision Revision 2 (SICA-B1A, SIBA-B1A, SIAA-B1A).

The document indicates which anomalies are fixed, inherited, or new compared to revision Revision 1.

2 Revision history

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nRF9160 Revision 2 v1.0	21.09.2020	• Added: No. 1. “Excessive power consumption after using STOP task” • Added: No. 2. “CPU code execution from RAM halted during flash page erase operation” • Added: No. 4. “Bits in GPIO LATCH register are incorrectly set to 1” • Added: No. 6. “SLEEPENTER and SLEEPEXIT events asserted after pin reset” • Added: No. 7. “Subsequent accesses between info_mem and main_mem of the flash may not work properly” • Added: No. 9. “Reduced SFDR” • Added: No. 15. “Supply regulators default to LDO mode after reset” • Added: No. 21. “Disabling instruction cache causes skip of next instruction” • Added: No. 23. “TASKS_RESUME impacts UARTE” • Added: No. 24. “CPU is not halted for page erase in debug session” • Added: No. 26. “System locks up when set in System ON IDLE while waiting for EVENTS_LFCLKSTARTED” • Added: No. 28. “Events are not generated when switching from scan mode to no-scan mode” • Added: No. 29. “System reset does not work” • Added: No. 30. “False SEQEND[0] and SEQEND[1] events are generated” • Added: No. 31. “LFXO startup fails” • Added: No. 32. “Debug power-up request is not acknowledged” • Added: No. 33. “Non-secure code can detect secure events”

3 New and inherited anomalies

The following anomalies are present in revision Revision 2 of the nRF9160 chip.

ID	Module	Description	Inherited from Revision 1
1	I2S	Excessive power consumption after using STOP task	X
2	NVMC	CPU code execution from RAM halted during flash page erase operation	X
4	GPIO	Bits in GPIO LATCH register are incorrectly set to 1	X
6	POWER	SLEEPENTER and SLEEPEXIT events asserted after pin reset	X
7	KMU	Subsequent accesses between info_mem and main_mem of the flash may not work properly	X
9	SAADC	Reduced SFDR	X
15	REGULATORS	Supply regulators default to LDO mode after reset	X
21	NVMC	Disabling instruction cache causes skip of next instruction	X
23	UART	TASKS_RESUME impacts UARTE	X
24	NVMC	CPU is not halted for page erase in debug session	X
26	CLOCK, LFXO	System locks up when set in System ON IDLE while waiting for EVENTS_LFCLKSTARTED	X
28	SAADC	Events are not generated when switching from scan mode to no-scan mode	X
29	Debug and Trace	System reset does not work	X
30	PWM	False SEQEND[0] and SEQEND[1] events are generated	X
31	LFXO	LFXO startup fails	X
32	Debug and Trace	Debug power-up request is not acknowledged	X
33	DPPI	Non-secure code can detect secure events	X

Table 1: New and inherited anomalies

3.1 [1] I2S: Excessive power consumption after using STOP task

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

Current consumption too high (~900 µA) after using the STOP task.

Conditions

I2S was running and was stopped by triggering the STOP task.

Consequences

Current consumption higher than specified.

Workaround

Apply the below code after the STOP task. For secure mode:

```
*((volatile uint32_t *)0x50028038) = 1;
*((volatile uint32_t *)0x5002803C) = 1;
```

For non-secure mode:

```
*((volatile uint32_t *)0x40028038) = 1;
*((volatile uint32_t *)0x4002803C) = 1;
```

3.2 [2] NVMC: CPU code execution from RAM halted during flash page erase operation

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

The CPU gets stalled when executing code from RAM.

Conditions

Executing code from RAM while the NVMC is performing flash erase operation.

Consequences

The CPU is halted for the time it takes the NVMC to perform the erase in flash. See the NVMC electrical specification for time details.

Workaround

None.

3.3 [4] GPIO: Bits in GPIO LATCH register are incorrectly set to 1

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

The GPIO.LATCH[n] register is unexpectedly set to 1 (Latched).

Conditions

Set GPIO.PIN_CNF[n].SENSE at low level (3) at the same time as PIN_CNF[n].INPUT is set to Connect (0).

Consequences

The GPIO.LATCH[n] register is set to 1 (Latched). This could have side effects, depending on how the chip is configured to use this LATCH register.

Workaround

Always configure PIN_CNF[n].INPUT before PIN_CNF[n].SENSE.

3.4 [6] POWER: SLEEPENTER and SLEEPEXIT events asserted after pin reset

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

NRF_POWER->EVENT_SLEEPENTER and NRF_POWER->EVENT_SLEEPEXIT are asserted.

Conditions

After device reset.

Consequences

NRF_POWER->EVENT_SLEEPENTER and NRF_POWER->EVENT_SLEEPEXIT registers are set to true after reset.

Workaround

After reset, NRF_POWER->EVENT_SLEEPENTER and NRF_POWER->EVENT_SLEEPEXIT must be cleared before enabling them as IRQ sources.

3.5 [7] KMU: Subsequent accesses between info_mem and main_mem of the flash may not work properly

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

Expected CPU read operation to flash main memory area never happens.

Conditions

Two back to back consecutive CPU read operations to flash, where the first read is to the flash UICR info page, and the second read is to flash main memory area.

Consequences

The read operation results in undefined behavior.

Workaround

Add a data synchronization barrier (DSB) operation between the two consecutive CPU read operations, in cases where the first read is to the flash UICR info page, and the second to the flash main memory area.

```
uint32_t a = UICR_S->SOMEREGISTER;
__DSB();
uint32_t b = *((uint32_t *)SOMEFLASHADDR);
```

3.6 [9] SAADC: Reduced SFDR

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

Reduced SFDR on SAADC.

Conditions

DC/DC refresh mode.

Consequences

Typical SFDR reduced to 60 dBc in DC/DC refresh mode.

Workaround

Set register as below. For secure mode:

```
*((volatile uint32_t *)0x50004A38) = 0;
```

For non-secure mode:

```
*((volatile uint32_t *)0x40004A38) = 0;
```

3.7 [15] REGULATORS: Supply regulators default to LDO mode after reset

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

Regulators staying in LDO mode causes higher current consumption.

Conditions

Startup from reset.

Consequences

1. The device current consumption will be higher. Exactly how much higher depends on the difference in efficiency in DC/DC and LDO regulators at a given supply level and the current draw of the device.
2. The device is qualified using DC/DC converters. Qualifications and certificates created without DC/DC converters will hence be void.

Workaround

Application software needs to set the regulators into DC/DC mode before starting up the modem. Set register at startup as described below. For secure mode:

```
NRF_REGULATORS_S->DCDCEN = REGULATORS_DCDCEN_DCDCEN_Enabled <<
 REGULATORS_DCDCEN_DCDCEN_Pos;
```

For non-secure mode:

```
NRF_REGULATORS_NS->DCDCEN = REGULATORS_DCDCEN_DCDCEN_Enabled <<
 REGULATORS_DCDCEN_DCDCEN_Pos;
```

Note: Workaround included as of MDK 8.21.1 and later releases.

3.8 [21] NVMC: Disabling instruction cache causes skip of next instruction

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

The CPU skips first instruction after instruction cache is disabled.

Conditions

The code executes instructions to disable the instruction cache.

Consequences

The program does not execute as expected.

Workaround

Use the following function to disable instruction cache:

```
_attribute_((aligned(ICACHE_LINE_SIZE)))

void icache_disable(void) {
    int key = DisableInterrupts();
    __ISB();
    NRF_NVMC->ICACHECNF = 0;
    __ISB();
    EnableInterrupts(key);
}
```

3.9 [23] UART: TASKS_RESUME impacts UARTE

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

Issuing TASKS_RESUME results in bit(s) being set in the UARTE ERRORSRC register after it is enabled, even when not started.

Conditions

The internal state of a disabled UARTE changes when any of the tasks TASKS_RESUME, TASKS_STARTRX, and TASKS_STARTTX is triggered. These tasks are shared by UARTE, TWIM, TWIS, and SPIM.

Consequences

UARTE will start transmitting immediately after being enabled.

Workaround

Depending on which UARTE instance is affected, apply the following steps before enabling UARTE.

- If TXENABLE reads '1', trigger TASKS_STOPTX.
- If RXENABLE reads '1':

- Enable UARTE.
- Trigger TASKS_STOPRX.
- Wait until RXENABLE reads '0'.
- Clear ERRORSRC register.

The exact address depends on the UARTE instance. See the following table.

UARTE Instance	RXENABLE	TXENABLE
UARTE0:NS	0x40008564	0x40008568
UARTE0:S	0x50008564	0x50008568
UARTE1:NS	0x40009564	0x40009568
UARTE1:S	0x50009564	0x50009568
UARTE2:NS	0x4000A564	0x4000A568
UARTE2:S	0x5000A564	0x5000A568
UARTE3:NS	0x4000B564	0x4000B568
UARTE3:S	0x5000B564	0x5000B568

Table 2: Register addresses

3.10 [24] NVMC: CPU is not halted for page erase in debug session

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

Application core crashes during a debug session.

Conditions

- Debugger is connected.
- Debug system power request is triggered.
- Application core software executes NVM page erase.
- Debugger single steps page erase code.

Consequences

Debug session is interrupted due to the CPU crash.

Workaround

Avoid doing single steps or setting breakpoints around the execution of the NVM page erase instruction.

3.11 [26] CLOCK, LFXO: System locks up when set in System ON IDLE while waiting for EVENTS_LFCLKSTARTED

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

LFCLOCK is not precise after reset until LFXO is available.

Conditions

The LFXO is enabled and EVENTS_LFCLKSTARTED not received yet.

Consequences

Imprecise LFCLOCK may lead to system lockup while waiting for the LFXO to become available.

Workaround

Do not enter System ON IDLE in the period between writing TASK_LFCLKSTART= 1 and receiving EVENTS_LFCLKSTARTED. The startup time for the LFXO is stated in the electrical parameter t_{START_LFXO} in 32.768 kHz high accuracy oscillator (LFXO) in nRF9160 Product Specification.

Note: The LTE modem requires LFXO as LFCLK source.

3.12 [28] SAADC: Events are not generated when switching from scan mode to no-scan mode

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

SAADC stops working.

Conditions

- Switching from multiple channels to a single channel when BURST is disabled and acquisition time is <10 us
- Switching from multiple channels to a single channel when BURST is enabled

Consequences

SAADC internally locks up and does not generate the expected events.

Workaround

Execute the following code before changing the channel configuration.

- Secure mode:

```
NRF_SAADC_S->TASKS_STOP = 1;
```

- Non-secure mode:

```
NRF_SAADC_NS->TASKS_STOP = 1;
```

3.13 [29] Debug and Trace: System reset does not work

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

Debugger is unable to trigger a system reset through AIRCR.SYSRESETREQ.

Conditions

The CPU is running non-secure code and has set the AIRCR.SYSRESETREQ bit

Consequences

Reset request is ignored.

Workaround

Complete the following steps:

1. Halt the CPU through a connected debugger.
2. Force the processor into secure mode by setting DSCSR.SDS (see Register Specification in Arm®v8-M Architecture Reference Manual):

   ```
   SCB_DSCSR = (SCB_DSCSR &  ~(1 << 17)) | 1 << 16;
   ```

   This sets bit 17 (CDSKEY) to 0 to allow writes to CDS and bit 16 (CDS) to 1 to force secure execution.
3. Reset CPU through AIRCR.SYSRESETREQ (see Register Specification in Arm®v8-M Architecture Reference Manual).

   The system resets.

3.14 [30] PWM: False SEQEND[0] and SEQEND[1] events are generated

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

False SEQEND[0] and SEQEND[1] events are being generated.

Conditions

Any of the LOOPSDONE_SEQSTARTn shortcuts are enabled. LOOP register is nonzero and SEQ[1].CNT is set to 1.

Consequences

SEQEND[0] and SEQEND[1] events might falsely trigger other tasks if they are routed through the PPI.

Workaround

Avoid using the LOOPSDONE_SEQSTARTn shortcuts when the LOOP register is nonzero and SEQ[1].CNT is set to 1.

3.15 [31] LFXO: LFXO startup fails

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

LFXO does not start up.

Conditions

LFXO is set up in a wrong mode and unable to start up in all conditions.

Consequences

LTE modem does not work.

Workaround

Apply the following code after any reset:

```
*((volatile uint32_t *)0x5000470Cul) = 0x0;
*((volatile uint32_t *)0x50004710ul) = 0x1;
```

This workaround is implemented in MDK version 8.29.0.

3.16 [32] Debug and Trace: Debug power-up request is not acknowledged

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

In the CTRL/STAT register of the debug port (see *ARM CoreSight SoC-400 Technical Reference Manual, revision r3p2*):

- CDBGPWRUPREQ powers up the system but does not assert CDBGPWRUPACK.
- CSYSPWRUPREQ does not trigger any power requests but asserts CDBGPWRUPACK and CSYSPWRUPACK.

Conditions

Always when starting a debug session.

Consequences

If the debug probe writes the debug port CTRL/STAT.DBGPWRUPREQ and waits on CTRL/STAT.DBGPWRUPACK, it does not finish.

Workaround

When enabling debug domain power, write CTRL/STAT.DBGPWRUPREQ and CTRL/STAT.SYSPWRUPREQ.

3.17 [33] DPPI: Non-secure code can detect secure events

This anomaly applies to IC Rev. Revision 2, build codes SICA-B1A, SIBA-B1A, SIAA-B1A.

It was inherited from the previous IC revision Revision 1.

Symptoms

Non-secure code is able to detect that a secure event has been published to a secure DPPI channel.

Conditions

In a non-secure DPPI channel group, SUBSCRIBE_CHG[n].EN or SUBSCRIBE_CHG[n].DIS is setup to be connected to a secure DPPI channel.

Consequences

Non-secure code can detect that a secure event has been published to a secure DPPI channel. The non-secure code cannot detect which event has been published.

Workaround

Perform one of the following:

- Avoid using DPPI in secure mode.
- Configure all channel groups (CHG[n]) to include at least one DPPI channel that is configured as secure. This makes the channel groups secure and blocks them from being used on the non-secure side.

> **Note:** The non-secure domain can still use the DPPI tasks and events system, but it does not have any available channel groups.

4 Fixed anomalies

The anomalies listed in this table are no longer present in the current chip version.

For a detailed description of the fixed anomalies, see the Errata for revision Revision 1.

ID	Module	Description
27	CryptoCell	Arm CryptoCell true random number generator (TRNG) has wrong configuration

Table 3: Fixed anomalies