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nRF9160 Revision 1 Errata

This Errata document contains anomalies for the nRF9160 chip, revision Revision 1 (SICA-B0A). The document indicates which anomalies are fixed, inherited, or new compared to revision Engineering A.
# Change Log

See the following list for an overview of changes from previous versions of this document.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>nRF9160</td>
<td>03.03.2020</td>
<td>• Added: No. 32. “Debug power-up request is not acknowledged”</td>
</tr>
<tr>
<td>Revision 1 v1.3</td>
<td></td>
<td>• Added: No. 33. “Non-secure code can detect secure events”</td>
</tr>
<tr>
<td>nRF9160</td>
<td>15.11.2019</td>
<td>• Added: No. 28. “Events are not generated when switching from scan mode to no-scan mode”</td>
</tr>
<tr>
<td>Revision 1 v1.2</td>
<td></td>
<td>• Added: No. 29. “System reset does not work”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added: No. 30. “False SEQEND[0] and SEQEND[1] events are generated”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added: No. 31. “LFXO startup fails”</td>
</tr>
<tr>
<td>nRF9160</td>
<td>18.09.2019</td>
<td>• Added: No. 23. “TASKS_RESUME impacts UARTE”</td>
</tr>
<tr>
<td>Revision 1 v1.1</td>
<td></td>
<td>• Added: No. 24. “CPU is not halted for page erase in debug session”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added: No. 26. “System locks up when set in System ON IDLE while waiting for EVENTS_LFCLKSTARTED”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added: No. 27. “Arm CryptoCell true random number generator (TRNG) has wrong configuration”</td>
</tr>
<tr>
<td>nRF9160</td>
<td>28.05.2019</td>
<td>• Added: No. 1. “Excessive power consumption after using STOP task”</td>
</tr>
<tr>
<td>Revision 1 v1.0</td>
<td></td>
<td>• Added: No. 2. “CPU code execution from RAM halted during flash page erase operation”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added: No. 4. “Bits in GPIO LATCH register are incorrectly set to 1”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added: No. 6. “SLEEPENTER and SLEEPEXIT events asserted after pin reset”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added: No. 7. “Subsequent accesses between info_mem and main_mem of the flash may not work properly”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added: No. 9. “Reduced SFDR”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added: No. 15. “Supply regulators default to LDO mode after reset”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added: No. 21. “Disabling instruction cache causes skip of next instruction”</td>
</tr>
</tbody>
</table>
New and inherited anomalies

The following anomalies are present in revision Revision 1 of the nRF9160 chip.

<table>
<thead>
<tr>
<th>ID</th>
<th>Module</th>
<th>Description</th>
<th>New in Revision 1</th>
<th>Inherited from Engineering A</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I2S</td>
<td>Excessive power consumption after using STOP task</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>2</td>
<td>NVMC</td>
<td>CPU code execution from RAM halted during flash page erase operation</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>4</td>
<td>GPIO</td>
<td>Bits in GPIO LATCH register are incorrectly set to 1</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>6</td>
<td>POWER</td>
<td>SLEEPENTER and SLEEPEXIT events asserted after pin reset</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>7</td>
<td>KMU</td>
<td>Subsequent accesses between info_mem and main_mem of the flash may not work properly</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>9</td>
<td>SAADC</td>
<td>Reduced SFDR</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>15</td>
<td>REGULATORS</td>
<td>Supply regulators default to LDO mode after reset</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>21</td>
<td>NVMC</td>
<td>Disabling instruction cache causes skip of next instruction</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>23</td>
<td>UART</td>
<td>TASKS_RESUME impacts UARTE</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>24</td>
<td>NVMC</td>
<td>CPU is not halted for page erase in debug session</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>26</td>
<td>CLOCK, LFXO</td>
<td>System locks up when set in System ON IDLE while waiting for EVENTS_LFCLKSTARTED</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>27</td>
<td>CryptoCell</td>
<td>Arm CryptoCell true random number generator (TRNG) has wrong configuration</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>28</td>
<td>SAADC</td>
<td>Events are not generated when switching from scan mode to no-scan mode</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>29</td>
<td>Debug and Trace</td>
<td>System reset does not work</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>30</td>
<td>PWM</td>
<td>False SEQEND[0] and SEQEND[1] events are generated</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>31</td>
<td>LFXO</td>
<td>LFXO startup fails</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>32</td>
<td>Debug and Trace</td>
<td>Debug power-up request is not acknowledged</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>33</td>
<td>DPPI</td>
<td>Non-secure code can detect secure events</td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>

Table 1: New and inherited anomalies
3.1 [1] I2S: Excessive power consumption after using STOP task

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.
It was inherited from the previous IC revision Engineering A.

**Symptoms**

Current consumption too high (~900 µA) after using the STOP task.

**Conditions**

I2S was running and was stopped by triggering the STOP task.

**Consequences**

Current consumption higher than specified.

**Workaround**

Apply the below code after the STOP task. For secure mode:

```
*(((volatile uint32_t *)0x50028038) = 1;
*(((volatile uint32_t *)0x5002803C) = 1;
```

For non-secure mode:

```
*(((volatile uint32_t *)0x40028038) = 1;
*(((volatile uint32_t *)0x4002803C) = 1;
```

3.2 [2] NVMC: CPU code execution from RAM halted during flash page erase operation

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.
It was inherited from the previous IC revision Engineering A.

**Symptoms**

The CPU gets stalled when executing code from RAM.

**Conditions**

Executing code from RAM while the NVMC is performing flash erase operation.

**Consequences**

The CPU is halted for the time it takes the NVMC to perform the erase in flash. See the NVMC electrical specification for time details.
Workaround
None.

3.3 [4] GPIO: Bits in GPIO LATCH register are incorrectly set to 1

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.
It was inherited from the previous IC revision Engineering A.

Symptoms
The GPIO.LATCH[n] register is unexpectedly set to 1 (Latched).

Conditions
Set GPIO.PIN_CNF[n].SENSE at low level (3) at the same time as PIN_CNF[n].INPUT is set to Connect (0).

Consequences
The GPIO.LATCH[n] register is set to 1 (Latched). This could have side effects, depending on how the chip is configured to use this LATCH register.

Workaround
Always configure PIN_CNF[n].INPUT before PIN_CNF[n].SENSE.

3.4 [6] POWER: SLEEPENTER and SLEEPEXIT events asserted after pin reset

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.
It was inherited from the previous IC revision Engineering A.

Symptoms
NRF_POWER->EVENT_SLEEPENTER and NRF_POWER->EVENT_SLEEPEXIT are asserted.

Conditions
After device reset.

Consequences
NRF_POWER->EVENT_SLEEPENTER and NRF_POWER->EVENT_SLEEPEXIT registers are set to true after reset.

Workaround
After reset, NRF_POWER->EVENT_SLEEPENTER and NRF_POWER->EVENT_SLEEPEXIT must be cleared before enabling them as IRQ sources.
### 3.5 [7] KMU: Subsequent accesses between info_mem and main_mem of the flash may not work properly

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

It was inherited from the previous IC revision Engineering A.

**Symptoms**

Expected CPU read operation to flash main memory area never happens.

**Conditions**

Two back to back consecutive CPU read operations to flash, where the first read is to the flash UICR info page, and the second read is to flash main memory area.

**Consequences**

The read operation results in undefined behavior.

**Workaround**

Add a data synchronization barrier (DSB) operation between the two consecutive CPU read operations, in cases where the first read is to the flash UICR info page, and the second to the flash main memory area.

```c
uint32_t a = UICR_S->SOMEREGISTER;
__DSB();
uint32_t b = *((uint32_t *)SOMEFLASHADDR);
```

### 3.6 [9] SAADC: Reduced SFDR

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

**Symptoms**

Reduced SFDR on SAADC.

**Conditions**

DC/DC refresh mode.

**Consequences**

Typical SFDR reduced to 60 dBc in DC/DC refresh mode.

**Workaround**

Set register as below. For secure mode:

```c
*{(volatile uint32_t *)0x50004A38} = 0;
```
For non-secure mode:

```
*(volatile uint32_t *)0x40004A38) = 0;
```

### 3.7 [15] REGULATORS: Supply regulators default to LDO mode after reset

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

**Symptoms**

Regulators staying in LDO mode causes higher current consumption.

**Conditions**

Startup from reset.

**Consequences**

1. The device current consumption will be higher. Exactly how much higher depends on the difference in efficiency in DC/DC and LDO regulators at a given supply level and the current draw of the device.
2. The device is qualified using DC/DC converters. Qualifications and certificates created without DC/DC converters will hence be void.

**Workaround**

Application software needs to set the regulators into DC/DC mode before starting up the modem. Set register at startup as described below. For secure mode:

```
NRF_REGULATORS_S->DCDCEN = REGULATORS_DCDCEN_DCDCEN_Enabled <<
                     REGULATORS_DCDCEN_DCDCEN_Pos;
```

For non-secure mode:

```
NRF_REGULATORS_NS->DCDCEN = REGULATORS_DCDCEN_DCDCEN_Enabled <<
                     REGULATORS_DCDCEN_DCDCEN_Pos;
```

**Note:** Workaround included as of MDK 8.21.1 and later releases.

### 3.8 [21] NVMC: Disabling instruction cache causes skip of next instruction

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

It was inherited from the previous IC revision Engineering A.
New and inherited anomalies

Symptoms
The CPU skips first instruction after instruction cache is disabled.

Conditions
The code executes instructions to disable the instruction cache.

Consequences
The program does not execute as expected.

Workaround
Use the following function to disable instruction cache:

```c
_attribute__((aligned(ICACHE_LINE_SIZE)))

void icache_disable(void) {
    int key = DisableInterrupts();
    __ISB();
    NRF_NVMC->ICACHECNF = 0;
    __ISB();
    EnableInterrupts(key);
}
```

3.9 [23] UART: TASKS_RESUME impacts UARTE

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.
It was inherited from the previous IC revision Engineering A.

Symptoms
Issuing TASKS_RESUME results in bit(s) being set in the UARTE ERRORSRC register after it is enabled, even when not started.

Conditions
The internal state of a disabled UARTE changes when any of the tasks TASKS_RESUME, TASKS_STARTRX, and TASKS_STARTTX is triggered. These tasks are shared by UARTE, TWIM, TWIS, and SPIM.

Consequences
UARTE will start transmitting immediately after being enabled.

Workaround
Depending on which UARTE instance is affected, apply the following steps before enabling UARTE.
- If TXENABLE reads '1', trigger TASKS_STOPTX.
- If RXENABLE reads '1':

---

This document is a part of the Nordic Semiconductor development kit. The information provided is subject to change without notice. For the most up-to-date information, please refer to the latest Nordic Semiconductor documentation.
• Enable UARTE.
• Trigger TASKS_STOPRX.
• Wait until RXENABLE reads '0'.
• Clear ERRORSRC register.

The exact address depends on the UARTE instance. See the following table.

<table>
<thead>
<tr>
<th>UARTE Instance</th>
<th>RXENABLE</th>
<th>TXENABLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>UARTE0:NS</td>
<td>0x40008564</td>
<td>0x40008568</td>
</tr>
<tr>
<td>UARTE0:S</td>
<td>0x50008564</td>
<td>0x50008568</td>
</tr>
<tr>
<td>UARTE1:NS</td>
<td>0x40009564</td>
<td>0x40009568</td>
</tr>
<tr>
<td>UARTE1:S</td>
<td>0x50009564</td>
<td>0x50009568</td>
</tr>
<tr>
<td>UARTE2:NS</td>
<td>0x4000A564</td>
<td>0x4000A568</td>
</tr>
<tr>
<td>UARTE2:S</td>
<td>0x5000A564</td>
<td>0x5000A568</td>
</tr>
<tr>
<td>UARTE3:NS</td>
<td>0x4000B564</td>
<td>0x4000B568</td>
</tr>
<tr>
<td>UARTE3:S</td>
<td>0x5000B564</td>
<td>0x5000B568</td>
</tr>
</tbody>
</table>

Table 2: Register addresses

3.10 [24] NVMC: CPU is not halted for page erase in debug session

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A. It was inherited from the previous IC revision Engineering A.

Symptoms
Application core crashes during a debug session.

Conditions
• Debugger is connected.
• Debug system power request is triggered.
• Application core software executes NVM page erase.
• Debugger single steps page erase code.

Consequences
Debug session is interrupted due to the CPU crash.

Workaround
Avoid doing single steps or setting breakpoints around the execution of the NVM page erase instruction.
3.11 [26] CLOCK, LFXO: System locks up when set in System ON IDLE while waiting for EVENTS_LFCLKSTARTED

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

It was inherited from the previous IC revision Engineering A.

**Symptoms**

LFCLOCK is not precise after reset until LFXO is available.

**Conditions**

The LFXO is enabled and EVENTS_LFCLKSTARTED not received yet.

**Consequences**

Imprecise LFCLOCK may lead to system lockup while waiting for the LFXO to become available.

**Workaround**

Do not enter System ON IDLE in the period between writing TASK_LFCLKSTART= 1 and receiving EVENTS_LFCLKSTARTED. The startup time for the LFXO is stated in the electrical parameter $t_{START_LFXO}$ in 32.768 kHz high accuracy oscillator (LFXO) in nRF9160 Product Specification.

*Note:* The LTE modem requires LFXO as LFCLK source.

3.12 [27] CryptoCell: Arm CryptoCell true random number generator (TRNG) has wrong configuration

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

**Symptoms**

Trying to initialize the Arm® CryptoCell CC310 hardware module on nRF9160 devices using the mbedtls_platform_setup API results in undefined behavior.

**Conditions**

- Using samples marked nRF9160-SICA-B0A with the year <YY> number 19 and assembly week <WW> number lower than 25 (see IC marking in nRF9160 Product Specification)
- Using an nrf_cc310_mbedcrypto library version older than 0.8.1
- Using the mbedtls_platform_setup API to initialize the CC310 hardware

**Consequences**

Normal operation is prevented.
New and inherited anomalies

**Workaround**

Use nrf_cc310_mbedcrypto library version 0.8.1 or higher.

**Note:** This erratum applies only to nRF9160-SICA-B0A with the year <YY> number 19 and assembly week <WW> number lower than 25. See [IC marking](#) in nRF9160 Product Specification.

---

**3.13 [28] SAADC: Events are not generated when switching from scan mode to no-scan mode**

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.
It was inherited from the previous IC revision [Engineering A](#).

**Symptoms**

SAADC stops working.

**Conditions**

- Switching from multiple channels to a single channel when BURST is disabled and acquisition time is <10 us
- Switching from multiple channels to a single channel when BURST is enabled

**Consequences**

SAADC internally locks up and does not generate the expected events.

**Workaround**

Execute the following code before changing the channel configuration.

- Secure mode:

```c
NRF_SAADC_S->TASKS_STOP = 1;
```

- Non-secure mode:

```c
NRF_SAADC_NS->TASKS_STOP = 1;
```

---

**3.14 [29] Debug and Trace: System reset does not work**

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.
It was inherited from the previous IC revision [Engineering A](#).

**Symptoms**

Debugger is unable to trigger a system reset through AIRCR.SYSRESETREQ.
**Conditions**

The CPU is running non-secure code and has set the AIRCR.SYSRESETREQ bit.

**Consequences**

Reset request is ignored.

**Workaround**

Complete the following steps:

1. Halt the CPU through a connected debugger.
2. Force the processor into secure mode by setting DSCSR.SDS (see Register Specification in Arm® v8-M Architecture Reference Manual):

   ```
   SCB_DSCSR = (SCB_DSCSR & ~((1 << 17)) | 1 << 16;
   ```

   This sets bit 17 (CDSKEY) to 0 to allow writes to CDS and bit 16 (CDS) to 1 to force secure execution.

   The system resets.

**3.15 [30] PWM: False SEQEND[0] and SEQEND[1] events are generated**

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

It was inherited from the previous IC revision Engineering A.

**Symptoms**

False SEQEND[0] and SEQEND[1] events are being generated.

**Conditions**

Any of the LOOPSDONE_SEQSTARTn shortcuts are enabled. LOOP register is nonzero and SEQ[1].CNT is set to 1.

**Consequences**

SEQEND[0] and SEQEND[1] events might falsely trigger other tasks if they are routed through the PPI.

**Workaround**

Avoid using the LOOPSDONE_SEQSTARTn shortcuts when the LOOP register is nonzero and SEQ[1].CNT is set to 1.

**3.16 [31] LFXO: LFXO startup fails**

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.
New and inherited anomalies

It was inherited from the previous IC revision Engineering A.

**Symptoms**

LFXO does not start up.

**Conditions**

LFXO is set up in a wrong mode and unable to start up in all conditions.

**Consequences**

LTE modem does not work.

**Workaround**

Apply the following code after any reset:

```
*(((volatile uint32_t *)0x5000470Cul)) = 0x0;
*(((volatile uint32_t *)0x50004710ul)) = 0x1;
```

This workaround is implemented in MDK version 8.29.0.

### 3.17 [32] Debug and Trace: Debug power-up request is not acknowledged

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

It was inherited from the previous IC revision Engineering A.

**Symptoms**

In the CTRL/STAT register of the debug port (see ARM CoreSight SoC-400 Technical Reference Manual, revision r3p2):

- CDBGWRUPREQ powers up the system but does not assert CDBGWRUPACK.
- CSYSPWRUPREQ does not trigger any power requests but asserts CDBGWRUPACK and CSYSPWRUPACK.

**Conditions**

Always when starting a debug session.

**Consequences**

If the debug probe writes the debug port CTRL/STAT.DBGPWRUPREQ and waits on CTRL/STAT.DBGPWRUPACK, it does not finish.

**Workaround**

When enabling debug domain power, write CTRL/STAT.DBGPWRUPREQ and CTRL/STAT.SYSPWRUPREQ.
3.18 [33] DPPI: Non-secure code can detect secure events

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.
It was inherited from the previous IC revision Engineering A.

**Symptoms**
Non-secure code is able to detect that a secure event has been published to a secure DPPI channel.

**Conditions**
In a non-secure DPPI channel group, SUBSCRIBE_CHG[n].EN or SUBSCRIBE_CHG[n].DIS is setup to be connected to a secure DPPI channel.

**Consequences**
Non-secure code can detect that a secure event has been published to a secure DPPI channel. The non-secure code cannot detect which event has been published.

**Workaround**
Perform one of the following:
- Avoid using DPPI in secure mode.
- Configure all channel groups (CHG[n]) to include at least one DPPI channel that is configured as secure. This makes the channel groups secure and blocks them from being used on the non-secure side.

**Note:** The non-secure domain can still use the DPPI tasks and events system, but it does not have any available channel groups.
The anomalies listed in this table are no longer present in the current chip version.

For a detailed description of the fixed anomalies, see the Errata for revision Engineering A.

<table>
<thead>
<tr>
<th>ID</th>
<th>Module</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>SAADC</td>
<td>Reduced SFDR</td>
</tr>
<tr>
<td>10</td>
<td>LTE Modem</td>
<td>MAGPIO and MIPI RFFE - high initial voltage</td>
</tr>
<tr>
<td>12</td>
<td>Debug and</td>
<td>SWD debugger scan</td>
</tr>
<tr>
<td></td>
<td>Trace</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>REGULATORS</td>
<td>Supply regulators default to LDO mode after reset</td>
</tr>
<tr>
<td>16</td>
<td>SAADC</td>
<td>SAADC result</td>
</tr>
<tr>
<td>17</td>
<td>Debug and</td>
<td>LTE modem stops when debugging through SWD interface</td>
</tr>
<tr>
<td></td>
<td>Trace</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>RAM</td>
<td>RAM content cannot be trusted upon waking up from System ON IDLE or System</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF mode</td>
</tr>
</tbody>
</table>

*Table 3: Fixed anomalies*