nRF9160

Revision 1

Errata

v1.0

NORDIC® SEMICONDUCTOR

Contents

1 nRF9160 Revision 1 Errata

This Errata document contains anomalies for the nRF9160 chip, revision Revision 1 (SICA-B0A).

The document indicates which anomalies are fixed, inherited, or new compared to revision Engineering A.

2 Change log

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nRF9160 Revision 1 v1.0	28.05.2019	• Added: No. 1. “Excessive power consumption after using STOP task” • Added: No. 2. “CPU code execution from RAM halted during flash page erase operation” • Added: No. 4. “Bits in GPIO LATCH register are incorrectly set to 1” • Added: No. 6. “SLEEPENTER and SLEEPEXIT events asserted after pin reset” • Added: No. 7. “Subsequent accesses between info_mem and main_mem of the flash may not work properly” • Added: No. 9. “Reduced SFDR” • Added: No. 15. “Supply regulators default to LDO mode after reset” • Added: No. 21. “Disabling instruction cache causes skip of next instruction”

3 New and inherited anomalies

The following anomalies are present in revision Revision 1 of the nRF9160 chip.

ID	Module	Description	New in Revision 1	Inherited from Engineering A
1	I2S	Excessive power consumption after using STOP task		X
2	NVMC	CPU code execution from RAM halted during flash page erase operation		X
4	GPIO	Bits in GPIO LATCH register are incorrectly set to 1		X
6	POWER	SLEEPENTER and SLEEPEXIT events asserted after pin reset		X
7	KMU	Subsequent accesses between info_mem and main_mem of the flash may not work properly		X
9	SAADC	Reduced SFDR	X	
15	REGULATORS	Supply regulators default to LDO mode after reset	X	
21	NVMC	Disabling instruction cache causes skip of next instruction		X

Table 1: New and inherited anomalies

3.1 [1] I2S: Excessive power consumption after using STOP task

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

It was inherited from the previous IC revision Engineering A.

Symptoms

Current consumption too high (~900 µA) after using the STOP task.

Conditions

I2S was running and was stopped by triggering the STOP task.

Consequences

Current consumption higher than specified.

Workaround

Apply the below code after the STOP task. For secure mode:

```
*((volatile uint32_t *)0x50028038) = 1;
*((volatile uint32_t *)0x5002803C) = 1;
```

For non-secure mode:

```
*((volatile uint32_t *)0x40028038) = 1;
*((volatile uint32_t *)0x4002803C) = 1;
```

3.2 [2] NVMC: CPU code execution from RAM halted during flash page erase operation

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

It was inherited from the previous IC revision Engineering A.

Symptoms

The CPU gets stalled when executing code from RAM.

Conditions

Executing code from RAM while the NVMC is performing flash erase operation.

Consequences

The CPU is halted for the time it takes the NVMC to perform the erase in flash. See the NVMC electrical specification for time details.

Workaround

None.

3.3 [4] GPIO: Bits in GPIO LATCH register are incorrectly set to 1

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

It was inherited from the previous IC revision Engineering A.

Symptoms

The GPIO.LATCH[n] register is unexpectedly set to 1 (Latched).

Conditions

Set GPIO.PIN_CNF[n].SENSE at low level (3) at the same time as PIN_CNF[n].INPUT is set to Connect (0).

Consequences

The GPIO.LATCH[n] register is set to 1 (Latched). This could have side effects, depending on how the chip is configured to use this LATCH register.

Workaround

Always configure PIN_CNF[n].INPUT before PIN_CNF[n].SENSE.

3.4 [6] POWER: SLEEPENTER and SLEEPEXIT events asserted after pin reset

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

It was inherited from the previous IC revision Engineering A.

Symptoms

NRF_POWER->EVENT_SLEEPENTER and NRF_POWER->EVENT_SLEEPEXIT are asserted.

Conditions

After device reset.

Consequences

NRF_POWER->EVENT_SLEEPENTER and NRF_POWER->EVENT_SLEEPEXIT registers are set to true after reset.

Workaround

After reset, NRF_POWER->EVENT_SLEEPENTER and NRF_POWER->EVENT_SLEEPEXIT must be cleared before enabling them as IRQ sources.

3.5 [7] KMU: Subsequent accesses between info_mem and main_mem of the flash may not work properly

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

It was inherited from the previous IC revision Engineering A.

Symptoms

Expected CPU read operation to flash main memory area never happens.

Conditions

Two back to back consecutive CPU read operations to flash, where the first read is to the flash UICR info page, and the second read is to flash main memory area.

Consequences

The read operation results in undefined behavior.

Workaround

Add a data synchronization barrier (DSB) operation between the two consecutive CPU read operations, in cases where the first read is to the flash UICR info page, and the second to the flash main memory area.

```
uint32_t a = UICR_S->SOMEREGISTER;
__DSB();
uint32_t b = *((uint32_t *)SOMEFLASHADDR);
```

3.6 [9] SAADC: Reduced SFDR

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

Symptoms

Reduced SFDR on SAADC.

Conditions

DC/DC refresh mode.

Consequences

Typical SFDR reduced to 60 dBc in DC/DC refresh mode.

Workaround

Set register as below. For secure mode:

```
*((volatile uint32_t *)0x50004A38) = 0;
```

For non-secure mode:

```
*((volatile uint32_t *)0x40004A38) = 0;
```

3.7 [15] REGULATORS: Supply regulators default to LDO mode after reset

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

Symptoms

Regulators staying in LDO mode causes higher current consumption.

Conditions

Startup from reset.

Consequences

1. The device current consumption will be higher. Exactly how much higher depends on the difference in efficiency in DC/DC and LDO regulators at a given supply level and the current draw of the device.
2. The device is qualified using DC/DC converters. Qualifications and certificates created without DC/DC converters will hence be void.

Workaround

Application software needs to set the regulators into DC/DC mode before starting up the modem. Set register at startup as described below. For secure mode:

```
NRF_REGULATORS_S->DCDCEN = REGULATORS_DCDCEN_DCDCEN_Enabled <<
 REGULATORS_DCDCEN_DCDCEN_Pos;
```

For non-secure mode:

```
NRF_REGULATORS_NS->DCDCEN = REGULATORS_DCDCEN_DCDCEN_Enabled <<
 REGULATORS_DCDCEN_DCDCEN_Pos;
```

Note: Workaround included as of MDK 8.21.1 and later releases.

3.8 [21] NVMC: Disabling instruction cache causes skip of next instruction

This anomaly applies to IC Rev. Revision 1, build codes SICA-B0A.

It was inherited from the previous IC revision Engineering A.

Symptoms

The CPU skips first instruction after instruction cache is disabled.

Conditions

The code executes instructions to disable the instruction cache.

Consequences

The program does not execute as expected.

Workaround

Use the following function to disable instruction cache:

```
_attribute_((aligned(ICACHE_LINE_SIZE)))

void icache_disable(void) {
    int key = DisableInterrupts();
    __ISB();
    NRF_NVMC->ICACHECNF = 0;
    __ISB();
    EnableInterrupts(key);
}
```

4 Fixed anomalies

The anomalies listed in this table are no longer present in the current chip version.

For a detailed description of the fixed anomalies, see the Errata for revision Engineering A.

ID	Module	Description
8	SAADC	Reduced SFDR
10	LTE Modem	MAGPIO and MIPI RFFE - high initial voltage
12	Debug and Trace	SWD debugger scan
14	REGULATORS	Supply regulators default to LDO mode after reset
16	SAADC	SAADC result
17	Debug and Trace	LTE modem stops when debugging through SWD interface
20	RAM	RAM content cannot be trusted upon waking up from System ON IDLE or System OFF mode

Table 2: Fixed anomalies