

nRF9160

Engineering A

Errata

v1.1

Contents

1	nRF9160 Engineering A Errata	3
2	Change log	4
3	New and inherited anomalies	5
3.1	[1] I2S: Excessive power consumption after using STOP task	5
3.2	[2] NVMC: CPU code execution from RAM halted during flash page erase operation	6
3.3	[4] GPIO: Bits in GPIO LATCH register are incorrectly set to 1	6
3.4	[6] POWER: SLEEPENTER and SLEEPEXIT events asserted after pin reset	7
3.5	[7] KMU: Subsequent accesses between info_mem and main_mem of the flash may not work properly	7
3.6	[8] SAADC: Reduced SFDR	8
3.7	[10] LTE Modem: MAGPIO and MIPI RFFE - high initial voltage	8
3.8	[12] Debug and Trace: SWD debugger scan	9
3.9	[14] REGULATORS: LDO mode at startup	9
3.10	[16] SAADC: SAADC result	10
3.11	[17] Debug and Trace: LTE modem stops when debugging through SWD interface	10

1 nRF9160 Engineering A Errata

This Errata document contains anomalies for the nRF9160 chip, revision Engineering A (SICA-BAA).

2 Change log

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nRF9160 Engineering A v1.1	10.01.2019	<ul style="list-style-type: none">• Added: No. 17. "LTE modem stops when debugging through SWD interface"
nRF9160 Engineering A v1.0	12.12.2018	<ul style="list-style-type: none">• Added: No. 1. "Excessive power consumption after using STOP task"• Added: No. 2. "CPU code execution from RAM halted during flash page erase operation"• Added: No. 4. "Bits in GPIO LATCH register are incorrectly set to 1"• Added: No. 6. "SLEEPENTER and SLEEPEXIT events asserted after pin reset"• Added: No. 7. "Subsequent accesses between info_mem and main_mem of the flash may not work properly"• Added: No. 8. "Reduced SFDR"• Added: No. 10. "MAGPIO and MIPI RFFE - high initial voltage"• Added: No. 12. "SWD debugger scan"• Added: No. 14. "LDO mode at startup"• Added: No. 16. "SAADC result"

3 New and inherited anomalies

The following anomalies are present in revision Engineering A of the nRF9160 chip.

ID	Module	Description	New in Engineering A
1	I2S	Excessive power consumption after using STOP task	X
2	NVMC	CPU code execution from RAM halted during flash page erase operation	X
4	GPIO	Bits in GPIO LATCH register are incorrectly set to 1	X
6	POWER	SLEEPENTER and SLEEPEXIT events asserted after pin reset	X
7	KMU	Subsequent accesses between info_mem and main_mem of the flash may not work properly	X
8	SAADC	Reduced SFDR	X
10	LTE Modem	MAGPIO and MIPI RFFE - high initial voltage	X
12	Debug and Trace	SWD debugger scan	X
14	REGULATORS	LDO mode at startup	X
16	SAADC	SAADC result	X
17	Debug and Trace	LTE modem stops when debugging through SWD interface	X

Table 1: New and inherited anomalies

3.1 [1] I2S: Excessive power consumption after using STOP task

This anomaly applies to IC Rev. Engineering A, build codes SICA-BAA.

Symptoms

Current consumption too high (~900 μ A) after using the STOP task.

Conditions

I2S was running and was stopped by triggering the STOP task.

Consequences

Current consumption higher than specified.

Workaround

Apply the below code after the STOP task. For secure mode:

```
*((volatile uint32_t *)0x50028038) = 1;  
*((volatile uint32_t *)0x5002803C) = 1;
```

For non-secure mode:

```
*((volatile uint32_t *)0x40028038) = 1;  
*((volatile uint32_t *)0x4002803C) = 1;
```

3.2 [2] NVMC: CPU code execution from RAM halted during flash page erase operation

This anomaly applies to IC Rev. Engineering A, build codes SICA-BAA.

Symptoms

The CPU gets stalled when executing code from RAM.

Conditions

Executing code from RAM while the NVMC is performing flash erase operation.

Consequences

The CPU is halted for the time it takes the NVMC to perform the erase in flash. See the NVMC electrical specification for time details.

Workaround

None.

3.3 [4] GPIO: Bits in GPIO LATCH register are incorrectly set to 1

This anomaly applies to IC Rev. Engineering A, build codes SICA-BAA.

Symptoms

The GPIO.LATCH[n] register is unexpectedly set to 1 (Latched).

Conditions

Set GPIO.PIN_CNF[n].SENSE at low level (3) at the same time as PIN_CNF[n].INPUT is set to Connect (0).

Consequences

The GPIO.LATCH[n] register is set to 1 (Latched). This could have side effects, depending on how the chip is configured to use this LATCH register.

Workaround

Always configure PIN_CNF[n].INPUT before PIN_CNF[n].SENSE.

3.4 [6] POWER: SLEEPENTER and SLEEPEXIT events asserted after pin reset

This anomaly applies to IC Rev. Engineering A, build codes SICA-BAA.

Symptoms

NRF_POWER->EVENT_SLEEPENTER and NRF_POWER->EVENT_SLEEPEXIT are asserted.

Conditions

After device reset.

Consequences

NRF_POWER->EVENT_SLEEPENTER and NRF_POWER->EVENT_SLEEPEXIT registers are set to true after reset.

Workaround

After reset, NRF_POWER->EVENT_SLEEPENTER and NRF_POWER->EVENT_SLEEPEXIT must be cleared before enabling them as IRQ sources.

3.5 [7] KMU: Subsequent accesses between info_mem and main_mem of the flash may not work properly

This anomaly applies to IC Rev. Engineering A, build codes SICA-BAA.

Symptoms

Expected CPU read operation to flash main memory area never happens.

Conditions

Two back to back consecutive CPU read operations to flash, where the first read is to the flash UICR info page, and the second read is to flash main memory area.

Consequences

The read operation results in undefined behavior.

Workaround

Add a data synchronization barrier (DSB) operation between the two consecutive CPU read operations, in cases where the first read is to the flash UICR info page, and the second to the flash main memory area.

```
uint32_t a = UICR_S->SOMEREGISTER;
__DSB();
uint32_t b = *((uint32_t *)SOMEFLASHADDR);
```

3.6 [8] SAADC: Reduced SFDR

This anomaly applies to IC Rev. Engineering A, build codes SICA-BAA.

Symptoms

Reduced SFDR on SAADC.

Conditions

DC/DC refresh mode used.

Consequences

SFDR reduced to 60 dBc.

Workaround

Set registers as below before use of SAADC. For secure mode:

```
*((volatile uint32_t *)0x50004A38) = 1;
```

For non-secure mode:

```
*((volatile uint32_t *)0x40004A38) = 1;
```

Note: Consequence is 7-10 mA increased current consumption. The consequence of this item will be fixed on the production version of nRF9160-SICA.

3.7 [10] LTE Modem: MAGPIO and MIPI RFFE - high initial voltage

This anomaly applies to IC Rev. Engineering A, build codes SICA-BAA.

Symptoms

The 1.8 V GPIOs MAGPIO[0,1,2] and MIPI RFFE[SCLK, SDATA] have a higher voltage than specified for the first millisecond.

Conditions

Use of any of the 1.8 V GPIOs:

- MAGPIO[0,1,2]
- SCLK
- SDATA

Consequences

Voltage increase up to 2.2 V for 1 ms after reset.

Workaround

None.

Note: This item will be fixed on the production version of nRF9160-SICA.

3.8 [12] Debug and Trace: SWD debugger scan

This anomaly applies to IC Rev. Engineering A, build codes SICA-BAA.

Symptoms

Some access ports lock up when reading IDR.

Conditions

Always.

Consequences

AP scan fails when encountering these locked APs.

Workaround

Use one of the following solutions:

1. Use Nordic Semiconductor programming tools.
2. If an AP read times out on an unknown AP, write 0x0000001F to DP->ABORT to stop the transfer and continue the session.

Note: This item will be fixed on the production version of nRF9160-SICA.

3.9 [14] REGULATORS: LDO mode at startup

This anomaly applies to IC Rev. Engineering A, build codes SICA-BAA.

Symptoms

The device is set to LDO mode.

Conditions

Startup from reset.

Consequences

LTE modem is certified to operate in DC/DC mode. The certifications are not valid if the LDO mode is used.

Workaround

Application software needs to set the regulators into DC/DC mode before starting up the modem. Set registers at startup as described below. For secure mode:

```
*((volatile uint32_t *)0x50004A38) = 1;
```

For non-secure mode:

```
*((volatile uint32_t *)0x40004A38) = 1;
```

NRF_REGULATORS->DCDCEN = 0x01.

Note: Workaround included as of MDK 8.21.0 and later releases.

3.10 [16] SAADC: SAADC result

This anomaly applies to IC Rev. Engineering A, build codes SICA-BAA.

Symptoms

Wrong SAADC output.

Conditions

VDD_GPIO higher than 2.1 V.

Consequences

Not able to read out correct value from SAADC output.

Workaround

Keep VDD_GPIO at or below 2.1 V.

Note: This item will be fixed on the production version of nRF9160-SICA.

3.11 [17] Debug and Trace: LTE modem stops when debugging through SWD interface

This anomaly applies to IC Rev. Engineering A, build codes SICA-BAA.

Symptoms

LTE modem operation might fail during debugging.

Note: Using nRF Connect SDK, `bsd_recoverable_error_handler` number 3 is triggered.

Conditions

Debugging the application through SWD interface.

Consequences

The LTE modem operation might stop.

Workaround

When debugging, register 0xC04 in the peripheral CLOCK/POWER must be set to the value 0x02 before the modem is initialized (`bsd_init()`). When using nRF Connect SDK, we recommend adding the following code at the end of the function `SystemInit ()` in file `...\\zephyr\\ext\\hal\\nordic\\nrfx\\mdk\\system_nrf9160.c`.

```
#if defined(NRF_TRUSTZONE_NONSECURE)
    *(volatile uint32_t *)0x40005C04 = 0x02ul;
#endif
```

This workaround will increase overall power consumption and is not suitable for power measurement. When you want to disable this patch, remove the code and perform a pin reset or power cycle the device.