nRF5340

Revision 1

Errata

v1.8

NORDIC® SEMICONDUCTOR

Contents

1 nRF5340 Revision 1 Errata

This Errata document contains anomalies and configurations for the nRF5340 chip, Revision 1 (QKAA-D00, CLAA-D00).

The document indicates which anomalies are fixed, inherited, or new compared to Engineering D.

2 Revision history

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nRF5340 Revision 1 v1.8	10.01.2024	• Added: No. 159. “Data can be corrupted in certain clock configurations ” • Added: No. 166. “VREGMAIN can malfunction in LDO mode” • Added: No. 167. “SPU FLASHACCERR is generated after re-enabling USBD ” • Added: No. 168. “CPU can malfunction after sleep”
nRF5340 Revision 1 v1.7	13.09.2023	• Added: No. 155. “Incorrect value for ED_RSSISCALE” • Added: No. 157. “On-the-fly decryption fails for direction finding packets” • Added: No. 162. “WLCSP package dimension A3 is incorrect” • Added: No. 163. “Gain error exceeds specified value when using VDD as reference ” • Added: No. 165. “Network core can malfunction after CPU sleep” • Updated: No. 161. “Network core is not fully reset after Force-OFF”
nRF5340 Revision 1 v1.6	01.03.2023	• Added: No. 160. “VREGMAIN and VREGRADIO can malfunction in DC/DC mode” • Added: No. 161. “Core is not fully reset after Force-OFF”
nRF5340 Revision 1 v1.5	04.11.2022	• Added: No. 158. “Using POWER register clears RADIO trim values ”
nRF5340 Revision 1 v1.4	06.09.2022	• Added: No. 152. “Incorrect value for I_S10” • Added: No. 153. “GPIOTE with low-power latency setting does not register IN events in System ON IDLE” • Added: No. 154. “WLCSP package dimension L is incorrect”
nRF5340 Rev 1 v1.3	10.02.2022	• Added: No. 140. “Soft reset during LFRC calibration prevents watchdog reset and LFCLK from being started”
nRF5340 Rev 1 v1.2	03.12.2021	• Added: No. 133. “Degraded radio performance with QSPI” • Added: No. 135. “No output from SPIM4” • Added: No. 136. “QSPI has limited supply voltage range” • Added: No. 137. “LFRC calibration is not performed”
nRF5340 Rev 1 v1.1	22.10.2021	• Added: No. 134. “Incorrect value for IRADIO_TX3” • Added: No. 138. “LPCOMP consumes additional current”

Version	Date	Change
nRF5340 Rev1 v1.0	03.12.2020	• Added: No. 6. “Disabling instruction cache causes skip of next instruction” • Added: No. 43. “Reading QSPI registers after XIP might halt application CPU” • Added: No. 44. “TASKS_RESUME impacts UARTE” • Added: No. 47. “I2C timing spec is violated at 400 kHz” • Added: No. 55. “Bits in RESETREAS are set when they should not be” • Added: No. 65. “Events are not generated when switching from scan mode to no-scan mode with BURST disabled” • Added: No. 70. “Event FIELDDETECTED may be generated too early” • Added: No. 71. “Frame delay timing is too short after SLP_REQ” • Added: No. 75. “False SEQEND[0] and SEQEND[1] events are generated” • Added: No. 76. “Non-secure code can detect secure events” • Added: No. 87. “RSSI parameter adjustment” • Added: No. 99. “Mode 3 is not functional at 96 MHz” • Added: No. 112. “24-bit sample in a 32-bit half-frame is received incorrectly” • Added: No. 113. “Reading DTX in MODECNF0 gives incorrect value” • Added: No. 117. “Changing MODE requires additional configuration” • Added: No. 119. “Writes to LATCH register take several CPU cycles to take effect” • Added: No. 121. “Configuration of peripheral requires additional steps” • Added: No. 122. “Successive triggering of CTRLAP.ERASEALL has no effect”

3 New and inherited anomalies

The following anomalies are present in Revision 1 of the nRF5340 chip.

ID	Domain	Module	Description	New in Revision 1	Inherited from Engineering D
6	Network	NVMC	Disabling instruction cache causes skip of next instruction		X
43	Application	QSPI	Reading QSPI registers after XIP might halt application CPU		X
44	Application, Network	UARTE	TASKS_RESUME impacts UARTE		X
47	Application, Network	TWIM	I2C timing spec is violated at 400 kHz		X
55	Application, Network	RESET	Bits in RESETREAS are set when they should not be		X
65	Application	SAADC	Events are not generated when switching from scan mode to no-scan mode with BURST disabled		X
70	Application	NFCT	Event FIELDDETECTED may be generated too early		X
71	Application	NFCT	Frame delay timing is too short after SLP_REQ		X
75	Application	PWM	False SEQEND[0] and SEQEND[1] events are generated		X
76	Application	DPPI	Non-secure code can detect secure events		X
87	Network	RADIO	RSSI parameter adjustment		X
99	Application	QSPI	Mode 3 is not functional at 96 MHz		X
112	Application	I2S	24-bit sample in a 32-bit half-frame is received incorrectly		X
113	Network	RADIO	Reading DTX in MODECNF0 gives incorrect value		X
117	Network	RADIO	Changing MODE requires additional configuration		X
119	Network	GPIO	Writes to LATCH register take several CPU cycles to take effect		X
121	Application	QSPI	Configuration of peripheral requires additional steps		X
122	Network	CTRL-AP	Successive triggering of CTRLAP.ERASEALL has no effect		X
133	Application	QSPI	Degraded radio performance with QSPI	X	
134	Network	RADIO	Incorrect value for IRADIO_TX3	X	

ID	Domain	Module	Description	New in Revision 1	Inherited from Engineering D
135	Application, Network	SPIM	No output from SPIM4	X	
136	Application	QSPI	QSPI has limited supply voltage range	X	
137	Application, Network	CLOCK	LFRC calibration is not performed	X	
138	Application	COMP	LPCOMP consumes additional current	X	
140	Application	CLOCK	Soft reset during LFRC calibration prevents watchdog reset and LFCLK from being started		X
152	Application, Network	RADIO	Incorrect value for I_S10	X	
153	Application	GPIOTE	GPIOTE with low-power latency setting does not register IN events in System ON IDLE	X	
154	Application, Network	Package	WLCSP package dimension L is incorrect	X	
155	Network	RADIO	Incorrect value for ED_RSSISCALE	X	
157	Network	CCM	On-the-fly decryption fails for direction finding packets	X	
158	Network	RADIO	Using POWER register clears RADIO trim values	X	
159	Application	QSPI	Data can be corrupted in certain clock configurations	X	
160	Application, Network	REGULATORS	VREGMAIN and VREGRADIO can malfunction in DC/DC mode	X	
161	Application, Network	RESET	Network core is not fully reset after Force-OFF	X	
162	Application, Network	Package	WLCSP package dimension A3 is incorrect	X	
163	Application	SAADC	Gain error exceeds specified value when using VDD as reference	X	
165	Application, Network	DEVICE	Network core can malfunction after CPU sleep	X	
166	Application	REGULATOR	VREGMAIN can malfunction in LDO mode	X	
167	Application	USBD	SPU FLASHACCERR is generated after re-enabling USBD	X	
168	Application, Network	CPU	CPU can malfunction after sleep	X	

Table 1: New and inherited anomalies

3.1 [6] NVMC: Disabling instruction cache causes skip of next instruction

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Network

Symptoms

The CPU skips the first instruction after instruction cache is disabled.

Conditions

The code executes instructions to disable the instruction cache.

Consequences

The program does not execute as expected.

Workaround

Use the following function to disable instruction cache:

```
_attribute_((aligned(ICACHE_LINE_SIZE)))

void icache_disable(void) {
    int key = DisableInterrupts();
    __ISB();
    NRF_NVMC->ICACHECNF = 0;
    __ISB();
    EnableInterrupts(key);
}
```

3.2 [43] QSPI: Reading QSPI registers after XIP might halt application CPU

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

Application CPU halts.

Conditions

Init and start QSPI, use XIP, then write to or read any QSPI register starting from offset 0x600 and above.

Consequences

Application CPU halts.

Workaround

Trigger QSPI TASKS_ACTIVATE after XIP is used before accessing any QSPI register with an offset above 0x600.

3.3 [44] UARTE: TASKS_RESUME impacts UARTE

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application, Network

Symptoms

Issuing TASKS_RESUME results in bits being set in the UARTE ERRORSRC register after it is enabled, even when not started.

Conditions

The internal state of a disabled UARTE changes when any of the tasks TASKS_RESUME, TASKS_STARTRX, or TASKS_STARTTX is triggered. These tasks are shared by UARTE, TWIM, TWIS, and SPIM.

Consequences

UARTE starts transmitting immediately after being enabled.

Workaround

Depending on which UARTE instance is affected, apply the following steps before enabling UARTE.

- If TXENABLE reads '1', trigger TASKS_STOPTX.
- If RXENABLE reads '1':
  - Enable UARTE.
  - Trigger TASKS_STOPRX.
  - Wait until RXENABLE reads '0'.
  - Clear ERRORSRC register.

The exact address depends on the UARTE instance. See the following table.

UARTE Instance	RXENABLE	TXENABLE
UARTE0:NS	0x40008564	0x40008568
UARTE0:S	0x50008564	0x50008568
UARTE1:NS	0x40009564	0x40009568
UARTE1:S	0x50009564	0x50009568
UARTE2:NS	0x4000B564	0x4000B568
UARTE2:S	0x5000B564	0x5000B568
UARTE3:NS	0x4000C564	0x4000C568
UARTE3:S	0x5000C564	0x5000C568

Table 2: Register addresses

3.4 [47] TWIM: I2C timing spec is violated at 400 kHz

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application, Network

Symptoms

The low period of the SCL clock is too short to meet the I2C specification at 400 kHz. The actual low period of the SCL clock is 1.25 µs while the I2C specification requires the SCL clock to have a minimum low period of 1.3 µs.

Conditions

Using TWIM at 400 kHz.

Consequences

TWI communication might not work at 400 kHz with I2C compatible devices.

Workaround

If communication does not work at 400 kHz with an I2C compatible device that requires the SCL clock to have a minimum low period of 1.3 µs, use 390 kHz instead of 400 kHz by writing 0x06200000 to the FREQUENCY register. With this setting, the SCL low period is greater than 1.3 µs.

3.5 [55] RESET: Bits in RESETREAS are set when they should not be

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application, Network

Symptoms

After pin reset, RESETREAS bits other than RESETPIN might also be set.

Conditions

A pin reset has triggered.

Consequences

If the firmware evaluates RESETREAS, it might take the wrong action.

Workaround

When RESETREAS shows a pin reset (RESETPIN), ignore other reset reason bits.

> **Note:** RESETREAS bits must be cleared between resets.

Apply the following code after any reset:

```
For Application:
if (NRF_RESET_S->RESETREAS & RESET_RESETREAS_RESETPIN_Msk)
{
    NRF_RESET_S->RESETREAS = ~RESET_RESETREAS_RESETPIN_Msk;
}
For Network:
if (NRF_RESET->RESETREAS & RESET_RESETREAS_RESETPIN_Msk)
{
    NRF_RESET->RESETREAS = ~RESET_RESETREAS_RESETPIN_Msk;
}
```

This workaround is implemented in MDK version 8.29.0 and later.

3.6 [65] SAADC: Events are not generated when switching from scan mode to no-scan mode with BURST disabled

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

SAADC stops working.

Conditions

Switching from single channel to multiple channels when BURST is disabled and acquisition time less than 10 us.

Consequences

SAADC internally locks up and does not generate the expected events.

Workaround

Execute the following code before changing the channel configuration.

- Secure mode:

```
NRF_SAADC_S->TASKS_STOP = 1;
```

- Non-secure mode:

```
NRF_SAADC_NS->TASKS_STOP = 1;
```

3.7 [70] NFCT: Event FIELDDETECTED may be generated too early

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

Reset of the operating state after FIELDLOST event. In some cases, communication with the peer device is not possible.

Conditions

Especially with stronger field strengths.

Consequences

Restart of transfer is required.

Workaround

On FIELDDETECTED event, wait 1 ms using timer before starting NFC communication with NRF_NFCT->TASKS_ACTIVATE.

This workaround is included in nrfx v2.0.0 and later.

3.8 [71] NFCT: Frame delay timing is too short after SLP_REQ

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

Reader may not accept the response from the tag.

Conditions

The time between SLP_REQ and ALL_REQ sent by the Reader is shorter than the time configured in FRAMEDELAYMAX.

Consequences

The protocol timing is violated, and a Reader may not accept the response from the tag.

Workaround

Ensure that FRAMEDELAYMAX is set to the default value when the NFCT is in states IDLE or SLEEP_A. The workaround is included in nrfx v2.0.0 and later.

3.9 [75] PWM: False SEQEND[0] and SEQEND[1] events are generated

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

False SEQEND[0] and SEQEND[1] events are generated.

Conditions

Any of the LOOPSDONE_SEQSTARTn shortcuts are enabled. LOOP register is nonzero and SEQ[1].CNT is set to 1.

Consequences

SEQEND[0] and SEQEND[1] events might falsely trigger other tasks if they are routed through the PPI.

Workaround

Avoid using the LOOPSDONE_SEQSTARTn shortcuts when the LOOP register is nonzero and SEQ[1].CNT is set to 1.

3.10 [76] DPPI: Non-secure code can detect secure events

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

Non-secure code is able to detect that a secure event has been published to a secure DPPI channel.

Conditions

In a non-secure DPPI channel group, SUBSCRIBE_CHG[n].EN or SUBSCRIBE_CHG[n].DIS is set up to be connected to a secure DPPI channel.

Consequences

Non-secure code can detect that a secure event has been published to a secure DPPI channel. The non-secure code cannot detect which event has been published.

Workaround

Perform one of the following:

- Avoid using DPPI in secure mode.
- Configure all channel groups (CHG[n]) to include at least one DPPI channel that is configured as secure. This makes the channel groups secure and blocks them from being used on the non-secure side.

> **Note:** The non-secure domain can still use the DPPI tasks and events system, but it does not have any available channel groups.

3.11 [87] RADIO: RSSI parameter adjustment

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Network

Symptoms

RSSI varies with temperature and input power level.

Conditions

Always.

Consequences

RSSI parameter is not within specified accuracy.

Workaround

Add the following compensation to the RSSI sample value based on temperature measurement and RSSISAMPLE. The on-chip TEMP peripheral can be used to measure temperature.

```
compensated_rssi = (uint8_t)round(
    (float)((float)(1.56f * rssi_sample) + (float)(4.9e-5 * pow(rssi_sample, 3)) -
    (float)(9.9e-3 * pow(rssi_sample, 2)) - (0.05f * ((float)(temp)*0.25f)) - 7.2f));
```

where

temp
: Temperature sample value as reported by register NRF_TEMP.TEMP in increments of 0.25.

drssi_sample
: Sample value as reported by register NRF_RADIO.RSSISAMPLE.

3.12 [99] QSPI: Mode 3 is not functional at 96 MHz

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

Mode 3 is not functional at 96 MHz.

Conditions

Always.

Consequences

Mode 3 can be used only from 6 to 48 MHz.

Workaround

Use speed between 6 and 48 MHz or use Mode 0 to have full speed range.

3.13 [112] I2S: 24-bit sample in a 32-bit half-frame is received incorrectly

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

24-bit sample in a 32-bit half-frame is received incorrectly.

Conditions

CONFIG.SWIDTH is configured to 24BitIn32.

Consequences

24-bit sample in 32-bit word has incorrect data from bits 25-31.

Workaround

Leave the first 24 bits in 32-bit word as is. Replace the 8 MSB bits of the 32-bit word by sign-extending the 24th bit.

3.14 [113] RADIO: Reading DTX in MODECNF0 gives incorrect value

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Network

Symptoms

Reading DTX in MODECNF0 gives incorrect value.

Conditions

Always.

Consequences

Reading the MODECNF0.DTX field returns an incorrect value.

Workaround

Treat the MODECNF0.DTX field as write only.

3.15 [117] RADIO: Changing MODE requires additional configuration

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Network

Symptoms

Radio modulation index is lower than expected.

Conditions

Always.

Consequences

RADIO may fail qualification tests or have higher than expected packet loss. Measured modulation characteristics for Bluetooth and error vector magnitude for IEEE802.15.4 are affected.

Workaround

After writing the RADIO.MODE register, perform the following additional configuration steps.

- When RADIO.MODE is set to Nrf_2Mbit, Ble_2Mbit, or Ieee802154_250Kbit, use the following:

```
*((volatile uint32_t *)0x41008588) = *((volatile uint32_t *)0x01FF0084);
```

- When RADIO.MODE is set to any other mode, use the following:

```
*((volatile uint32_t *)0x41008588) = *((volatile uint32_t *)0x01FF0080);
```

3.16 [119] GPIO: Writes to LATCH register take several CPU cycles to take effect

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Network

Symptoms

A bit in the LATCH register reads '1' even after clearing it by writing '1'.

Conditions

Reading the LATCH register right after writing to it.

Consequences

Old value of the LATCH register is read.

Workaround

Have at least 4 CPU cycles of delay between the write and the subsequent read to the LATCH register. This can be achieved by having 4 dummy reads of the LATCH register.

3.17 [121] QSPI: Configuration of peripheral requires additional steps

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

QSPI is unstable or not working at all.

Conditions

Always.

Consequences

QSPI does not work as expected.

Workaround

When configuring QSPI, ensure register IFTIMING.RXDELAY = 6 and perform the following additional configuration steps.

- For operation at 96 MHz, perform the following extra configuration step:

```
NRF_QSPI.IFCONFIG0 |= ((1<<16) | (1<<17));
```

- For operation between 6 and 48 MHz, use this configuration step:

```
NRF_QSPI.IFCONFIG0 &= ~(1<<17);
NRF_QSPI.IFCONFIG0 |= (1<<16);
```

3.18 [122] CTRL-AP: Successive triggering of CTRLAP.ERASEALL has no effect

This anomaly applies to Revision 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Network

Conditions

Triggering CTRLAP.ERASEALL more than once.

Consequences

Subsequent triggering of CTRLAP.ERASEALL has no effect.

Workaround

Triggering CTRLAP.ERASEALL multiple times requires a pin reset between each triggering of CTRLAP.ERASEALL.

3.19 [133] QSPI: Degraded radio performance with QSPI

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application

Symptoms

Degraded radio performance during QSPI communication:

- Reduced RX sensitivity during reception.
- Reduced modulation gain during transmission.

Conditions

When radio is receiving or transmitting while QSPI is reading or writing.

Consequences

Radio performance is severely degraded.

Workaround

Use one of the following:

- Use VDD voltage between 1.7 V and 2.0 V to limit the degradation of RX sensitivity to 3 dB across the channels.
- Ensure that QSPI and radio are not operating concurrently.

3.20 [134] RADIO: Incorrect value for IRADIO_TX3

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Network

Symptoms

Radio current higher than stated in Product Specification v1.1.

Conditions

Radio transmitting at 0 dBm output power, 1 Mbps Bluetooth low energy (BLE) mode, clock = HFXO64M, regulator LDO.

Consequences

Current is higher, value in Product Specification v1.2 or newer has the corrected value.

Workaround

None.

3.21 [135] SPIM: No output from SPIM4

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application, Network

Symptoms

There is no output from SPIM4.

Conditions

CPU sleep is triggered after the SPIM4 is enabled but before it starts transmitting.

Consequences

SPIM4 is not functional.

Workaround

Before enabling SPIM4, perform the following step:

```
*(volatile uint32_t *)0x5000ac04 = 1;
```

After disabling SPIM4, perform the following step:

```
*(volatile uint32_t *)0x5000ac04 = 0;
```

3.22 [136] QSPI: QSPI has limited supply voltage range

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application

Symptoms

The QSPI interface is non-functional. The error depends on temperature, voltage and device.

Conditions

VDD voltage is higher than 2.0 V, and the clock frequency is set to 96 MHz.

Consequences

The QSPI interface may operate incorrectly because digital timing is not met.

Workaround

Use one of the following:

- Use VDD voltage between 1.7 V and 2.0 V.
- Use QSPI clock frequency of 48 MHz.

3.23 [137] CLOCK: LFRC calibration is not performed

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application, Network

Symptoms

The DONE event is missing, and the LFRC clock frequency might be incorrect.

Conditions

The LFRC is used with calibration, and one of the following conditions occurs:

- The other CPU is requesting a higher priority source (LFSYNTH or LFXO) during the calibration.
- The user is switching from a higher priority clock source shortly before starting the calibration.

Consequences

The LFRC calibration might not occur, which results in the LFRC not meeting the specified frequency tolerance after calibration.

Workaround

Repeat the calibration every 1 ms until the DONE event is generated.

3.24 [138] COMP: LPCOMP consumes additional current

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application

Symptoms

LPCOMP current might be significantly higher than stated in the Product Specification.

Conditions

LPCOMP is used in System ON mode.

Consequences

Current consumption is high. Error has voltage and temperature dependency with device-to-device variation.

Workaround

None.

3.25 [140] CLOCK: Soft reset during LFRC calibration prevents watchdog reset and LFCLK from being started

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

LFCLK cannot be started. PCLK32KI is stopped.

Conditions

LFCLK calibration is started, and the application core soft resets before the calibration is complete.

Consequences

LFCLK cannot be started and watchdog timer doesn't operate.

Workaround

Use the following application core startup code:

```
if (*(volatile uint32_t *)0x50032420 & 0x80000000)
 {
  /* Reset occured during calibration */
   NRF_CLOCK_S->LFCLKSRC = CLOCK_LFCLKSRC_SRC_LFSYNT;
   NRF_CLOCK_S->TASKS_LFCLKSTART = 1;
   while (NRF_CLOCK_S->EVENTS_LFCLKSTARTED == 0) {}
   NRF_CLOCK_S->EVENTS_LFCLKSTARTED = 0;
   NRF_CLOCK_S->TASKS_LFCLKSTOP = 1;
   NRF_CLOCK_S->LFCLKSRC = CLOCK_LFCLKSRC_SRC_LFRC;
 }
```

3.26 [152] RADIO: Incorrect value for I_S10

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application, Network

Symptoms

Compound current I_S10 is higher than specified in nRF5340 Product Specification v1.2.

Conditions

Application and Network CPUs are running CoreMark from flash, and radio is transmitting at +3 dBm output power in 1 Mbps Bluetooth® Low Energy mode. Application core clock source is set to HFXO at 128 MHz, and Network core is set to HFXO at 64 MHz.

Consequences

Current is higher than 9.1 mA.

Workaround

Use 9.9 mA for nRF5340 Product Specification v1.2 and older.

3.27 [153] GPIOTE: GPIOTE with low-power latency setting does not register IN events in System ON IDLE

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application

Symptoms

GPIOTE IN event is not registered.

Conditions

System is configured in System ON IDLE with HFCLK not running and waking on GPIOTE input IN events with latency set to LATENCY=LowPower.

Consequences

IN event is not functional with GPIOTE LowPower setting.

Workaround

Use PORT event or IN event with LATENCY=LowLatency for detecting transitions on inputs.

3.28 [154] Package: WLCSP package dimension L is incorrect

This anomaly applies to Revision 1, build codes CLAA-D00.

Domains

Application, Network

Symptoms

In nRF5340 Product Specification v1.2's WLCSP dimensions in millimeters table, value L is incorrect.

Conditions

Always.

Consequences

nRF5340-CLAA can be placed too close to other components in PCB assembly.

Workaround

Use correct value 1.9907 mm for L.

3.29 [155] RADIO: Incorrect value for ED_RSSISCALE

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Network

Symptoms

Using value ED_RSSISCALE=5 causes incorrect mapping of the energy detection data and does not comply with the IEEE 802.15.4 standard.

Conditions

The IEEE 802.15.4 energy detection is active and using the ED_RSSISCALE value specified in the nRF5340 Product Specification v1.2 or earlier.

Consequences

Hardware and software combination is not compliant with the IEEE 802.15.4 standard.

Workaround

Use ED_RSSISCALE value specified in nRF5340 Product Specification v1.3 or later.

3.30 [157] CCM: On-the-fly decryption fails for direction finding packets

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Network

Symptoms

MICSTATUS reports CheckFail, and decrypted data is wrong.

Conditions

The header of the received Bluetooth packets has the CP bit set and contains the CTEInfo byte.

Consequences

Direction finding packets are incorrectly rejected.

Workaround

Replace the PPI connection from RADIO EVENTS_ADDRESS event to CCM TASKS_CRYPT with a PPI connection from RADIO EVENTS_BCMATCH to CCM TASKS_CRYPT and configure the RADIO register BCC with the value 3.

3.31 [158] RADIO: Using POWER register clears RADIO trim values

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Network

Symptoms

RADIO performance is degraded.

Conditions

RADIO->POWER register is set to Disabled and then back to Enabled.

Consequences

RADIO trim values in the device startup SystemInit() function are not reloaded.

Workaround

After writing RADIO->POWER to Enabled, perform the following configuration steps before writing to any other RADIO register.

```
/* Copy all the RADIO trim values from FICR into the target addresses.*/
uint32_t index = 0;
for (index = 0; index < 32ul && NRF_FICR_NS->TRIMCNF[index].ADDR != (uint32_t
 *)0xFFFFFFFFul; index++){
    #if defined ( __ICCARM__ )
        /* IAR will complain about the order of volatile pointer accesses. */
        #pragma diag_suppress=Pa082
    #endif
    if (((uint32_t)NRF_FICR_NS->TRIMCNF[index].ADDR & 0xFFFFF000ul) == (volatile
 uint32_t)NRF_RADIO_NS)
    {
        *((volatile uint32_t *)NRF_FICR_NS->TRIMCNF[index].ADDR) = NRF_FICR_NS-
>TRIMCNF[index].DATA;
    }
    #if defined ( __ICCARM__ )
        #pragma diag_default=Pa082
    #endif
}
```

3.32 [159] QSPI: Data can be corrupted in certain clock configurations

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application

Symptoms

QSPI data is corrupted.

Conditions

CLOCK.HFCLK192MCTRL.HCLK192M is not set to 0x0, or CLOCK.HFCLKCTRL.HCLK is not set to 0x1 during QSPI transfer. This means that during QSPI transfer, the scalable QSPI clock (PCLK192M) is not set to 192 MHz or the scalable CPU clock (HCLK128M) is not set to 64 MHz.

Consequences

QSPI transfer and signaling are unreliable.

Workaround

Use CLOCK.HFCLK192MCTRL.HCLK192M = 0x0 and CLOCK.HFCLKCTRL.HCLK = 0x1 during a QSPI transfer. This means that during QSPI transfer, the scalable QSPI clock (PCLK192M) must be set to 192 MHz and the scalable CPU clock (HCLK128M) must be set to 64 MHz.

To save power, use CLOCK.HFCLK192MCTRL.HCLK192M=0x2 when QSPI is disabled.

3.33 [160] REGULATORS: VREGMAIN and VREGRADIO can malfunction in DC/DC mode

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application, Network

Symptoms

Device behaves erratically. This occurs more likely at lower than room temperatures.

Conditions

VREGMAIN or VREGRADIO is in DC/DC mode.

Consequences

CPU lockup reset is triggered, watchdog reset is triggered if watchdog is enabled, or device is unresponsive.

Workaround

On the application core, perform the following operations before enabling DC/DC operation on VREGMAIN or VREGRADIO.

```
*((volatile uint32_t *)0x5000470C) = 0x7Eul;
*((volatile uint32_t *)0x5000493C) = 0x7Eul;
*((volatile uint32_t *)0x50002118) = 0x7Ful;
*((volatile uint32_t *)0x50039E04) = 0x0ul;
*((volatile uint32_t *)0x50039E08) = 0x0ul;
*((volatile uint32_t *)0x50101110) = 0x0ul;
*((volatile uint32_t *)0x50002124) = 0x0ul;
*((volatile uint32_t *)0x5000212C) = 0x0ul;
*((volatile uint32_t *)0x502012A0) = 0x0ul;
```

On the network core, perform the following operations at boot:

```
*((volatile uint32_t *)0x41002118) = 0x7Ful;
*((volatile uint32_t *)0x41080E04) = 0x0ul;
*((volatile uint32_t *)0x41080E08) = 0x0ul;
*((volatile uint32_t *)0x41002124) = 0x0ul;
*((volatile uint32_t *)0x4100212C) = 0x0ul;
*((volatile uint32_t *)0x41101110) = 0x0ul;
```

nRF5340 Product Specification electrical parameters $I_{NETCPU1}$, $I_{NETCPU2}$, $I_{NETCPU4}$, $I_{NETCPU5}$, $I_{APPCPU3}$, $I_{APPCPU5}$, $I_{APPCPU9}$, and $I_{APPCPU11}$ are increased by 5-10%.

In addition to the register write, there is a runtime requirement. Ensure that CPU is not switched between active and sleep (WFI/WFE) more than five times within a 200 µs period.

Implemented workaround:

- Register writes are included in MDK version 8.53.0.
- Workaround is included in nRF Connect SDK version 2.3.0. It covers the register writes and the timing restriction for switching between active and sleep mode. The workaround for the timing restriction is implemented in k_cpu_idle() and k_cpu_atomic_idle().
  - Requirements for application:
    - Must use k_cpu_idle() or k_cpu_atomic_idle() when requesting CPU sleep.
    - Must ensure that the Zephyr system clock is running (CONFIG_SYS_CLOCK_EXISTS=y).

3.34 [161] RESET: Network core is not fully reset after Force-OFF

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application, Network

Symptoms

Network core peripherals or CPU behave erratically after Force-OFF release.

Conditions

Network core is in System ON IDLE state when it is entering Force-OFF or the device enters System OFF mode.

Consequences

Network core peripherals and CPU are not reset. CPU does not restart from the reset vector, and peripherals can behave erratically.

Workaround

When releasing the network core from Force-OFF, use the following code on application core:

```
*(volatile uint32_t *) 0x50005618ul = 1ul;
NRF_RESET->NETWORK.FORCEOFF = (RESET_NETWORK_FORCEOFF_FORCEOFF_Release <<
 RESET_NETWORK_FORCEOFF_FORCEOFF_Pos);
delay_us(5); // Wait for at least five microseconds
NRF_RESET->NETWORK.FORCEOFF = (RESET_NETWORK_FORCEOFF_FORCEOFF_Hold <<
 RESET_NETWORK_FORCEOFF_FORCEOFF_Pos);
delay_us(1); // Wait for at least one microsecond
NRF_RESET->NETWORK.FORCEOFF = (RESET_NETWORK_FORCEOFF_FORCEOFF_Release <<
 RESET_NETWORK_FORCEOFF_FORCEOFF_Pos);
*(volatile uint32_t *) 0x50005618ul = 0ul;
```

3.35 [162] Package: WLCSP package dimension A3 is incorrect

This anomaly applies to Revision 1, build codes CLAA-D00.

Domains

Application, Network

Symptoms

In nRF5340 Product Specification v1.3 and earlier, the value of dimension A3 in the WLCSP dimensions in millimeters table is incorrect.

Conditions

Always.

Consequences

The nRF5340-CLAA wafer thickness does not correspond with the package height.

Workaround

Use 0.266 mm for the A3 Min. value, 0.294 mm for the A3 Nom. value, and 0.322 mm for the A3 Max. value.

3.36 [163] SAADC: Gain error exceeds specified value when using VDD as reference

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application

Symptoms

Gain error is outside the expected range.

Conditions

Supply voltage is 2.1 V or lower, CH[n].CONFIG.REFSEL is set to VDD1_4, and CH[n].CONFIG.GAIN is set to Gain1 or Gain1_2.

Consequences

The minimum specification of parameters $E_{G1/2}$ and E_{G1} can be down to -4%.

Workaround

Use internal reference.

3.37 [165] DEVICE: Network core can malfunction after CPU sleep

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application, Network

Symptoms

Network core behaves erratically.

Conditions

This anomaly depends on the device and temperature and does not apply to all devices. The anomaly can occur when the device is in the following state:

- Both application and network CPU are sleeping (WFI/WFE).
- Both cores are in Low-power submode.
- All peripherals are disabled or enabled and in IDLE state. The following peripherals can be in the listed states:
  - LPCOMP is started.
  - NFC is enabled and in SENSE_FIELD state.
  - GPIOTE input is enabled.

  - RTC is running.
  - WDT is running.
- Network core peripheral or CPU is reacting to GPIOTE PORT event, RTC event, watchdog timeout, LFCLKSTARTED event, power-fail warning event, or SPIS/TWIS activity.

Failures are more likely to occur with short sleep durations and unlikely to occur with sleep durations longer than 150 ms. The estimated failure rates for sleep durations shorter than 30 ms are the following:

- -40°C: On average 150 failures per one million wakeups with device variation between 0 and 100% failures per wakeup.
- -20°C: On average 50 failures per one million wakeups with device variation between 0 and 100% failures per wakeup.
- 0°C: On average 5 failures per one million wakeups with device variation between 0 and 50 failures per one million wakeups.
- +25°C: On average one failure per one million wakeups with device variation between 0 and 25 failures per one million wakeups.

Consequences

Network core CPU can hard-fault, trigger lockup reset, or become unresponsive. Network core can behave erratically.

Workaround

Use nRF Connect SDK version 2.5 or later. The workaround provided in nRF Connect SDK consists of the following parts:

- Mechanism to ensure safe RTC wakeup from sleep
- Mechanism in application core for recovery

The implemented workaround uses system resources such as DPPI and IPC channels, RTC, and WDT. See nRF Connect SDK release notes for details. Do not use the following network core wakeup sources:

- GPIOTE PORT event
- Wakeup from SPIS or TWIS
- Power-fail warning event
- LFCLKSTARTED event

The workaround implemented in nRF Connect SDK reduces the likelihood of the anomaly occurring but does not remove it completely.

With the mechanism to ensure safe RTC wakeup from sleep, the estimated failure rates for sleep durations shorter than 30 ms at -40°C to +25°C are on average 0.05 failures per one million wakeups with device variation between 0 and 20 failures per one million wakeups.

Use the recovery mechanism in nRF SDK version 2.5 or later to recover if a network core lockup reset occurs or the CPU is unresponsive.

Fix for this anomaly is scheduled to be included in the next hardware revision of the nRF5340 SoC.

3.38 [166] REGULATORS: VREGMAIN can malfunction in LDO mode

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application

Symptoms

Device behaves erratically.

Conditions

Device is in a state where the following conditions apply:

- VREGMAIN is in LDO mode.
- Application core register HFCLKCTRL is not set to Div1, which means that the core is not running at 128 MHz.
- Application core register HFCLK192MCTRL is not set to Div1, which means that the scalable 192 MHz clock for QSPI is not running at 192 MHz.
- USBD is disabled.
- SAADC is disabled.
- Application core CPU is entering or exiting sleep mode (WFI/WFE).

Consequences

Application core CPU can hard-fault, trigger lockup reset, or become unresponsive. Application core can behave erratically.

Workaround

If using VREGMAIN in LDO mode, apply the following code after any application core reset:

```
*((volatile uint32_t *)0x50300C00) = 0x00009375ul;
*((volatile uint32_t *)0x503000E4) = 0x0ul;
*((volatile uint32_t *)0x50300C00) = 0x00009375ul;
```

The workaround has the following effect on the electrical parameters specified in the nRF5340 Product Specification v1.3:

Symbol	Description	Typical value in Product Specification	Typical value after workaround	Unit
$I_{ON\_IDLE1,LDO}$	System ON, 0k application RAM, wake on any event, regulator = LDO	3.3	105	µA
$I_{ON\_IDLE2,LDO}$	System ON, wake on any event, regulator = LDO	3.4	105	
$I_{PWM,RUN1,LDO}$	PWM running at 16 MHz, top = 10, duty = 50%; regulator = LDO	1035	1410	
$I_{TIMER2,LDO}$	One TIMER running @ 16 MHz; regulator = LDO	1040	1300	
$I_{TIMER3,LDO}$	One TIMER running @ 16 MHz, clock = HFXO64M; regulator = LDO	1280	1540	
$I_{WDT,APP,LDO}$	Application MCU WDT started; regulator = LDO	4.9	110	
$I_{USB,SUSPEND,VDDH,LDO}$	Current from VDDH supply (high voltage mode), VDD=3 V (VREGH output), all RAM retained, CPU sleeping, USB suspended, regulator = LDO	125	210	

Table 3: Affected electrical parameters in nRF5340 Product Specification v1.3

3.39 [167] USBD: SPU FLASHACCERR is generated after re-enabling USBD

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application

Symptoms

SPU flash access error EVENTS_FLASHACCERROR is generated after USBD EasyDMA transfer is started.

Conditions

The anomaly occurs after the following sequence:

- Write to flash region 0 is prevented by SPU configuration.
- USBD is enabled.
- The sum of all bytes transferred using USBD EasyDMA is odd.
- USBD is disabled.
- USBD is re-enabled.
- USBD EasyDMA transfer is started.

Consequences

The FLASHACCERR event is generated from SPU.

Workaround

If the sum of all bytes transferred using USBD EasyDMA is odd, perform the following steps before disabling USBD:

1. Configure dummy 1-byte transfer on EP IN0.
2. Start TASKS_STARTEPIN[0].
3. Wait for EVENTS_ENDEPIN[0].

The workaround is included in nRF Connect SDK version 2.5.0.

3.40 [168] CPU: CPU can malfunction after sleep

This anomaly applies to Revision 1, build codes CLAA-D00, QKAA-D00.

Domains

Application, Network

Symptoms

The device behaves erratically.

Conditions

Shortly after the CPU and all peripherals have entered IDLE state, the network or application core CPU is woken up by one of the following sources:

- RTC: All events
- GPIOTE: PORT event
- LPCOMP: All events
- NFCT: Field detect event
- WDT: All events
- POWER: All events
- CLOCK: All events
- USBREG: All events
- IPC: All events

Consequences

Network or application core CPU can hard-fault, trigger lockup reset, or become unresponsive. Network or application core can behave erratically.

Workaround

In the network core and application core, disable IRQ before executing WFE or WFI by using the following code:

```
SCB->SCR |= SCB_SCR_SEVONPEND_Msk;
__disable_irq();
__WFE(); // or __WFI();
__nop();__nop();__nop();__nop();__nop();__nop();__nop();__nop(); // 8 NOPs
__enable_irq();
```

If the application core is executing WFE or WFI from RAM with the CPU running at 128 MHz, use 26 NOPs instead of 8 NOPs.

The workaround is included in nRF Connect SDK version 2.5.1.

By default, the workaround is enabled for the application and network cores when running from flash. For additional configurations for running from RAM, see the nRF Connect SDK release notes.