nRF5340

Revision 1

Errata

v1.3

NORDIC® SEMICONDUCTOR

Contents

1 nRF5340 Rev 1 Errata

This Errata document contains anomalies and configurations for the nRF5340 chip, revision Rev 1 (QKAA-D00, CLAA-D00).

The document indicates which anomalies are fixed, inherited, or new compared to revision Engineering D.

2 Revision history

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nRF5340 Rev 1 v1.3	10.02.2022	• Added: No. 140. “Soft reset during LFRC calibration prevents watchdog reset and LFCLK from being started”
nRF5340 Rev 1 v1.2	03.12.2021	• Added: No. 133. “Degraded radio performance with QSPI” • Added: No. 135. “No output from SPIM4” • Added: No. 136. “QSPI has limited supply voltage range” • Added: No. 137. “LFRC calibration is not performed”
nRF5340 Rev 1 v1.1	22.10.2021	• Added: No. 134. “Incorrect value for IRADIO_TX3” • Added: No. 138. “LPCOMP consumes additional current”
nRF5340 Rev1 v1.0	03.12.2020	• Added: No. 6. “Disabling instruction cache causes skip of next instruction” • Added: No. 43. “Reading QSPI registers after XIP might halt application CPU” • Added: No. 44. “TASKS_RESUME impacts UARTE” • Added: No. 47. “I2C timing spec is violated at 400 kHz” • Added: No. 55. “Bits in RESETREAS are set when they should not be” • Added: No. 65. “Events are not generated when switching from scan mode to no-scan mode with BURST disabled” • Added: No. 70. “Event FIELDDETECTED may be generated too early” • Added: No. 71. “Frame delay timing is too short after SLP_REQ” • Added: No. 75. “False SEQEND[0] and SEQEND[1] events are generated” • Added: No. 76. “Non-secure code can detect secure events” • Added: No. 87. “RSSI parameter adjustment” • Added: No. 99. “Mode 3 is not functional at 96 MHz” • Added: No. 112. “24-bit sample in a 32-bit half-frame is received incorrectly” • Added: No. 113. “Reading DTX in MODECNF0 gives incorrect value” • Added: No. 117. “Changing MODE requires additional configuration” • Added: No. 119. “Writes to LATCH register take several CPU cycles to take effect” • Added: No. 121. “Configuration of peripheral requires additional steps” • Added: No. 122. “Successive triggering of CTRLAP.ERASEALL has no effect”

3 New and inherited anomalies

The following anomalies are present in revision Rev 1 of the nRF5340 chip.

ID	Domain	Module	Description	New in Rev 1	Inherited from Engineering D
6	Network	NVMC	Disabling instruction cache causes skip of next instruction		X
43	Application	QSPI	Reading QSPI registers after XIP might halt application CPU		X
44	Application, Network	UARTE	TASKS_RESUME impacts UARTE		X
47	Application, Network	TWIM	I2C timing spec is violated at 400 kHz		X
55	Application, Network	RESET	Bits in RESETREAS are set when they should not be		X
65	Application	SAADC	Events are not generated when switching from scan mode to no-scan mode with BURST disabled		X
70	Application	NFCT	Event FIELDDETECTED may be generated too early		X
71	Application	NFCT	Frame delay timing is too short after SLP_REQ		X
75	Application	PWM	False SEQEND[0] and SEQEND[1] events are generated		X
76	Application	DPPI	Non-secure code can detect secure events		X
87	Network	RADIO	RSSI parameter adjustment		X
99	Application	QSPI	Mode 3 is not functional at 96 MHz		X
112	Application	I2S	24-bit sample in a 32-bit half-frame is received incorrectly		X
113	Network	RADIO	Reading DTX in MODECNF0 gives incorrect value		X
117	Network	RADIO	Changing MODE requires additional configuration		X
119	Network	GPIO	Writes to LATCH register take several CPU cycles to take effect		X
121	Application	QSPI	Configuration of peripheral requires additional steps		X
122	Network	CTRL-AP	Successive triggering of CTRLAP.ERASEALL has no effect		X
133	Application	QSPI	Degraded radio performance with QSPI	X	
134	Network	RADIO	Incorrect value for IRADIO_TX3	X	

ID	Domain	Module	Description	New in Rev 1	Inherited from Engineering D
135	Application, Network	SPIM	No output from SPIM4	X	
136	Application	QSPI	QSPI has limited supply voltage range	X	
137	Application, Network	CLOCK	LFRC calibration is not performed	X	
138	Application	COMP	LPCOMP consumes additional current	X	
140	Application	CLOCK	Soft reset during LFRC calibration prevents watchdog reset and LFCLK from being started		X

Table 1: New and inherited anomalies

3.1 [6] NVMC: Disabling instruction cache causes skip of next instruction

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Network

Symptoms

The CPU skips the first instruction after instruction cache is disabled.

Conditions

The code executes instructions to disable the instruction cache.

Consequences

The program does not execute as expected.

Workaround

Use the following function to disable instruction cache:

```
_attribute_((aligned(ICACHE_LINE_SIZE)))

void icache_disable(void) {
    int key = DisableInterrupts();
    __ISB();
    NRF_NVMC->ICACHECNF = 0;
    __ISB();
    EnableInterrupts(key);
}
```

3.2 [43] QSPI: Reading QSPI registers after XIP might halt application CPU

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

Application CPU halts.

Conditions

Init and start QSPI, use XIP, then write to or read any QSPI register starting from offset 0x600 and above.

Consequences

Application CPU halts.

Workaround

Trigger QSPI TASKS_ACTIVATE after XIP is used before accessing any QSPI register with an offset above 0x600.

3.3 [44] UARTE: TASKS_RESUME impacts UARTE

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application, Network

Symptoms

Issuing TASKS_RESUME results in bits being set in the UARTE ERRORSRC register after it is enabled, even when not started.

Conditions

The internal state of a disabled UARTE changes when any of the tasks TASKS_RESUME, TASKS_STARTRX, or TASKS_STARTTX is triggered. These tasks are shared by UARTE, TWIM, TWIS, and SPIM.

Consequences

UARTE starts transmitting immediately after being enabled.

Workaround

Depending on which UARTE instance is affected, apply the following steps before enabling UARTE.

- If TXENABLE reads '1', trigger TASKS_STOPTX.
- If RXENABLE reads '1':
  - Enable UARTE.
  - Trigger TASKS_STOPRX.
  - Wait until RXENABLE reads '0'.
  - Clear ERRORSRC register.

The exact address depends on the UARTE instance. See the following table.

UARTE Instance	RXENABLE	TXENABLE
UARTE0:NS	0x40008564	0x40008568
UARTE0:S	0x50008564	0x50008568
UARTE1:NS	0x40009564	0x40009568
UARTE1:S	0x50009564	0x50009568
UARTE2:NS	0x4000B564	0x4000B568
UARTE2:S	0x5000B564	0x5000B568
UARTE3:NS	0x4000C564	0x4000C568
UARTE3:S	0x5000C564	0x5000C568

Table 2: Register addresses

3.4 [47] TWIM: I2C timing spec is violated at 400 kHz

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application, Network

Symptoms

The low period of the SCL clock is too short to meet the I2C specification at 400 kHz. The actual low period of the SCL clock is 1.25 µs while the I2C specification requires the SCL clock to have a minimum low period of 1.3 µs.

Conditions

Using TWIM at 400 kHz.

Consequences

TWI communication might not work at 400 kHz with I2C compatible devices.

Workaround

If communication does not work at 400 kHz with an I2C compatible device that requires the SCL clock to have a minimum low period of 1.3 µs, use 390 kHz instead of 400 kHz by writing 0x06200000 to the FREQUENCY register. With this setting, the SCL low period is greater than 1.3 µs.

3.5 [55] RESET: Bits in RESETREAS are set when they should not be

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application, Network

Symptoms

After pin reset, RESETREAS bits other than RESETPIN might also be set.

Conditions

A pin reset has triggered.

Consequences

If the firmware evaluates RESETREAS, it might take the wrong action.

Workaround

When RESETREAS shows a pin reset (RESETPIN), ignore other reset reason bits.

> **Note:** RESETREAS bits must be cleared between resets.

Apply the following code after any reset:

```
For Application:
if (NRF_RESET_S->RESETREAS & RESET_RESETREAS_RESETPIN_Msk)
{
    NRF_RESET_S->RESETREAS = ~RESET_RESETREAS_RESETPIN_Msk;
}
For Network:
if (NRF_RESET->RESETREAS & RESET_RESETREAS_RESETPIN_Msk)
{
    NRF_RESET->RESETREAS = ~RESET_RESETREAS_RESETPIN_Msk;
}
```

This workaround is implemented in MDK version 8.29.0 and later.

3.6 [65] SAADC: Events are not generated when switching from scan mode to no-scan mode with BURST disabled

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

SAADC stops working.

Conditions

Switching from single channel to multiple channels when BURST is disabled and acquisition time less than 10 us.

Consequences

SAADC internally locks up and does not generate the expected events.

Workaround

Execute the following code before changing the channel configuration.

- Secure mode:

```
NRF_SAADC_S->TASKS_STOP = 1;
```

- Non-secure mode:

```
NRF_SAADC_NS->TASKS_STOP = 1;
```

3.7 [70] NFCT: Event FIELDDETECTED may be generated too early

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

Reset of the operating state after FIELDLOST event. In some cases, communication with the peer device is not possible.

Conditions

Especially with stronger field strengths.

Consequences

Restart of transfer is required.

Workaround

On FIELDDETECTED event, wait 1 ms using timer before starting NFC communication with NRF_NFCT->TASKS_ACTIVATE.

This workaround is included in nrfx v2.0.0 and later.

3.8 [71] NFCT: Frame delay timing is too short after SLP_REQ

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

Reader may not accept the response from the tag.

Conditions

The time between SLP_REQ and ALL_REQ sent by the Reader is shorter than the time configured in FRAMEDELAYMAX.

Consequences

The protocol timing is violated, and a Reader may not accept the response from the tag.

Workaround

Ensure that FRAMEDELAYMAX is set to the default value when the NFCT is in states IDLE or SLEEP_A. The workaround is included in nrfx v2.0.0 and later.

3.9 [75] PWM: False SEQEND[0] and SEQEND[1] events are generated

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

False SEQEND[0] and SEQEND[1] events are generated.

Conditions

Any of the LOOPSDONE_SEQSTARTn shortcuts are enabled. LOOP register is nonzero and SEQ[1].CNT is set to 1.

Consequences

SEQEND[0] and SEQEND[1] events might falsely trigger other tasks if they are routed through the PPI.

Workaround

Avoid using the LOOPSDONE_SEQSTARTn shortcuts when the LOOP register is nonzero and SEQ[1].CNT is set to 1.

3.10 [76] DPPI: Non-secure code can detect secure events

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

Non-secure code is able to detect that a secure event has been published to a secure DPPI channel.

Conditions

In a non-secure DPPI channel group, SUBSCRIBE_CHG[n].EN or SUBSCRIBE_CHG[n].DIS is set up to be connected to a secure DPPI channel.

Consequences

Non-secure code can detect that a secure event has been published to a secure DPPI channel. The non-secure code cannot detect which event has been published.

Workaround

Perform one of the following:

- Avoid using DPPI in secure mode.
- Configure all channel groups (CHG[n]) to include at least one DPPI channel that is configured as secure. This makes the channel groups secure and blocks them from being used on the non-secure side.

> **Note:** The non-secure domain can still use the DPPI tasks and events system, but it does not have any available channel groups.

3.11 [87] RADIO: RSSI parameter adjustment

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Network

Symptoms

RSSI varies with temperature and input power level.

Conditions

Always.

Consequences

RSSI parameter is not within specified accuracy.

Workaround

Add the following compensation to the RSSI sample value based on temperature measurement and RSSISAMPLE. The on-chip TEMP peripheral can be used to measure temperature.

```
compensated_rssi = (uint8_t)round(
    (float)((float)(1.56f * rssi_sample) + (float)(4.9e-5 * pow(rssi_sample, 3)) -
    (float)(9.9e-3 * pow(rssi_sample, 2)) - (0.05f * ((float)(temp)*0.25f)) - 7.2f));
```

where

temp
: Temperature sample value as reported by register NRF_TEMP.TEMP in increments of 0.25.

drssi_sample
: Sample value as reported by register NRF_RADIO.RSSISAMPLE.

3.12 [99] QSPI: Mode 3 is not functional at 96 MHz

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

Mode 3 is not functional at 96 MHz.

Conditions

Always.

Consequences

Mode 3 can be used only from 6 to 48 MHz.

Workaround

Use speed between 6 and 48 MHz or use Mode 0 to have full speed range.

3.13 [112] I2S: 24-bit sample in a 32-bit half-frame is received incorrectly

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

24-bit sample in a 32-bit half-frame is received incorrectly.

Conditions

CONFIG.SWIDTH is configured to 24BitIn32.

Consequences

24-bit sample in 32-bit word has incorrect data from bits 25-31.

Workaround

Leave the first 24 bits in 32-bit word as is. Replace the 8 MSB bits of the 32-bit word by sign-extending the 24th bit.

3.14 [113] RADIO: Reading DTX in MODECNF0 gives incorrect value

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Network

Symptoms

Reading DTX in MODECNF0 gives incorrect value.

Conditions

Always.

Consequences

Reading the MODECNF0.DTX field returns an incorrect value.

Workaround

Treat the MODECNF0.DTX field as write only.

3.15 [117] RADIO: Changing MODE requires additional configuration

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Network

Symptoms

Radio modulation index is lower than expected.

Conditions

Always.

Consequences

RADIO may fail qualification tests or have higher than expected packet loss. Measured modulation characteristics for Bluetooth and error vector magnitude for IEEE802.15.4 are affected.

Workaround

After writing the RADIO.MODE register, perform the following additional configuration steps.

- When RADIO.MODE is set to Nrf_2Mbit, Ble_2Mbit, or Ieee802154_250Kbit, use the following:

```
*((volatile uint32_t *)0x41008588) = *((volatile uint32_t *)0x01FF0084);
```

- When RADIO.MODE is set to any other mode, use the following:

```
*((volatile uint32_t *)0x41008588) = *((volatile uint32_t *)0x01FF0080);
```

3.16 [119] GPIO: Writes to LATCH register take several CPU cycles to take effect

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Network

Symptoms

A bit in the LATCH register reads '1' even after clearing it by writing '1'.

Conditions

Reading the LATCH register right after writing to it.

Consequences

Old value of the LATCH register is read.

Workaround

Have at least 4 CPU cycles of delay between the write and the subsequent read to the LATCH register. This can be achieved by having 4 dummy reads of the LATCH register.

3.17 [121] QSPI: Configuration of peripheral requires additional steps

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

QSPI is unstable or not working at all.

Conditions

Always.

Consequences

QSPI does not work as expected.

Workaround

When configuring QSPI, ensure register IFTIMING.RXDELAY = 6 and perform the following additional configuration steps.

- For operation at 96 MHz, perform the following extra configuration step:

```
NRF_QSPI.IFCONFIG0 |= ((1<<16) | (1<<17));
```

- For operation between 6 and 48 MHz, use this configuration step:

```
NRF_QSPI.IFCONFIG0 &= ~(1<<17);
NRF_QSPI.IFCONFIG0 |= (1<<16);
```

3.18 [122] CTRL-AP: Successive triggering of CTRLAP.ERASEALL has no effect

This anomaly applies to IC Rev. Rev 1, build codes QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Network

Conditions

Triggering CTRLAP.ERASEALL more than once.

Consequences

Subsequent triggering of CTRLAP.ERASEALL has no effect.

Workaround

Triggering CTRLAP.ERASEALL multiple times requires a pin reset between each triggering of CTRLAP.ERASEALL.

3.19 [133] QSPI: Degraded radio performance with QSPI

This anomaly applies to IC Rev. Rev 1, build codes CLAA-D00, QKAA-D00.

Domains

Application

Symptoms

Degraded radio performance during QSPI communication:

- Reduced RX sensitivity during reception.
- Reduced modulation gain during transmission.

Conditions

When radio is receiving or transmitting while QSPI is reading or writing.

Consequences

Radio performance is severely degraded.

Workaround

Use one of the following:

- Use VDD voltage between 1.7 V and 2.0 V to limit the degradation of RX sensitivity to 3 dB across the channels.
- Ensure that QSPI and radio are not operating concurrently.

3.20 [134] RADIO: Incorrect value for IRADIO_TX3

This anomaly applies to IC Rev. Rev 1, build codes CLAA-D00, QKAA-D00.

Domains

Network

Symptoms

Radio current higher than stated in Product Specification v1.1.

Conditions

Radio transmitting at 0 dBm output power, 1 Mbps Bluetooth low energy (BLE) mode, clock = HFXO64M, regulator LDO.

Consequences

Current is higher, value in Product Specification v1.2 or newer has the corrected value.

Workaround

None.

3.21 [135] SPIM: No output from SPIM4

This anomaly applies to IC Rev. Rev 1, build codes CLAA-D00, QKAA-D00.

Domains

Application, Network

Symptoms

There is no output from SPIM4.

Conditions

CPU sleep is triggered after the SPIM4 is enabled but before it starts transmitting.

Consequences

SPIM4 is not functional.

Workaround

Before enabling SPIM4, perform the following step:

```
*(volatile uint32_t *)0x5000ac04 = 1;
```

After disabling SPIM4, perform the following step:

```
*(volatile uint32_t *)0x5000ac04 = 0;
```

3.22 [136] QSPI: QSPI has limited supply voltage range

This anomaly applies to IC Rev. Rev 1, build codes CLAA-D00, QKAA-D00.

Domains

Application

Symptoms

The QSPI interface is non-functional. The error depends on temperature, voltage and device.

Conditions

VDD voltage is higher than 2.0 V, and the clock frequency is set to 96 MHz.

Consequences

The QSPI interface may operate incorrectly because digital timing is not met.

Workaround

Use one of the following:

- Use VDD voltage between 1.7 V and 2.0 V.
- Use QSPI clock frequency of 48 MHz.

3.23 [137] CLOCK: LFRC calibration is not performed

This anomaly applies to IC Rev. Rev 1, build codes CLAA-D00, QKAA-D00.

Domains

Application, Network

Symptoms

The DONE event is missing, and the LFRC clock frequency might be incorrect.

Conditions

The LFRC is used with calibration, and one of the following conditions occurs:

- The other CPU is requesting a higher priority source (LFSYNTH or LFXO) during the calibration.
- The user is switching from a higher priority clock source shortly before starting the calibration.

Consequences

The LFRC calibration might not occur, which results in the LFRC not meeting the specified frequency tolerance after calibration.

Workaround

Repeat the calibration every 1 ms until the DONE event is generated.

3.24 [138] COMP: LPCOMP consumes additional current

This anomaly applies to IC Rev. Rev 1, build codes CLAA-D00, QKAA-D00.

Domains

Application

Symptoms

LPCOMP current might be significantly higher than stated in the Product Specification.

Conditions

LPCOMP is used in System ON mode.

Consequences

Current consumption is high. Error has voltage and temperature dependency with device-to-device variation.

Workaround

None.

3.25 [140] CLOCK: Soft reset during LFRC calibration prevents watchdog reset and LFCLK from being started

This anomaly applies to IC Rev. Rev 1, build codes CLAA-D00, QKAA-D00.

It was inherited from the previous IC revision Engineering D.

Domains

Application

Symptoms

LFCLK cannot be started. PCLK32KI is stopped.

Conditions

LFCLK calibration is started, and the application core soft resets before the calibration is complete.

Consequences

LFCLK cannot be started and watchdog timer doesn't operate.

Workaround

Use the following application core startup code:

```
if (*(volatile uint32_t *)0x50032420 & 0x80000000)
 {
  /* Reset occured during calibration */
   NRF_CLOCK_S->LFCLKSRC = CLOCK_LFCLKSRC_SRC_LFSYNT;
   NRF_CLOCK_S->TASKS_LFCLKSTART = 1;
   while (NRF_CLOCK_S->EVENTS_LFCLKSTARTED == 0) {}
   NRF_CLOCK_S->EVENTS_LFCLKSTARTED = 0;
   NRF_CLOCK_S->TASKS_LFCLKSTOP = 1;
   NRF_CLOCK_S->LFCLKSRC = CLOCK_LFCLKSRC_SRC_LFRC;
 }
```