nRF52840

Rev 2

Errata

v1.1

NORDIC® SEMICONDUCTOR

Contents

1 nRF52840 Rev 2 Errata

This Errata document contains anomalies for the nRF52840 chip, revision Rev 2 (QIAA-Dx0, CKAA-Dx0).

The document indicates which anomalies are fixed, inherited, or new compared to revision Engineering D nRF52840.

2 Change log

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nRF52840 Rev 2 v1.1	12.09.2019	• Added: No. 213. “WDT configuration is cleared when entering system OFF” • Added: No. 214. “Incorrect data transferred” • Added: No. 215. “Reading QSPI registers after XIP might halt CPU” • Added: No. 219. “I2C timing spec is violated at 400 kHz”

Version	Date	Change
nRF52840 Rev 2 v1.0	31.01.2019	• Added: No. 20. “Register values are invalid” • Added: No. 36. “Some registers are not reset when expected” • Added: No. 55. “RXPTRUPD and TXPTRUPD events asserted after STOP” • Added: No. 66. “Linearity specification not met with default settings” • Added: No. 78. “High current consumption when using timer STOP task only” • Added: No. 81. “PIN_CNF is not retained when in debug interface mode” • Added: No. 87. “Unexpected wake from System ON Idle when using FPU” • Added: No. 122. “QSPI uses current after being disabled” • Added: No. 136. “Bits in RESETREAS are set when they should not be” • Added: No. 153. “RSSI parameter adjustment” • Added: No. 155. “IN event may occur more than once on input edge” • Added: No. 166. “ISO double buffering not functional” • Added: No. 170. “NRF_I2S->PSEL CONNECT fields are not readable” • Added: No. 171. “USB might not power up” • Added: No. 172. “BLE long range co-channel performance ” • Added: No. 173. “Writes to LATCH register take several CPU cycles to take effect” • Added: No. 174. “SPIM3 events incorrectly connected to the PPI” • Added: No. 176. “Flash erase through CTRL-AP fails due to watchdog time-out” • Added: No. 179. “COMPARE event is generated twice from a single RTC compare match” • Added: No. 183. “False SEQEND[0] and SEQEND[1] events” • Added: No. 184. “Erase or write operations from the external debugger fail when CPU is not halted” • Added: No. 187. “USB cannot be enabled” • Added: No. 190. “Event FIELDDETECTED may be generated too early” • Added: No. 191. “High packet error rate in BLE Long Range mode” • Added: No. 193. “SPIM3 does not generate EVENTS_END and halts if suspended during last byte” • Added: No. 194. “STOP task does not switch off all resources” • Added: No. 195. “SPIM3 continues to draw current after disable” • Added: No. 196. “PSEL acquires GPIOs regardless of ENABLE” • Added: No. 198. “SPIM3 transmit data might be corrupted” • Added: No. 199. “USBD cannot receive tasks during DMA” • Added: No. 204. “Switching beween TX and RX causes unwanted emissions” • Added: No. 208. “PPI Deactivate task does not switch off all resources” • Added: No. 209. “LFRC ULP mode calibration not functional” • Added: No. 210. “Bits in GPIO LATCH register are incorrectly set to 1”

3 New and inherited anomalies

The following anomalies are present in revision Rev 2 of the nRF52840 chip.

ID	Module	Description	Inherited from Engineering D nRF52840
20	RTC	Register values are invalid	X
36	CLOCK	Some registers are not reset when expected	X
55	I2S	RXPTRUPD and TXPTRUPD events asserted after STOP	X
66	TEMP	Linearity specification not met with default settings	X
78	TIMER	High current consumption when using timer STOP task only	X
81	GPIO	PIN_CNF is not retained when in debug interface mode	X
87	CPU	Unexpected wake from System ON Idle when using FPU	X
122	QSPI	QSPI uses current after being disabled	X
136	System	Bits in RESETREAS are set when they should not be	X
153	RADIO	RSSI parameter adjustment	X
155	GPIOTE	IN event may occur more than once on input edge	X
166	USBD	ISO double buffering not functional	X
170	I2S	NRF_I2S->PSEL CONNECT fields are not readable	X
171	USB,USBD	USB might not power up	X
172	RADIO	BLE long range co-channel performance	X
173	GPIO	Writes to LATCH register take several CPU cycles to take effect	X
174	SPIM	SPIM3 events incorrectly connected to the PPI	X
176	System	Flash erase through CTRL-AP fails due to watchdog time-out	X
179	RTC	COMPARE event is generated twice from a single RTC compare match	X
183	PWM	False SEQEND[0] and SEQEND[1] events	X
184	NVMC	Erase or write operations from the external debugger fail when CPU is not halted	X
187	USBD	USB cannot be enabled	X
190	NFCT	Event FIELDDETECTED may be generated too early	X
191	RADIO	High packet error rate in BLE Long Range mode	X
193	SPIM	SPIM3 does not generate EVENTS_END and halts if suspended during last byte	X

ID	Module	Description	Inherited from Engineering D nRF52840
194	I2S	STOP task does not switch off all resources	X
195	SPIM	SPIM3 continues to draw current after disable	X
196	I2S	PSEL acquires GPIOs regardless of ENABLE	X
198	SPIM	SPIM3 transmit data might be corrupted	X
199	USBD	USBD cannot receive tasks during DMA	X
204	RADIO	Switching beween TX and RX causes unwanted emissions	X
208	QSPI	PPI Deactivate task does not switch off all resources	X
209	CLOCK	LFRC ULP mode calibration not functional	X
210	GPIO	Bits in GPIO LATCH register are incorrectly set to 1	X
213	WDT	WDT configuration is cleared when entering system OFF	X
214	SPIS	Incorrect data transferred	X
215	QSPI	Reading QSPI registers after XIP might halt CPU	X
219	TWIM	I2C timing spec is violated at 400 kHz	X

Table 1: New and inherited anomalies

3.1 [20] RTC: Register values are invalid

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

RTC registers will not contain the correct/expected value if read.

Conditions

The RTC has been idle.

Consequences

RTC configuration cannot be determined by reading RTC registers.

Workaround

Execute the below code before you use RTC.

```
NRF_CLOCK->EVENTS_LFCLKSTARTED  = 0;
NRF_CLOCK->TASKS_LFCLKSTART     = 1;
while (NRF_CLOCK->EVENTS_LFCLKSTARTED == 0) {}
NRF_RTC0->TASKS_STOP = 0;
```

3.2 [36] CLOCK: Some registers are not reset when expected

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

After watchdog timeout reset, CPU lockup reset, soft reset, or pin reset, the following CLOCK peripheral registers are not reset:

- CLOCK->EVENTS_DONE
- CLOCK->EVENTS_CTTO
- CLOCK->CTIV

Conditions

After watchdog timeout reset, CPU Lockup reset, soft reset, and pin reset.

Consequences

Register reset values might be incorrect. It may cause undesired interrupts in case of enabling interrupts without clearing the DONE or CTTO events.

Workaround

Clear affected registers after reset. This workaround has already been added into system_nrf52.c file. This workaround has already been added into system_nrf52840.c file present in MDK 8.11.0 or later.

3.3 [55] I2S: RXPTRUPD and TXPTRUPD events asserted after STOP

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

The RXPTRUPD event is generated when the STOP task is triggered, even though reception (RX) is disabled. Similarly, the TXPTRUPD event is generated when the STOP task is triggered, even though transmission (TX) is disabled.

Conditions

A previous transfer has been performed with RX/TX enabled, respectively.

Consequences

The indication that RXTXD.MAXCNT words were received/transmitted is false.

Workaround

Ignore the RXPTRUPD and TXPTRUPD events after triggering the STOP task. Clear these events before starting the next transfer.

3.4 [66] TEMP: Linearity specification not met with default settings

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

TEMP module provides non-linear temperature readings over the specified temperature range.

Conditions

Always.

Consequences

TEMP module returns out of spec temperature readings.

Workaround

Execute the following code after reset:

```
NRF_TEMP->A0 = NRF_FICR->TEMP.A0;
NRF_TEMP->A1 = NRF_FICR->TEMP.A1;
NRF_TEMP->A2 = NRF_FICR->TEMP.A2;
NRF_TEMP->A3 = NRF_FICR->TEMP.A3;
NRF_TEMP->A4 = NRF_FICR->TEMP.A4;
NRF_TEMP->A5 = NRF_FICR->TEMP.A5;
NRF_TEMP->B0 = NRF_FICR->TEMP.B0;
NRF_TEMP->B1 = NRF_FICR->TEMP.B1;
NRF_TEMP->B2 = NRF_FICR->TEMP.B2;
NRF_TEMP->B3 = NRF_FICR->TEMP.B3;
NRF_TEMP->B4 = NRF_FICR->TEMP.B4;
NRF_TEMP->B5 = NRF_FICR->TEMP.B5;
NRF_TEMP->T0 = NRF_FICR->TEMP.T0;
NRF_TEMP->T1 = NRF_FICR->TEMP.T1;
NRF_TEMP->T2 = NRF_FICR->TEMP.T2;
NRF_TEMP->T3 = NRF_FICR->TEMP.T3;
NRF_TEMP->T4 = NRF_FICR->TEMP.T4;
```

This code is already present in the latest system_nrf52.c file and in the system_nrf52840.c file released in MDK 8.12.0.

3.5 [78] TIMER: High current consumption when using timer STOP task only

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

Increased current consumption when the timer has been running and the STOP task is used to stop it.

Conditions

The timer has been running (after triggering a START task) and then it is stopped using a STOP task only.

Consequences

Increased current consumption.

Workaround

Use the SHUTDOWN task after the STOP task or instead of the STOP task.

3.6 [81] GPIO: PIN_CNF is not retained when in debug interface mode

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

GPIO pin configuration is reset on wakeup from System OFF.

Conditions

The system is in debug interface mode.

Consequences

GPIO state unreliable until PIN_CNF is reconfigured.

3.7 [87] CPU: Unexpected wake from System ON Idle when using FPU

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

The CPU is unexpectedly awoken from System ON Idle.

Conditions

The FPU has been used.

Consequences

The CPU is awoken from System ON Idle.

Workaround

The FPU can generate pending interrupts just like other peripherals, but unlike other peripherals there are no INTENSET, INTENCLR registers for enabling or disabling interrupts at the peripheral level. In order to prevent unexpected wake-up from System ON Idle, add this code before entering sleep:

```
#if (__FPU_USED == 1)
 _set_FPSCR(_get_FPSCR() & ~(0x0000009F));
 (void) __get_FPSCR();
 NVIC_ClearPendingIRQ(FPU_IRQn);
#endif
 __WFE();
```

3.8 [122] QSPI: QSPI uses current after being disabled

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

Current consumption is too high.

Conditions

After QSPI has been activated by the use of TASKS_ACTIVATE task.

Consequences

Current consumption is too high.

Workaround

Execute the following code before disabling QSPI:

```
*(volatile uint32_t *)0x40029010ul = 1ul;
*(volatile uint32_t *)0x40029054ul = 1ul
```

3.9 [136] System: Bits in RESETREAS are set when they should not be

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

After pin reset, RESETREAS bits other than RESETPIN might also be set.

Conditions

A pin reset has triggered.

Consequences

If the firmware evaluates RESETREAS, it might take the wrong action.

Workaround

When RESETREAS shows a pin reset (RESETPIN), ignore other reset reason bits.

> **Important:** RESETREAS bits must be cleared between resets.

Apply the following code after any reset:

```
if (NRF_POWER->RESETREAS & POWER_RESETREAS_RESETPIN_Msk){
    NRF_POWER->RESETREAS =  ~POWER_RESETREAS_RESETPIN_Msk;
}
```

This workaround is implemented in MDK version 8.13.0 and later.

3.10 [153] RADIO: RSSI parameter adjustment

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

RSSI changes over temperature.

Conditions

Temperature ≤ +10°C or > +30°C.

Consequences

RSSI parameter not within specified accuracy.

Workaround

Add the following compensation to the RSSI sample value based on temperature measurement (the on-chip TEMP peripheral can be used to measure temperature):

- For TEMP ≤ -30°C, RSSISAMPLE = RSSISAMPLE +3
- For TEMP > -30°C and TEMP ≤ -10°C, RSSISAMPLE = RSSISAMPLE +2
- For TEMP > -10°C and TEMP ≤ +10°C, RSSISAMPLE = RSSISAMPLE +1
- For TEMP > +10°C and TEMP ≤ +30°C, RSSISAMPLE = RSSISAMPLE + 0
- For TEMP > +30°C and TEMP ≤ +50°C, RSSISAMPLE = RSSISAMPLE - 1
- For TEMP > +50°C and TEMP ≤ +70°C, RSSISAMPLE = RSSISAMPLE - 2
- For TEMP > +70°C, RSSISAMPLE = RSSISAMPLE - 3

3.11 [155] GPIOTE: IN event may occur more than once on input edge

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

IN event occurs more than once on an input edge.

Conditions

Input signal edges are closer together than 1.3 µs or >= 750 kHz for a periodic signal.

Consequences

Tasks connected through PPI or SHORTS to this event might be triggered twice.

Workaround

Apply the following code when any GPIOTE channel is configured to generate an IN event on edges that can occur within 1.3 µs of each other:

```
*(volatile uint32_t *)(NRF_GPIOTE_BASE + 0x600 + (4 * GPIOTE_CH_USED)) = 1;
```

Important: A clock is kept on by the workaround and must be reverted to avoid higher current consumption when GPIOTE is not in use, using the following code:

```
*(volatile uint32_t *)(NRF_GPIOTE_BASE + 0x600 + (4 * GPIOTE_CH_USED)) = 0;
```

3.12 [166] USBD: ISO double buffering not functional

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

The double buffering of the ISO EPs of the USBD is not functional.

Conditions

Always. With default settings, the buffers overlap.

Consequences

During ISO transition, received or transmitted data is likely to be corrupted.

Workaround

Reconfigure ISO buffers during initialization of USBD. After each time the USBD peripheral is enabled, apply the following code:

```
*((volatile uint32_t *)(NRF_USBD_BASE + 0x800)) = 0x7E3;
*((volatile uint32_t *)(NRF_USBD_BASE + 0x804)) = 0x40;
```

3.13 [170] I2S: NRF_I2S->PSEL CONNECT fields are not readable

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

- CONNECT field of NRF_I2S->PSEL.MCK is not readable.
- CONNECT field of NRF_I2S->PSEL.SCK is not readable.
- CONNECT field of NRF_I2S->PSEL.LRCK is not readable.
- CONNECT field of NRF_I2S->PSEL.SDIN is not readable.
- CONNECT field of NRF_I2S->PSEL.SDOUT is not readable.

Conditions

Always.

Consequences

When reading the value of NRF_I2S->PSEL registers, the CONNECT field might not return the same value that has been written to it.

Workaround

None.

3.14 [171] USB,USBD: USB might not power up

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

The USBD might not reach its active state. It is also possible that the USBD reaches its active state, but with an increased delay.

Conditions

Firmware enables USBD or exits USBD low power mode (clears USBD->LOWPOWER) and enters System ON IDLE before the USBD module is fully powered up.

Consequences

The USBD sometimes does not function.

Workaround

To enable the USBD (USBD.ENABLE = 1) or to wake the USBD during SUSPEND (USBD.LOWPOWER = 0), apply the following code:

```
if(*(volatile uint32_t *)0x4006EC00 == 0x00000000)
{
  *(volatile uint32_t *)0x4006EC00 = 0x00009375;
}
*(volatile uint32_t *)0x4006EC14 = 0x000000C0;
*(volatile uint32_t *)0x4006EC00 = 0x00009375;

NRF_USBD->ENABLE = 0x00000001; // or NRF_USBD->LOWPOWER = 0x00000000;
```

After receiving the corresponding acknowledgment event (i.e. USBD.EVENTS_USBEVENT with USBD.EVENTCAUSE.READY=1 in case of enabling or USBD->EVENTCAUSE.USBWUALLOWED=1 in case of wakeup), apply the following code:

```
if(*(volatile uint32_t *)0x4006EC00 == 0x00000000)
{
  *(volatile uint32_t *)0x4006EC00 = 0x00009375;
}
*(volatile uint32_t *)0x4006EC14 = 0x00000000;
*(volatile uint32_t *)0x4006EC00 = 0x00009375;
```

3.15 [172] RADIO: BLE long range co-channel performance

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

Packet loss when a blocker signal is present.

Conditions

BLE long range (Ble_LR125Kbit or Ble_LR500Kbit). Blocker signal present at the same or nearby RF frequency.

Consequences

Fails BLE test with co-channel interference (RF-PHY/RCV/BV-29-C) without FW workaround.

Workaround

Workaround is incorporated into S140 SoftDevice v6.1.1 and the DTM example in SDK v15.3.0. See the following document for a description of the workarounds:

nRF52840 Errata Attachment Anomaly 172 Addendum

3.16 [173] GPIO: Writes to LATCH register take several CPU cycles to take effect

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

A bit in the LATCH register reads '1' even after clearing it by writing '1'.

Conditions

Reading the LATCH register right after writing to it.

Consequences

Old value of the LATCH register is read.

Workaround

Have at least 3 CPU cycles of delay between the write and the subsequent read to the LATCH register. This can be achieved by having 3 dummy reads to the LATCH register.

3.17 [174] SPIM: SPIM3 events incorrectly connected to the PPI

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

Tasks triggered from the PPI using EVENTS_ENDRX or EVENTS_ENDTX of SPIM3 do not happen when expected.

Conditions

Always.

Consequences

EVENTS_ENDRX and EVENTS_ENDTX of SPIM3 have their connections to the PPI swapped. Tasks triggered by the PPI from EVENTS_ENDRX or EVENTS_ENDTX of SPIM3 do not happen when expected.

Workaround

When configuring the PPI to trigger a task on EVENTS_ENDRX, program the CH[N].EEP register with the address of EVENTS_ENDTX. When configuring the PPI to trigger a task on EVENTS_ENDTX, program the CH[N].EEP register with the address of EVENTS_ENDRX.

This only applies to the SPIM3 instance.

3.18 [176] System: Flash erase through CTRL-AP fails due to watchdog time-out

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

Full flash erase through CTRL-AP is not successful.

Conditions

WDT is enabled.

Consequences

Flash is not erased. If the device has a WDT time-out less than 1 ms and is readback-protected through UICR.APPROTECT, there is a risk of permanently preventing the erasing of the flash.

Workaround

Try again.

3.19 [179] RTC: COMPARE event is generated twice from a single RTC compare match

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

Tasks connected to RTC COMPARE event through PPI are triggered twice per compare match.

Conditions

RTC registers are being accessed by CPU while RTC is running.

Consequences

Tasks connected to RTC COMPARE event through PPI are triggered more often than expected.

Workaround

Do not access the RTC registers, including the COMPARE event register, from CPU while waiting for the RTC COMPARE event. Note that CPU interrupt from this event can still be enabled.

3.20 [183] PWM: False SEQEND[0] and SEQEND[1] events

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

False SEQEND[0] and SEQEND[1] events are being generated.

Conditions

Any of the LOOPSDONE_SEQSTARTn shortcuts are enabled. LOOP register is non-zero and sequence 1 is one value long.

Consequences

SEQEND[0] and SEQEND[1] events might falsely trigger other tasks if these are routed through the PPI.

Workaround

Avoid using the LOOPSDONE_SEQSTARTn shortcuts, when LOOP register is non-zero and sequence 1 is one value long.

3.21 [184] NVMC: Erase or write operations from the external debugger fail when CPU is not halted

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

The erase or write operation fails or takes longer time than specified.

Conditions

NVMC erase or write operation initiated using an external debugger. CPU is not halted.

Consequences

The NVMC erase or write operation fails or takes longer time than specified.

Workaround

Halt the CPU by writing to DHCSR (Debug Halting Control and Status Register) before starting NVMC erase or write operation from the external debugger. See the ARM infocenter to get the details of the DHCSR register.

Programming tools provided by Nordic Semiconductor comply with this.

3.22 [187] USBD: USB cannot be enabled

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

After writing to NRF_USBD->ENABLE, no EVENTS_USBEVENT is triggered, and USB->EVENTCAUSE is not updated.

Conditions

Most recent reset type is soft reset or CPU lockup reset, or after a new firmware update to flash.

Consequences

USB is not working.

Workaround

Implement code similar to the following around the USB enabling:

```
*(volatile uint32_t *)0x4006EC00 = 0x00009375;
*(volatile uint32_t *)0x4006ED14 = 0x00000003;
*(volatile uint32_t *)0x4006EC00 = 0x00009375;

/* Enable the peripheral */
NRF_USBD->ENABLE = USBD_ENABLE_ENABLE_Enabled<< USBD_ENABLE_ENABLE_Pos;

/* Waiting for peripheral to enable, this should take a few µs */
while (0 == (NRF_USBD->EVENTCAUSE & USBD_EVENTCAUSE_READY_Msk))
{
    /* Empty loop */
}
NRF_USBD->EVENTCAUSE &= ~USBD_EVENTCAUSE_READY_Msk;

*(volatile uint32_t *)0x4006EC00 = 0x00009375;
*(volatile uint32_t *)0x4006ED14 = 0x00000000;
*(volatile uint32_t *)0x4006EC00 = 0x00009375;
```

nRF5 SDK version 15 will include this workaround.

3.23 [190] NFCT: Event FIELDDETECTED may be generated too early

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

Reset of the operating state after FIELDLOST event. In some cases, communication with the peer device is not possible.

Conditions

Always. Especially with stronger field strengths.

Consequences

Restart of transfer required.

Workaround

On FIELDDETECTED event, wait 1 ms (using timer) before starting NFC communication with NRF_NFCT->TASKS_ACTIVATE.

This workaround is included in SDK v15.0.0.

3.24 [191] RADIO: High packet error rate in BLE Long Range mode

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

High packet error rate.

Conditions

BLE Long Range mode.

Consequences

Poor communication link.

Workaround

Use the following setting for the radio in BLE LR mode (set after power-on-reset and whenever NRF_RADIO->POWER has been low):

```
*(volatile uint32_t *) 0x40001740 = ((*((volatile uint32_t *) 0x40001740)) & 0x7FFF00FF) |
 0x80000000 | (((uint32_t)(196)) << 8);
```

When switching from BLE LR mode to any other radio mode, use the following code to return to default settings:

```
*(volatile uint32_t *) 0x40001740 = ((*((volatile uint32_t *) 0x40001740)) & 0x7FFFFFFF);
```

3.25 [193] SPIM: SPIM3 does not generate EVENTS_END and halts if suspended during last byte

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

SPIM3 stops working.

Conditions

Using TASKS_SUSPEND on SPIM3 during last byte.

Consequences

EVENTS_END is not generated and SPIM3 stops working.

Workaround

Do not use TASKS_SUSPEND for SPIM3 unless the application can guarantee that it will not be triggered during the transfer of the last byte. There is no indication from SPIM3 that it is currently in the last byte transfer.

If TASKS_SUSPEND was used during transmission of the last byte, recover SPIM3 by power cycling the device or restart SPIM3 using the following code:

```
*(volatile uint32_t *)0x4002FFFC = 0;
*(volatile uint32_t *)0x4002FFFC;
*(volatile uint32_t *)0x4002FFFC = 1;
```

3.26 [194] I2S: STOP task does not switch off all resources

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

Current consumption too high (~900 µA) after using the STOP task.

Conditions

I2S was running and was stopped by triggering the STOP task.

Consequences

Current consumption higher than specified.

Workaround

Apply the following code after the STOP task:

```
*((volatile uint32_t *)0x40025038) = 1;
*((volatile uint32_t *)0x4002503C) = 1;
```

3.27 [195] SPIM: SPIM3 continues to draw current after disable

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

Current consumption higher than specified when disabling the SPIM3.

Conditions

When disabling the SPIM3.

Consequences

Current consumption around 900 µA higher than specified.

Workaround

Apply the following workaround after disabling the SPIM3 (`NRF_SPIM3->ENABLE = 0`):

```
*(volatile uint32_t *)0x4002F004 = 1;
```

3.28 [196] I2S: PSEL acquires GPIOs regardless of ENABLE

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

I2S controls GPIO even when I2S is not enabled.

Conditions

When using I2S->PSEL to configure GPIO.

Consequences

GPIO selected for I2S cannot be used for any other peripheral.

Workaround

Do not rely on the pins selected in I2S->PSEL registers being free when I2S->ENABLE is set to DISABLE.

Only set the CONNECT bit in the I2S->PSEL registers to CONNECTED immediately before enabling I2S. When disabling I2S, set the CONNECT bit in the I2S->PSEL registers to DISCONNECTED.

3.29 [198] SPIM: SPIM3 transmit data might be corrupted

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

Transmit data from SPIM3 is corrupted.

Conditions

Data accessed by CPU location in the same RAM block as where the SPIM3 TXD.PTR is pointing, and CPU does a read or write operation at the same clock cycle as the SPIM3 EasyDMA is fetching data.

Consequences

Transmit data from SPIM3 is corrupted.

Workaround

Reserve dedicated RAM blocks for the SPIM3 transmit buffer, not overlapping with application data used by the CPU. In addition, synchronize so that the CPU is not writing data to the transmit buffer while SPIM is transmitting data.

3.30 [199] USBD: USBD cannot receive tasks during DMA

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

The USBD does not perform incoming tasks.

Conditions

The USBD is performing a DMA transfer.

Consequences

If any EasyDMA transfer is in progress, USB tasks cannot be used.

Workaround

To enable incoming tasks when using DMA, use the following code when starting a DMA transfer:

```
*(volatile uint32_t *)0x40027C1C = 0x00000082;
```

After the DMA transfer is completed, use:

```
*(volatile uint32_t *)0x40027C1C = 0x00000000;
```

3.31 [204] RADIO: Switching beween TX and RX causes unwanted emissions

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

Unwanted emissions are experienced when switching from TX to RX.

Conditions

Switching from TX to RX without using DISABLE.

Consequences

Unwanted emissions occur on the channel used for RX.

Workaround

Always use DISABLE when switching from TX to RX.

3.32 [208] QSPI: PPI Deactivate task does not switch off all resources

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

Current consumption is higher than expected after triggering TASKS_DEACTIVATE from the PPI.

Conditions

QSPI was running and was stopped by triggering TASKS_DEACTIVATE from the PPI.

Consequences

Current consumption higher than expected.

Workaround

Use software to write to the TASKS_DEACTIVATE register instead of triggering TASKS_DEACTIVATE from the PPI.

3.33 [209] CLOCK: LFRC ULP mode calibration not functional

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

LFRC stops.

Conditions

Sometimes when using LFRC ULP mode and performing calibration.

Consequences

LFRC ULP mode cannot be calibrated.

Workaround

Use LFRC ULP mode without calibrating, or use LFRC normal mode if calibration is required.

3.34 [210] GPIO: Bits in GPIO LATCH register are incorrectly set to 1

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

The GPIO.LATCH[n] register is unexpectedly set to 1 (Latched).

Conditions

Set GPIO.PIN_CNF[n].SENSE at low level (3) at the same time as PIN_CNF[n].INPUT is set to Connect (0).

Consequences

The GPIO.LATCH[n] register is set to 1 (Latched). This could have side effects, depending on how the chip is configured to use this LATCH register.

Workaround

Always configure PIN_CNF[n].INPUT before PIN_CNF[n].SENSE.

3.35 [213] WDT: WDT configuration is cleared when entering system OFF

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

WDT configuration has been cleared when device wakes from System OFF.

Conditions

Always.

Consequences

WDT does not resume function as expected.

Workaround

Reconfigure WDT after wake-up from System OFF.

3.36 [214] SPIS: Incorrect data transferred

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

Wrong data is transferred.

Conditions

If SPIS is disabled while CSN is asserted.

Consequences

Unsent byte from previous transmission is transferred as first byte of new transmission.

Workaround

After disabling the SPIS*n* instance (writing `SPIS`*`n`*`->ENABLE = SPIS_ENABLE_ENABLE_Disable`), apply the following code:

```
*(volatile uint32_t *) (NRF_SPIS*n*_BASE + 0xA4ul) = 1ul;
*(volatile uint32_t *) (NRF_SPIS*n*_BASE + 0xACul) = 1ul;
```

3.37 [215] QSPI: Reading QSPI registers after XIP might halt CPU

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

CPU halts.

Conditions

Init and start QSPI, use XIP, then write to or read any QSPI register with an offset above 0x600.

Consequences

CPU halts.

Workaround

Trigger QSPI TASKS_ACTIVATE after XIP is used before accessing any QSPI register with an offset above 0x600.

3.38 [219] TWIM: I2C timing spec is violated at 400 kHz

This anomaly applies to IC Rev. Rev 2, build codes QIAA-Dx0, CKAA-Dx0.

It was inherited from the previous IC revision Engineering D nRF52840.

Symptoms

The low period of the SCL clock is too short to meet the I2C specification at 400 kHz. The actual low period of the SCL clock is 1.25 µs while the I2C specification requires the SCL clock to have a minimum low period of 1.3 µs.

Conditions

Using TWIM at 400 kHz.

Consequences

TWI communication might not work at 400 kHz with I2C compatible devices.

Workaround

If communication does not work at 400 kHz with an I2C compatible device that requires the SCL clock to have a minimum low period of 1.3 µs, use 390 kHz instead of 400kHz by writing 0x06200000 to the FREQUENCY register. With this setting, the SCL low period is greater than 1.3 µs.