

nRF52840 Objective Product Specification v0.5.1

Key feature

- Bluetooth® 5, IEEE 802.15.4-2006, 2.4 GHz transceiver
 - -95 dBm sensitivity in 1 Mbps *Bluetooth* * low energy (BLE) mode
 - -103 dBm sensitivity in 125 kbps BLE mode (long range)
 - +8 dBm TX power (down to -20 dBm in 4 dB steps)
 - On-air compatible with nRF52, nRF51, nRF24L and nRF24AP Series
 - Supported data rates:
 - Bluetooth 5: 2 Mbps, 1 Mbps, 500 kbps, 125 kbps
 - IEEE 802.15.4-2006: 250 kbps
 - Proprietary 2.4 GHz: 2 Mbps, 1 Mbps
 - Single-ended antenna output (on-chip balun)
 - 4.9 mA peak current in TX (0 dBm)
 - 4.8 mA peak current in RX
 - RSSI (1 dB resolution)
- ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz
 - 212 EEMBC CoreMark® score running from flash memory
 - 56 μA/MHz running from flash memory
 - Watchpoint and trace debug modules (DWT, ETM and ITM)
 - Serial wire debug (SWD)
- Flexible power management
 - Supply voltage range 1.7 V to 5.5 V
 - On-chip DC/DC and LDO regulators with automated low current modes
 - ullet Regulated supply for external components from 1.8 V to 3.3 V
 - Automated peripheral power management
 - Fast wake-up using 64 MHz internal oscillator
 - 0.4 μA at 3 V in OFF mode, no RAM retention
- 1.3 μA at 3 V in ON mode, no RAM retention, wake on RTC
- Memory
- 1 MB flash/256 kB RAM
- HW accelerated security
 - ARM® TrustZone® Cryptocell 310 cryptographic accelerator
 - 128 bit AES/ECB/CCM/AAR co-processor (on-the-fly packet encryption)
- Advanced on-chip interfaces
 - USB 2.0 full speed (12 Mbps) controller
 - QSPI 32 MHz interface
 - High speed 32 MHz SPI
 - Type 2 near field communication (NFC-A) tag with wake-on field
 - Touch-to-pair support
 - Programmable peripheral interconnect (PPI)
 - 48 general purpose I/O pins
 - EasyDMA automated data transfer without CPU processing on peripherals
- Nordic SoftDevice ready and with support for concurrent multi-protocol
- 12-bit, 200 ksps ADC 8 configurable channels with programmable gain
- 64 level comparator
- 15 level low-power comparator with wake-up from System OFF mode
- Temperature sensor
- 4x 4-channel pulse width modulator (PWM) units with EasyDMA
- Audio peripherals: I2S, digital microphone interface (PDM)
- 5x 32-bit timers with counter mode
- Up to 4x SPI masters/3x SPI slaves with EasyDMA
- Up to 2x I2C compatible 2-wire masters/slaves
- 2x UART (CTS/RTS) with EasyDMA
- Quadrature decoder (QDEC)
- 3x real-time counters (RTC)
- Package variants
 - AQFN73 package, 7 × 7 mm

Application

- Advanced computer peripherals and I/O devices
 - Mouse
 - Keyboard
 - Multi-touch trackpad
- Advanced wearables
 - · Health/fitness sensor and monitor devices
 - Wireless payment enabled devices
- Internet of things (IoT)
 - Smart home sensors and controllers
 - Industrial IoT sensors and controllers
- Interactive entertainment devices
 - Remote controls
 - Gaming controllers



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1 Revision history

Date	Version	Description
July 2017	0.5.1	The following content is changed in this version:
July 2017	0.5.1	The following content is changed in this version: Pin assignments on page 13: Added description for trace pins CPU on page 18: Improved SysTick timer description Memory on page 20: Memory map figure updated AHB multilayer on page 25: Added SPIM3 and updated RAMPRI registers EasyDMA on page 26: Miscellaneous documentation improvements UICR — User information configuration registers on page 44: Improved APPROTECT description and added DEBUGCTRL register SPIM — Serial peripheral interface master with EasyDMA on page 340: Fixed error in mode table and changed the base address of SPIM3 Debug and trace on page 62: Added r_pull parameter for CTRL-AP, in addition to miscellaneous documentation improvements POWER — Power supply on page 66:
		Added clarifications for supplying external circuitry Improved register descriptions Removed deprecated RAMON and RAMONB registers Removed pin reset from CTRL-AP feature Improved description of POFCON CLOCK — Clock control on page 141: Added HFXO debounce functionality Changed LFRC accuracy to +- 500 ppm Improved description in TRACECONFIG register RADIO — 2.4 GHz Radio on page 249:
		 Removed 9 dBm output power option Updated TX sequence figure Improved TIFS description Added PHYEND event Added PDUSTAT register Removed 250 kbit/s Nordic proprietary mode Changed to using term bps instead of sps for data rate in electrical specifications
		SAADC — Successive approximation analog-to-digital converter on page 418: Updated VDD/5 input specification COMP — Comparator on page 453: REFSEL AREF value changed PWM — Pulse width modulation on page 558: Changed width of DECODER.LOAD field
		 PDM — Pulse density modulation interface on page 499: Fixed error in electrical specification units I2S — Inter-IC sound interface on page 508: PSEL registers PORT field updated Reference circuitry on page 688: Reference schematics updated and erroneous sentence for VDD/VDDH connection removed
5 1 2015		Block diagram on page 12: Miscellaneous improvements
December 2016	0.5	First release



2 About this document

This product specification is organized into chapters based on the modules and peripherals that are available in this IC.

The peripheral descriptions are divided into separate sections that include the following information:

- A detailed functional description of the peripheral
- · Register configuration for the peripheral
- Electrical specification tables, containing performance data which apply for the operating conditions described in *Recommended operating conditions* on page 17.

2.1 Document naming and status

Nordic uses three distinct names for this document, which are reflecting the maturity and the status of the document and its content.

Table 1: Defined document names

Document name	Description
Objective Product Specification (OPS)	Applies to document versions up to 0.7.
Preliminary Product Specification (PPS)	This product specification contains target specifications for product development. Applies to document versions 0.7 and up to 1.0.
Product Specification (PS)	This product specification contains preliminary data. Supplementary data may be published from Nordic Semiconductor ASA later. Applies to document versions 1.0 and higher.
	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

2.2 Peripheral naming and abbreviations

Every peripheral has a unique capitalized name or an abbreviation of its name, e.g. TIMER, used for identification and reference. This name is used in chapter headings and references, and it will appear in the ARM® Cortex® Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer to identify the peripheral.

The peripheral instance name, which is different from the peripheral name, is constructed using the peripheral name followed by a numbered postfix, starting with 0, for example, TIMER0. A postfix is normally only used if a peripheral can be instantiated more than once. The peripheral instance name is also used in the CMSIS to identify the peripheral instance.

2.3 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

2.3.1 Fields and values

The **Id** (**Field Id**) row specifies the bits that belong to the different fields in the register. If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column.

A blank space means that the field is reserved and read as undefined, and it also must be written as 0 to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column. The **Value Id** may be omitted in the single-bit bit fields when values can be substituted with a Boolean type enumerator range, e.g. true/false, disable(d)/enable(d), on/off, and so on.



Values are usually provided as decimal or hexadecimal. Hexadecimal values have a 0x prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example 1, 3, 9.
- Range of values, e.g. [0..4], indicating all values from and including 0 and 4.
- Implicit values. If no values are indicated in the Value column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value** Id, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with '..'.

A feature marked **Deprecated** should not be used for new designs.

2.4 Registers

Table 2: Register Overview

Register	Offset	Description
DUMMY	0x514	Example of a register controlling a dummy feature

2.4.1 DUMMY

Address offset: 0x514

Example of a register controlling a dummy feature

Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Id	Bit num	nhai			21	20	20	20	27	26	25	24	22	าา	21 1	20 1	10 1	10	17	16 '	1 = -	1 / 1	10 1	12 1	1 1	0 0	8	7	c	5	4	າ າ	1	0
Reset 0x00050002 Id RW Field Value Id Value B RW FIELD_A RW FIELD_B RESET 0x00050002 RESET 0x00050000 RESET 0x000500000 RESET 0x00050000 RESET 0x00050000 RESET 0x000500000 RESET 0x000500000 RESET 0x000500000 RESET 0x0005000000 RESET 0x00050000000 RESET 0x000500000000000000000000000000000000		iibei			31	. 30	23	20					23 .	22	21 4	20 1					13.	14 1	15.	12 1	.1 1	0 9			U	5	4	3 Z	. 1	
Id RW Field Value Id Value Description A RW FIELD_A Example of a field with several enumerated values Disabled 0 The example feature is disabled NormalMode 1 The example feature is enabled in normal mode ExtendedMode 2 The example feature is enabled along with extra functionality B RW FIELD_B Fixample of a deprecated field Deprecated	ld								D	D	D	D						С	С	С							В						Α	Α
A RW FIELD_A Disabled 0 The example feature is disabled NormalMode 1 The example feature is enabled in normal mode ExtendedMode 2 The example feature is enabled along with extra functionality B RW FIELD_B Example of a field with several enumerated values The example feature is enabled in normal mode ExtendedMode 2 The example feature is enabled along with extra functionality	Reset 0	0x00	0050002		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0 (0 (0	0	0	0	0	0	0 0	1	0
Disabled 0 The example feature is disabled NormalMode 1 The example feature is enabled in normal mode ExtendedMode 2 The example feature is enabled along with extra functionality B RW FIELD_B Example of a deprecated field Deprecated	Id R	w	Field	Value Id	Va	lue							Des	cri	ptio	n																		
NormalMode 1 The example feature is enabled in normal mode ExtendedMode 2 The example feature is enabled along with extra functionality B RW FIELD_B Example of a deprecated field Deprecated	A R\	W	FIELD_A										Exa	mp	le o	f a t	fiel	d w	ith	sev	era	l en	um	era	ted	valu	ıes							
ExtendedMode 2 The example feature is enabled along with extra functionality B RW FIELD_B Example of a deprecated field Deprecated				Disabled	0 The example feature is disabled																													
B RW FIELD_B Example of a deprecated field Deprecated				NormalMode	1 The example feature is enabled in normal mode																													
				ExtendedMode	2 The example feature is enabled along with extra functionality																													
Disabled 0 The override feature is disabled	B R\	W	FIELD_B		Example of a deprecated field Dep				Depr	eca	ed																							
				Disabled	0 The override feature is disabled																													
Enabled 1 The override feature is enabled				Enabled	1 The override feature is enabled																													
C RW FIELD_C Example of a field with a valid range of values	C R\	W	FIELD_C		Example of a field with a valid range of values																													
ValidRange [27] Example of allowed values for this field				ValidRange	[2	7]							Exa	mp	le o	f all	low	ed	val	ues	for	thi	s fie	eld										
D RW FIELD_D Example of a field with no restriction on the values	D R\	W	FIELD_D										Exa	mp	le o	f a t	fiel	d w	ith	no	res	trict	ion	on	the	val	ues							



3 Block diagram

This block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

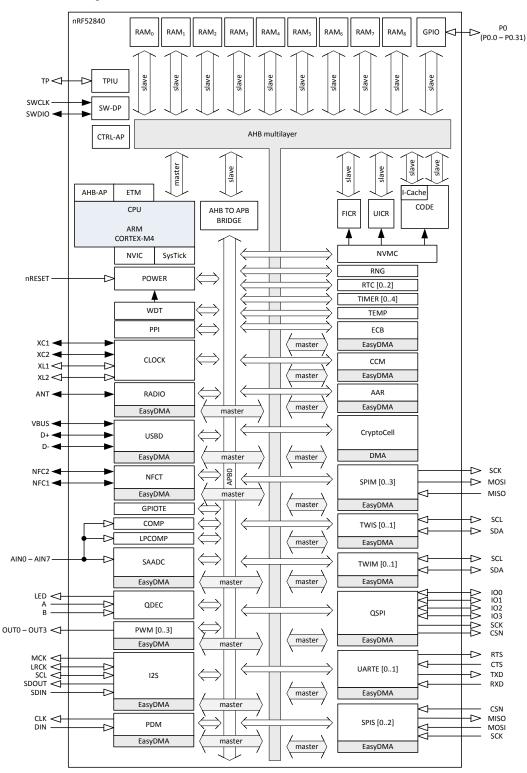


Figure 1: Block diagram



4 Pin assignments

This section describes the pin assignment and the pin functions.

This device provides flexibility when it comes to routing and configuration of the GPIO pins. However, some pins have recommendations for how the pin should be configured or what it should be used for. See *Table 3: QIAA pin assignments* on page 13 for more information about this.

4.1 QIAA pin assignments

This section describes the pin assignment and the pin functions.

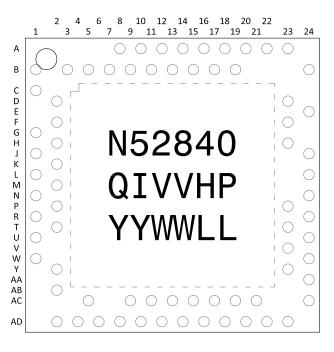


Figure 2: QIAA pin assignments, top view

Table 3: QIAA pin assignments

Pin	Name	Function	Description	Recommended usage
A8	P0.31	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
	AIN7	Analog input	Analog input	only.
A10	P0.29	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
	AIN5	Analog input	Analog input	only.
A12	P0.02	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
	AIN0	Analog input	Analog input	only.
A14	P1.15	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
				only.
A16	P1.13	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
				only.
A18	DEC2	Power	1.3 V regulator supply decoupling (Radio s	supply)
A20	P1.10	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
				only.
A22	VDD	Power	Power supply	
A23	XC2	Analog input	Connection for 32 MHz crystal.	
B1	VDD	Power	Power supply	
В3	DCC	Power	DC/DC converter output	



Pin	Name	Function	Description	Recommended usage
B5	DEC4	Power	1.3 V regulator supply decoupling	
В7	VSS	Power	Ground	
В9	P0.30	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
	AIN6	Analog input	Analog input	only.
B11	P0.28	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
	AIN4	Analog input	Analog input	only.
B13	P0.03	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
				only.
B15	AIN1 P1.14	Analog input Digital I/O	Analog input General purpose I/O	Standard drive, low frequency I/O
B13	P1.14	Digital I/O	deneral purpose I/O	only.
B17	P1.12	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
B19	P0.11	Digital I/O	General purpose I/O pin.	Standard drive, low frequency I/O
	TRACEDATA2	Trace data	Trace buffer TRACEDATA[2].	only.
B24	XC1	Analog input	Connection for 32 MHz crystal	
C1	DEC1	Power	1.1 V regulator supply decoupling	
D2	P0.00	Digital I/O	General purpose I/O	
	XL1	Analog input	Connection for 32.768 kHz crystal	
D23	DEC3	Power	Power supply, decoupling	
E24	DEC6	Power	1.3 V regulator supply decoupling (Radio supply)	
F2	P0.01	Digital I/O	General purpose I/O	
	VI 2			
F23	XL2 VSS_PA	Analog input Power	Connection for 32.768 kHz crystal Ground (Radio supply)	
-23 31	P0.26	Digital I/O	General purpose I/O	
H2	P0.27	Digital I/O	General purpose I/O	
H23	ANT	RF	Single-ended radio antenna connection	See <i>Reference circuitry</i> on page
			•	688 for guidelines on how to ensure good RF performance.
J1	P0.04	Digital I/O	General purpose I/O	
	AIN2	Analog input	Analog input	
J24	P0.10	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
	NFC2	NFC input	NFC antenna connection	only.
K2	P0.05	Digital I/O	General purpose I/O	
	AIN3	Analog input	Analog input	
L1	P0.06	Digital I/O	General purpose I/O	
L24	P0.09	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
	NFC1	NFC input	NFC antenna connection	only.
M2	P0.07	Digital I/O	General purpose I/O pin	
		-	, , , ,	
	TRACECLK	Trace clock	Trace buffer clock	
N1	P0.08	Digital I/O	General purpose I/O	
N24	DEC5	Power	1.3 V regulator supply decoupling (flash supply)	
P2	P1.08	Digital I/O	General purpose I/O	6. 1.11. 1.6
P23	P1.07	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
R1	P1.09	Digital I/O	General purpose I/O pin.	
	TRACEDATA3	Trace data	Trace buffer TRACEDATA[3].	
R24	P1.06	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
T2	P0.11	Digital I/O	General purpose I/O	
T23	P1.05	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only.
U1	P0.12	Digital I/O	General purpose I/O pin.	
	TRACEDATA1	Trace data	Trace buffer TRACEDATA[1].	
	INACLUATAI	Trace data	Hace build! TRACEDATA[1].	



Pin	Name	Function	Description	Recommended usage
U24	P1.04	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
				only.
V23	P1.03	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
				only.
W1	VDD	Power	Power supply	
W24	P1.02	Digital I/O	General purpose I/O	Standard drive, low frequency I/O
				only.
Y2	VDDH	Power	High voltage power supply	
Y23	P1.01	Digital I/O	General purpose I/O Standard drive, low frequen	
			only.	
AA24	SWDCLK	Debug	Serial wire debug clock input for debug and	
			programming	
AB2	DCCH	Power	DC/DC converter output	
AC5	DECUSB	Power	Decoupling for USB 3.3 V	
AC9	P0.14	Digital I/O	General purpose I/O	
AC11	P0.16	Digital I/O	General purpose I/O	
AC13	P0.18	Digital I/O	General purpose I/O	QSPI/CSN
	nRESET		Configurable as system RESET	
AC15	P0.19	Digital I/O	General purpose I/O	QSPI/SCK
AC17	P0.21	Digital I/O	General purpose I/O	QSPI
AC19	P0.23	Digital I/O	General purpose I/O	QSPI
AC21	P0.25	Digital I/O	General purpose I/O	
AC24	SWDIO	Debug	Debug serial data	
AD2	VBUS	Power	5 V input for USB 3.3 V regulator	
AD4	D-	Digital I/O	USB D-	USB
AD6	D+	Digital I/O	USB D+	USB
AD8	P0.13	Digital I/O	General purpose I/O	
AD10	P0.15	Digital I/O	General purpose I/O	
AD12	P0.17	Digital I/O	General purpose I/O	
AD14	VDD	Power	Power supply	
AD16	P0.20	Digital I/O	General purpose I/O	
AD18	P0.22	Digital I/O	General purpose I/O	QSPI
AD20	P0.24	Digital I/O	General purpose I/O	
AD22	P1.00	Digital I/O	General purpose I/O pin.	QSPI
	TRACEDATA0	Trace data	Trace buffer TRACEDATA[0].	
	TITICLUATIO			
			Serial wire output (SWO).	
AD23	VDD	Power	Flash supply pad	
Bottom of chip				
Die pad	VSS	Power	Ground pad. Exposed die pad must be connected to	
			ground (VSS) for proper device operation.	

Important: For more information on Standard drive, see *GPIO* — *General purpose input/output* on page 154. Low frequency I/O is signals with a frequency up to 10 kHz.



5 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Table 4: Absolute maximum ratings

Supply voltages VDD -0.3 +3.9 V VDDH -0.3 +5.8 V VBUS -0.3 +5.8 V VSS 0 V I/O pin voltage V _{I/O} , VDD ≤3.6 V -0.3 VDD + 0.3 V V VI/O pin voltage -0.3 3.9 V V NFC antenna pin current I _{NFC1/2} 80 mA Radio RF input level 80 mA Re pinput level Environmental (AQFN package) Storage temperature -40 +125 °C	
VDDH -0.3 +5.8 V VBUS -0.3 +5.8 V VSS 0 V I/O pin voltage V _{I/O} , VDD ≤3.6 V -0.3 VDD + 0.3 V V V _{I/O} , VDD >3.6 V -0.3 3.9 V V NFC antenna pin current INFCI/2 80 mA Radio 80 mA RF input level 10 dBm Environmental (AQFN package)	
VBUS -0.3 +5.8 V VSS 0 V I/O pin voltage V V VDD + 0.3 V V V _{I/O} , VDD ≥3.6 V -0.3 3.9 V V NFC antenna pin current 80 mA Radio RF input level 10 dBm Environmental (AQFN package)	
VSS 0 0 V V V V V V V V V	
I/O pin voltage $V_{I/O}$, VDD ≤3.6 V -0.3 VDD + 0.3 V V $V_{I/O}$, VDD >3.6 V -0.3 3.9 V V NFC antenna pin current 80 mA $I_{NFCI/2}$ 80 mA Radio 10 dBm Environmental (AQFN package) Environmental (AQFN package)	
$V_{1/O}$, VDD ≤3.6 V	
V _{I/O} , VDD > 3.6 V -0.3 3.9 V V NFC antenna pin current 80 mA Radio RF input level 10 dBm Environmental (AQFN package) 10 dBm	
NFC antenna pin current I _{NFC1/2} 80 mA Radio RF input level 10 dBm Environmental (AQFN package)	
I _{NFC1/2} 80 mA Radio RF input level 10 dBm Environmental (AQFN package)	
Radio RF input level 10 dBm Environmental (AQFN package)	
RF input level 10 dBm Environmental (AQFN package)	
Environmental (AQFN package)	
Storage temperature -40 +125 °C	
MSL Moisture Sensitivity Level 2	
ESD HBM Human Body Model 4 kV	
ESD CDM _{QF} Charged Device Model 750 V	
(AQFN73, 7×7 mm package)	
Flash memory	
Endurance 10 000 Write/erase cycles	es
Retention 10 years at 40°C	





6 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Table 5: Recommended operating conditions

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	VDD supply voltage, independent of DCDC enable	!	1.7	3.0	3.6	V
VDD _{POR}	VDD supply voltage needed during power-on reset		1.75			V
VDDH	VDDH supply voltage, independent of DCDC enable		2.5	3.7	5.5	V
VBUS	VBUS USB supply voltage		4.35	5	5.5	V
t _{R_VDD}	Supply rise time (0 V to 1.7 V)				60	ms
t _{R_VDDH}	Supply rise time (0 V to 3.7 V)				100	ms
TĀ	Operating temperature		-40	25	85	°C

Important: The on-chip power-on reset circuitry may not function properly for rise times longer than the specified maximum.



7 CPU

The ARM® Cortex®-M4 processor with floating-point unit (FPU) has a 32-bit instruction set (Thumb®-2 technology) that implements a superset of 16 and 32-bit instructions to maximize code density and performance.

This processor implements several features that enable energy-efficient arithmetic and high-performance signal processing, including:

- Digital signal processing (DSP) instructions
- Single-cycle multiply and accumulate (MAC) instructions
- · Hardware divide
- 8- and 16-bit single instruction multiple data (SIMD) instructions
- Single-precision floating-point unit (FPU)

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex processor series is implemented and available for the M4 CPU.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the nested vectored interrupt controller (NVIC).

Executing code from flash will have a wait state penalty on the nRF52 series. An instruction cache can be enabled to minimize flash wait states when fetching instructions. For more information on cache, see *Cache* on page 29. The section *Electrical specification* on page 18 shows CPU performance parameters including wait states in different modes, CPU current and efficiency, and processing power and efficiency based on the CoreMark® benchmark.

The ARM System Timer (SysTick) is present on nRF52840. The SysTick's clock will only tick when the CPU is running or when the system is in debug interface mode.

7.1 Floating point interrupt

The floating point unit (FPU) may generate exceptions when used due to e.g. overflow or underflow, which in turn will trigger the FPU interrupt.

See Instantiation on page 23 for more information about the exceptions triggering the FPU interrupt.

To clear the IRQ (interrupt request) line when an exception has occurred, the relevant exception bit within the floating-point status and control register (FPSCR) needs to be cleared. For more information about the FPSCR or other FPU registers, see *Cortex-M4 Devices Generic User Guide*.

7.2 Electrical specification

7.2.1 CPU performance

The CPU clock speed is 64 MHz. Current and efficiency data is taken when in System ON and the CPU is executing the CoreMark[™] benchmark. It includes power regulator and clock base currents. All other blocks are IDLE.

Symbol	Description	Min.	Тур.	Max.	Units
W _{FLASH}	CPU wait states, running CoreMark from flash, cache disabled			2	
W _{FLASHCACHE}	CPU wait states, running CoreMark from flash, cache enabled			3	
W _{RAM}	CPU wait states, running CoreMark from RAM			0	
I _{DDFLASHCACHE}	CPU current, running CoreMark from flash, cache enabled, LDO		6.5		mA
I _{DDFLASHCACHEDCDC}	CPU current, running CoreMark from flash, cache enabled,		3.6		mA
	DCDC 3V				
I _{DDFLASH}	CPU current, running CoreMark from flash, cache disabled, LDO				mA



Symbol	Description	Min.	Тур.	Max.	Units
I _{DDFLASHDCDC}	CPU current, running CoreMark from flash, cache disabled,				mA
	DCDC 3V				
I _{DDRAM}	CPU current, running CoreMark from RAM, LDO				mA
I _{DDRAMDCDC}	CPU current, running CoreMark from RAM, DCDC 3V				mA
I _{DDFLASH/MHz}	CPU efficiency, running CoreMark from flash, cache enabled,		102		μΑ/
	LDO				MHz
I _{DDFLASHDCDC/MHz}	CPU efficiency, running CoreMark from flash, cache enabled,		56		μΑ/
	DCDC 3V				MHz
CM_{FLASH}	CoreMark, running CoreMark from flash, cache enabled		212		CoreN
CM _{FLASH/MHz}	CoreMark per MHz, running CoreMark from flash, cache		3.3		CoreN
	enabled				MHz
CM _{FLASH/mA}	CoreMark per mA, running CoreMark from flash, cache enabled,		59		CoreN
	DCDC 3V				mA

7.3 CPU and support module configuration

The ARM® Cortex®-M4 processor has a number of CPU options and support modules implemented on the device.

Option / Module	Description	Implemented
Core options		
NVIC	Nested vector interrupt controller	37 vectors
PRIORITIES	Priority bits	3
WIC	Wakeup interrupt controller	NO
Endianness	Memory system endianness	Little endian
Bit-banding	Bit banded memory	NO
DWT	Data watchpoint and trace	YES
SysTick	System tick timer	YES
Modules		
MPU	Memory protection unit	YES
FPU	Floating-point unit	YES
DAP	Debug access port	YES
ETM	Embedded trace macrocell	YES
ITM	Instrumentation trace macrocell	YES
TPIU	Trace port interface unit	YES
ETB	Embedded trace buffer	NO
FPB	Flash patch and breakpoint unit	YES
HTM	AMBA™ AHB trace macrocell	NO



8 Memory

The nRF52840 contains 1 MB of flash and 256 kB of RAM that can be used for code and data storage.

The CPU and the peripherals having EasyDMA can access memory via the AHB multilayer interconnect.

The CPU is also able to access peripherals via the AHB multilayer interconnect, as illustrated in *Figure 3: Memory layout* on page 20.

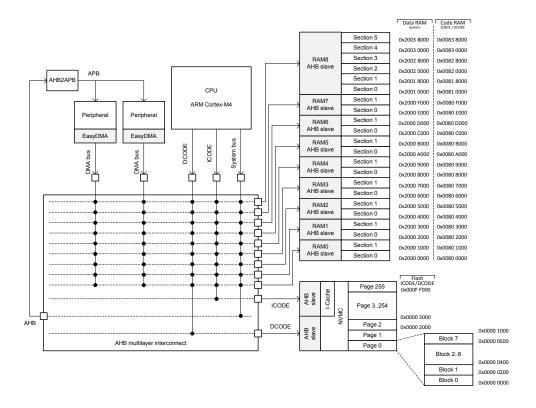


Figure 3: Memory layout

See *AHB multilayer* on page 25 and *EasyDMA* on page 26 for more information about the AHB multilayer interconnect and the EasyDMA.

The same physical RAM is mapped to both the Data RAM region and the Code RAM region. It is up to the application to partition the RAM within these regions so that one does not corrupt the other.

8.1 RAM - Random access memory

The RAM interface is divided into 9 RAM AHB slaves.

RAM AHB slave 0-7 is connected to 2x4 kB RAM sections each and RAM AHB slave 8 is connected to 6x32 kB sections, as shown in *Figure 3: Memory layout* on page 20.

Each of the RAM sections have separate power control for System ON and System OFF mode operation, which is configured via RAM register (see the *POWER — Power supply* on page 66).

8.2 Flash - Non-volatile memory

The flash can be read an unlimited number of times by the CPU, but it has restrictions on the number of times it can be written and erased and also on how it can be written.



Writing to flash is managed by the non-volatile memory controller (NVMC), see *NVMC* — *Non-volatile memory controller* on page 28.

The flash is divided into 256x4 kB pages that can be accessed by the CPU via both the ICODE and DCODE buses as shown in *Figure 3: Memory layout* on page 20. Each page is divided into 8 blocks.

8.3 Memory map

The complete memory map is shown in *Figure 4: Memory map* on page 22. As described in *Memory* on page 20, Code RAM and the Data RAM are the same physical RAM.



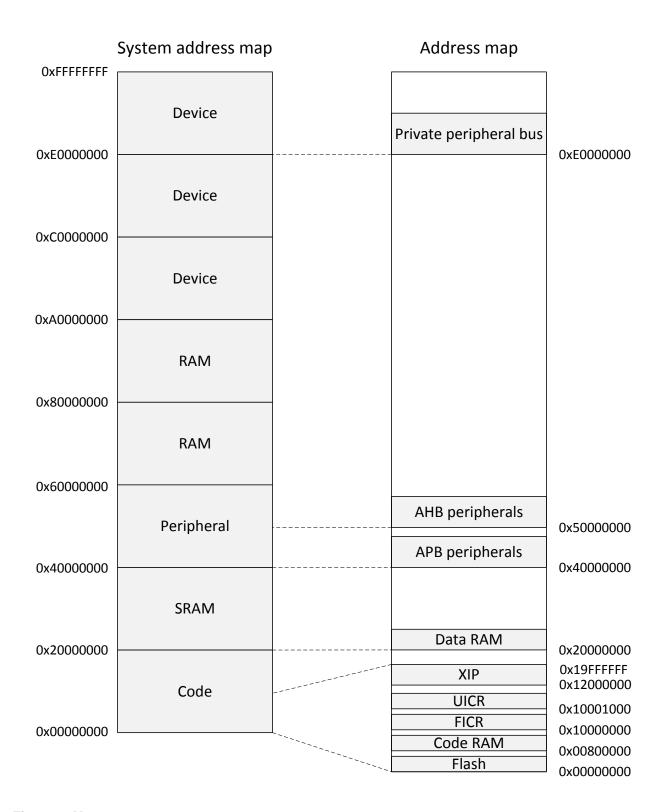


Figure 4: Memory map



8.4 Instantiation

Table 6: Instantiation table

ID	Base Address	Peripheral	Instance	Description	
0	0x40000000	CLOCK	CLOCK	Clock control	
0	0x40000000	POWER	POWER	Power control	
1	0x40001000	RADIO	RADIO	2.4 GHz radio	
2	0x40002000	UARTE	UARTE0	Universal asynchronous receiver/transmitter with EasyDMA, unit 0	
2	0x40002000	UART	UARTO	Universal asynchronous receiver/transmitter	Deprecated
3	0x40003000	TWIM	TWIM0	Two-wire interface master 0	
3	0x40003000	SPIS	SPIS0	SPI slave 0	
3	0x40003000	SPIM	SPIM0	SPI master 0	
3	0x40003000	SPI	SPI0	SPI master 0	Deprecated
3	0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
3	0x40003000	TWI	TWI0	Two-wire interface master 0	Deprecated
4	0x40004000	TWIS	TWIS1	Two-wire interface slave 1	
4	0x40004000	SPIS	SPIS1	SPI slave 1	
4	0x40004000	SPIM	SPIM1	SPI master 1	
4	0x40004000	TWI	TWI1	Two-wire interface master 1	Deprecated
4	0x40004000	TWIM	TWIM1	Two-wire interface master 1	
4	0x40004000	SPI	SPI1	SPI master 1	Deprecated
5	0x40005000	NFCT	NFCT	Near field communication tag	
6	0x40006000	GPIOTE	GPIOTE	GPIO tasks and events	
7	0x40007000	SAADC	SAADC	Analog to digital converter	
8	0x40008000	TIMER	TIMER0	Timer 0	
9	0x40009000	TIMER	TIMER1	Timer 1	
10	0x4000A000	TIMER	TIMER2	Timer 2	
11	0x4000B000	RTC	RTC0	Real-time counter 0	
12	0x4000C000	TEMP	TEMP	Temperature sensor	
13	0x4000D000	RNG	RNG	Random number generator	
14	0x4000E000	ECB	ECB	AES electronic code book (ECB) mode block encryption	
15	0x4000F000	AAR	AAR	Accelerated address resolver	
15	0x4000F000	CCM	CCM	AES counter with CBC-MAC (CCM) mode block encryption	
16	0x40001000	WDT	WDT	Watchdog timer	
17		RTC	RTC1	Real-time counter 1	
	0x40011000				
18	0x40012000	QDEC	QDEC	Quadrature decoder	
19	0x40013000	LPCOMP	LPCOMP	Low power comparator	
19	0x40013000	COMP	COMP	General purpose comparator	
20	0x40014000	EGU	EGU0	Event generator unit 0	
20	0x40014000	SWI	SWI0	Software interrupt 0	
21	0x40015000	EGU	EGU1	Event generator unit 1	
21	0x40015000	SWI	SWI1	Software interrupt 1	
22	0x40016000	EGU	EGU2	Event generator unit 2	
22	0x40016000	SWI	SWI2	Software interrupt 2	
23	0x40017000	EGU	EGU3	Event generator unit 3	
23	0x40017000	SWI	SWI3	Software interrupt 3	
24	0x40018000	SWI	SWI4	Software interrupt 4	
24	0x40018000	EGU	EGU4	Event generator unit 4	
25	0x40019000	SWI	SWI5	Software interrupt 5	
	0x40019000	EGU	EGU5	Event generator unit 5	
25		TIMED	TIMER3	Timer 3	
	0x4001A000	TIMER			
26	0x4001A000 0x4001B000	TIMER	TIMER4	Timer 4	
26 27			TIMER4 PWM0	Timer 4 Pulse width modulation unit 0	
26 27 28	0x4001B000	TIMER			
25 26 27 28 29 30	0x4001B000 0x4001C000	TIMER PWM	PWM0	Pulse width modulation unit 0	



ID	Base Address	Peripheral	Instance	Description	
31	0x4001F000	PPI	PPI	Programmable peripheral interconnect	
32	0x40020000	MWU	MWU	Memory watch unit	
33	0x40021000	PWM	PWM1	Pulse width modulation unit 1	
34	0x40022000	PWM	PWM2	Pulse width modulation unit 2	
35	0x40023000	SPIM	SPIM2	SPI master 2	
35	0x40023000	SPIS	SPIS2	SPI slave 2	
35	0x40023000	SPI	SPI2	SPI master 2	Deprecated
36	0x40024000	RTC	RTC2	Real-time counter 2	
37	0x40025000	I2S	I2S	Inter-IC sound interface	
38	0x40026000	FPU	FPU	FPU interrupt	
39	0x40027000	USBD	USBD	Universal serial bus device	
40	0x40028000	UARTE	UARTE1	Universal asynchronous receiver/transmitter with EasyDMA, unit 1	
41	0x40029000	QSPI	QSPI	External memory interface	
45	0x4002D000	PWM	PWM3	Pulse width modulation unit 3	
47	0x4002F000	SPIM	SPIM3	SPI master 3	
0	0x50000000	GPIO	GPIO	General purpose input and output	Deprecated
0	0x50000000	GPIO	PO	General purpose input and output, port 0	
0	0x50000300	GPIO	P1	General purpose input and output, port 1	
42	0x5002A000	CRYPTOCELL	CRYPTOCELL	CryptoCell subsystem control interface	
N/A	0x10000000	FICR	FICR	Factory information configuration	
N/A	0x10001000	UICR	UICR	User information configuration	



9 AHB multilayer

AHB multilayer enables parallel access paths between multiple masters and slaves in a system. Access is resolved using priorities.

Each bus master is connected to the slave devices using an interconnection matrix. The bus masters are assigned priorities. Priorities are used to resolve access when two (or more) bus masters request access to the same slave device. The following applies:

- If two (or more) bus masters request access to the same slave device, the master with the highest priority is granted the access first.
- Bus masters with lower priority are stalled until the higher priority master has completed its transaction.
- If the higher priority master pauses at any point during its transaction, the lower priority master in queue is temporarily granted access to the slave device until the higher priority master resumes its activity.
- · Bus masters that have the same priority are mutually exclusive, thus cannot be used concurrently.

Below is a list of bus masters in the system and their priorities.

Table 7: AHB bus masters (listed in priority order, highest to lowest)

Bus master name	Description
CPU	
CTRL-AP	
USB	
CRYPTOCELL	
SPIM1/SPIS1/TWIM1/TWIS1	Same priority and mutually exclusive
RADIO	
CCM/ECB/AAR	Same priority and mutually exclusive
SAADC	
UARTEO	
SPIMO/SPISO/TWIMO/TWISO	Same priority and mutually exclusive
SPIM2/SPIS2	Same priority and mutually exclusive
NFCT	
12S	
PDM	
PWM0	
PWM1	
PWM2	
QSPI	
PWM3	
UARTE1	
SPIM3	

Defined bus masters are the CPU and the peripherals with implemented EasyDMA, and the available slaves are RAM AHB slaves. How the bus masters and slaves are connected using the interconnection matrix is illustrated in *Memory* on page 20.



10 EasyDMA

EasyDMA is a module implemented by some peripherals to gain direct access to Data RAM.

EasyDMA is an AHB bus master similar to CPU and is connected to the AHB multilayer interconnect for direct access to Data RAM. EasyDMA is not able to access flash.

A peripheral can implement multiple EasyDMA instances to provide dedicated channels. For example, for reading and writing of data between the peripheral and RAM. This concept is illustrated in *Figure 5: EasyDMA example* on page 26.

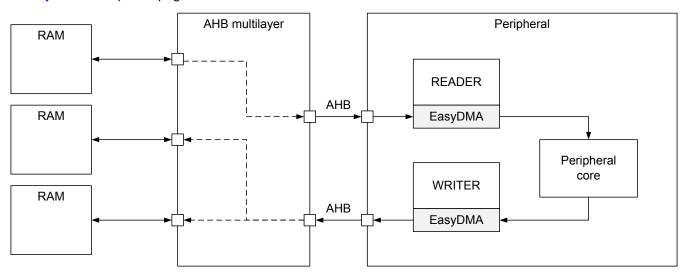


Figure 5: EasyDMA example

An EasyDMA channel is usually implemented like illustrated by the code below, but some variations may occur:

```
READERBUFFER_SIZE 5
WRITERBUFFER_SIZE 6

uint8_t readerBuffer[READERBUFFER_SIZE] __at__ 0x20000000;
uint8_t writerBuffer[WRITERBUFFER_SIZE] __at__ 0x20000005;

// Configuring the READER channel
MYPERIPHERAL->READER.MAXCNT = READERBUFFER_SIZE;
MYPERIPHERAL->READER.PTR = &readerBuffer;

// Configure the WRITER channel
MYPERIPHERAL->WRITER.MAXCNT = WRITEERBUFFER_SIZE;
MYPERIPHERAL->WRITER.PTR = &writerBuffer;
```

This example shows a peripheral called MYPERIPHERAL that implements two EasyDMA channels - one for reading called READER, and one for writing called WRITER. When the peripheral is started, it is assumed that the peripheral will:

- Read 5 bytes from the readerBuffer located in RAM at address 0x20000000.
- · Process the data.
- Write no more than 6 bytes back to the writerBuffer located in RAM at address 0x20000005.

The memory layout of these buffers is illustrated in Figure 6: EasyDMA memory layout on page 27.



0x20000000	readerBuffer[0]	readerBuffer[1]	readerBuffer[2]	readerBuffer[3]
0x20000004	readerBuffer[4]	writerBuffer[0]	writerBuffer[1]	writerBuffer[2]
0x20000008	writerBuffer[3]	writerBuffer[4]	writerBuffer[5]	

Figure 6: EasyDMA memory layout

The WRITER.MAXCNT register should not be specified larger than the actual size of the buffer (writerBuffer). Otherwise, the channel would overflow the writerBuffer.

Once an EasyDMA transfer is completed, the AMOUNT register can be read by the CPU to see how many bytes were transferred. For example, CPU can read MYPERIPHERAL->WRITER.AMOUNT register to see how many bytes WRITER wrote to RAM.

10.1 EasyDMA array list

EasyDMA is able to operate in a mode called array list.

READER.PTR = &ReaderList

The array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

The EasyDMA array list can be implemented by using the data structure ArrayList_type as illustrated in the code example below:

```
#define BUFFER_SIZE 4

typedef struct ArrayList
{
   uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type ReaderList[3];

READER.MAXCNT = BUFFER_SIZE;
READER.PTR = &ReaderList;
```

The data structure only includes a buffer with size equal to the size of READER.MAXCNT register. EasyDMA uses the READER.MAXCNT register to determine when the buffer is full.

0x20000000 : ReaderList[0] buffer[0] buffer[1] buffer[2] buffer[3] 0x20000004 : ReaderList[1] buffer[0] buffer[1] buffer[2] buffer[3] 0x20000008 : ReaderList[2] buffer[0] buffer[1] buffer[2] buffer[3]

Figure 7: EasyDMA array list



11 NVMC — Non-volatile memory controller

The non-volatile memory controller (NVMC) is used for writing and erasing the internal flash memory and the UICR.

Before a write can be performed, the NVMC must be enabled for writing in CONFIG.WEN. Similarly, before an erase can be performed, the NVMC must be enabled for erasing in CONFIG.EEN, see *CONFIG* on page 30. The user must make sure that writing and erasing are not enabled at the same time. Failing to do so may result in unpredictable behavior.

11.1 Writing to flash

When writing is enabled, the flash is written by writing a full 32-bit word to a word-aligned address in the flash

The NVMC is only able to write '0' to bits in the flash that are erased, that is, set to '1'. It cannot write back a bit to '1'.

As illustrated in *Memory* on page 20, the flash is divided into multiple pages that are further divided into multiple blocks. The same block in the flash can only be written n_{WRITE} number of times before an erase must be performed using *ERASEPAGE* or *ERASEALL*. See the memory size and organization in *Memory* on page 20 for block size.

Only full 32-bit words can be written to flash using the NVMC interface. To write less than 32 bits to flash, write the data as a word, and set all the bits that should remain unchanged in the word to '1'. Note that the restriction about the number of writes (see above) still applies in this case.

The time it takes to write a word to the flash is specified by t_{WRITE} . The CPU is halted if the CPU executes code from the flash while the NVMC is writing to the flash.

Only word-aligned writes are allowed. Byte or half-word-aligned writes will result in a hard fault.

11.2 Erasing a page in flash

When erase is enabled, the flash can be erased page by page using the ERASEPAGE register.

After erasing a flash page, all bits in the page are set to '1'. The time it takes to erase a page is specified by $t_{ERASEPAGE}$. The CPU is halted if the CPU executes code from the flash while the NVMC performs the erase operation.

11.3 Writing to user information configuration registers (UICR)

User information configuration registers (UICR) are written in the same way as flash. After UICR has been written, the new UICR configuration will only take effect after a reset.

UICR can only be written n_{WRITE} number of times before an erase must be performed using ERASEUICR or ERASEALL.

The time it takes to write a word to the UICR is specified by t_{WRITE} . The CPU is halted if the CPU executes code from the flash while the NVMC is writing to the UICR.

11.4 Erasing user information configuration registers (UICR)

When erase is enabled, UICR can be erased using the ERASEUICR register.

After erasing UICR all bits in UICR are set to '1'. The time it takes to erase UICR is specified by *t*_{ERASEPAGE}. The CPU is halted if the CPU executes code from the flash while the NVMC performs the erase operation.



11.5 Erase all

When erase is enabled, the whole flash and UICR can be erased in one operation by using the ERASEALL register. ERASEALL will not erase the factory information configuration registers (FICR).

The time it takes to perform an ERASEALL command is specified by $t_{ERASEALL}$ The CPU is halted if the CPU executes code from the flash while the NVMC performs the erase operation.

11.6 Cache

An instruction cache (I-Cache) can be enabled for the ICODE bus in the NVMC.

See the Memory map in *Memory map* on page 21 for the location of flash.

A cache hit is an instruction fetch from the cache, and it has a 0 wait-state delay. The number of wait-states for a cache miss, where the instruction is not available in the cache and needs to be fetched from flash, depends on the processor frequency and is shown in *CPU* on page 18

Enabling the cache can increase CPU performance and reduce power consumption by reducing the number of wait cycles and the number of flash accesses. This will depend on the cache hit rate. Cache will use some current when enabled. If the reduction in average current due to reduced flash accesses is larger than the cache power requirement, the average current to execute the program code will reduce.

When disabled, the cache does not use current and does not retain its content.

It is possible to enable cache profiling to analyze the performance of the cache for your program using the *ICACHECNF* register. When profiling is enabled, the *IHIT* and *IMISS* registers are incremented for every instruction cache hit or miss respectively. The hit and miss profiling registers do not wrap around after reaching the maximum value. If the maximum value is reached, consider profiling for a shorter duration to get correct numbers.

11.7 Registers

Table 8: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001E000	NVMC	NVMC	Non-volatile memory controller	

Table 9: Register Overview

Register	Offset	Description	
READY	0x400	Ready flag	
CONFIG	0x504	Configuration register	
ERASEPAGE	0x508	Register for erasing a page in code area	
ERASEPCR1	0x508	Register for erasing a page in code area. Equivalent to ERASEPAGE.	Deprecated
ERASEALL	0x50C	Register for erasing all non-volatile user memory	
ERASEPCR0	0x510	Register for erasing a page in code area. Equivalent to ERASEPAGE.	Deprecated
ERASEUICR	0x514	Register for erasing user information configuration registers	
ICACHECNF	0x540	I-code cache configuration register.	
IHIT	0x548	I-code cache hit counter.	
IMISS	0x54C	I-code cache miss counter.	

11.7.1 READY

Address offset: 0x400

Ready flag



Bit	numbe	er		31 3	30 29	9 28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14 :	13 :	12 1	111	0 9	8	7	6	5	4	3	2	1 0
Id																																Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe						De	scri	ipti	on																		
Α	R	READY									ΝV	MC	C is	read	dy c	or bu	ısy															
			Busy	0							ΝV	MC	C is	bus	y (o	n-g	oin	g w	rite	or	era	se c	per	atio	n)							
			Ready	1							ΝV	MC	C is	read	dy																	

11.7.2 **CONFIG**

Address offset: 0x504 Configuration register

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 1	8 1	7 16	5 15	14	13	12	11	10 !	9	8 .	7 (6 5	5 4	4 3	2	1	0
Id																																Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 () (0 (0	0	0	0	0	0	0	0	0	0 () (0 (0 (0 0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	1																		
Α	RW	WEN										Pro	grai	m m	em	ory	aco	ess	mo	de.	It is	str	ong	y re	coı	mm	enc	led					
												to c	only	acti	vat	e e	rase	an	d w	rite	mo	des	wh	en t	hey	are	e ac	tive	ely				
												use	d. E	nab	ling	w g	ite	or e	rase	e wi	ill in	vali	date	the	e ca	che	an	d ke	eep)			
												it ir	ıvali	idate	ed.																		
			Ren	0								Rea	id o	nly a	СС	ess																	
			Wen	1								Wri	ite e	enab	led	ı																	
			Een	2								Era	se e	nab	led																		

11.7.3 ERASEPAGE

Address offset: 0x508

Register for erasing a page in code area

Bit	numbe	er		31	30	29	28 2	27 :	26 2	25 :	24 2	23 2	22 2	21 2	0 1	9 1	8 1	7 16	15	14	13	12	11	10	9	8	7 (6 5	5 4	3	2	1 (O
Id				Α	Α	Α	Α	Α	Α ,	Α	A	Α	Α ,	A A	4	Δ ,	. Δ	A	Α	Α	Α	Α	Α	Α	Α	A A	Δ ,	Α Α	A A	Α	Α	Α /	Δ
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 (0 0) (0 (0	0	0	0	0	0	0	0	0	0 () (0 (0	0	0	0 (o
Id	RW	Field	Value Id	Va	alue							Des	crip	tior	١																		
Α	RW	ERASEPAGE									F	Reg	iste	r fo	st	arti	ng e	eras	e of	ар	age	in o	ode	e ar	ea								
											Т	Γhe	valı	ue is	s th	ie a	ddre	ess 1	o th	ne p	oage	e to	be (eras	sed.	. (Ac	ldre	esse	s of				
											f	irst	t wo	ord i	n p	age). N	ote	tha	t th	e er	ase	mu	st b	e e	nab	led	usi	ng				
											C	CON	NFIG	S.W	EN I	bef	ore	the	pag	e c	an b	e e	rase	d. A	٩tte	emp	ts t	o er	ase				
											p	oag	es t	hat	are	ou	tsid	e th	e co	ode	are	a m	ay r	esu	ılt ir	n un	des	sirat	le				
											b	oeh	avio	our,	e.g	. th	e w	ron	g pa	ge	may	/ be	era	sed	١.								

11.7.4 ERASEPCR1 (Deprecated)

Address offset: 0x508

Register for erasing a page in code area. Equivalent to ERASEPAGE.

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19	18 1	17 1	16 1	.5 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	Δ Δ	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	۱ ۸	4 А
Res	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	ERASEPCR1										Re	giste	er fo	or e	ras	ing	ара	age	in c	ode	are	a. E	quiv	vale	nt i	to						
												ER	ASE	PAC	ŝΕ.																		

11.7.5 ERASEALL

Address offset: 0x50C

Register for erasing all non-volatile user memory



Bitı	numbe	er		31	1 30	29	28	3 27	7 26	5 2	5 2	24 :	23	22	21	20	19	18	3 17	7 10	5 1	5 1	4 1	3 1	2 1	.1 1	0	9	8	7	6	5	4	3	2	1	0
Id																																					Α
Res	et 0x0	0000000		0	0	0	0	0	0	C)	0	0	0	0	0	0	0	0	0	C) () () (0	0 ()	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							ı	Des	scri	pti	on																					
Α	RW	ERASEALL										ı	Era	se i	all ı	nor	ı-vc	olat	ile	me	mo	ry	ncl	udi	ng	UIC	Rr	egi	ste	rs. I	Not	e.					
												1	tha	t th	ne e	eras	se r	nus	t b	e e	nal	ole	d us	ing	CC	NF	IG.	WE	N Ł	efo	ore	the	è				
													nor	า-v	olat	ile	me	emo	ry	car	be	e er	ase	d.													
			NoOperation	0								-	No	ор	era	tio	n																				
			Erase	1								:	Sta	rt c	hip	er	ase																				

11.7.6 ERASEPCR0 (Deprecated)

Address offset: 0x510

Register for erasing a page in code area. Equivalent to ERASEPAGE.

Bit	numb	er		31	L 30	29	28	27	26	25	24	23	22 2	21 2	20 19	9 18	3 17	16	15	14	13	12 1	.1 1	0 9	8	7	6	5	4	3	2	1 0	
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A ,	А А	. A	А	Α	Α	Α	Α	A .	4 4	Α Α	. A	Α	Α	Α	Α	Α	Δ,	А А	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0	
Id	RW	Field	Value Id	Va	alue							Des	crip	tio	n																		
Α	RW	ERASEPCR0										Reg	iste	r fo	r sta	rtir	ng ei	rase	of	а ра	ige	in c	ode	are	a. E	quiv	/ale	nt t	o				
												ER/	SEP	AG	E.																		

11.7.7 ERASEUICR

Address offset: 0x514

Register for erasing user information configuration registers

Bit r	iumbe	r		31	1 30	29	28	8 27	7 2	6 2	5 2	4 2	23 2	22	21	20	19	18	3 1	.7 1	6	15	14	13	12	11	. 10	9	8	7	6	5	4	3	2	1	0
Id																																					Α
Res	et 0x0	0000000		0	0	0	0	0	C) () (0	0	0	0	0	0	0	(0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue								Des	cri	ptio	on																					
Α	RW	ERASEUICR										F	Reg	iste	er s	tar	tin	g e	ras	se o	of a	IIι	ise	rin	for	ma	tior	со	nfig	ura	tio	n					
												r	egi	ste	rs.	No	te	tha	at t	he	era	se	m	ust	be	en	able	d u	sin	g							
												(CON	۱FI	G.V	۷E۱	N b	efc	re	th	e U	ICF	R ca	ın b	e e	era	sed.										
			NoOperation	0								١	No (оре	era	tioi	n																				
			Erase	1								5	Star	t e	ras	e o	of U	IICF	3																		

11.7.8 ICACHECNF

Address offset: 0x540

I-code cache configuration register.

nber		31	30 2	29	28	27	26	6 25	5 24	4 2	3 2	2 2:	1 20	0 1	9 1	8 1	7 1	6 1	5 1	4 1	3 1	2 1	1 1	0 9	8	7	6	5	4	3	2	1 0	ı
																									В							А	l
0x00000000		0	0	0	0	0	0	0	0) (0	0	0) (0) () () () (0 (0	0 (0 (0	0	0	0	0	0	0	0	0 0	l
W Field	Value Id	Va	lue							D	esc	ript	tion	,																			l
W CACHEEN										С	ach	e e	nab	le																			
	Disabled	0								D	isal	ble (cacl	he.	Inv	alio	date	es a	II c	ach	e e	ntri	es.										
	Enabled	1								Ε	nab	le c	cach	ne																			
W CACHEPROFEN										С	ach	ер	rofi	ling	g er	abl	e																
	Disabled	0								D	isal	ble	cacl	he	pro	filir	ng																
	Enabled	1								Ε	nab	le c	cach	ne p	orof	ilin	g																
		DX00000000 W Field Value Id W CACHEEN Disabled Enabled W CACHEPROFEN Disabled	DX00000000 0 0 W Field Value Id Va W CACHEEN Disabled 0 Enabled 1 W CACHEPROFEN Disabled 0	DXX00000000 0 0 0 W Field Value Id Value W CACHEEN Disabled 0 Enabled 1 W CACHEPROFEN Disabled 0	DXX00000000	Disabled 0 CACHEPROFEN Disabled 0 Enabled 0 Enabled 0 Disabled 0 Disabled 0 Disabled 0 Disabled 0 Disabled 0	Disabled 0 CACHEPROFEN Disabled 0 Enabled 0 Enabled 0 Disabled 0 Disabled 0 Enabled 0	DX00000000	DX00000000	DXX000000000	Disabled Disabled Disabled O	DXX000000000 0 <t< td=""><td>Disabled Disabled 1 Cache point Cache poi</td><th>DXX00000000</th><th>Dxx000000000 <t< th=""><th>DXX000000000</th><th>DXX000000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0</th><td>Dxx000000000 <t< td=""><td>DXX000000000</td><td>Disabled Disabled Disabled O</td><td>Disabled Disabled Disabled</td><td>Disabled Disabled Disabled</td><td>Disabled Disabled 1 Enabled 1 Enabled Cache profiling enable W CACHEPROFEN Disabled 0</td><td>Disabled Disabled 1 Enabled 1 Enabled 0<</td><td>Disabled Disabled 1 Enabled 1 Enabled 0<</td><td> Background</td><td>Disabled 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>Disabled 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>Disabled 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>Disabled Disabled Disable cache profiling enable</td><td>Disabled O CACHEPROFEN Disabled O CACHEPROFEN Disable cache profiling enable</td><td>Disabled O</td><td>A DAXODOODOOOOOOOOOOOOOOOOOOOOOOOOOOOOOO</td></t<></td></t<></th></t<>	Disabled Disabled 1 Cache point Cache poi	DXX00000000	Dxx000000000 0 <t< th=""><th>DXX000000000</th><th>DXX000000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0</th><td>Dxx000000000 <t< td=""><td>DXX000000000</td><td>Disabled Disabled Disabled O</td><td>Disabled Disabled Disabled</td><td>Disabled Disabled Disabled</td><td>Disabled Disabled 1 Enabled 1 Enabled Cache profiling enable W CACHEPROFEN Disabled 0</td><td>Disabled Disabled 1 Enabled 1 Enabled 0<</td><td>Disabled Disabled 1 Enabled 1 Enabled 0<</td><td> Background</td><td>Disabled 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>Disabled 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>Disabled 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>Disabled Disabled Disable cache profiling enable</td><td>Disabled O CACHEPROFEN Disabled O CACHEPROFEN Disable cache profiling enable</td><td>Disabled O</td><td>A DAXODOODOOOOOOOOOOOOOOOOOOOOOOOOOOOOOO</td></t<></td></t<>	DXX000000000	DXX000000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Dxx000000000 0 <t< td=""><td>DXX000000000</td><td>Disabled Disabled Disabled O</td><td>Disabled Disabled Disabled</td><td>Disabled Disabled Disabled</td><td>Disabled Disabled 1 Enabled 1 Enabled Cache profiling enable W CACHEPROFEN Disabled 0</td><td>Disabled Disabled 1 Enabled 1 Enabled 0<</td><td>Disabled Disabled 1 Enabled 1 Enabled 0<</td><td> Background</td><td>Disabled 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>Disabled 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>Disabled 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>Disabled Disabled Disable cache profiling enable</td><td>Disabled O CACHEPROFEN Disabled O CACHEPROFEN Disable cache profiling enable</td><td>Disabled O</td><td>A DAXODOODOOOOOOOOOOOOOOOOOOOOOOOOOOOOOO</td></t<>	DXX000000000	Disabled Disabled Disabled O	Disabled Disabled	Disabled Disabled	Disabled Disabled 1 Enabled 1 Enabled Cache profiling enable W CACHEPROFEN Disabled 0	Disabled Disabled 1 Enabled 1 Enabled 0<	Disabled Disabled 1 Enabled 1 Enabled 0<	Background	Disabled 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Disabled 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Disabled 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Disabled Disable cache profiling enable	Disabled O CACHEPROFEN Disable cache profiling enable	Disabled O	A DAXODOODOOOOOOOOOOOOOOOOOOOOOOOOOOOOOO

11.7.9 IHIT

Address offset: 0x548 I-code cache hit counter.



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW HITS	Number of cache hits

11.7.10 IMISS

Address offset: 0x54C

I-code cache miss counter.

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW MISSES		Number of cache misses

11.8 Electrical specification

11.8.1 Flash programming

Symbol	Description	Min.	Тур.	Max.	Units
n _{WRITE,BLOCK}	Amount of writes allowed in a block between erase			403	
n _{WRITE}	Number of times an address can be written between erase ¹			2	
t _{WRITE}	Time to write one 32-bit word			41 ²	μs
t _{ERASEPAGE}	Time to erase one page			85 ³	ms
t _{ERASEALL}	Time to erase all flash			169 ⁴	ms
I _{write}	Flash write current			5	mA
l _{erasepage}	Flash erase page current			5	mA
I _{eraseall}	Flash erase all current			5	mA

11.8.2 Cache size

Symbol	Description	Min.	Тур.	Max.	Units
Size _{ICODE}	I-Code cache size		2048		Bytes

¹ The page must be erased when either of $n_{WRITE,BLOCK}$ or n_{WRITE} is not satisfied

² HFXO is used here, this may vary upto +/-5% when HFINT is used ³ HFXO is used here, this may vary upto +/-5% when HFINT is used

⁴ HFXO is used here, this may vary upto +/-5% when HFINT is used



12 FICR — Factory information configuration registers

Factory information configuration registers (FICR) are pre-programmed in factory and cannot be erased by the user. These registers contain chip-specific information and configuration.

12.1 Registers

Table 10: Instances

Base address	Peripheral	Instance	Description	Configuration
0x10000000	FICR	FICR	Factory information configuration	

Table 11: Register Overview

Register	Offset	Description	
CODEPAGESIZE	0x010	Code memory page size	
CODESIZE	0x014	Code memory size	
DEVICEID[0]	0x060	Device identifier	
DEVICEID[1]	0x064	Device identifier	
ER[0]	0x080	Encryption root, word 0	
ER[1]	0x084	Encryption root, word 1	
ER[2]	0x088	Encryption root, word 2	
ER[3]	0x08C	Encryption root, word 3	
IR[0]	0x090	Identity Root, word 0	
IR[1]	0x094	Identity Root, word 1	
IR[2]	0x098	Identity Root, word 2	
IR[3]	0x09C	Identity Root, word 3	
DEVICEADDRTYPE	0x0A0	Device address type	
DEVICEADDR[0]	0x0A4	Device address 0	
DEVICEADDR[1]	0x0A8	Device address 1	
INFO.PART	0x100	Part code	
INFO.VARIANT	0x104	Part variant (hardware version and production configuration)	
INFO.PACKAGE	0x108	Package option	
INFO.RAM	0x10C	RAM variant	
INFO.FLASH	0x110	Flash variant	
	0x114		Reserved
	0x118		Reserved
	0x11C		Reserved
TEMP.A0	0x404	Slope definition A0	
TEMP.A1	0x408	Slope definition A1	
TEMP.A2	0x40C	Slope definition A2	
TEMP.A3	0x410	Slope definition A3	
TEMP.A4	0x414	Slope definition A4	
TEMP.A5	0x418	Slope definition A5	
TEMP.BO	0x41C	Y-intercept B0	
TEMP.B1	0x420	Y-intercept B1	
TEMP.B2	0x424	Y-intercept B2	
TEMP.B3	0x428	Y-intercept B3	
TEMP.B4	0x42C	Y-intercept B4	
TEMP.B5	0x430	Y-intercept B5	
TEMP.TO	0x434	Segment end TO	
TEMP.T1	0x438	Segment end T1	
TEMP.T2	0x43C	Segment end T2	
TEMP.T3	0x440	Segment end T3	
TEMP.T4	0x444	Segment end T4	



Register	Offset	Description
NFC.TAGHEADER0	0x450	Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER1	0x454	Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER2	0x458	Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER3	0x45C	Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.

12.1.1 CODEPAGESIZE

Address offset: 0x010 Code memory page size

Bit	nur	nbe	r		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A A A A A A A A A A A A A A A A A A A
Re	set (0xFF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	R	RW	Field	Value Id	Value Description
^	_		CODEDACECIZE		Code manuscriptor

A R CODEPAGESIZE Code memory page size

12.1.2 CODESIZE

Address offset: 0x014 Code memory size

Bit nu	ımbe	er		31	30	29	28	27	26	25	24	23	22	21 :	20 :	19 :	18 1	17 1	16 :	15 1	L4 1	13 :	12 :	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	А А
Reset	0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	1 1
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																			
Α	R	CODESIZE										Cod	le n	nen	nor	/ siz	e ir	า ทน	ımb	er	of p	ag	es											

Total code space is: CODEPAGESIZE * CODESIZE

12.1.3 DEVICEID[0]

Address offset: 0x060

Device identifier

Bi	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 :	16 :	15 1	.4 13	12	11 :	10 9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 A	Α	Α	A A	A	Α	Α	Α	Α	Α	Α	Α	Α
Re	set 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1	1 :	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	R	DEVICEID										64	bit ı	uni	que	de	vice	ide	enti	fier													
												ide		ier.	DE	VIC	EID				sign								ie				

12.1.4 DEVICEID[1]

Address offset: 0x064

Device identifier

Bit number	31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Id	A A A A	A A A A A A A A A	A A A A A A A A A A A A A A A	Α
Reset 0xFFFFFFF	1 1 1 1 :	1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1
Id RW Field Value Id	Value	Description		

A R DEVICEID 64 bit unique device identifier



Reset 0xFFFFFFFF 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
2 10	1 1 1 1 1 1 1 1 1 1 1 1 1
Id	. A A A A A A A A A A A
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 1	4 13 12 11 10 9 8 7 6 5 4 3 2 1 0

 $\label{eq:decomposition} DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier.$

12.1.5 ER[0]

Address offset: 0x080 Encryption root, word 0

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 1	19 18 17 16 15 14 13 12	2 11 10 9 8 7 6	5 4 3 2 1 0
Id		$A \ A \ A \ A \ A$. A A A A A A	A	A A A A A A	A A A A A
Reset OxFFFF	FFF	1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1	1 1 1 1 1 1
ld RW Fi	ld Value Id	Value	Description			
A R F			Encryption ro	ot_word 0		

12.1.6 ER[1]

Address offset: 0x084 Encryption root, word 1

Bit num	ber		33	1 30	29	28	3 2	7 26	25	5 24	1 2	3 22	2 21	20	19	18	17	16	15	14	13	12 :	11 1	0 9	8	7	6	5	4	3	2 :	1 0	
Id			Α	Α	A	. A	A	A A	А	A	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	. A	Α	Α	Α	Α	Α	A A	4 A	
Reset 0	xFFFFFFF		1	1	. 1	1	1	1	1	. 1	1	. 1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	1	1	1	1	1	1	1 1	1 1	
Id R\	W Field	Value Id	V	alue	е						D	esci	ript	ion																			
A R	ER										Eı	ncrv	ptio	on r	oot	. wo	ord	1															

12.1.7 ER[2]

Address offset: 0x088 Encryption root, word 2

Bit n	umb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 :	13 :	12 1	11 :	10 !	9	8	7	6	5 4	4 3	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A	Α.	Α.	Α	Α	A A	Δ ,	А А	Α	Α
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	1	1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	R	ER										End	ryp	tio	n ro	ot,	wo	rd 2	2															

12.1.8 ER[3]

Address offset: 0x08C Encryption root, word 3

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0												
Id		A A A A A A A A A A A A A A A A A A A												
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												
Id RW Field	Value Id	Value Description												
A R ER		Encryption root, word 3												

12.1.9 IR[0]

Address offset: 0x090 Identity Root, word 0



Bitı	numb	er		31	30	29	28	3 2	7 20	5 2	5 2	4 2	3 2	2 2:	L 2	0 19	9 1	8 17	7 1	6 15	5 14	1 13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	A	A A	. 4	Α Α			A		Α Α	. 4	A A	. 4	A	. Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	_ 1	L 1	. 1	. 1	1	1	l 1	. 1	l 1	. 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							D	esc	ript	ior	1																		
Α	R	IR										lc	len	tity	Ro	ot, v	10%	rd 0																

12.1.10 IR[1]

Address offset: 0x094 Identity Root, word 1

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 :	13 :	L2 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Α	. A	Α	Α	Α	Α	Α	Α	АА
Res	et 0x	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	R	IR		Identity Root, word 1																													

12.1.11 IR[2]

Address offset: 0x098 Identity Root, word 2

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0											
Id		A A A A A A A A A A A A A A A A A A A											
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1											
Id RW Field	Value Id	Value Description											
A R IR		Identity Root, word 2											

12.1.12 IR[3]

Address offset: 0x09C Identity Root, word 3

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0												
Id		A A A A A A A A A A A A A A A A A A A												
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												
ld RW Field	Value Id	Value Description												
A R IR		Identity Root, word 3												

12.1.13 DEVICEADDRTYPE

Address offset: 0x0A0

Device address type

Bit	numbe	er		31 30	29	28	27	26	25	24	23	22	21	20	19	18	17 1	16 1	.5 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																																Α
Res	et OxF	FFFFFF		1 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	1	1	1	1	1	1	1	1	1 :	l 1	. 1
Id	RW	Field	Value Id	Valu	9						De	scri	ptic	on																		
Α	R	DEVICEADDRTYPE									De	vice	ad	dre	ss t	ype																
			Public	0							Pul	blic	ado	dres	SS																	
			Random	1							Rai	ndo	m a	ddı	ress	5																

12.1.14 DEVICEADDR[0]

Address offset: 0x0A4

Device address 0



Bit	numbe	er		31	. 30	29	9 28	8 2	27	26	25	24	1 2	3 2	2 2	1 2	20	19	18	17	16	15	14	13	12	2 13	1 10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Δ	. 4	۱ ،	Α	Α	Α	Α		۱ ۱	۱ ۸	4	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0xF	FFFFFF		1	1	1	. 1	:	1	1	1	1	. 1	1 :	ι :	ı	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	alue	:							D	esc	rip	tio	n																				
Α	R	DEVICEADDR											4	8 b	it d	evi	ce	ado	lre:	SS																	

DEVICEADDR[0] contains the least significant bits of the device address. DEVICEADDR[1] contains the most significant bits of the device address. Only bits [15:0] of DEVICEADDR[1] are used.

12.1.15 **DEVICEADDR**[1]

Address offset: 0x0A8

Device address 1

Bit r	numbe	er		31	1 30	29	28	3 2	7 26	25	5 24	1 23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	alue							De	escr	ipti	on																			
Α	R	DEVICEADDR										48	bit	de	/ice	ado	dre	SS																

DEVICEADDR[0] contains the least significant bits of the device address. DEVICEADDR[1] contains the most significant bits of the device address. Only bits [15:0] of DEVICEADDR[1] are used.

12.1.16 INFO.PART

Address offset: 0x100

Part code

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	9 18	3 17	16	15	14	13	L2 1	.1 10	9	8	7	6	5	4	3	2 :	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 A	. A	Α	Α	Α	Α	A A	ДД	Α	Α	Α	Α	Α	Α	Α	A A	A A
Res	et 0x(00052840		0	0	0	0	0	0	0	0	0	0	0	0 (0 1	0	1	0	0	1	0	1 0	0	0	0	1	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																	
Α	R	PART										Par	t co	de																		
			N52840	0x	528	40						nRl	528	840																		
			Unspecified	0x	FFF	FFF	FF					Un	spe	cifie	d																	

12.1.17 INFO.VARIANT

Address offset: 0x104

Part variant (hardware version and production configuration)

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	1 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1 :	1 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	1 1
Id	RW	Field	Value Id	Va	lue	:						Des	crip	tion																			
Α	R	VARIANT										Par	t var	iant	(ha	ırdv	vare	ve	rsio	n a	nd	pro	duc	tio	n cc	onfi	gur	atic	n).				
												Enc	ode	d as	AS	CII.																	
			AAAA	0x	414	1141	141					AAA	ΔА																				
			AAAB	0x	414	1141	142					AAA	4Β																				
			AABA	0x	414	1142	241					AAE	ВА																				
			AABB	0x	414	1142	242					AAE	ВВ																				
			AAB0	0x	414	1142	230					AAE	В0																				
			ABBA	0x	414	1242	241					ABE	ВА																				
			Unspecified	0x	FFF	FFF	FF					Uns	spec	ified																			

12.1.18 INFO.PACKAGE

Address offset: 0x108

Package option



Bitı	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 19	9 18	3 17	16	15	14	13	12 1	11 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 A	Α	Α	Α	Α	Α	Α	Α.	A A	A	Α	Α	Α	Α	Α	Α	A A	А А
Res	et 0x	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1 :	l 1	1	1	1	1	1	1	1	1 1	l 1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	1																	
Α	R	PACKAGE										Pac	kag	e op	tior	1																
			QI	0x	200	4						QIx	x - 7	73-р	in a	QFN																
			Unspecified	0x	FFFI	FF	FF					Uns	pec	ifie	b																	

12.1.19 INFO.RAM

Address offset: 0x10C

RAM variant

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 :	12 1	.1 1	9	8	7	6	5	4	3 2	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	4 Δ	Α	Α	Α	Α	Α	Α	Α Α	A A	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1 :	1 1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	R	RAM										RA	M v	aria	nt																		
			K16	0x	10							16	kBy	te l	RAN	Л																	
			K32	0x	20							32	kBy	te I	RAN	Л																	
			K64	0x	40							64	kBy	te I	RAN	Л																	
			K128	0x	80							12	8 kB	yte	RA	M																	
			K256	0x	100							25	6 kB	yte	RA	M																	
			Unspecified	0x	FFF	FFF	FF					Ur	spe	cifie	ed																		

12.1.20 INFO.FLASH

Address offset: 0x110

Flash variant

Bit	numbe	er		31	1 3	0 29	9 2	8 27	7 2	6 25	5 24	23	22	21	20	19	18	17	16	15	14 1	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	A	4 A	. 4	A A	Δ	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	Α	Α	Α	Α	Α	Α	Α	Α	A A	. A	Α
Res	et OxF	FFFFFF		1	1	l 1	. 1	l 1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	alu	e						De	scri	ptic	on																		
Α	R	FLASH										Fla	sh v	/aria	ant																		
			K128	0>	ĸ80)						12	8 kB	yte	FL	ASH	1																
			K256	0>	κ 1 0	00						25	6 kB	yte	FL	ASH	1																
			K512	0>	k20	00						51	2 kB	yte	FL	ASH	1																
			K1024	0>	κ40	00						1 N	⁄ΙВу	te F	LA	SH																	
			K2048	0>	ĸ80	00						2 N	⁄ΙВу	te F	LA	SH																	
			Unspecified	0>	ĸFF	FFFF	FFF	:				Un	spe	cifie	ed																		

12.1.21 TEMP.A0

Address offset: 0x404 Slope definition A0

Bit r	numbe	er		31 30 29 28 27 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Id					A A A A A A A A	A A A A
Rese	et OxF	FFFF320		1 1 1 1 1 1	$1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \$	0 0 0 0
Id	RW	Field	Value Id	Value	Description	
Α	R	Α			A (slope definition) register.	

12.1.22 TEMP.A1

Address offset: 0x408 Slope definition A1



12.1.23 TEMP.A2

Address offset: 0x40C Slope definition A2

12.1.24 TEMP.A3

Address offset: 0x410 Slope definition A3

12.1.25 TEMP.A4

Address offset: 0x414 Slope definition A4

12.1.26 TEMP.A5

Address offset: 0x418 Slope definition A5

12.1.27 TEMP.B0

Address offset: 0x41C

Y-intercept B0



Bit sumbles of the proper shadows of the pro

12.1.28 TEMP.B1

Address offset: 0x420

Y-intercept B1

12.1.29 TEMP.B2

Address offset: 0x424

Y-intercept B2

Bi	t nu	ımbe	er		31	30 29	9 2	8 27	7 26	25	24	23 2	22 2	1 2	0 1	9 18	3 17	7 16	15	14	13	12 1	.1 1	9	8	7	6	5	4	3	2	1 0
Id																					Α	Α.	4 Δ	Α	Α	Α	Α	Α	Α	Α	A	А А
R	set	0xF	FFF3F98		1	1 1	. 1	l 1	1	1	1	1	1 :	1 1	L 1	1	1	1	0	0	1	1	1 1	1	1	1	0	0	1	1	0	0 0
Id		RW	Field	Value Id	Val	ue						Des	crip	tior	ı																	
Α		R	В									В (у	-int	erce	ept)																	

12.1.30 TEMP.B3

Address offset: 0x428

Y-intercept B3

-	R		В					В	(y-in	terc	ept)																
ı	d RI	W	Field	Value Id	Value			De	escri	ptio	n																
ı	eset 0	xFI	FF0012		1 1 1 1 1	۱ 1	1 :	1 1	1	1	1 1	1	1	1 (0 0	0	0	0 0	0	0	0	0	0	1	0 0	1	0
1	d l															Α	Α	ΑА	Α	Α	Α	Α	Α	Α	A A	Α	Α
E	it num	nbe	r		31 30 29 28 2	7 26	25 2	4 23	22	21 2	20 19	18	17	16 1	.5 14	13	12	11 10	9	8	7	6	5	4	3 2	1	0

12.1.31 TEMP.B4

Address offset: 0x42C

Y-intercept B4

Bit r	numb	er		31	30 2	9 2	8 27	26	25 2	24 2	23 2	22 2	1 2	0 1	9 18	3 17	16	15	14 1	.3 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																				Α ,	λ Δ	A	Α	Α	Α	Α	Α	Α	4 А	Α	Α
Res	et Oxl	FFF004D		1	1	1 1	. 1	1	1	1	1	1 :	1 :	l 1	. 1	1	1	0	0	0 (0	0	0	0	0	1	0	0	1 1	0	1
Id	RW	Field	Value Id	Val	lue					1	Des	crip	tio	1																	
Α	R	В									3 (y	-int	erce	ept)																	

12.1.32 TEMP.B5

Address offset: 0x430

Y-intercept B5



12.1.33 TEMP.T0

Address offset: 0x434 Segment end T0

Bitı	numbe	er		31 30 2	9 2	8 27	7 26	25	24	23 2	22 2	1 20	19	18	17 1	6 1	5 14	13	12	11 10	9	8	7	6	5	4	3	2	1 0
Id																							Α	Α	Α	Α	Α	A	А А
Res	et 0xF	FFFFFE2		1 1 1	L 1	l 1	1	1	1	1	1 1	. 1	1	1	1 :	L 1	. 1	1	1	1 1	. 1	1	1	1	1	0	0	0	1 0
Id	RW	Field	Value Id	Value						Des	cript	tion																	
Α	R	Т								T (se	egm	ent	end	reg	iste														

12.1.34 TEMP.T1

Address offset: 0x438 Segment end T1

Bit r	numbe	er		31	30 2	9 2	28 27	7 26	5 25	24	23	22	21	20	19 1	8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id																										Α	Α	Α	A	Α Α	A	Α
Res	et OxF	FFFFF00		1	1 1	. 1	1 1	1	1	1	1	1	1	1	1	1 :	1 1	l 1	1	1	1	1	1	1	1	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Val	ue						De	scri	ptic	on																		
Α	R	Т									T (s	egi	mer	nt e	nd) i	regi	stei	-														

12.1.35 TEMP.T2

Address offset: 0x43C Segment end T2

Bit	numbe	er		31 3	30 2	9 28	27	26	25 2	24 2	23 2	22 2	1 2	0 19	9 18	17	16	15	14 1	3 1	2 11	10	9	8	7	6	5 4	4 3	2	1	0
Id																									Α	Α.	Α ,	4 A	Α	Α	Α
Res	et 0xF	FFFFF14		1	1 1	. 1	1	1	1	1	1	1 1	L 1	l 1	1	1	1	1	1	1 1	. 1	1	1	1	0	0	0 :	1 0	1	0	0
Id	RW	Field	Value Id	Valu	ue					ı	Des	crip	tior	1																	
Α	R	Т								1	Γ(se	egm	ent	enc	d) re	gist	er														_

12.1.36 TEMP.T3

Address offset: 0x440 Segment end T3

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16	6 15 14 13 12 11	1 10 9 8	7 6	5 4	3	2 1	O
Id						АА	A A	· Α .	А А	Α
Reset 0xFFI	FFF19	1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1	11111	1 1 1	0 0	0 1	. 1	0 0	1
Id RW I	ield Value Id	Value	Description							
A R			T (segment end) register							

12.1.37 TEMP.T4

Address offset: 0x444 Segment end T4



Bit number	31 30	29 28 27 26 25 2	4 23 22 21 20	0 19 18 17	16 15 14 1	3 12 11 10	9 8 7	6	5 4	3 2	1 0
Id							Д	Α.	А А	А А	АА
Reset 0xFFFFFF50	1 1	1 1 1 1 1 1	1111	111	1 1 1 1	1111	1 1 0	1	0 1	0 0	0 0
ld RW Field Val	lue Id Value		Description	ı							
ΔRT			T (segment	end) registe	or						

12.1.38 NFC.TAGHEADER0

Address offset: 0x450

Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bitı	numbe	er		31	. 30	29	28	3 27	7 26	25	24	23	22	21	20 :	19	18 1	7 1	.6 1	5 1	4 13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	C (C (C E	3 E	3 B	В	В	В	В	В	Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0xF	FFFFF5F		1	1	1	1	1	. 1	1	1	1	1	1	1	1	1 :	1	1 1	L 1	L 1	1	1	1	1	1	0	1	0	1	1	1	1	1
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	n																			
Α	R	MFGID										De	faul	t M	anu	ıfac	ture	r IC): N	ord	ic Se	mic	one	duct	tor	AS/	\ ha	s IC	M					
												0x5	5F																					
В	R	UD1										Un	ique	e id	enti	ifie	byt	e 1																
С	R	UD2										Un	ique	e id	enti	ifie	byt	e 2																
D	R	UD3										Un	ique	e id	enti	ifie	byt	e 3																

12.1.39 NFC.TAGHEADER1

Address offset: 0x454

Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 :	21	20	19 :	18	17 1	16 1	L5 1	4 13	12	11	10	9	8	7	6	5 -	4	3 2	1	0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	ВЕ	3 B	В	В	В	В	В.	Α	Α	A .	Α /	4 A	Α	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	l 1	1	1	1	1	1	1	1	1	1 :	l 1	1	1
Id	RW	Field	Value Id	Va	lue							De	scrip	otic	n																		
Α	R	UD4										Un	ique	e id	enti	fier	by	te 4	ļ														
В	R	UD5										Un	ique	e id	enti	fier	by	te 5	,														
С	R	UD6										Un	ique	ide	enti	fier	by	te 6	;														
D	R	UD7										Un	ique	ide	enti	fier	by	te 7	,														

12.1.40 NFC.TAGHEADER2

Address offset: 0x458

Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

A A A A
1 1 1 1

12.1.41 NFC.TAGHEADER3

Address offset: 0x45C

Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.



Bit r	numbe	er		31	1 30	29	28	27	26	25	24	23 :	22 2	1 20) 19	18	17	16	15	14 1	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id				D	D	D	D	D	D	D	D	С	c c	: c	. c	С	С	С	В	ВЕ	В	В	В	В	В	Α	Α	Α	Α	А А	A	А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1 1	. 1	. 1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1	1 1	. 1	. 1
Id	RW	Field	Value Id	Va	alue	:						Des	cript	tion	ı																	
Α	R	UD12										Uni	que	ider	ntifie	er b	yte	12														
В	R	UD13										Uni	que	ider	ntifie	er b	yte	13														
С	R	UD14										Uni	que	ider	ntifie	er b	yte	14														
D	R	UD15										Uni	que	ider	ntifie	er b	yte	15														



13 UICR — User information configuration registers

The user information configuration registers (UICRs) are non-volatile memory (NVM) registers for configuring user-specific settings.

For information on writing UICR registers, see the *NVMC* — *Non-volatile memory controller* on page 28 and *Memory* on page 20 chapters.

13.1 Registers

Table 12: Instances

Base address	Peripheral	Instance	Description	Configuration
0x10001000	UICR	UICR	User information configuration	

Table 13: Register Overview

Register	Offset	Description	
	0x000		Reserved
	0x004		Reserved
	0x008		Reserved
	0x010		Reserved
NRFFW[0]	0x014	Reserved for Nordic firmware design	
NRFFW[1]	0x018	Reserved for Nordic firmware design	
NRFFW[2]	0x01C	Reserved for Nordic firmware design	
NRFFW[3]	0x020	Reserved for Nordic firmware design	
NRFFW[4]	0x024	Reserved for Nordic firmware design	
NRFFW[5]	0x028	Reserved for Nordic firmware design	
NRFFW[6]	0x02C	Reserved for Nordic firmware design	
NRFFW[7]	0x030	Reserved for Nordic firmware design	
NRFFW[8]	0x034	Reserved for Nordic firmware design	
NRFFW[9]	0x038	Reserved for Nordic firmware design	
NRFFW[10]	0x03C	Reserved for Nordic firmware design	
NRFFW[11]	0x040	Reserved for Nordic firmware design	
NRFFW[12]	0x044	Reserved for Nordic firmware design	
NRFFW[13]	0x048	Reserved for Nordic firmware design	
NRFFW[14]	0x04C	Reserved for Nordic firmware design	
NRFHW[0]	0x050	Reserved for Nordic hardware design	
NRFHW[1]	0x054	Reserved for Nordic hardware design	
NRFHW[2]	0x058	Reserved for Nordic hardware design	
NRFHW[3]	0x05C	Reserved for Nordic hardware design	
NRFHW[4]	0x060	Reserved for Nordic hardware design	
NRFHW[5]	0x064	Reserved for Nordic hardware design	
NRFHW[6]	0x068	Reserved for Nordic hardware design	
NRFHW[7]	0x06C	Reserved for Nordic hardware design	
NRFHW[8]	0x070	Reserved for Nordic hardware design	
NRFHW[9]	0x074	Reserved for Nordic hardware design	
NRFHW[10]	0x078	Reserved for Nordic hardware design	
NRFHW[11]	0x07C	Reserved for Nordic hardware design	
CUSTOMER[0]	0x080	Reserved for customer	
CUSTOMER[1]	0x084	Reserved for customer	
CUSTOMER[2]	0x088	Reserved for customer	
CUSTOMER[3]	0x08C	Reserved for customer	
CUSTOMER[4]	0x090	Reserved for customer	
CUSTOMER[5]	0x094	Reserved for customer	
CUSTOMER[6]	0x098	Reserved for customer	



Register	Offset	Description
CUSTOMER[7]	0x09C	Reserved for customer
CUSTOMER[8]	0x0A0	Reserved for customer
CUSTOMER[9]	0x0A4	Reserved for customer
CUSTOMER[10]	0x0A8	Reserved for customer
CUSTOMER[11]	0x0AC	Reserved for customer
CUSTOMER[12]	0x0B0	Reserved for customer
CUSTOMER[13]	0x0B4	Reserved for customer
CUSTOMER[14]	0x0B8	Reserved for customer
CUSTOMER[15]	0x0BC	Reserved for customer
CUSTOMER[16]	0x0C0	Reserved for customer
CUSTOMER[17]	0x0C4	Reserved for customer
CUSTOMER[18]	0x0C8	Reserved for customer
CUSTOMER[19]	0x0CC	Reserved for customer
CUSTOMER[20]	0x0D0	Reserved for customer
CUSTOMER[21]	0x0D4	Reserved for customer
CUSTOMER[22]	0x0D8	Reserved for customer
CUSTOMER[23]	0x0DC	Reserved for customer
CUSTOMER[24]	0x0E0	Reserved for customer
CUSTOMER[25]	0x0E4	Reserved for customer
CUSTOMER[26]	0x0E8	Reserved for customer
CUSTOMER[27]	0x0EC	Reserved for customer
CUSTOMER[28]	0x0F0	Reserved for customer
CUSTOMER[29]	0x0F4	Reserved for customer
CUSTOMER[30]	0x0F8	Reserved for customer
CUSTOMER[31]	0x0FC	Reserved for customer
PSELRESET[0]	0x200	Mapping of the nRESET function
PSELRESET[1]	0x204	Mapping of the nRESET function
APPROTECT	0x208	Access port protection
NFCPINS	0x20C	Setting of pins dedicated to NFC functionality: NFC antenna or GPIO
DEBUGCTRL	0x210	Processor debug control
EXTSUPPLY	0x300	Enable external circuitry to be supplied from VDD pin. Applicable in high voltage mode only.
REGOUT0	0x304	GPIO reference voltage / external output supply voltage in high voltage mode

13.1.1 NRFFW[0]

Address offset: 0x014

Reserved for Nordic firmware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Id		A A A A A A A A A A A A A A A A A A A	A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1
Id RW Field	Value Id	Value Description	
A RW NRFFW		Reserved for Nordic firmware design	

13.1.2 NRFFW[1]

Address offset: 0x018

Reserved for Nordic firmware design

Bit n	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17 1	16	15 1	14 :	13 :	12 :	11 :	10	9	8	7	6	5	4	3 2	1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А	. Α	A A
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	. 1
Id	RW	Field	Value Id	Va	lue							De	cri	ptic	n																			
Α	RW	NRFFW										Res	erv	ed '	for	Nor	dic	firr	nw	are	des	sign	ı											

13.1.3 NRFFW[2]

Address offset: 0x01C



Reserved for Nordic firmware design

Bit	numb	er		31	30	29	28	27 :	26	25 2	24 2	23 2	22 2	1 20	19	18	17	16	15 1	l4 1	3 12	2 11	. 10	9	8	7	6	5 4	4 3	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α.	Α	Α.	ДД	. A	A	Α	Α	Α	Α.	A A	A A	Α	Α	Α	Α	Α	Α	A	Δ /	A A	Α	Α
Re	set 0xl	FFFFFFF		1	1	1	1	1	1	1	1	1	1 1	. 1	. 1	1	1	1	1	1 :	l 1	1	1	1	1	1	1	1	1 1	1 1	1	1
Id	RW	Field	Value Id	Va	lue							Des	cript	ion																		
Α	RW	NRFFW									F	Rese	erve	d fo	r No	ordio	c fir	mw	are	des	ign											

13.1.4 NRFFW[3]

Address offset: 0x020

Reserved for Nordic firmware design

Bit r	iumbe	er		31	1 30	29	9 28	8 2	7 2	6 2	25 2	24 :	23 2	22 :	21 :	20	19 1	18 :	17 1	16 :	15 1	14	13 1	12 1	1 1) 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	. 4	۱ ۸	Δ 4	4 /	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α .	A A	A	Α	Α	Α	Α	Α	Α	Α.	А А
Rese	et OxF	FFFFFF		1	1	1	. 1	L 1	L 1	1 :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	alue	9						ı	Des	crip	otio	n																		
Α	RW	NRFFW											Res	erv	ed 1	for	Nor	dic	firn	nw	are	de	sign											

13.1.5 NRFFW[4]

Address offset: 0x024

Reserved for Nordic firmware design

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19	18 1	7 1	5 15	14	13	12	11 1	.0 9	9 8	3 7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	Α	Α	Α	Α	A	4 4	4 4	A	. A	Α	Α	Α .	Α.	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	1	1	1	1	1	1 :	1 1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																	
Α	RW	NRFFW										Res	erv	ed	for	Nor	dic	firm	war	e de	esigi	n										

13.1.6 NRFFW[5]

Address offset: 0x028

Reserved for Nordic firmware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFFW		Reserved for Nordic firmware design

13.1.7 NRFFW[6]

Address offset: 0x02C

Reserved for Nordic firmware design

Bit	nui	mbe	r		31	. 3	0 2	9 2	28 :	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1)
Id					Α	A	۱,	Д	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A .	A
Re	set	0xF	FFFFFF		1	1	L	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	L
Id	F	RW	Field	Value Id	Va	alu	e							De	scr	ipti	on																				
Δ	F	R/V/	NRFFW											Re	ser	ved	foi	· No	rdi	r fir	mu	are	de	ciøi	n												7

13.1.8 NRFFW[7]

Address offset: 0x030

Reserved for Nordic firmware design



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFFW		Reserved for Nordic firmware design

13.1.9 NRFFW[8]

Address offset: 0x034

Reserved for Nordic firmware design

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13	12	11 :	LO	9	8	7	6	5	4	3 2	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	A A	Δ Δ	A A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	l 1	1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	NRFFW										Re	serv	ved	for	No	rdic	fir	nw	are	de	sigr												

13.1.10 NRFFW[9]

Address offset: 0x038

Reserved for Nordic firmware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field Value Id	Value Description
A RW NRFFW	Reserved for Nordic firmware design

13.1.11 NRFFW[10]

Address offset: 0x03C

Reserved for Nordic firmware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value Description
A RW NRFFW		Reserved for Nordic firmware design

13.1.12 NRFFW[11]

Address offset: 0x040

Reserved for Nordic firmware design

Bit r	numbe	er		31	30 :	29 :	28 :	27 :	26	25 :	24	23 :	22 2	21 2	20 1	9 1	8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id			,	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 4	A /	Α Δ	A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Α	Α
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	L 1	L 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Val	lue							Des	crip	otio	n																		
Α	RW	NRFFW										Res	erv	ed f	or N	lor	dic f	irm	wai	re d	esig	n											

13.1.13 NRFFW[12]

Address offset: 0x044

Reserved for Nordic firmware design

Bit number	31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A	
Reset 0xFFFFFFF	1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description

A RW NRFFW Reserved for Nordic firmware design



13.1.14 NRFFW[13]

Address offset: 0x048

Reserved for Nordic firmware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFFW		Reserved for Nordic firmware design

13.1.15 NRFFW[14]

Address offset: 0x04C

Reserved for Nordic firmware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFFW		Reserved for Nordic firmware design

13.1.16 NRFHW[0]

Address offset: 0x050

Reserved for Nordic hardware design

Bit n	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17 1	16	15	14	13	12 :	11 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	. Δ	Α	Α	Α	Α	Α	Α	Α.	А А
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	NRFHW										Res	erv	ed	for	Noi	dic	har	rdw	vare	de	sig	า										

13.1.17 NRFHW[1]

Address offset: 0x054

Reserved for Nordic hardware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value Description
A RW NRFHW		Reserved for Nordic hardware design

13.1.18 NRFHW[2]

Address offset: 0x058

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15	5 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id	A A A A A A A	A A A A A A A A		A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1111111	1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description		

A RW NRFHW Reserved for Nordic hardware design

13.1.19 NRFHW[3]

Address offset: 0x05C

Reserved for Nordic hardware design



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFHW		Reserved for Nordic hardware design

13.1.20 NRFHW[4]

Address offset: 0x060

Reserved for Nordic hardware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFHW		Reserved for Nordic hardware design

13.1.21 NRFHW[5]

Address offset: 0x064

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFHW	Reserved for Nordic hardware design

13.1.22 NRFHW[6]

Address offset: 0x068

Reserved for Nordic hardware design

Bit n	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 1	6 1	15 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ,	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А	. A	Α
Rese	t 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	. 1	1	1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	lue							De	cri	ptic	n																		
Α	RW	NRFHW										Res	erv	ed '	for	Nor	dic	har	dw	are	desi	gn											

13.1.23 NRFHW[7]

Address offset: 0x06C

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	_ A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFHW	Reserved for Nordic hardware design

13.1.24 NRFHW[8]

Address offset: 0x070

Reserved for Nordic hardware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description

A RW NRFHW Reserved for Nordic hardware design



13.1.25 NRFHW[9]

Address offset: 0x074

Reserved for Nordic hardware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value Description
A RW NRFHW		Reserved for Nordic hardware design

Reserved for Nordic hardware design

13.1.26 NRFHW[10]

Address offset: 0x078

Reserved for Nordic hardware design

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	NRFHW										Res	serv	/ed	for	Noi	rdic	ha	rdw	vare	e de	esig	n											

13.1.27 NRFHW[11]

Address offset: 0x07C

Reserved for Nordic hardware design

Bit r	iumbe	er		31	. 30	29	28	27	7 26	25	24	23	22	21	20 1	19	18 :	17 1	16 1	L5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	Δ,	Α Α	A 4	A	Α	Α	Α	Α	Α	Α	Α ,	Δ.	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1	1 :	L 1	. 1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	cri	otic	n																		
Α	RW	NRFHW										Res	erv	ed ·	for I	Nor	dic	har	dw	are	de	ign											

13.1.28 CUSTOMER[0]

Address offset: 0x080 Reserved for customer

Bit nu	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	A .	Α	A A	. A	A A
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	l 1
ld	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Δ	RW/	CUSTOMER										Res	erv	ed	for	CIIS	ton	ner																

13.1.29 CUSTOMER[1]

Address offset: 0x084 Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 1	18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description	

A RW CUSTOMER Reserved for customer

13.1.30 CUSTOMER[2]

Address offset: 0x088 Reserved for customer



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

13.1.31 CUSTOMER[3]

Address offset: 0x08C Reserved for customer

Bit	numb	er		31 3	30 2	9 2	8 2	7 26	25	24	23	22 2	21 2	0 19	9 18	3 17	16	15	14	13	L2 1	11 1	0 9	8	7	6	5	4	3 2	2 1	1 0
Id				А	A A	A /	Α Α	A	Α	Α	Α	Α	Α.	А А	A	Α.	Α	Α	Α	Α	Α.	A A	A	Α	Α	Α	Α	Α	A A	A A	A A
Res	et 0x	FFFFFF		1	1 1	L 1	L 1	. 1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1 :	. 1	1	1	1	1	1	1 :	L 1	l 1
Id	RW	Field	Value Id	Valu	ıe						Des	crip	tio	n																	
Α	RW	CUSTOMER									Res	erv	ed f	or cu	usto	me	r														

13.1.32 CUSTOMER[4]

Address offset: 0x090 Reserved for customer

Bit num	ber		31	30	29	28	27	26	25	24	23	22	21	20	19 1	18 1	17 1	16 1	L5 1	4 13	3 12	11	10	9	8	7	6	5 .	4 3	2	1	0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A	Α	Α	Α	Α	Α	Α	Α	A .	A A	A	Α	Α
Reset 0	xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1	1 1	. 1	1	1
Id RV	V Field	Value Id	Va	lue							De	scri	ptic	n																		
A RV	V CUSTOMER										Res	serv	ed	for	cus	tom	ner															

13.1.33 CUSTOMER[5]

Address offset: 0x094 Reserved for customer

Bitı	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

13.1.34 CUSTOMER[6]

Address offset: 0x098 Reserved for customer

Bit r	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α.	ΑА	
Res	et 0x	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																				ı
Α	RW	CUSTOMER										Re	serv	/ed	for	cus	ton	ner																	1

13.1.35 CUSTOMER[7]

Address offset: 0x09C Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 1	18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description	

A RW CUSTOMER Reserved for customer



13.1.36 CUSTOMER[8]

Address offset: 0x0A0 Reserved for customer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

13.1.37 CUSTOMER[9]

Address offset: 0x0A4
Reserved for customer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

13.1.38 CUSTOMER[10]

Address offset: 0x0A8
Reserved for customer

Bit	numbe	er		31	L 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 A
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1 1
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																			
Α	RW	CUSTOMER										Res	serv	ed	for	cus	ton	ner																

13.1.39 CUSTOMER[11]

Address offset: 0x0AC Reserved for customer

Bit r	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 1	.7 1	6 1	5 14	13	12	11 1	10 9	9 8	3 7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Α Α	4 <i>A</i>	A A	Α	Α	Α.	A A	A A	A A	Α	Α	Α	Α ,	۱ ۸	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	۱ 1	1	1	1	1 :	1 1	1	1	1	1	1 :	ι :	1 1
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	n																	
Α	RW	CUSTOMER		Reserved for customer																												

13.1.40 CUSTOMER[12]

Address offset: 0x0B0 Reserved for customer

Bit number		31	30	29 :	28 2	27 2	26 2	5 2	4 23	3 22	21	20	19 :	18 1	.7 1	6 1	5 14	13	12	11 :	10 9	9 8	7	6	5	4	3	2 :	1 0
Id		А	Α	Α	Α.	Α ,	A A	Δ Α	Α Α	Α	Α	Α	Α	Α /	Δ /	A A	A A	Α	Α	Α	A A	λ /	A	Α	Α	Α	A	Δ ,	А А
Reset 0xFFFFFFF		1	1	1	1	1	1 1	1 1	1 1	1	1	1	1	1 :	1 1	L 1	. 1	1	1	1	1 :	L 1	. 1	1	1	1	1	1 1	1 1
Id RW Field	Value Id	Val	ue						D	escr	iptio	on																	
A RW CUSTO	MER	Reserved for customer																											

13.1.41 CUSTOMER[13]

Address offset: 0x0B4 Reserved for customer



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0											
Id		A A A A A A A A A A A A A A A A A A A											
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1											
Id RW Field	Value Id	Value Description											
A RW CUSTOMER		Reserved for customer											

13.1.42 CUSTOMER[14]

Address offset: 0x0B8 Reserved for customer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0											
Id		A A A A A A A A A A A A A A A A A A A											
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1											
Id RW Field	Value Id	Value Description											
A RW CUSTOMER		Reserved for customer											

13.1.43 CUSTOMER[15]

Address offset: 0x0BC Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0										
Id	A A A A A A A A A A A A A A A A A A A										
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1										
Id RW Field Value Id	Value Description										
A RW CUSTOMER	Reserved for customer										

13.1.44 CUSTOMER[16]

Address offset: 0x0C0 Reserved for customer

Bitı	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

13.1.45 CUSTOMER[17]

Address offset: 0x0C4 Reserved for customer

Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 .	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Α.	А А
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1	1 1
Id	RW	Field	Value Id	1 1 1 1 1 1 1 1 Value									scr	ipti	on																			
Α	RW	CUSTOMER		Reserved for customer																														

13.1.46 CUSTOMER[18]

Address offset: 0x0C8
Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18	8 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description	

A RW CUSTOMER Reserved for customer



13.1.47 CUSTOMER[19]

Address offset: 0x0CC Reserved for customer

Bit number			33	L 30	29	28	27	26	25	24	23	22 :	21	20 :	19 1	18 1	17 :	16 1	15 :	14 1	L3 1	12 1	1 1	9	8	7	6	5	4	3	2 :	1 0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α	Α	Α	Α	Α	Α ,	Δ <i>A</i>	A	Α	Α	Α	Α	Α	A	Δ ,	4 А
Reset 0xFFI	FFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	1	1	1	1	1	1	1 1	1 1
Id RW I	Field	Value Id	V	alue							De	scrip	otic	n																		
A RW	CUSTOMER		Value Description Reserved for customer																													

13.1.48 CUSTOMER[20]

Address offset: 0x0D0 Reserved for customer

Bi	t nu	ımb	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 А
Re	set	t Oxl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1
Id		RW	Field	Value Id	Va	lue							Des	cri	ptic	n																			
Α		RW	CUSTOMER		Reserved for customer																														

13.1.49 CUSTOMER[21]

Address offset: 0x0D4 Reserved for customer

Bitı	numbe	r		31	1 30	29	9 28	3 2	7 26	5 25	24	23	22	21	20	19	18 :	17 :	16 1	15 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	A	. 4	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	Δ Α	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	А
Res	et 0xF	FFFFFF		1	1	1	. 1	1	. 1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	1	1	1	1	1	1	1	1	1	1 1	l 1	. 1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	on																		
Α	RW	CUSTOMER		Reserved for customer																													

13.1.50 CUSTOMER[22]

Address offset: 0x0D8
Reserved for customer

Bit nu	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	A .	Α	A A	. A	A A
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	l 1
ld	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Δ	RW/	CUSTOMER										Res	erv	ed	for	CIIS	ton	ner																

13.1.51 CUSTOMER[23]

Address offset: 0x0DC Reserved for customer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

13.1.52 CUSTOMER[24]

Address offset: 0x0E0
Reserved for customer



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

13.1.53 CUSTOMER[25]

Address offset: 0x0E4
Reserved for customer

Bit	numbe	er		31	1 30	29	28	3 27	7 26	25	24	23	22	21	20	19	18 1	17 :	16 1	15 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A	Α,	Δ Α	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	1	1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	on																		
Α	RW	CUSTOMER										Res	erv	ed	for	cus	tom	ner															

13.1.54 CUSTOMER[26]

Address offset: 0x0E8
Reserved for customer

Bit nu	umber		31 30 29 28 27	['] 26 25 24 23 22 21 20 19 18 17 16	6 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			AAAAA	A A A A A A A A A A	
Reset	t OxFFFFFFFF		1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW Field	Value Id	Value	Description	
Α	RW CUSTOMER			Reserved for customer	

13.1.55 CUSTOMER[27]

Address offset: 0x0EC Reserved for customer

Bitı	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

13.1.56 CUSTOMER[28]

Address offset: 0x0F0 Reserved for customer

Е	Bit nu	mbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 1	16 1	L5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 /	C
10	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	Δ ,	Α ,	A A	A	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Δ
F	leset	0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 :	1 1	1	1	1	1	1	1	1	1	1	1	1
1	d I	RW	Field	Value Id	Va	alue							De	scri	ptic	n																			
A	Α Ι	RW	CUSTOMER										Res	erv	ed	for	cus	tom	ner																

13.1.57 CUSTOMER[29]

Address offset: 0x0F4
Reserved for customer

Bit number	31 30 29 28 2	27 26 25 24 23 22 21 20 19 18	8 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A .	A A A A A A A A A	
Reset 0xFFFFFFF	1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description	

A RW CUSTOMER Reserved for customer



13.1.58 CUSTOMER[30]

Address offset: 0x0F8
Reserved for customer

Bit r	numbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16 1	l5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ ,	Δ Α	. Δ	A	Α	Α	Α	Α	Α	Α	Α ,	Δ ,	4 А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	L 1	1	. 1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	otic	on																		
Α	RW	CUSTOMER										Res	erv	ed	for	cus	ton	ner															

13.1.59 CUSTOMER[31]

Address offset: 0x0FC Reserved for customer

Bit n	umbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16	15 1	.4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α ,	Δ Α	Δ Δ	A	Α	Α	Α	Α	Α	Α	A	A A	A A
Rese	t OxFI	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	1	. 1	1	1	1	1	1	1	1 :	1 1	1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	CUSTOMER										Res	serv	ed	for	cus	ton	ner															

13.1.60 PSELRESET[0]

Address offset: 0x200

Mapping of the nRESET function

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If they do not, there will be no nRESET function exposed on a GPIO, and the device will always start independently of the levels present on any of the GPIOs.

Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	B A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		18	Pin number of PORT onto which nRESET is exposed
В	RW	PORT		0	Port number onto which nRESET is exposed
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

13.1.61 PSELRESET[1]

Address offset: 0x204

Mapping of the nRESET function

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If they do not, there will be no nRESET function exposed on a GPIO, and the device will always start independently of the levels present on any of the GPIOs.

Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ваааа
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		18	Pin number of PORT onto which nRESET is exposed
В	RW	PORT		0	Port number onto which nRESET is exposed
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect



13.1.62 APPROTECT

Address offset: 0x208 Access port protection

Bitı	numbe	er		31 30	29	28 2	7 26	25	24 2	23 2	2 21	L 20	19	18	17 1	16 1	.5 14	13	12 3	11 10	9	8	7	6	5 4	4 3	2	1	0
Id																							Α	Α	A	Δ Δ	A	Α	Α
Res	et 0xF	FFFFFF		1 1	1	1	1 1	1	1	1 1	1 1	1	1	1	1	1 :	1 1	1	1	1 1	1	1	1	1	1	1 1	1	1	1
Id	RW	Field	Value Id	Value					1	Desc	cript	ion																	
Α	RW	PALL							ı	nat	ole o	r di	sabl	e ac	cess	ро	rt pı	ote	ction										
									9	See I	Debi	ug d	and t	trac	e on	pa	ge 6	2 for	mo	re inf	orm	atio	n.						
			Disabled	0xFF					1	Disa	ble																		
			Enabled	0x00					1	nat	ole																		

13.1.63 NFCPINS

Address offset: 0x20C

Setting of pins dedicated to NFC functionality: NFC antenna or GPIO

Bit	numbe	er		33	1 30	29	28	8 27	7 26	6 25	5 24	4 2	3 2	2 2	1 2	0 1	L9 1	18 :	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																				Α
Res	et 0xF	FFFFFF		1	1	. 1	1	. 1	1	1	. 1	L 1	L 1	1 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	V	alu	е						D	esc	crip	tio	n																				
Α	RW	PROTECT										S	etti	ing	of p	oins	s de	dic	ate	d t	o N	IFC	fun	ctio	ona	lity										
			Disabled	0								С	pe	rati	on	as (GPI	O p	ins	. Sa	me	e pr	ote	ctio	on a	s no	orm	al (GPI) pi	ns					
			NFC	1								С	pe	rati	on	as I	NFC	ar	nter	nna	pir	ns.	Con	fig	ıres	the	e pr	ote	ctio	n f	or					
												Ν	IFC	оре	erat	tior	า																			

13.1.64 DEBUGCTRL

Address offset: 0x210
Processor debug control

Bit r	iumbe	er		31 30 2	29 28	27 2	26 25	5 24	23	22 2	21 2	0 19	18	17	16 1	15 1	4 13	12	11 1	0 9	8	7	6	5	4	3 2	1	0
Id																ВЕ	В	В	В	3 B	В	Α	Α	Α	Α /	4 A	Α	Α
Res	et OxF	FFFFFF		1 1	1 1	1	1 1	1	1	1	1 1	1	1	1	1	1 1	. 1	1	1 :	l 1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Value					Des	crip	tior	١																
Α	RW	CPUNIDEN							Cor	nfigu	ıre C	: US	non	-intr	usiv	e de	bug	feat	ures	;								Τ
			Enabled	0xFF					Ena	ble	CPU	ITM	1 an	d ET	M f	unct	iona	lity (defa	ult	beh	avic	or)					
			Disabled	0x00					Disa	able	CPL	J ITN	∕l ar	nd E1	M 1	func	tiona	ality										
В	RW	CPUFPBEN							Cor	nfigu	ıre C	CPU f	flasł	n pat	ch a	and	brea	kpoi	nt (I	PB)	uni	t be	hav	ior				
			Enabled	0xFF					Ena	ble	CPU	FPB	un	it (d	efau	ılt b	ehav	ior)										
			Disabled	0x00					Disa	able	CPL	J FPE	B un	nit. V	Vrite	es in	to th	ne FF	B re	gist	ers v	will	be					
									igno	ored	ı.																	

13.1.65 EXTSUPPLY

Address offset: 0x300

Enable external circuitry to be supplied from VDD pin. Applicable in high voltage mode only.

Bit r	numbe	r		31 3	29	28	3 27	26	25	24	23	22 :	21 2	20 1	9 1	8 1	7 16	5 15	5 14	1 13	12	11	10	9	8 7	7 6	5	4	3	2	1 ()
Id																															A	
Res	et OxF	FFFFFF		1 1	1	1	1	1	1	1	1	1	1	1 :	1 1	L 1	. 1	. 1	. 1	1	1	1	1	1	1 :	l 1	. 1	1	1	1	1 1	
Id	RW	Field	Value Id	Valu	9						Des	scrip	otio	n																		
Α	RW	EXTSUPPLY									Ena	able	ext	ern	al ci	rcu	itry	to l	be s	upp	lied	fro	m V	DD	pin	(ou	tpu	t of				
											REC	30 s	tage	e)																		
			Disabled	0							No	cur	rent	caı	n be	dra	awn	fro	m t	the	VDD	pin	1									
			Enabled	1							It is	allo	owe	d to	su	pply	ex /	teri	nal	circ	uitry	fro	m tl	he ۱	/DD	pin						



13.1.66 REGOUT0

Address offset: 0x304

GPIO reference voltage / external output supply voltage in high voltage mode

Bit number	31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		ААА
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description
A RW VOUT		Output voltage from of REGO regulator stage. The maximum
		output voltage from this stage is given as VDDH - VEXDIF.
1V8	0	1.8 V
2V1	1	2.1 V
2V4	2	2.4 V
2V7	3	2.7 V
3V0	4	3.0 V
3V3	5	3.3 V
DEFAULT	7	Default voltage: 1.8 V



14 Peripheral interface

Peripherals are controlled by the CPU by writing to configuration registers and task registers. Peripheral events are indicated to the CPU by event registers and interrupts if they are configured for a given event.

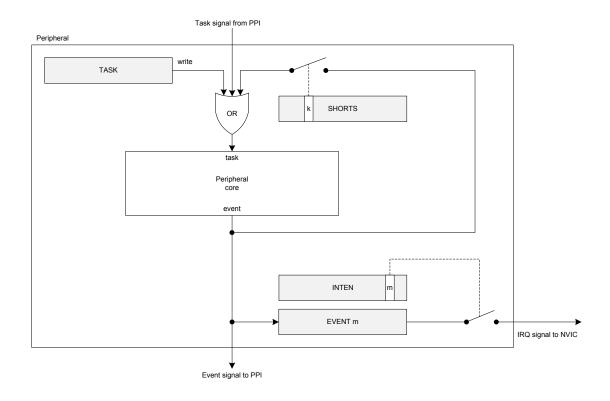


Figure 8: Tasks, events, shortcuts, and interrupts

14.1 Peripheral ID

Every peripheral is assigned a fixed block of 0x1000 bytes of address space, which is equal to 1024 x 32 bit registers.

See *Instantiation* on page 23 for more information about which peripherals are available and where they are located in the address map.

There is a direct relationship between the peripheral ID and base address. For example, a peripheral with base address 0x40000000 is assigned ID=0, a peripheral with base address 0x40001000 is assigned ID=1, and a peripheral with base address 0x4001F000 is assigned ID=31.

Peripherals may share the same ID, which may impose one or more of the following limitations:

- · Some peripherals share some registers or other common resources.
- Operation is mutually exclusive. Only one of the peripherals can be used at a time.
- Switching from one peripheral to another must follow a specific pattern (disable the first, then enable the second peripheral).

14.2 Peripherals with shared ID

In general (with the exception of ID 0), peripherals sharing an ID and base address may not be used simultaneously. The user can only enable one peripheral at the time on this specific ID.



When switching between two peripherals that share an ID, the user should do the following to prevent unwanted behavior:

- Disable the previously used peripheral.
- Remove any programmable peripheral interconnect (PPI) connections set up for the peripheral that is being disabled.
- Clear all bits in the INTEN register, i.e. INTENCLR = 0xFFFFFFF.
- Explicitly configure the peripheral that you enable and do not rely on configuration values that may be inherited from the peripheral that was disabled.
- Enable the now configured peripheral.

See *Instantiation* on page 23 to see which peripherals are sharing ID.

14.3 Peripheral registers

Most peripherals feature an ENABLE register. Unless otherwise specified in the relevant chapter, the peripheral registers (in particular the PSEL registers) must be configured before enabling the peripheral.

Note that the peripheral must be enabled before tasks and events can be used.

14.4 Bit set and clear

Registers with multiple single-bit bit fields may implement the set-and-clear pattern. This pattern enables firmware to set and clear individual bits in a register without having to perform a read-modify-write operation on the main register.

This pattern is implemented using three consecutive addresses in the register map, where the main register is followed by dedicated SET and CLR registers (in that exact order).

The SET register is used to set individual bits in the main register while the CLR register is used to clear individual bits in the main register. Writing 1 to a bit in the SET or CLR register will set or clear the same bit in the main register respectively. Writing 0 to a bit in the SET or CLR register has no effect. Reading the SET or CLR registers returns the value of the main register.

Restriction: The main register may not be visible and hence not directly accessible in all cases.

14.5 Tasks

Tasks are used to trigger actions in a peripheral, for example to start a particular behavior. A peripheral can implement multiple tasks with each task having a separate register in that peripheral's task register group.

A task is triggered when firmware writes 1 to the task register or when the peripheral itself or another peripheral toggles the corresponding task signal. See *Figure 8: Tasks, events, shortcuts, and interrupts* on page 59.

14.6 Events

Events are used to notify peripherals and the CPU about events that have happened, for example a state change in a peripheral. A peripheral may generate multiple events with each event having a separate register in that peripheral's event register group.

An event is generated when the peripheral itself toggles the corresponding event signal, and the event register is updated to reflect that the event has been generated. See *Figure 8: Tasks, events, shortcuts, and interrupts* on page 59. An event register is only cleared when firmware writes 0 to it.

Events can be generated by the peripheral even when the event register is set to 1.



14.7 Shortcuts

A shortcut is a direct connection between an event and a task within the same peripheral. If a shortcut is enabled, its associated task is automatically triggered when its associated event is generated.

Using a shortcut is the equivalent to making the same connection outside the peripheral and through the PPI. However, the propagation delay through the shortcut is usually shorter than the propagation delay through the PPI.

Shortcuts are predefined, which means their connections cannot be configured by firmware. Each shortcut can be individually enabled or disabled through the shortcut register, one bit per shortcut, giving a maximum of 32 shortcuts for each peripheral.

14.8 Interrupts

All peripherals support interrupts. Interrupts are generated by events.

A peripheral only occupies one interrupt, and the interrupt number follows the peripheral ID. For example, the peripheral with ID=4 is connected to interrupt number 4 in the nested vectored interrupt controller (NVIC).

Using the INTEN, INTENSET and INTENCLR registers, every event generated by a peripheral can be configured to generate that peripheral's interrupt. Multiple events can be enabled to generate interrupts simultaneously. To resolve the correct interrupt source, the event registers in the event group of peripheral registers will indicate the source.

Some peripherals implement only INTENSET and INTENCLR, and the INTEN register is not available on those peripherals. Refer to the individual chapters for details. In all cases, however, reading back the INTENSET or INTENCLR register returns the same information as in INTEN.

Each event implemented in the peripheral is associated with a specific bit position in the INTEN, INTENSET and INTENCLR registers.

The relationship between tasks, events, shortcuts, and interrupts is shown in *Figure 8: Tasks, events, shortcuts, and interrupts* on page 59.

14.8.1 Interrupt clearing

When clearing an interrupt by writing 0 to an event register, or disabling an interrupt using the INTENCLR register, it can take up to four CPU clock cycles to take effect. This means that an interrupt may reoccur immediatelly even if a new event has not come, if the program exits an interrupt handler after the interrupt is cleared or disabled, but before four clock cycles have passed.

Important: To avoid an interrupt reoccurring before a new event has come, the program should perform a read from one of the peripheral registers, for example, the event register that has been cleared, or the INTENCLR register that has been used to disable the interrupt.

This will cause a one to three-cycle delay and ensure the interrupt is cleared before exiting the interrupt handler. Care should be taken to ensure the compiler does not remove the read operation as an optimization. If the program can guarantee a four-cycle delay after event clear or interrupt disable another way, then a read of a register is not required.



15 Debug and trace

The debug and trace system offers a flexible and powerful mechanism for non-intrusive debugging.

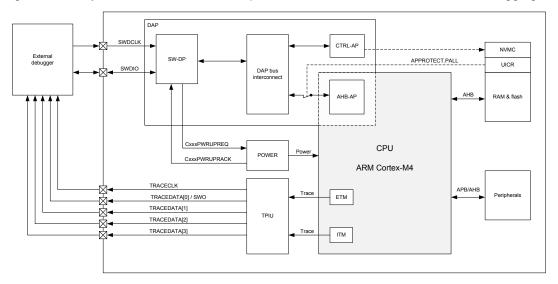


Figure 9: Overview

The main features of the debug and trace system are:

- Two-pin serial wire debug (SWD) interface
- Flash patch and breakpoint unit (FPB) supports:
 - Two literal comparators
 - · Six instruction comparators
- · Data watchpoint and trace unit (DWT)
 - Four comparators
- Instrumentation trace macrocell (ITM)
- Embedded trace macrocell (ETM)
- Trace port interface unit (TPIU)
 - 4-bit parallel trace of ITM and ETM trace data
 - Serial wire output (SWO) trace of ITM data

15.1 DAP - Debug access port

An external debugger can access the device via the DAP.

The DAP implements a standard ARM® CoreSight™ SW-DP (serial wire debug port).

The SW-DP implements the SWD (serial wire debug) protocol that is a two-pin serial interface, see SWDCLK and SWDIO in *Debug and trace* on page 62.

In addition to the default access port in the CPU (AHB-AP), the DAP includes a custom control access port (CTRL-AP). The CTRL-AP is described in more detail in *CTRL-AP - Control access port* on page 63.

Important:

- The SWDIO line has an internal pull-up resistor.
- The SWDCLK line has an internal pull-down resistor.



15.2 CTRL-AP - Control access port

The control access port (CTRL-AP) is a custom access port that enables control of the device even if the other access ports in the DAP are being disabled by the access port protection.

Access port protection blocks the debugger from read and write access to all CPU registers and memory-mapped addresses. See the UICR register *APPROTECT* on page 57 for more information about enabling access port protection.

This access port enables the following features:

- Soft reset, see Reset on page 73 for more information
- Disable access port protection

Access port protection can only be disabled by issuing an ERASEALL command via CTRL-AP. This command will erase flash, UICR, and RAM.

15.2.1 Registers

Table 14: Register Overview

Register	Offset	Description
RESET	0x000	Soft reset triggered through CTRL-AP
ERASEALL	0x004	Erase all
ERASEALLSTATUS	0x008	Status register for the ERASEALL operation
APPROTECTSTATUS	0x00C	Status register for access port protection
IDR	0x0FC	CTRL-AP identification register, IDR

RESET

Address offset: 0x000

Soft reset triggered through CTRL-AP

Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW RESET			Soft reset triggered through CTRL-AP. See Reset behaviour in
			POWER chapter for more details.
	NoReset	0	Reset is not active
	Reset	1	Reset is active. Device is held in reset.

ERASEALL

Address offset: 0x004

Erase all

Bitı	numbe	er		31 30	29	28	27	26	25 2	24 2	23 2	22 2	1 2) 19	18	17	16	15 1	4 1	3 12	11	10	9	3 7	7 6	5	4	3	2	1 0
Id																														Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0	0 () (0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value	•						Des	crip	tion																	
Α	W	ERASEALL								E	Eras	e al	l fla	sh a	nd F	RAN	ı													
			NoOperation	0						1	No d	oper	ratio	n																
			Erase	1						E	Eras	e al	l fla	sh a	nd F	RAN	ı													

ERASEALLSTATUS

Address offset: 0x008

Status register for the ERASEALL operation



Bitı	numbe	er		31 30	29	28	3 27	26	25	24	23	22	21	20	19	18 1	.7 1	.6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4 3	2	1	0
Id																																Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Valu	е						Des	scri	ptic	on																		
Α	R	ERASEALLSTATUS									Sta	tus	reg	iste	r fo	r th	e E	RAS	EAL	L op	era	tior	1									
			Ready	0							ER/	ASE	ALL	is r	ead	У																
			Busy	1							ER/	ASE	ALL	is b	usy	(or	n-gc	ing)													

APPROTECTSTATUS

Address offset: 0x00C

Status register for access port protection

Bit	num	nbei	r		31 3	30 2	9 2	8 2	7 2	6 2	5 24	4 2	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id																																		Α
Res	et 0)x00	000000		0	0 () (0 () (0 0	0	(0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0
Id	R۱	W	Field	Value Id	Valu	ıe						D	escr	ript	ion																			
Α	R		APPROTECTSTATUS									S	tatu	s re	gist	er f	or a	cce	ss p	ort	t pr	ote	ctic	n										
				Enabled	0							Α	cces	ss p	ort	pro	ect	ion	ena	able	ed													
				Disabled	1							Α	cces	ss p	ort	pro	ect	ion	not	t en	abl	ed												

IDR

Address offset: 0x0FC

CTRL-AP identification register, IDR

Bit	numbe	er		31	. 30	29	28	27	26 2	25 2	4 2	3 22	21	20	19	18	17	16	15	14	13	12	11 :	.0 9	9 8	3 7	ϵ	5	4	3	2	1	0
Id				Ε	Ε	Ε	Ε	D	D	D [0 0	. C	С	С	С	С	С	В	В	В	В					А	. 4	A	. A	. Α	Α	Α	Α
Res	et 0x0	2880000		0	0	0	0	0	0	1 (0 1	. 0	0	0	1	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																			
Α	R	APID									Α	P ide	enti	fica	tior	ı																	
В	R	CLASS									Α	cces	s pc	ort (AP)	cla	SS																
			NotDefined	0x	0						N	o de	fine	ed c	lass	;																	
			MEMAP	0x	8						N	lem	ory	acc	ess	noq	t																
С	R	JEP106ID									JE	DEC	JEF	100	5 id	ent	ity	coc	e														
D	R	JEP106CONT									JE	DEC	JEF	2106	5 cc	nti	nua	itio	n co	ode													
Е	R	REVISION									R	evisi	on																				

15.2.2 Electrical specification

Control access port

Symbol	Description	Min.	Тур.	Max.	Units
R _{pull}	Internal SWDIO and SWDCLK pull up/down resistance		13		kΩ

15.3 Debug interface mode

Before the external debugger can access the CPU's access port (AHB-AP) or the control access port (CTRL-AP), the debugger must first request the device to power up via CxxxPWRUPREQ in the SWJ-DP.

As long as the debugger is requesting power via CxxxPWRUPREQ, the device will be in debug interface mode. If the debugger is not requesting power via CxxxPWRUPREQ, the device will be in normal mode.

Some peripherals will behave differently in debug interface mode compared to normal mode. These differences are described in more detail in the chapters of the peripherals that are affected.

When a debug session is over, the external debugger must make sure to put the device back into normal mode since the overall power consumption will be higher in debug interface mode compared to normal mode.

For details on how to use the debug capabilities please read the debug documentation of your IDE.



If the device is in System OFF when power is requested via CxxxPWRUPREQ, the system will wake up and the DIF flag in *RESETREAS* on page 77 will be set.

15.4 Real-time debug

The nRF52840 supports real-time debugging.

Real-time debugging will allow interrupts to execute to completion in real time when breakpoints are set in thread mode or lower priority interrupts. This enables the developer to set a breakpoint and single-step through their code without a failure of the real-time event-driven threads running at higher priority. For example, this enables the device to continue to service the high-priority interrupts of an external controller or sensor without failure or loss of state synchronization while the developer steps through code in a low-priority thread.

15.5 Trace

The device supports ETM and ITM trace.

Trace data from the ETM and the ITM is sent to an external debugger via a 4-bit wide parallel trace port (TPIU), see TRACEDATA[0] through TRACEDATA[3] and TRACECLK in *Figure 9: Overview* on page 62. In addition to parallel trace, the TPIU supports serial trace via the serial wire output (SWO) trace protocol. Parallel and serial trace cannot be used at the same time.

ETM trace is only supported in parallel trace mode, while ITM trace is supported in both parallel and serial trace modes. For details on how to use the trace capabilities, please read the debug documentation of your IDE.

TPIU's trace pins are multiplexed with GPIOs, and SWO and TRACEDATA[0] use the same GPIO, see *Pin assignments* on page 13 for more information. The speed of the trace pins depends on the drive setting of the GPIOs that the trace pins are multiplexed with. Trace speed is configured in the *TRACECONFIG* on page 149 register.

Only S0S1 and H0H1 drives are suitable for debugging. S0S1 is the default drive at reset. If parallel or serial trace port signals are not fast enough in the debugging conditions, all GPIOs in use for tracing should be set to high drive (H0H1). The user must make sure that these GPIOs' drive is not overwritten by software during the debugging session.

15.5.1 Electrical specification

Trace port

Symbol	Description	Min.	Тур.	Max.	Units
T _{cyc}	Clock period, as defined by ARM (See ARM Infocenter,	62.5		500	ns
	Embedded Trace Macrocell Architecture Specification, Trace				
	Port Physical Interface, Timing specifications)				



16 POWER — Power supply

The power supply consists of a number of LDO and DC/DC regulators that are utilized to maximize the system's power efficiency.

This device has the following power supply features:

- · On-chip LDO and DC/DC regulators
- · Global System ON/OFF modes
- Individual RAM section power control for all system modes
- Analog or digital pin wakeup from System OFF
- Supervisor HW to manage power-on reset, brownout, and power fail
- · Auto-controlled refresh modes for LDO and DC/DC regulators to maximize efficiency
- · External circuitry supply
- Separate USB supply

16.1 Main supply

The main supply voltage is connected to **VDD/VDDH** pins. The system will enter one of two supply voltage modes, normal or high voltage mode, depending on how the supply voltage is connected to these pins.

Normal voltage mode is entered when the supply voltage is connected to both the VDD and VDDH pins (so that VDD equals VDDH).

High voltage mode is entered when the supply voltage is only connected to the VDDH pin and the VDD pin is not connected to any voltage supply.

The *MAINREGSTATUS* on page 81 register can be used for reading out the current supply voltage mode.

For the supply voltage range of the two supply voltage modes, see *Regulator operating conditions* on page 138.

16.1.1 Main voltage regulators

The system contains two main supply regulator stages, REG0 and REG1.

Each of the regulator stages have the following regulator type options:

- Low-dropout regulator (LDO)
- Buck regulator (DC/DC)

In normal voltage mode, only the REG1 regulator stage is used and the REG0 stage is automatically disabled. In high voltage mode, both regulator stages (REG0 and REG1) are used. The output voltage of REG0 can be configured in register *REGOUT0* on page 58 listed in *UICR* — *User information configuration registers* on page 44. This output voltage is connected to **VDD** and is the input voltage to REG1.

By default, the LDO regulators are enabled and the DC/DC regulators are disabled. Registers *DCDCENO* on page 81 and *DCDCEN* on page 80 are used to independently enable the DC/DC regulators for the two stages (REG0 and REG1 respectively).

When a DC/DC converter is enabled, the LDO for the corresponding regulator stage will be disabled. External LC filters must be connected for each of the DC/DC regulators being used. The advantage of using a DC/DC regulator is that the overall power consumption is normally reduced as the efficiency of such a regulator is higher than that of a LDO. The efficiency benefit of using a DC/DC regulator becomes particularly prominent at high dropout voltage (between the input voltage and the output voltage). The efficiency of internal regulators vary with the supply voltage and the current drawn from the regulators.

Important: Do not enable DCDC regulator without an external LC filter being connected as this will inhibit device operation, including debug access, until an LC filter is connected.



16.1.2 GPIO levels

The GPIO high reference voltage always equals the level on the VDD pin.

In normal voltage mode, the GPIO high level equals the voltage supplied to the VDD pin, and in high voltage mode it equals the level specified in the register *REGOUTO* on page 58 listed in *UICR* — *User information configuration registers* on page 44.

16.1.3 External circuitry supply

In high voltage mode, the output from REG0 can be used to supply external circuitry from the VDD pin.

Before any current can be drawn from the **VDD** pin, this feature must be enabled in the **EXTSUPPLY** on page 57 UICR register.

The VDD output voltage is configured in the *REGOUT0* on page 58 UICR register.

The supported output voltage range depends on the supply voltage provided on the **VDDH** pin. Minimum difference between voltage supplied on the **VDDH** pin and the voltage output on the **VDD** pin is defined by **V**_{EXDIF} parameter in *Regulator operating conditions* on page 138.

Supplying external circuitry is allowed in both System OFF and System ON mode.

Important: When in System OFF mode, 1 mA is the maximum current draw allowed by external circuitry (as defined by the **I**_{EX.OFF} parameter in *Regulator operating conditions* on page 138).

16.1.4 Regulator configuration examples

The voltage regulators can be configured in several ways, depending on the selected supply voltage mode (normal/high) and the regulator type option (LDO or DC/DC).

Four configuration examples are illustrated in images below.

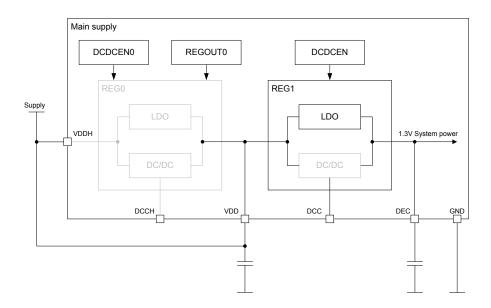


Figure 10: Normal voltage mode, LDO only



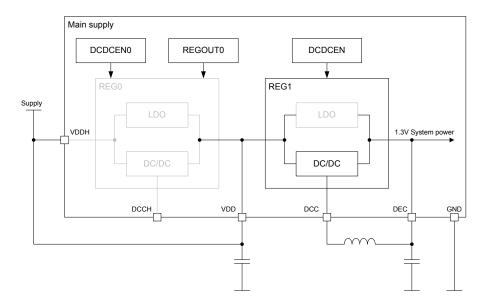


Figure 11: Normal voltage mode, DC/DC REG1 enabled

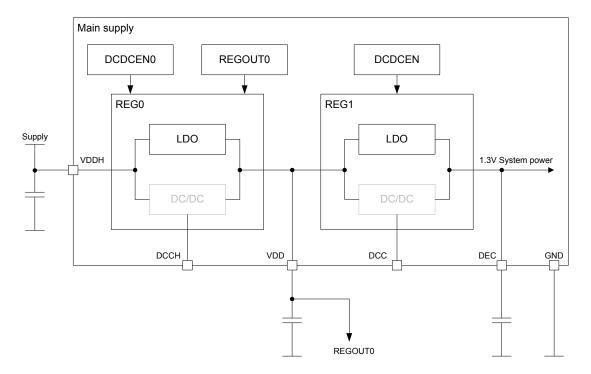


Figure 12: High voltage mode, LDO only



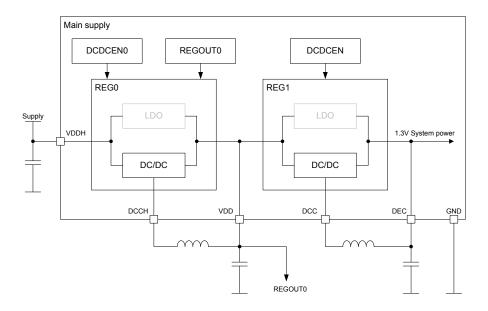


Figure 13: High voltage mode, DC/DC for REG0 and REG1 enabled

16.1.5 Power supply supervisor

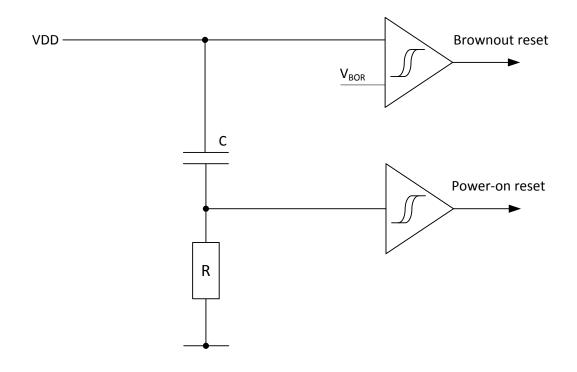
The power supply supervisor enables monitoring of the connected power supply.

The power supply supervisor provides:

- Power-on reset, signalling to the circuit when a supply is connected.
- An optional power-fail comparator (POF), to signal the application when the supply voltages drop below a configured threshold.
- A fixed brownout reset detector, to hold the system in reset when the voltage is too low for safe operation.

The power supply supervisor is illustrated in *Figure 14: Power supply supervisor* on page 70. To enable and configure the power-fail comparator, see the register *POFCON* on page 79.





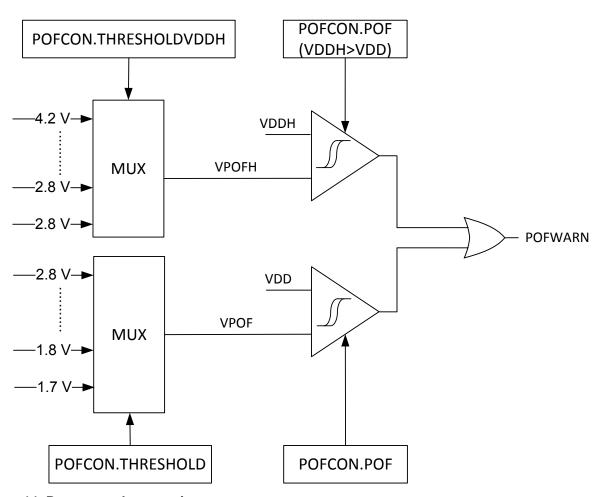


Figure 14: Power supply supervisor



16.1.6 Power-fail comparator

Using the power-fail comparator (POF) is optional. When enabled, it can provide the CPU with an early warning of an impending power supply failure.

To enable and configure the power-fail comparator, see the register *POFCON* on page 79.

The threshold (V_{POF}) must be configured to a suitable level. When the supply voltage falls below the defined threshold, the power-fail comparator will generate an event (POFWARN) which can be used by an application to prepare for power failure. This event will also be generated if the supply voltage is already below the threshold at the time the power-fail comparator is enabled, or if the threshold is re-configured to a level above the supply voltage.

If the power-fail warning is enabled and the supply voltage is below the threshold, the power-fail comparator will prevent the *NVMC* from performing write operations to the NVM.

The comparator features a hysteresis of V_{HYST}, as illustrated in *Figure 15: Power-fail comparator (BOR = brownout reset)* on page 71.

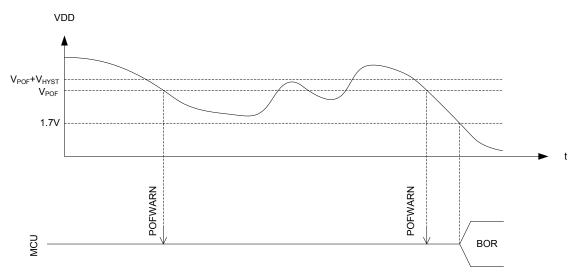


Figure 15: Power-fail comparator (BOR = brownout reset)

To save power, the power-fail comparator is not active in System OFF or in System ON when HFCLK is not running.

16.2 USB supply

When using the USB peripheral, a 5 V USB supply needs to be provided on the VBUS pin.

The USB peripheral has a dedicated internal voltage regulator for converting the V_{BUS} supply to 3.3 V used by the USB signalling interface (D+ and D- lines, and pull-up on D+). The rest of the USB peripheral (USBD) is supplied through the main supply like any other on-chip feature. As a consequence, both V_{BUS} and either V_{DDH} or V_{DD} supplies are required for USB peripheral operation.

When V_{BUS} rises into its valid range, the software is notified through a USBDETECTED event. A USBREMOVED event is sent when V_{BUS} goes below its valid range. Use these events to implement the USBD start-up sequence described in the *USBD* chapter.

When V_{BUS} rises into its valid range while the device is in System OFF, the device resets and transitions to System ON mode. The *RESETREAS* register will have the VBUS bit set to indicate the source of the wake-up.

See VBUS detection specifications on page 140 for the levels at which the events are sent ($V_{BUS,DETECT}$ and $V_{BUS,REMOVE}$) or at which the system is woken up from System OFF ($V_{BUS,DETECT}$).



When the USBD peripheral is enabled through the *ENABLE* register and V_{BUS} is detected, the regulator is turned on. A USBPWRRDY event is sent when the regulator's worst case settling time has elapsed, indicating to the software that it can enable the USB pull-up to signal a USB connection to the host.

The software can read the state of the V_{BUS} detection and regulator output readiness at any time through the *USBREGSTATUS* register.

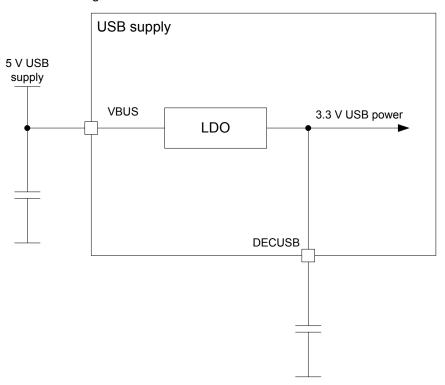


Figure 16: USB voltage regulator

To ensure stability, the input and output of the USB regulator need to be decoupled with a suitable decoupling capacitor. See *Reference circuitry* on page 688 for the recommended values.

16.3 System OFF mode

System OFF is the deepest power saving mode the system can enter. In this mode, the system's core functionality is powered down and all ongoing tasks are terminated.

The device can be put into System OFF mode using the POWER register interface. When in System OFF mode, the device can be woken up through one of the following signals:

- 1. The DETECT signal, optionally generated by the GPIO peripheral.
- 2. The ANADETECT signal, optionally generated by the LPCOMP module.
- 3. The SENSE signal, optionally generated by the NFC module to wake-on-field.
- **4.** Detecting a *valid USB voltage* on the V_{BUS} pin (V_{BUS DETECT}).
- 5. A reset.

The system is reset when it wakes up from the System OFF mode.

One or more RAM sections can be retained in System OFF mode, depending on the settings in the RAM[n].POWER registers. RAM[n].POWER are retained registers. Note that these registers are usually overwritten by the start-up code provided with the nRF application examples.

Before entering the System OFF mode, the user must make sure that all on-going EasyDMA transactions have been completed. See peripheral specific chapters for more information about how to acquire the status of EasyDMA transactions.



16.3.1 Emulated System OFF mode

If the device is in debug interface mode, System OFF will be emulated to secure that all required resources needed for debugging are available during System OFF.

See *Debug and trace* on page 62 for more information. Required resources needed for debugging include the following key components: *Debug and trace* on page 62, *CLOCK* — *Clock control* on page 141, *POWER* — *Power supply* on page 66, *NVMC* — *Non-volatile memory controller* on page 28, CPU, flash, and RAM. Since the CPU is kept on in an emulated System OFF mode, it is recommended to add an infinite loop directly after entering System OFF, to prevent the CPU from executing code that normally should not be executed.

16.4 System ON mode

System ON is the default state after power-on reset. In System ON, all functional blocks such as the CPU or peripherals, can be in IDLE or RUN mode, depending on the configuration set by the software and the state of the application executing.

Register RESETREAS on page 77 provides information about the source causing the wakeup or reset.

The system can switch the appropriate internal power sources on and off, depending on how much power is needed at any given time. The power requirement of a peripheral is directly related to its activity level, and the activity level of a peripheral is usually raised and lowered when specific tasks are triggered or events are generated.

16.4.1 Sub power modes

In System ON mode, when both the CPU and all the peripherals are in IDLE mode, the system can reside in one of the two sub power modes.

The sub power modes are:

- Constant latency
- · Low power

In constant latency mode, the CPU wakeup latency and the PPI task response are constant and kept at a minimum. This is secured by forcing a set of basic resources to be turned on while in sleep. Having a constant and predictable latency is at cost of having increased power consumption. The constant latency mode is selected by triggering the CONSTLAT task.

In low power mode, the automatic power management system described in *System ON mode* on page 73 ensures that the most efficient supply option is chosen to save most power. Having the lowest power possible is at cost of having a varying CPU wakeup latency and PPI task response. The low power mode is selected by triggering the LOWPWR task.

When the system enters System ON mode, it is by default in low power sub power mode.

16.5 RAM power control

RAM power control is used for RAM retention in System OFF mode and for powering down unused sections in System ON mode.

Each RAM section can power up and down independently in both System ON and System OFF mode. See chapter *Memory* on page 20 for more information on RAM sections.

RAM sections can be retained in System OFF mode, depending on the settings in the RAM[n].POWER registers. RAM[n].POWER are retained registers.

16.6 Reset

Several sources may trigger a reset.



After a reset has occurred, register *RESETREAS* can be read to determine which source has triggered the reset.

16.6.1 Power-on reset

The power-on reset generator initializes the system at power-on.

The system is held in a reset state until the power supply has reached the minimum operating voltage and the internal voltage regulators have started.

16.6.2 Pin reset

A pin reset is generated when the physical reset pin on the device is asserted.

Pin reset is configured via the PSELRESET[0] and PSELRESET[1] registers.

16.6.3 Wakeup from System OFF mode reset

The device is reset when it wakes up from System OFF mode.

The debug access port (DAP) is not reset following a wake up from System OFF mode if the device is in debug interface mode. See chapter *Debug and trace* on page 62 for more information.

16.6.4 Soft reset

A soft reset is generated when the SYSRESETREQ bit of the Application Interrupt and Reset Control Register (AIRCR register) in the ARM® core is set.

See ARM documentation for more details.

A soft reset can also be generated via the register RESET on page 63 in the CTRL-AP.

16.6.5 Watchdog reset

A watchdog reset is generated when the watchdog times out.

See chapter WDT — Watchdog timer on page 470 for more information.

16.6.6 Brownout reset

The brownout reset generator puts the system in reset state if the supply voltage drops below the brownout reset (BOR) threshold.

See section *Power fail comparator* on page 139 for more information.

16.7 Retained registers

A retained register is a register that will retain its value in System OFF mode and through a reset, depending on reset source. See individual peripheral chapters for information of which registers are retained for the various peripherals.

16.8 Reset behavior

Reset behavior of the different reset sources is summarized in a table.

Reset source	Reset target CPU	Peripherals	GPIO	Debug ^a	SWJ-DP	RAM	WDT	Retained registers	RESETREAS
CPU lockup ⁵	X	X	x						
Soft reset	X	X	x						

^a All debug components excluding SWJ-DP. See *Debug and trace* on page 62 chapter for more information about the different debug components.

⁵ Reset from CPU lockup is disabled if the device is in debug interface mode. CPU lockup is not possible in System OFF.



Reset source	Reset target								
	СРИ	Peripherals	GPIO	Debug ^a	SWJ-DP	RAM	WDT	Retained registers	RESETREAS
Wakeup from System OFF mode reset	х	х		x ⁶		x ⁷		-	
Watchdog reset ⁸	х	x	Х	х		x	х	Х	
Pin reset	х	x	х	х		x	x	х	
Brownout reset	х	x	Х	х	X	x	x	X	x
Power-on reset	v	v	v	v	v	v	v	v	v

Important: The RAM is never reset, but depending on a reset source the content of RAM may be corrupted.

16.9 Registers

Table 15: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40000000	POWER	POWER	Power control		

Table 16: Register Overview

Register	Offset	Description	
TASKS_CONSTLAT	0x078	Enable constant latency mode	
TASKS_LOWPWR	0x07C	Enable low power mode (variable latency)	
EVENTS_POFWARN	0x108	Power failure warning	
EVENTS_SLEEPENTER	0x114	CPU entered WFI/WFE sleep	
EVENTS_SLEEPEXIT	0x118	CPU exited WFI/WFE sleep	
EVENTS_USBDETECTED	0x11C	Voltage supply detected on VBUS	
EVENTS_USBREMOVED	0x120	Voltage supply removed from VBUS	
EVENTS_USBPWRRDY	0x124	USB 3.3 V supply ready	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
RESETREAS	0x400	Reset reason	
RAMSTATUS	0x428	RAM status register	Deprecated
USBREGSTATUS	0x438	USB supply status	
SYSTEMOFF	0x500	System OFF register	
POFCON	0x510	Power failure comparator configuration	
GPREGRET	0x51C	General purpose retention register	
GPREGRET2	0x520	General purpose retention register	
DCDCEN	0x578	Enable DC/DC converter for REG1 stage.	
DCDCEN0	0x580	Enable DC/DC converter for REG0 stage.	
MAINREGSTATUS	0x640	Main supply status	
RAM[0].POWER	0x900	RAMO power control register	
RAM[0].POWERSET	0x904	RAM0 power control set register	
RAM[0].POWERCLR	0x908	RAM0 power control clear register	
RAM[1].POWER	0x910	RAM1 power control register	
RAM[1].POWERSET	0x914	RAM1 power control set register	
RAM[1].POWERCLR	0x918	RAM1 power control clear register	
RAM[2].POWER	0x920	RAM2 power control register	
RAM[2].POWERSET	0x924	RAM2 power control set register	
RAM[2].POWERCLR	0x928	RAM2 power control clear register	
RAM[3].POWER	0x930	RAM3 power control register	
RAM[3].POWERSET	0x934	RAM3 power control set register	
RAM[3].POWERCLR	0x938	RAM3 power control clear register	
RAM[4].POWER	0x940	RAM4 power control register	

⁶ The Debug components will not be reset if the device is in debug interface mode.

⁷ RAM is not reset on wakeup from OFF mode, but depending on settings in the RAM registers parts, or the whole RAM, may not be retained after the device has entered System OFF mode.

⁸ Watchdog reset is not available in System OFF.



Register	Offset	Description
RAM[4].POWERSET	0x944	RAM4 power control set register
RAM[4].POWERCLR	0x948	RAM4 power control clear register
RAM[5].POWER	0x950	RAM5 power control register
RAM[5].POWERSET	0x954	RAM5 power control set register
RAM[5].POWERCLR	0x958	RAM5 power control clear register
RAM[6].POWER	0x960	RAM6 power control register
RAM[6].POWERSET	0x964	RAM6 power control set register
RAM[6].POWERCLR	0x968	RAM6 power control clear register
RAM[7].POWER	0x970	RAM7 power control register
RAM[7].POWERSET	0x974	RAM7 power control set register
RAM[7].POWERCLR	0x978	RAM7 power control clear register
RAM[8].POWER	0x980	RAM8 power control register
RAM[8].POWERSET	0x984	RAM8 power control set register
RAM[8].POWERCLR	0x988	RAM8 power control clear register

16.9.1 INTENSET

Address offset: 0x304

Enable interrupt

	iable interrupt			
Bit	number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F E D C B A
Res	set 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW POFWARN			Write '1' to Enable interrupt for POFWARN event
				See EVENTS_POFWARN
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW SLEEPENTER			Write '1' to Enable interrupt for SLEEPENTER event
				See EVENTS_SLEEPENTER
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW SLEEPEXIT			Write '1' to Enable interrupt for SLEEPEXIT event
				See EVENTS_SLEEPEXIT
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW USBDETECTED			Write '1' to Enable interrupt for USBDETECTED event
				See EVENTS_USBDETECTED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Ε	RW USBREMOVED			Write '1' to Enable interrupt for USBREMOVED event
				See EVENTS_USBREMOVED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW USBPWRRDY			Write '1' to Enable interrupt for USBPWRRDY event
		Set	1	See EVENTS_USBPWRRDY Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
		Lilubica	<u> </u>	



16.9.2 INTENCLR

Address offset: 0x308

Disable interrupt

		e interrupt																															
Bit	numbe	er		31	30	29	28 2	7 2	6 2	5 24	4 2	23 :	22 21	L 20	19	18	17	16	15	14	13	3 12	2 1	1 10) 9	9 8	7	6	5	4	3	2	1 (
Id																									F	: E	D	С	В			Α	
Res	et 0x0	0000000		0	0	0	0 (0 (0	0) (0	0 0	0	0	0	0	0	0	0	0	0	(0	C) (0	0	0	0	0	0	0 (
Id	RW	Field	Value Id	Va	lue						D	Des	scripti	ion																			
Α	RW	POFWARN									٧	۷ri	ite '1'	to I	Disa	ble	int	err	upt	for	P(DFV	VΑ	RN	eve	nt							
											S	ee	e EVEN	NTS_	_PO	FW	ARI	٧															
			Clear	1							D	Disa	able																				
			Disabled	0							R	Rea	ad: Dis	sabl	ed																		
			Enabled	1							R	Rea	ad: En	able	ed																		
В	RW	SLEEPENTER									٧	۷ri	ite '1'	to I	Disa	ble	int	err	upt	for	· SL	EEF	PEI	NTE	R e	ven	t						
											S	ee	e EVEN	NTS_	SLE	ΕP	EN7	ER															
			Clear	1							D	Disa	able																				
			Disabled	0							R	Rea	ad: Dis	sabl	ed																		
			Enabled	1							R	Rea	ad: En	able	ed																		
С	RW	SLEEPEXIT									٧	۷ri	ite '1'	to I	Disa	ble	int	err	upt	for	· SL	EEF	PE)	KIT 6	eve	nt							
											S	ee	e EVEN	NTS_	SLE	ΕP	EXI	-															
			Clear	1							D	Disa	able																				
			Disabled	0							R	Rea	ad: Dis	sabl	ed																		
			Enabled	1							R	Rea	ad: En	able	ed																		
D	RW	USBDETECTED									٧	۷ri	ite '1'	to I	Disa	ble	int	err	upt	for	· U	SBC	DET	ECT	ED	eve	ent						
											S	ee	e EVEN	NTS_	US	BDI	TE	CTE	D														
			Clear	1							D	Disa	able																				
			Disabled	0							R	Rea	ad: Dis	sabl	ed																		
			Enabled	1							R	Rea	ad: En	able	ed																		
Ε	RW	USBREMOVED									٧	۷ri	ite '1'	to I	Disa	ble	int	err	upt	for	· U	SBR	REN	/OV	ΈD	ev	ent						
											S	ee	e EVEN	NTS_	_US	BRE	М	OVE	D														
			Clear	1							D	Disa	able																				
			Disabled	0							R	Rea	ad: Dis	sabl	ed																		
			Enabled	1							R	Rea	ad: En	able	ed																		
F	RW	USBPWRRDY									٧	۷ri	ite '1'	to I	Disa	ble	int	err	upt	for	· U	SBP	w	RRD	Υe	ver	it						
											S	ee	e EVEN	NTS_	US	BP	VRI	RD)	,														
			Clear	1							D	Disa	able																				
			Disabled	0							R	Rea	ad: Dis	sabl	ed																		
			Enabled	1							R	Rea	ad: En	able	ed																		

16.9.3 RESETREAS

Address offset: 0x400

Reset reason

Unless cleared, the RESETREAS register will be cumulative. A field is cleared by writing '1' to it. If none of the reset sources are flagged, this indicates that the chip was reset from the on-chip reset generator, which will indicate a power-on-reset or a brownout reset.

Bitı	numbe	er		31	30 2	9 :	28 2	7 2	6 2	5 24	4 23	3 2	2 2	1 2	20 :	19	18	17	16	15	14	13	12	11	10	9	8 7	7 (6 !	5 .	4	3 2	2 :	1 0
Id															L	Н	G	F	Ε												- 1	D (C 1	ВА
Res	et 0x0	0000000		0	0 (0	0 () (0	0	0	(0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0 () (0 0
Id	RW	Field	Value Id	Val	ue						D	esc	rip	tio	n																			
Α	RW	RESETPIN									R	ese	t fr	om	ı pi	n-r	ese	et d	ete	ecte	d													
			NotDetected	0							Ν	ot (det	ect	ed																			
			Detected	1							D	ete	cte	d																				
В	RW	DOG									R	ese	t fr	om	ı w	atc	hdo	og (det	ect	ed													
			NotDetected	0							N	ot (det	ect	ed																			



Bit	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Detected	1	Detected
С	RW SREQ			Reset from soft reset detected
		NotDetected	0	Not detected
		Detected	1	Detected
D	RW LOCKUP			Reset from CPU lock-up detected
		NotDetected	0	Not detected
		Detected	1	Detected
Ε	RW OFF			Reset due to wake up from System OFF mode when wakeup is
				triggered from DETECT signal from GPIO
		NotDetected	0	Not detected
		Detected	1	Detected
F	RW LPCOMP			Reset due to wake up from System OFF mode when wakeup is
				triggered from ANADETECT signal from LPCOMP
		NotDetected	0	Not detected
		Detected	1	Detected
G	RW DIF			Reset due to wake up from System OFF mode when wakeup is
				triggered from entering into debug interface mode
		NotDetected	0	Not detected
		Detected	1	Detected
Н	RW NFC			Reset due to wake up from System OFF mode by NFC field
				detect
		NotDetected	0	Not detected
		Detected	1	Detected
I	RW VBUS			Reset due to wake up from System OFF mode by Vbus rising
				into valid range
		NotDetected	0	Not detected
		Detected	1	Detected

16.9.4 RAMSTATUS (Deprecated)

Address offset: 0x428 RAM status register

Since this register is deprecated the following substitutions have been made: RAM block 0 is equivalent to a block comprising RAM0.S0 and RAM1.S0, RAM block 1 is equivalent to a block comprising RAM2.S0 and RAM3.S0, RAM block 2 is equivalent to a block comprising RAM4.S0 and RAM5.S0 and RAM block 3 is equivalent to a block comprising RAM6.S0 and RAM7.S0. A RAM block field will indicate ON as long as any of the RAM sections associated with a block are on.

Bitı	numbe	er		31	30 2	9 2	8 27	26	25	24	23 22	2 21	L 20	19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5 4	1 3	2	1 0
Id																												D	С	ВА
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	0 0
ld	RW	Field	Value Id	Val	lue						Desc	ript	ion																	
Α	R	RAMBLOCK0									RAM	blo	ck 0	is (on c	or of	f/p	ow	erin	g up)									
			Off	0							Off																			
			On	1							On																			
В	R	RAMBLOCK1									RAM	blo	ck 1	is (on c	or of	f/p	ow	erin	g up)									
			Off	0							Off																			
			On	1							On																			
С	R	RAMBLOCK2									RAM	blo	ck 2	is	on c	or of	f/p	ow	erin	g up)									
			Off	0							Off																			
			On	1							On																			
D	R	RAMBLOCK3									RAM	blo	ck 3	is	on c	or of	f/p	ow	erin	g up)									
			Off	0							Off																			
			On	1							On																			



16.9.5 USBREGSTATUS

Address offset: 0x438 USB supply status

Bit	numbe	er		31	30	29	28	27 :	26 :	25 :	24	23	22	21	20	19	18	17	16	15	L4 1	.3 1	12 1	1 1) 9	8	7	6	5	4	3	2 :	1 0
Id																																ı	ВА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	n																		
Α	R	VBUSDETECT										VBI	US i	npı	ıt d	ete	ctic	n s	tatı	ıs (JSB	DE.	ΓEC	ΓED	and	d US	BRI	EMC	OVE	D			
												eve	ents	are	de	rive	ed f	ron	n th	is i	nfor	ma	tior	1)									
			NoVbus	0								VBI	US١	/olt	age	be	low	va	id t	hre	sho	ld											
			VbusPresent	1								VBI	US١	/olt	age	ab	ove	va	id t	hre	sho	ld											
В	R	OUTPUTRDY										USI	B su	ppl	у о	utp	ut s	ett	ing	tin	e e	lap	sed										
			NotReady	0								USI	BRE	G o	utp	ut s	ett	ling	tin	ne i	ot	ela	ose	ł									
			Ready	1								USI	BRE	G o	utp	ut s	ett	ling	tin	ne e	lap	sec	(sa	me	info	rm	atio	n as	S				
												USI	BPV	VRR	DY	eve	nt)																

16.9.6 SYSTEMOFF

Address offset: 0x500 System OFF register

Bit r	numb	er		31 30 29 28	27 26 2	25 24	23 2	22 2	1 20	19	18 17	16	15	14 13	3 12 :	11 10	9	8	7	6	5	4 3	2	1 0
Id																								Α
Res	et 0x0	00000000		0 0 0 0	0 0	0 0	0	0 0	0	0	0 0	0	0	0 0	0	0 0	0	0	0	0	0	0 0	0	0 0
l al	DIA/	Field	Value Id	Value			_																	
Iu	KVV	Field	value iu	value			Des	crip	tion															
A	W	SYSTEMOFF	value id	value				•		m O	FF m	ode												

16.9.7 POFCON

Address offset: 0x510

Power failure comparator configuration

Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D D D D B B B B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	POF			Enable or disable power failure comparator
			Disabled	0	Disable
			Enabled	1	Enable
В	RW	THRESHOLD			Power failure comparator threshold setting. This setting applies
					both for normal voltage mode (supply connected to both VDD
					and VDDH) and high voltage mode (supply connected to VDDH
					only).
			V17	4	Set threshold to 1.7 V
			V18	5	Set threshold to 1.8 V
			V19	6	Set threshold to 1.9 V
			V20	7	Set threshold to 2.0 V
			V21	8	Set threshold to 2.1 V
			V22	9	Set threshold to 2.2 V
			V23	10	Set threshold to 2.3 V
			V24	11	Set threshold to 2.4 V
			V25	12	Set threshold to 2.5 V
			V26	13	Set threshold to 2.6 V
			V27	14	Set threshold to 2.7 V
			V28	15	Set threshold to 2.8 V



Bit number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			D D D D B B B B A
Reset 0x00000000		0 0 0 0 0 0 0	$0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;$
Id RW Field	Value Id	Value	Description
D RW THRESHOLDVDDH			Power failure comparator threshold setting for high voltage
			mode (supply connected to VDDH only). This setting does not
			apply for normal voltage mode (supply connected to both VDD
			and VDDH).
	V27	0	Set threshold to 2.7 V
	V28	1	Set threshold to 2.8 V
	V29	2	Set threshold to 2.9 V
	V30	3	Set threshold to 3.0 V
	V31	4	Set threshold to 3.1 V
	V32	5	Set threshold to 3.2 V
	V33	6	Set threshold to 3.3 V
	V34	7	Set threshold to 3.4 V
	V35	8	Set threshold to 3.5 V
	V36	9	Set threshold to 3.6 V
	V37	10	Set threshold to 3.7 V
	V38	11	Set threshold to 3.8 V
	V39	12	Set threshold to 3.9 V
	V40	13	Set threshold to 4.0 V
	V41	14	Set threshold to 4.1 V
	V42	15	Set threshold to 4.2 V

16.9.8 GPREGRET

Address offset: 0x51C

General purpose retention register

Bi	t numb	er		31	30 2	29 2	28 2	7 26	25	24	23	22	21 2	20 1	9 1	8 17	7 16	15	14	13 :	L2 1	1 1	0 9	8	7	6	5	4	3 2	2 2	1 0	
Id																									Α	Α	Α	Α	A A	Α Α	A A	
R	set 0x	00000000		0	0	0	0 (0 0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (D O	
Id	RW	Field	Value Id	Va	lue						De	scri	otio	n																		l
Α	RW	GPREGRET									Ge	nera	al pu	ırpo	se i	rete	ntio	n re	gist	er												1

This register is a retained register

16.9.9 GPREGRET2

Address offset: 0x520

General purpose retention register

Bit	numb	er		31	30 :	29 2	28 2	7 26	25	24	23 :	22 2	21 2	0 1	9 18	3 17	16	15	14 1	3 12	11	10	9	8 7	7 (5 5	4	3	2	1 ()
Id																								A	۱ ۸	4 Δ	A	Α	Α	A	A
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0 (0 (0	0	0	0	0	0 0	0	0	0	0	0 0) (0 0	0	0	0	0 ()
Id	RW	Field	Value Id	Va	lue						Des	crip	tior	1																	
Α	RW	GPREGRET									Ger	era	l pu	rpo	se r	eter	tioi	n reg	giste	r											7

This register is a retained register

16.9.10 DCDCEN

Address offset: 0x578

Enable DC/DC converter for REG1 stage.

Bit	num	nbei	•		31	1 30 2	29 2	28 27	7 26	25	24	23 2	22 2	1 20) 19	18	17	16	15 :	14 1	L3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																																Α
Re	set 0)x00	000000		0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 0
Id	R۱	w	Field	Value Id	Va	alue						Des	cript	tion																		
Α	R۱	w	DCDCEN									Enal	ble [DC/[ос с	onv	erte	r fo	r R	EG1	sta	ge.										



Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 1	11 10 9 8 7	6 5 4 3 2 1 0
Id						А
Reset 0x00000000		0 0 0 0 0	0000000000	0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description			
	Disabled	0	Disable			
	Enabled	1	Enable			

16.9.11 DCDCEN0

Address offset: 0x580

Enable DC/DC converter for REG0 stage.

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	LO !	9 8	3	7	6	5	4	3 2	2 :	1 0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue	!						De	scri	pti	on																			
Α	RW	DCDCEN										En	able	e Do	C/D	C c	onv	ert	er f	or F	EG	0 st	age											
			Disabled	0								Dis	abl	e																				
			Enabled	1								En	able	9																				

16.9.12 MAINREGSTATUS

Address offset: 0x640 Main supply status

Bit r	numbe	er		31 30	29	28 2	27 2	6 25	5 24	23	22 2	21 2	0 19	18	17	16	15 :	14 13	3 12	11	10 9	8	7	6	5	4	3	2 1	0
Id																													Α
Res	et 0x0	0000000		0 0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0 0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Value						De	scrip	otion	ı																
Α	R	MAINREGSTATUS								Ma	ain sı	uppl	y sta	atus															
			NORMAL	0						No	rma	l vol	tage	mo	de.	Vol	tage	e sup	plie	d on	VDD								
			HIGH	1						Hig	gh vo	oltag	e m	ode.	. Vo	ltag	e sı	ıppli	ed o	n VD	DH.								

16.9.13 RAM[0].POWER

Address offset: 0x900

RAM0 power control register

Bit	numl	ber			31	30	29	28	3 27	7 2	6 2	5 2	24 2	23 2	22 2	1 2	0 1	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id					f	е	d	С	b	â	1 2	<u> </u>	Υ	X١	W V	/ L	J	Т	S	R	Q	Р	О	Ν	M	L	K	J	1	Н	G	F	Ε	D (СВ	Α
Res	et O	k00	00FFFF		0	0	0	0	0	C) () (0	0	0 0) (0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1
Id	RV	v i	Field	Value Id	Va	lue	:						ı	Des	cript	tio	n																			
Α	RV	V S	SOPOWER										ŀ	Kee	p RA	M	sec	tio	n S	0 C	N (or (DFF	in S	yst	em	٥N	l m	ode	١.						
													F	RAN	1 se	ctic	ns	are	al	wa	ys r	eta	ine	d w	he	n O	N, Ł	out	can	als	o b	e				
													r	reta	inec	d w	hei	n O	FF	dep	en	dei	nt o	n th	ne s	etti	ngs	in	SOF	RET	ENT	ΓΙΟΙ	N.			
													A	All R	RAM	se	ctio	ons	wi	ll b	e 0	FF	in S	yste	em	OFF	m	ode	2.							
				Off	0								(Off																						
				On	1								(On																						
В	RV	V S	S1POWER										ŀ	Keel	p RA	M	sec	ctio	n S	1 C	N (or (DFF	in S	yst	em	ON	l m	ode	١.						
													F	RAN	1 se	ctic	ns	are	e al	wa	ys r	eta	ine	d w	he	n O	N, b	out	can	als	o b	e				
													r	reta	inec	l w	hei	n O	FF	dep	en	dei	nt o	n th	ne s	etti	ngs	in	S1F	RET	ENT	ΓΙΟΙ	N.			
													1	All R	RAM	se	ctio	ons	wi	ll b	e O	FF	in S	yste	em	OFF	m	ode	·.							
				Off	0								(Off																						
				On	1								(On																						
С	RV	v s	S2POWER										ŀ	Kee	p RA	М	sec	tio	n S	2 C	N	or (OFF	in S	yst	em	O١	l m	ode	١.						
													F	RAN	1 se	ctic	ns	are	e al	wa	ys r	eta	ine	d w	hei	n 0	N, b	out	can	als	o b	e				
													r	reta	inec	l w	hei	n O	FF	dep	en	dei	nt o	n th	ne s	etti	ngs	in	S2F	RET	ENT	ΓΙΟΙ	N.			
													1	All R	RAM	se	ctio	ons	wi	ll b	e O	FF	in S	yste	em	OFF	m	ode	·.							



Bit number	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	fedcbaZY	X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x0000FFFF	0 0 0 0 0 0 0	0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field Value		Description
Off On	0 1	Off On
D RW S3POWER	1	Keep RAM section S3 ON or OFF in System ON mode.
3 33. 3.1.2.1		
		RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION.
		All RAM sections will be OFF in System OFF mode.
Off	0	Off
On	1	On
E RW S4POWER		Keep RAM section S4 ON or OFF in System ON mode.
		RAM sections are always retained when ON, but can also be
		retained when OFF dependent on the settings in S4RETENTION.
0#	2	All RAM sections will be OFF in System OFF mode.
Off On	0 1	Off On
F RW S5POWER	-	Keep RAM section S5 ON or OFF in System ON mode.
		RAM sections are always retained when ON, but can also be
		retained when OFF dependent on the settings in SSRETENTION.
		All RAM sections will be OFF in System OFF mode.
Off	0	Off
On	1	On
G RW S6POWER		Keep RAM section S6 ON or OFF in System ON mode.
		RAM sections are always retained when ON, but can also be
		retained when OFF dependent on the settings in S6RETENTION. All RAM sections will be OFF in System OFF mode.
Off	0	Off
On	1	On
H RW S7POWER		Keep RAM section S7 ON or OFF in System ON mode.
		RAM sections are always retained when ON, but can also be
		retained when OFF dependent on the settings in S7RETENTION.
011	2	All RAM sections will be OFF in System OFF mode.
Off On	0 1	Off On
I RW S8POWER	-	Keep RAM section S8 ON or OFF in System ON mode.
		RAM sections are always retained when ON, but can also be
		retained when OFF dependent on the settings in SBRETENTION.
		All RAM sections will be OFF in System OFF mode.
Off	0	Off
On On	1	On
J RW S9POWER		Keep RAM section S9 ON or OFF in System ON mode.
		RAM sections are always retained when ON, but can also be
		retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode.
Off	0	Off
On	1	On
K RW S10POWER		Keep RAM section S10 ON or OFF in System ON mode.
		RAM sections are always retained when ON, but can
		also be retained when OFF dependent on the settings in
		S10RETENTION. All RAM sections will be OFF in System OFF
Off	0	mode. Off
On	1	On
L RW S11POWER		Keep RAM section S11 ON or OFF in System ON mode.



Bit r	number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			f e d c b a	Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0000FFFF		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1
Id	RW Field	Value Id	Value	Description
				RAM sections are always retained when ON, but can
				also be retained when OFF dependent on the settings in S11RETENTION. All RAM sections will be OFF in System OFF
				mode.
		Off	0	Off
		On	1	On
М	RW S12POWER			Keep RAM section S12 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can
				also be retained when OFF dependent on the settings in
				S12RETENTION. All RAM sections will be OFF in System OFF
				mode.
		Off	0	Off
N	RW S13POWER	On	1	On Keep RAM section S13 ON or OFF in System ON mode.
14	SISTOWER			
				RAM sections are always retained when ON, but can
				also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF
				mode.
		Off	0	Off
		On	1	On
0	RW S14POWER			Keep RAM section S14 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can
				also be retained when OFF dependent on the settings in
				S14RETENTION. All RAM sections will be OFF in System OFF .
		Off	0	mode. Off
		On	1	On
Р	RW S15POWER			Keep RAM section S15 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can
				also be retained when OFF dependent on the settings in
				S15RETENTION. All RAM sections will be OFF in System OFF
				mode.
		Off	0	Off
		On 	1	On Control of the Con
Q	RW SORETENTIC	Off	0	Keep retention on RAM section S0 when RAM section is in OFF Off
		On	1	On
R	RW S1RETENTIO			Keep retention on RAM section S1 when RAM section is in OFF
		Off	0	Off
		On	1	On
S	RW S2RETENTIC			Keep retention on RAM section S2 when RAM section is in OFF
		Off	0	Off
Т	RW S3RETENTIC	On N	1	On Keep retention on RAM section S3 when RAM section is in OFF
•	NVV JONETEIVIIC	Off	0	Off
		On	1	On
U	RW S4RETENTIC	N		Keep retention on RAM section S4 when RAM section is in OFF
		Off	0	Off
		On	1	On
V	RW S5RETENTIC			Keep retention on RAM section S5 when RAM section is in OFF
		Off On	0 1	Off On
W	RW S6RETENTIC		1	Keep retention on RAM section S6 when RAM section is in OFF
	JONETENTIC	**		



Bit r	number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcb	a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0000FFFF		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1
Id	RW Field	Value Id	Value	Description
		Off	0	Off
		On	1	On
Χ	RW S7RETENTION			Keep retention on RAM section S7 when RAM section is in OFF
		Off	0	Off
		On	1	On
Υ	RW S8RETENTION			Keep retention on RAM section S8 when RAM section is in OFF
		Off	0	Off
		On	1	On
Z	RW S9RETENTION			Keep retention on RAM section S9 when RAM section is in OFF
		Off	0	Off
		On	1	On
а	RW S10RETENTION			Keep retention on RAM section S10 when RAM section is in OFF
		Off	0	Off
		On	1	On
b	RW S11RETENTION			Keep retention on RAM section S11 when RAM section is in OFF
		Off	0	Off
		On	1	On
С	RW S12RETENTION			Keep retention on RAM section S12 when RAM section is in OFF
		Off	0	Off
		On	1	On
d	RW S13RETENTION			Keep retention on RAM section S13 when RAM section is in OFF
		Off	0	Off
		On	1	On
e	RW S14RETENTION			Keep retention on RAM section S14 when RAM section is in OFF
		Off	0	Off
		On	1	On
f	RW S15RETENTION			Keep retention on RAM section S15 when RAM section is in OFF
		Off	0	Off
		On	1	On

16.9.14 RAM[0].POWERSET

Address offset: 0x904

RAM0 power control set register

Bit r	numbe	er		31	30	29	28	27	26 2	25	24 2	23 :	22 2	21 2	20	19	18	17	16	15	14	13 :	2 1	1 10) 9	8	7	6	5	4	3	2 1	. 0
Id				f	e	d	С	b	а	Z	Υ	Х	W	V	U	Т	S	R	Q	Р	О	N I	И	L K	J	1	Н	G	F	Ε	D	СВ	ВА
Res	et 0x0	0000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1 :	1 1	1	1	1	1	1	1	1	1 1	. 1
Id	RW	Field	Value Id	Va	lue							Des	scrip	tio	n																		
Α	W	SOPOWER									ı	Kee	p R	ΑM	se	ctic	n S	0 O	f R	١M	0 o	n or	off	in S	/ste	m C	ı NC	nod	e				
			On	1							(On																					
В	W	S1POWER									ŀ	Kee	p R	ΑM	se	ctic	n S	61 o	f R	١M	0 o	n or	off	in S	/ste	m C	ı NC	nod	e				
			On	1							(On																					
С	W	S2POWER									ı	Kee	p R	ΑM	se	ctic	n S	2 o	f R	١M	0 o	n or	off	in S	/ste	m C	ı NC	nod	e				
			On	1							(On																					
D	W	S3POWER									ı	Kee	p R	AΜ	se	ctic	n S	3 o	f R	١M	0 o	n or	off	in S	/ste	m C	ı NC	nod	e				
			On	1							(On																					
Е	W	S4POWER									ı	Kee	p R	AΜ	se	ctic	n S	64 o	f R	١M	0 o	n or	off	in S	/ste	m C	ı NC	nod	e				
			On	1							(On																					
F	W	S5POWER									ı	Kee	p R	AΜ	se	ctic	n S	55 o	f R	١M	0 o	n or	off	in S	/ste	m C	ı NC	nod	e				
			On	1							(On																					
G	W	S6POWER									ı	Kee	p R	ΑM	se	ctic	n S	6 o	f R	١M	0 o	n or	off	in S	/ste	m C	ı NC	nod	e				
			On	1							(On																					



Bit r	numbe	er		31	30	29	28 2	27 26	5 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f	е	d	С	b a	Z	<u> </u>	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Res	et 0x0	000FFFF		0	0	0	0	0 0	0	0	0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
Id		Field	Value Id	Va	lue						Description (%) Control (%) Co
Н	W	S7POWER	00	1							Keep RAM section S7 of RAM0 on or off in System ON mode
1	W	S8POWER	On	1							On Keep RAM section S8 of RAM0 on or off in System ON mode
•	••	JOI OWER	On	1							On
J	W	S9POWER									Keep RAM section S9 of RAM0 on or off in System ON mode
			On	1							On
K	W	S10POWER									Keep RAM section S10 of RAM0 on or off in System ON mode
			On	1							On
L	W	S11POWER	On	1							Keep RAM section S11 of RAM0 on or off in System ON mode On
М	W	S12POWER									Keep RAM section S12 of RAM0 on or off in System ON mode
			On	1							On
N	W	S13POWER									Keep RAM section S13 of RAMO on or off in System ON mode
			On	1							On
0	W	S14POWER	0.5	4							Keep RAM section S14 of RAM0 on or off in System ON mode
Р	W	S15POWER	On	1							On Keep RAM section S15 of RAMO on or off in System ON mode
r	vv	SISFOWER	On	1							On
Q	W	SORETENTION									Keep retention on RAM section SO when RAM section is
											switched off
			On	1							On
R	W	S1RETENTION									Keep retention on RAM section S1 when RAM section is
											switched off
S	W	S2RETENTION	On	1							On Keep retention on RAM section S2 when RAM section is
3	VV	32RETEINTION									switched off
			On	1							On
Т	W	S3RETENTION									Keep retention on RAM section S3 when RAM section is
											switched off
			On	1							On
U	W	S4RETENTION									Keep retention on RAM section S4 when RAM section is
			On	1							switched off On
V	W	SSRETENTION	011	_							Keep retention on RAM section S5 when RAM section is
											switched off
			On	1							On
W	W	S6RETENTION									Keep retention on RAM section S6 when RAM section is
			•	_							switched off
Х	W	S7RETENTION	On	1							On Keen retention on RAM section 57 when RAM section is
^	VV	3/RETEINTION									Keep retention on RAM section S7 when RAM section is switched off
			On	1							On .
Υ	W	S8RETENTION									Keep retention on RAM section S8 when RAM section is
											switched off
			On	1							On
Z	W	S9RETENTION									Keep retention on RAM section S9 when RAM section is
			On	1							switched off
a	W	S10RETENTION	On	1							On Keep retention on RAM section S10 when RAM section is
<u>~</u>											switched off
			On	1							On
b	W	S11RETENTION									Keep retention on RAM section S11 when RAM section is
											switched off
			On	1							On



Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6 !	5 4	- 3	2	1	0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U	Т	S	R	Q	Р	О	N	M	L	K	J	1 1	4	G I	F E	D	С	В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	ı	1 :	1 1	. 1	1	1	1
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																			
С	W	S12RETENTION										Ke	ер	rete	enti	on	on I	RAN	1 se	ctio	on S	512	wh	en l	RAN	Λse	ectic	n i	S					
												SW	itch	ned	off																			
			On	1								Or	1																					
d	W	S13RETENTION										Ke	ер	rete	enti	on	on l	RAN	1 se	ctio	on S	513	wh	en l	RAN	∕l se	ectic	n i	S					
												sw	itch	ned	off																			
			On	1								Or	1																					
e	W	S14RETENTION										Ke	ер	rete	enti	on	on I	RAN	1 se	ctio	on S	514	wh	en	RAN	Λse	ectic	n i	S					
												sw	itch	ned	off																			
			On	1								Or	1																					
f	W	S15RETENTION										Ke	ер	rete	enti	on	on l	RAN	1 se	ctio	on S	515	wh	en l	RAN	∕l se	ectic	n i	S					
												SW	itch	ned	off																			
			On	1								Or	1																					

16.9.15 RAM[0].POWERCLR

Address offset: 0x908

RAM0 power control clear register

		_																											
Bitı	numb	er		31	30	29 2	8 27	7 26	25 2	4 2	23 22 21	20 1	19 1	8 1	7 1	6 15	14	13	12 :	11 10	9	8	7	6	5	4 3	2	1	0
Id				f	е	d	c b	а	Ζ,	Υ :	x w v	U .	Т 9	S F	RC	Q P	0	N	М	L K	J	1	Н	G '	F	E D	С	В	Α
Res	et 0x0	0000FFFF		0	0	0 (0 0	0	0 ()	0 0 0	0	0 (0	0	1	1	1	1	1 1	1	1	1	1	1	1 1	1	1	1
Id	RW	Field	Value Id	Va	lue					0	Descripti	on																	
Α	W	SOPOWER								K	Ceep RAN	M sec	ction	ո S0	of	RAN	10 o	n o	off	in S	/stei	n O	N m	ode	•				
			Off	1						C	Off																		
В	W	S1POWER								K	Keep RAN	M sec	ction	n S1	of	RAN	10 o	n o	off	in S	/stei	n O	N m	ode	•				
			Off	1						C	Off																		
С	W	S2POWER								K	Keep RAN	M sec	ction	ո S2	of	RAN	10 o	n o	off	in S	/stei	n O	N m	ode	•				
			Off	1						C	Off																		
D	W	S3POWER								K	Keep RAN	M sec	ction	1 S3	of	RAN	10 o	n o	off	in S	/stei	n O	N m	ode	<u> </u>				
			Off	1						C	Off																		
Е	W	S4POWER								K	Keep RAN	M sec	ction	ո S4	of	RAN	10 o	n o	off	in S	/stei	n O	N m	ode	•				
			Off	1						C	Off																		
F	W	S5POWER								K	Keep RAN	M sec	ction	1 S5	of	RAN	10 o	n o	off	in S	/stei	n O	N m	ode	•				
			Off	1						C	Off																		
G	W	S6POWER								K	Keep RAN	M sec	ction	ո S6	of	RAN	10 o	n o	off	in S	/stei	n O	N m	ode	<u> </u>				
			Off	1						C	Off																		
Н	W	S7POWER								K	Keep RAN	M sec	ction	1 S7	of	RAN	10 o	n o	off	in S	/stei	n O	N m	ode	•				
			Off	1						C	Off																		
I	W	S8POWER								K	(eep RAN	M sec	ction	1 S8	of	RAN	10 o	n o	off	in S	/stei	n O	N m	ode	9				
			Off	1						C	Off																		
J	W	S9POWER								K	Keep RAN	M sec	ction	1 S 9	of	RAN	10 o	n o	off	in S	/stei	n O	N m	ode	•				
			Off	1						C	Off																		
K	W	S10POWER								K	Keep RAN	M sec	ction	s1	0 0	f RA	M0	on (or of	ff in !	Syste	em (ı NC	nod	le				
			Off	1						C	Off																		
L	W	S11POWER								K	Keep RAN	M sec	ction	1 S1	1 o	f RA	M0	on (or of	ff in S	Syste	em (ı NC	nod	le				
			Off	1						C	Off																		
М	W	S12POWER								K	Keep RAN	M sec	ction	1 S1	2 o	f RA	M0	on (or of	ff in S	Syste	em (ı NC	nod	le				
			Off	1						C	Off																		
N	W	S13POWER									Keep RAN	M sec	ction	1 S1	.3 o	f RA	M0	on (or of	ff in :	Syste	em (ı NC	nod	le				
			Off	1							Off																		
0	W	S14POWER									Keep RAN	M sec	ction	1 S1	.4 o	f RA	M0	on (or of	ff in :	Syste	em (ı NC	nod	le				
			Off	1						C	Off																		
Р	W	S15POWER								K	Keep RAN	M sec	ction	1 S1	.5 o	f RA	M0	on (or of	ff in !	Syste	em (ı NC	nod	le				



Bit r	iumbe	er		31 30	29 28	3 27	26 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0	000FFFF		0 0	0 0	0	0	0 0	$0\ 0\ 0\ 0\ 0\ 0\ 0\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\$
ld	RW	Field	Value Id	Value					Description
Q	W	SORETENTION	Off	1					Off Keep retention on RAM section S0 when RAM section is switched off Off
R	W	S1RETENTION	Off	1					Keep retention on RAM section S1 when RAM section is switched off Off
S	W	S2RETENTION	Off	1					Keep retention on RAM section S2 when RAM section is switched off Off
Т	W	S3RETENTION	Off	1					Keep retention on RAM section S3 when RAM section is switched off Off
U	W	S4RETENTION	Off	1					Keep retention on RAM section S4 when RAM section is switched off Off
V	W	SSRETENTION	Off	1					Keep retention on RAM section S5 when RAM section is switched off Off
W	W	SGRETENTION	Off	1					Keep retention on RAM section S6 when RAM section is switched off Off
Х	W	S7RETENTION	Off	1					Keep retention on RAM section S7 when RAM section is switched off Off
Υ	W	S8RETENTION	Off	1					Keep retention on RAM section S8 when RAM section is switched off Off
Z	W	S9RETENTION	Off	1					Keep retention on RAM section S9 when RAM section is switched off Off
а	W	S10RETENTION	Off	1					Keep retention on RAM section S10 when RAM section is switched off Off
b	W	S11RETENTION	Off	1					Keep retention on RAM section S11 when RAM section is switched off Off
С	W	S12RETENTION	Off	1					Keep retention on RAM section S12 when RAM section is switched off Off
d	W	S13RETENTION	Off	1					Keep retention on RAM section S13 when RAM section is switched off Off
е	W	S14RETENTION	Off	1					Keep retention on RAM section S14 when RAM section is switched off Off
f	W	S15RETENTION							Keep retention on RAM section S15 when RAM section is switched off
			Off	1					Off

16.9.16 RAM[1].POWER

Address offset: 0x910

RAM1 power control register



Bitı	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZY	Y X W V U T S R Q P O N M L K J I H G F E D C B A
Res	set 0x0000FFFF		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1
Id	RW Field	Value Id	Value	Description
Α	RW SOPOWER			RAM section SO ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode.
		Off	0	Off
В	RW S1POWER	On	1	On Keep RAM section S1 ON or OFF in System ON mode.
D	NW SIFOWER	Off On	0 1	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off On
С	RW S2POWER			Keep RAM section S2 ON or OFF in System ON mode.
		Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION. All RAM sections will be OFF in System OFF mode. Off On
D	RW S3POWER			Keep RAM section S3 ON or OFF in System ON mode.
		Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off On
E	RW S4POWER	.	-	Keep RAM section S4 ON or OFF in System ON mode.
		Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off
F	RW S5POWER	On	1	On Keep RAM section S5 ON or OFF in System ON mode.
		Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SSRETENTION. All RAM sections will be OFF in System OFF mode. Off
		On	1	On
G	RW S6POWER	Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SGRETENTION. All RAM sections will be OFF in System OFF mode. Off
		On	1	On
Н	RW S7POWER	Off	0	Keep RAM section S7 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION. All RAM sections will be OFF in System OFF mode. Off
		On	1	On
ı	RW S8POWER			Keep RAM section S8 ON or OFF in System ON mode.



	number			4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	-+ 000005555			X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0000FFFF RW Field	Value Id	Value	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
		Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. Off
J	RW S9POWER	On	1	On Keep RAM section S9 ON or OFF in System ON mode.
J	NW 337 GWEN	Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. Off
		On	1	On
K	RW S10POWER	Off	0	RAM sections 310 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. Off
	RW S11POWER	On	1	On Keep RAM section S11 ON or OFF in System ON mode.
L	NW 311FOWER	Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S11RETENTION. All RAM sections will be OFF in System OFF mode. Off On
М	RW S12POWER	Oli	1	Keep RAM section S12 ON or OFF in System ON mode.
		Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. Off
N	RW S13POWER	On	1	On Keep RAM section S13 ON or OFF in System ON mode.
		Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode. Off On
0	RW S14POWER			Keep RAM section S14 ON or OFF in System ON mode.
		Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S14RETENTION. All RAM sections will be OFF in System OFF mode. Off On
P	RW S15POWER	Off	0	Keep RAM section S15 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF mode. Off



Bit r	numbe	er		31 30 29 28 27	7 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e d c b	a Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	000FFFF		0 0 0 0 0	0 0 0	$0\ 0\ 0\ 0\ 0\ 0\ 0\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\$
Id	RW	Field	Value Id	Value		Description
			On	1		On
Q	RW	SORETENTION				Keep retention on RAM section SO when RAM section is in OFF
			Off	0		Off
_			On	1		On
R	RW	S1RETENTION	011	•		Keep retention on RAM section S1 when RAM section is in OFF
			Off On	0		Off On
S	R\M/	S2RETENTION	Oil	1		Keep retention on RAM section S2 when RAM section is in OFF
,	1100	32KETERTION	Off	0		Off
			On	1		On
Т	RW	S3RETENTION				Keep retention on RAM section S3 when RAM section is in OFF
			Off	0		Off
			On	1		On
U	RW	S4RETENTION				Keep retention on RAM section S4 when RAM section is in OFF
			Off	0		Off
			On	1		On
٧	RW	S5RETENTION				Keep retention on RAM section S5 when RAM section is in OFF
			Off	0		Off
			On	1		On
W	RW	S6RETENTION				Keep retention on RAM section S6 when RAM section is in OFF
			Off	0		Off
V	DVA	CZDETENTION	On	1		On
Х	KVV	S7RETENTION	Off	0		Keep retention on RAM section S7 when RAM section is in OFF Off
			On	1		On
Υ	RW	S8RETENTION		•		Keep retention on RAM section S8 when RAM section is in OFF
			Off	0		Off
			On	1		On
Z	RW	S9RETENTION				Keep retention on RAM section S9 when RAM section is in OFF
			Off	0		Off
			On	1		On
а	RW	S10RETENTION				Keep retention on RAM section S10 when RAM section is in OFF
			Off	0		Off
			On	1		On
b	RW	S11RETENTION				Keep retention on RAM section S11 when RAM section is in OFF
			Off	0		Off
r	D\A/	S12DETENTION	On	1		On Keep retention on PAM section \$12 when PAM section is in OFF
С	ĸW	S12RETENTION	Off	0		Keep retention on RAM section S12 when RAM section is in OFF Off
			On	1		On On
d	RW	S13RETENTION	<u></u>	-		Keep retention on RAM section S13 when RAM section is in OFF
			Off	0		Off
			On	1		On
e	RW	S14RETENTION				Keep retention on RAM section S14 when RAM section is in OFF
			Off	0		Off
			On	1		On
f	RW	S15RETENTION				Keep retention on RAM section S15 when RAM section is in OFF
			Off	0		Off
			On	1		On

16.9.17 RAM[1].POWERSET

Address offset: 0x914

RAM1 power control set register



Bit r	numbe	er			25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
	et Ox0	0000FFFF			0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	W	SOPOWER			Keep RAM section S0 of RAM1 on or off in System ON mode
			On	1	On
В	W	S1POWER			Keep RAM section S1 of RAM1 on or off in System ON mode
			On	1	On
С	W	S2POWER			Keep RAM section S2 of RAM1 on or off in System ON mode
D	\A/	C2DOWED	On	1	On Keep RAM section S3 of RAM1 on or off in System ON mode
D	W	S3POWER	On	1	On
E	W	S4POWER	OII .	-	Keep RAM section S4 of RAM1 on or off in System ON mode
			On	1	On
F	W	S5POWER			Keep RAM section S5 of RAM1 on or off in System ON mode
			On	1	On
G	W	S6POWER			Keep RAM section S6 of RAM1 on or off in System ON mode
			On	1	On
Н	W	S7POWER			Keep RAM section S7 of RAM1 on or off in System ON mode
			On	1	On
ı	W	S8POWER			Keep RAM section S8 of RAM1 on or off in System ON mode
J	W	S9POWER	On	1	On Keep RAM section S9 of RAM1 on or off in System ON mode
J	VV	39FOWER	On	1	On
K	W	S10POWER	.	-	Keep RAM section S10 of RAM1 on or off in System ON mode
			On	1	On
L	W	S11POWER			Keep RAM section S11 of RAM1 on or off in System ON mode
			On	1	On
М	W	S12POWER			Keep RAM section S12 of RAM1 on or off in System ON mode
			On	1	On
N	W	S13POWER			Keep RAM section S13 of RAM1 on or off in System ON mode
_		C4 4DOWED	On	1	On W. Dank W. Gata (Dank)
0	W	S14POWER	On	1	Keep RAM section S14 of RAM1 on or off in System ON mode On
Р	W	S15POWER	OII	1	Keep RAM section S15 of RAM1 on or off in System ON mode
•	••	3131 0 WER	On	1	On
Q	W	SORETENTION			Keep retention on RAM section SO when RAM section is
					switched off
			On	1	On
R	W	S1RETENTION			Keep retention on RAM section S1 when RAM section is
					switched off
•		CORFTENITION	On	1	On
S	W	S2RETENTION			Keep retention on RAM section S2 when RAM section is
			On	1	switched off On
Т	W	S3RETENTION	OII	1	On Keep retention on RAM section S3 when RAM section is
	,,	232.2			switched off
			On	1	On
U	W	S4RETENTION			Keep retention on RAM section S4 when RAM section is
					switched off
			On	1	On
٧	W	SSRETENTION			Keep retention on RAM section S5 when RAM section is
					switched off
			On	1	On
W	W	S6RETENTION			Keep retention on RAM section S6 when RAM section is
			0	1	switched off
			On	1	On



Bit r	numb	er		31 30	0 29	28 2	27 26	5 25	24	23 22 21	20 19	18	3 17	16	15	14	13 1	12 1	1 10	9	8	7	6	5	4	3 2	1	. 0
Id				f e	d	С	b a	Z	Υ	x w v	U T	S	R	Q	Р	О	1 N	M L	. K	J	1	Н	G	F	Е	D C	В	Α
Res	et 0x0	0000FFFF		0 0	0	0	0 0	0	0	0 0 0	0 0	0	0	0	1	1	1	1 1	l 1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Value	е					Descripti	on																	
X	W	S7RETENTION	On	1						Keep rete switched On		on	RAN	√l se	ectio	on S	7 w	hen	RAN	∕l se	ctio	n is						
Y	W	S8RETENTION	On	1						Keep rete switched On		on	RAN	√l se	ectio	on S	8 w	hen	RAN	∕l se	ctio	n is						
Z	W	S9RETENTION	On	1						Keep rete switched On		on	RAN	√l se	ectio	on S	9 w	hen	RAN	∕l se	ctio	n is						
а	W	S10RETENTION	On	1						Keep rete switched On		on	RAN	√l se	ectio	on S	10 v	whe	n RA	M s	ecti	on i	S					
b	W	S11RETENTION	On	1						Keep rete switched On		on	RAN	√l se	ectio	on S	11 v	whe	n RA	M s	ecti	on i	S					
С	W	S12RETENTION	On	1						Keep rete switched On		on	RAN	√l se	ectio	on S	12 v	whe	n RA	M s	ecti	on i	S					
d	W	S13RETENTION	On	1						Keep rete switched On		on	RAN	√l se	ectio	on S	13 v	whe	n RA	M s	ecti	on i	S					
е	W	S14RETENTION	On	1						Keep rete switched On		on	RAN	√l se	ectio	on S	14 v	whe	n RA	M s	ecti	on i	S					
f	W	S15RETENTION	On	1						Keep rete switched On		on	RAN	√l se	ectio	on S	15 v	whe	n RA	M s	ecti	on i	S					

16.9.18 RAM[1].POWERCLR

Address offset: 0x918

RAM1 power control clear register

umbe	er		31	30	29	28 2	27 :	26 2	25 2	24 2	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 4	1 3	2	1	0
			f	е	d	С	b	а	Ζ'n	Y)	x w	٧	U	Т	S	R	Q	Р	О	Ν	М	L	K	J	1	н	G	F I	E D	С	В	Α
t 0x0	000FFFF		0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1 :	l 1	1	1	1
RW	Field	Value Id	Va	lue						D	escr	ipti	on																			
W	SOPOWER									K	еер	RAN	VI se	ecti	on !	S0 d	of R	ΑN	11 o	n o	r of	f in	Sys	ten	n Ol	N m	ode	9				
		Off	1							C	Off																					
W	S1POWER									K	еер	RAN	VI se	ecti	on !	S1 (of R	AN	11 o	n o	r of	f in	Sys	ten	n Ol	N m	ode	9				
		Off	1							C	Off																					
W	S2POWER									K	еер	RAN	VI se	ecti	on !	S2 (of R	ΑN	11 o	n o	r of	f in	Sys	ten	n Ol	N m	ode	9				
		Off	1							C	Off																					
W	S3POWER									K	еер	RAN	VI se	ecti	on !	S3 (of R	AN	11 o	n o	r of	f in	Sys	ten	n Ol	N m	ode	9				
		Off	1							C	Off																					
W	S4POWER									K	еер	RAN	VI se	ecti	on !	S4 (of R	AN	11 o	n o	r of	f in	Sys	ten	n Ol	N m	ode	è				
		Off	1							C	Off																					
W	S5POWER									K	еер	RAN	VI se	ecti	on !	S5 (of R	AN	11 o	n o	r of	f in	Sys	ten	n Ol	N m	ode	9				
		Off	1							C	Off																					
W	S6POWER									K	еер	RAN	VI se	ecti	on !	S6 (of R	AN	11 o	n o	r of	f in	Sys	ten	n Ol	N m	ode	è				
		Off	1							C	Off																					
W	S7POWER									K	еер	RAN	VI se	ecti	on !	S7 (of R	AN	11 o	n o	r of	f in	Sys	ten	n Ol	N m	ode	9				
		Off	1							C	Off																					
	t 0x0 RW W W W W W W	W S1POWER W S2POWER W S3POWER W S4POWER W S5POWER W S6POWER	t 0x00000FFFF RW Field Value Id W S0POWER Off W S1POWER Off W S2POWER Off W S3POWER Off W S4POWER Off W S5POWER Off W S6POWER Off W S7POWER Off	F T T T T T T T T T	F E E E E E E E E E	F E C C C C C C C C C	The content of the	The color of the	The content of the	f e d c b a 2 c c c c c c c c c c c c c c c c c c	F P D D D D D D D D D	F	F e d C b a Z Y X W V	Field Value Id Value	F e d c b a Z Y X W V U T	F e d c b a Z Y X W V U T S	F e d C b a Z Y X W V U T S R	F	F e d c b a Z Y X W V U T S R Q P	F P O C D O O O O O O O O O	F R R R R R R R R R	F e d c b a Z Y X W V U T S R Q P O N M	F R R R R R R R R R	F E D C D D D D D D D D	F E D C D D D D D D D D	F E D C D D D D D D D D	To volume to value to	Field Value Valu	Field Value Id	TO THE TRUE BY THE	The light with the li	The content of the



Bitı	numb	er		31 30	29 28 2	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
		0000FFFF			0 0	0 0	0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW W	Field S8POWER	Value Id	Value				Description Keep RAM section S8 of RAM1 on or off in System ON mode
'	VV	SOPOWER	Off	1				Off
J	W	S9POWER		_				Keep RAM section S9 of RAM1 on or off in System ON mode
			Off	1				Off
K	W	S10POWER						Keep RAM section S10 of RAM1 on or off in System ON mode
			Off	1				Off
L	W	S11POWER	Off	1				Keep RAM section S11 of RAM1 on or off in System ON mode Off
М	W	S12POWER		_				Keep RAM section S12 of RAM1 on or off in System ON mode
			Off	1				Off
N	W	S13POWER						Keep RAM section S13 of RAM1 on or off in System ON mode
			Off	1				Off
0	W	S14POWER						Keep RAM section S14 of RAM1 on or off in System ON mode
Р	W	S15POWER	Off	1				Off Keep RAM section S15 of RAM1 on or off in System ON mode
r	VV	SISPOWER	Off	1				Off
Q	W	SORETENTION	5	-				Keep retention on RAM section SO when RAM section is
								switched off
			Off	1				Off
R	W	S1RETENTION						Keep retention on RAM section S1 when RAM section is
								switched off
S	W	S2RETENTION	Off	1				Off Your retartion on PAM section 52 when PAM section is
3	VV	52RETEINTION						Keep retention on RAM section S2 when RAM section is switched off
			Off	1				Off
Т	W	S3RETENTION						Keep retention on RAM section S3 when RAM section is
								switched off
			Off	1				Off
U	W	S4RETENTION						Keep retention on RAM section S4 when RAM section is
			Off	1				switched off Off
V	W	S5RETENTION	OII	1				Keep retention on RAM section S5 when RAM section is
-	••	5511212111611						switched off
			Off	1				Off
W	W	S6RETENTION						Keep retention on RAM section S6 when RAM section is
								switched off
	,	CORTENTION	Off	1				Off
Х	W	S7RETENTION						Keep retention on RAM section S7 when RAM section is switched off
			Off	1				Off
Υ	W	S8RETENTION		_				Keep retention on RAM section S8 when RAM section is
								switched off
			Off	1				Off
Z	W	S9RETENTION						Keep retention on RAM section S9 when RAM section is
			0"					switched off
2	14/	CIOPETENTION	Off	1				Off Keen retention on PAM section \$10 when PAM section is
a	W	S10RETENTION						Keep retention on RAM section S10 when RAM section is switched off
			Off	1				Off
b	W	S11RETENTION						Keep retention on RAM section S11 when RAM section is
								switched off
			Off	1				Off
С	W	S12RETENTION						Keep retention on RAM section S12 when RAM section is
			Off	1				switched off Off
			OII	T				OII



Bit	numbe	er		31	. 30	29	28	27	26	25	24	23 :	22 2	1 2	20 1	.9 1	18 :	17 1	16 :	15	14 1	13 1	2 11	10	9	8	7	6	5	4 3	2	1	0
Id				f	е	d	С	b	а	Z	Υ	Х	w١	/	U -	Т	S	R	Q	Р	О	N N	1 L	K	J	1	Н	G	F	E C	С С	В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0 0)	0 (0	0	0	0	1	1	1 1	. 1	1	1	1	1	1	1	1 1	. 1	1	1
Id	RW	Field	Value Id	Va	lue							Des	scrip	tio	n																		
d	W	S13RETENTION										Kee	ep re	ter	ntio	n o	n R	AM	se	ctic	n S	13 w	hen	RA	M s	ecti	on	is					
											:	swi	tche	d c	off																		
			Off	1								Off																					
е	W	S14RETENTION										Kee	ep re	ter	ntio	n o	n R	AM	se	ctic	n S	14 w	hen	RA	M s	ecti	on	is					
											:	swi	tche	d c	off																		
			Off	1								Off																					
f	W	S15RETENTION										Kee	ep re	ter	ntio	n o	n R	AM	se	ctic	n S	15 w	hen	RA	M s	ecti	on	is					
												swi	tche	d c	off																		
			Off	1								Off																					

16.9.19 RAM[2].POWER

Address offset: 0x920

RAM2 power control register

RAM2 power control re	egister		
Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld		fedcbaZY	'XWVUTSRQPONMLKJIHGFEDCBA
Reset 0x0000FFFF		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value	Description
A RW SOPOWER			Keep RAM section S0 ON or OFF in System ON mode.
			RAM sections are always retained when ON, but can also be
			retained when OFF dependent on the settings in SORETENTION.
			All RAM sections will be OFF in System OFF mode.
	Off	0	Off
	On	1	On
B RW S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
			RAM sections are always retained when ON, but can also be
			retained when OFF dependent on the settings in S1RETENTION.
			All RAM sections will be OFF in System OFF mode.
	Off	0	Off
	On	1	On
C RW S2POWER			Keep RAM section S2 ON or OFF in System ON mode.
			RAM sections are always retained when ON, but can also be
			retained when OFF dependent on the settings in S2RETENTION.
			All RAM sections will be OFF in System OFF mode.
	Off	0	Off
D DW CODOWED	On	1	On
D RW S3POWER			Keep RAM section S3 ON or OFF in System ON mode.
			RAM sections are always retained when ON, but can also be
			retained when OFF dependent on the settings in S3RETENTION.
	2"		All RAM sections will be OFF in System OFF mode.
	Off	0 1	Off
E RW S4POWER	On	1	On Keep RAM section S4 ON or OFF in System ON mode.
E KW 541 OWEK			
			RAM sections are always retained when ON, but can also be
			retained when OFF dependent on the settings in S4RETENTION.
	Off	0	All RAM sections will be OFF in System OFF mode. Off
	On	1	On
F RW S5POWER			Keep RAM section S5 ON or OFF in System ON mode.
			RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SSRETENTION.
			All RAM sections will be OFF in System OFF mode.



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZY	XWVUTSRQPONMLKJIHGFEDCBA
Reset 0x0000FFFF			0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value	Description Off
	Off On	0	Off On
G RW S6POWER	3 11	-	Keep RAM section S6 ON or OFF in System ON mode.
	Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SGRETENTION. All RAM sections will be OFF in System OFF mode. Off
	On	1	On
H RW S7POWER	Off	0	Keep RAM section S7 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION. All RAM sections will be OFF in System OFF mode. Off
	On	1	On
I RW S8POWER	Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. Off On
J RW S9POWER			Keep RAM section S9 ON or OFF in System ON mode.
	Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. Off
K RW S10POWER	On	1	On Keen BAM section \$10 ON or OFF in System ON mode
K RW S10POWER	Off	0	RAM section S10 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. Off
	On	1	On
L RW S11POWER	Off On	0 1	Keep RAM section S11 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S11RETENTION. All RAM sections will be OFF in System OFF mode. Off On
M RW S12POWER			Keep RAM section S12 ON or OFF in System ON mode.
	Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. Off On
N RW S13POWER	·		Keep RAM section S13 ON or OFF in System ON mode.
			RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode.



Bit r	numbe	er		31 30	29 28	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	000FFFF						0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value				Description
			Off	0				Off
			On	1				On
0	RW	S14POWER						Keep RAM section S14 ON or OFF in System ON mode.
								RAM sections are always retained when ON, but can
								also be retained when OFF dependent on the settings in
								S14RETENTION. All RAM sections will be OFF in System OFF
								mode.
			Off	0				Off
			On	1				On
Р	RW	S15POWER						Keep RAM section S15 ON or OFF in System ON mode.
								RAM sections are always retained when ON, but can
								also be retained when OFF dependent on the settings in
								S15RETENTION. All RAM sections will be OFF in System OFF
								mode.
			Off	0				Off
_			On	1				On
Q	RW	SORETENTION	044	0				Keep retention on RAM section S0 when RAM section is in OFF
			Off On	0				Off On
R	RW	S1RETENTION	Oli	1				Keep retention on RAM section S1 when RAM section is in OFF
		SINETENTION	Off	0				Off
			On	1				On
S	RW	S2RETENTION						Keep retention on RAM section S2 when RAM section is in OFF
			Off	0				Off
			On	1				On
Т	RW	S3RETENTION						Keep retention on RAM section S3 when RAM section is in OFF
			Off	0				Off
			On	1				On
U	RW	S4RETENTION						Keep retention on RAM section S4 when RAM section is in OFF
			Off	0				Off
V	D\A/	SSRETENTION	On	1				On Keep retention on RAM section S5 when RAM section is in OFF
V	LVV	SORETEINTION	Off	0				Off
			On	1				On
W	RW	S6RETENTION		_				Keep retention on RAM section S6 when RAM section is in OFF
			Off	0				Off
			On	1				On
Χ	RW	S7RETENTION						Keep retention on RAM section S7 when RAM section is in OFF
			Off	0				Off
			On	1				On
Υ	RW	S8RETENTION						Keep retention on RAM section S8 when RAM section is in OFF
			Off	0				Off
7	Dist	CORETENTION	On	1				On
Z	KW	S9RETENTION	Off	0				Keep retention on RAM section S9 when RAM section is in OFF Off
			On	1				On
а	RW	S10RETENTION	VII					Keep retention on RAM section S10 when RAM section is in OFF
-			Off	0				Off
			On	1				On
b	RW	S11RETENTION						Keep retention on RAM section S11 when RAM section is in OFF
			Off	0				Off
			On	1				On
С	RW	S12RETENTION						Keep retention on RAM section S12 when RAM section is in OFF
			Off	0				Off



Bit	numb	er		31	30	29	28	27	26 2	25 2	24 2	3 2	2 21	20	19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4 3	2	1	0
Id				f	е	d	С	b	а	Z	Υ)	X V	/ V	U	Т	S	R	Q	Р	О	N N	νL	. K	J	1	Н	G	F	E D	С	В	Α
Res	et 0x0	0000FFFF		0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	1	1	1	1 1	. 1	1	1	1	1	1	1 1	1	1	1
Id	RW	Field	Value Id	Va	lue						C	esc	ripti	on																		
			On	1							C	n																				
d	RW	S13RETENTION									K	еер	rete	ent	ion	on I	RAN	1 se	ectio	on S	13 v	vhe	n RA	Ms	ecti	on	is in	OF	F			
			Off	0							C	Off																				
			On	1							C	n																				
е	RW	S14RETENTION									K	еер	rete	ent	ion	on I	RAN	1 se	ectio	on S	14 v	vhe	n RA	Ms	ecti	on	is in	OF	F			
			Off	0							C	Off																				
			On	1							C	n																				
f	RW	S15RETENTION									K	еер	rete	ent	ion	on I	RAN	1 se	ectio	on S	15 v	vhe	n RA	M	ecti	on	is in	OF	F			
			Off	0							C	Off																				
			On	1							C	n																				

16.9.20 RAM[2].POWERSET

Address offset: 0x924

RAM2 power control set register

Bit r	numb	er		3:	1 30	29	28 2	7 26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f	е	d	c b	а	Z	Y X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et Ox(0000FFFF		0	0	0	0 0	0	0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	V	alue					Description
Α	W	SOPOWER								Keep RAM section S0 of RAM2 on or off in System ON mode
			On	1						On
В	W	S1POWER								Keep RAM section S1 of RAM2 on or off in System ON mode
			On	1						On
С	W	S2POWER								Keep RAM section S2 of RAM2 on or off in System ON mode
			On	1						On
D	W	S3POWER								Keep RAM section S3 of RAM2 on or off in System ON mode
			On	1						On
Ε	W	S4POWER								Keep RAM section S4 of RAM2 on or off in System ON mode
			On	1						On
F	W	S5POWER								Keep RAM section S5 of RAM2 on or off in System ON mode
			On	1						On
G	W	S6POWER								Keep RAM section S6 of RAM2 on or off in System ON mode
			On	1						On
Н	W	S7POWER								Keep RAM section S7 of RAM2 on or off in System ON mode
			On	1						On
I	W	S8POWER								Keep RAM section S8 of RAM2 on or off in System ON mode
			On	1						On
J	W	S9POWER								Keep RAM section S9 of RAM2 on or off in System ON mode
			On	1						On
K	W	S10POWER								Keep RAM section S10 of RAM2 on or off in System ON mode
			On	1						On
L	W	S11POWER								Keep RAM section S11 of RAM2 on or off in System ON mode
			On	1						On
M	W	S12POWER	_							Keep RAM section S12 of RAM2 on or off in System ON mode
			On	1						On
N	W	S13POWER								Keep RAM section S13 of RAM2 on or off in System ON mode
			On	1						On "" " " " " " " " " " " " " " " " " "
0	W	S14POWER	_							Keep RAM section S14 of RAM2 on or off in System ON mode
			On	1						On
Р	W	S15POWER								Keep RAM section S15 of RAM2 on or off in System ON mode
			On	1						On



Bit r	numbe	er		31 30	29 2	28 2	7 26	25 2	4 23	22 21	. 20	19 1	18 17	16	15 1	L4 1	.3 12	2 11	10	9	8 7	6	5	4	3	2 1	. 0
Id				f e	d	c b	а	Z	Y X	w v	U	Т :	S R	Q	Р (0 N	N M	1 L	K	J	I F	G	F	Е	D	СВ	A
Res	et OxO	000FFFF		0 0	0	0 0	0	0	0 0	0 0	0	0	0 0	0	1	1 1	1 1	. 1	1	1	1 1	1	1	1	1	1 1	. 1
Id		Field	Value Id	Value						scripti																	
Q	W	SORETENTION	On	1						ep rete tched			n RAI	M se	ctio	n S0) wh	en F	RAM	sec	tion	is					
R	W	S1RETENTION	On	1						ep rete			n RAI	M se	ctio	n S1	L wh	en F	RAM	l sec	ction	is					
S	W	S2RETENTION	On	1					Kee	ep rete tched			n RAI	M se	ctio	n S2	2 wh	en F	RAM	sec	tion	is					
Т	W	S3RETENTION	On	1					Kee	ep rete tched			n RAI	M se	ctio	n S3	3 wh	ien F	RAM	sec	ction	is					
U	W	S4RETENTION	On	1					Kee	ep rete tched			n RAI	M se	ctio	n S4	l wh	en F	RAM	sec	tion	is					
V	W	SSRETENTION	On	1					Kee	ep rete tched			n RAI	M se	ctio	n S5	5 wh	en F	RAM	l sec	ction	is					
W	W	S6RETENTION	On	1						ep rete tched			n RAI	M se	ctio	n S6	5 wh	en F	RAM	sec	tion	is					
X	W	S7RETENTION	On	1					Kee	ep rete tched			n RAI	M se	ctio	n S7	7 wh	en F	RAM	l sec	ction	is					
Υ	W	S8RETENTION	On	1					Kee	ep rete tched			n RAI	M se	ctio	n S8	3 wh	en F	RAM	sec	tion	is					
Z	W	S9RETENTION	On	1						ep rete tched			n RAI	M se	ctio	n S9) wh	en F	RAM	l sec	ction	is					
а	W	S10RETENTION	On	1						ep rete tched			n RAI	M se	ctio	n S1	LO w	hen	RAI	VI se	ectio	n is					
b	W	S11RETENTION	On	1						ep rete			n RAI	M se	ctio	n S1	l1 w	hen	RAI	M se	ectio	n is					
С	W	S12RETENTION	On	1						ep rete			n RAI	M se	ctio	n S1	L2 w	hen	RAI	VI se	ectio	n is					
d	W	S13RETENTION	On	1						ep rete tched			n RAI	M se	ctio	n S1	L3 w	hen	RAI	M se	ectio	n is					
е	W	S14RETENTION	On	1						ep rete tched			n RAI	M se	ctio	n S1	L4 w	hen	RAI	VI se	ectio	n is					
f	W	S15RETENTION	On	1						ep rete tched			n RAI	M se	ctio	n S1	L5 w	hen	RAI	VI se	ectio	n is					

16.9.21 RAM[2].POWERCLR

Address offset: 0x928

RAM2 power control clear register



Bit r	numb	er		31 30 2	29 28 2	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e d	d c	b a	Z Y	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Res	et 0x0	0000FFFF		0 0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
Id		Field	Value Id	Value				Description
Α	W	SOPOWER	Off	1				Keep RAM section S0 of RAM2 on or off in System ON mode Off
В	W	S1POWER	Off	1				Keep RAM section S1 of RAM2 on or off in System ON mode Off
С	W	S2POWER	Off	1				Keep RAM section S2 of RAM2 on or off in System ON mode Off
D	W	S3POWER	Off	1				Keep RAM section S3 of RAM2 on or off in System ON mode Off
E	W	S4POWER	Off	1				Keep RAM section S4 of RAM2 on or off in System ON mode Off
F	W	S5POWER	Off	1				Keep RAM section S5 of RAM2 on or off in System ON mode Off
G	W	S6POWER	Off	1				Keep RAM section S6 of RAM2 on or off in System ON mode Off
Н	W	S7POWER	Off	1				Keep RAM section S7 of RAM2 on or off in System ON mode Off
I	W	S8POWER	Off					Keep RAM section S8 of RAM2 on or off in System ON mode Off
J	W	S9POWER	Off	1				Keep RAM section S9 of RAM2 on or off in System ON mode Off
K	W	S10POWER	Off	1				Keep RAM section S10 of RAM2 on or off in System ON mode Off
L	W	S11POWER						Keep RAM section S11 of RAM2 on or off in System ON mode
М	W	S12POWER	Off	1				Off Keep RAM section S12 of RAM2 on or off in System ON mode
N	W	S13POWER	Off	1				Off Keep RAM section S13 of RAM2 on or off in System ON mode
0	W	S14POWER	Off	1				Off Keep RAM section S14 of RAM2 on or off in System ON mode
Р	W	S15POWER	Off	1				Off Keep RAM section S15 of RAM2 on or off in System ON mode
Q	W	SORETENTION	Off	1				Off Keep retention on RAM section SO when RAM section is
			Off	1				switched off Off
R	W	S1RETENTION						Keep retention on RAM section S1 when RAM section is switched off
			Off	1				Off
S	W	S2RETENTION	Off	1				Keep retention on RAM section S2 when RAM section is switched off Off
Т	W	S3RETENTION		1				Keep retention on RAM section S3 when RAM section is switched off
U	W	S4RETENTION	Off	1				Off Keep retention on RAM section S4 when RAM section is switched off
			Off	1				Off
V	W	S5RETENTION						Keep retention on RAM section S5 when RAM section is switched off
141	,	CCRETENTION	Off	1				Off
W	W	S6RETENTION	O#	4				Keep retention on RAM section S6 when RAM section is switched off
Х	W	S7RETENTION	Off	1				Off Keep retention on RAM section S7 when RAM section is
~	VV	J. HETEINHON						switched off



Bit	numb	er		3:	1 30	29	28	27	26	25	24	23	3 22	2 21	. 20	19	18	17	16	15	14	13	12 1	.1 1	0 9	8	7	6	5	4	3 2	2 1	. 0
Id				f	е	d	С	b	а	Z	Υ	Х	W	/ V	U	Т	S	R	Q	Р	О	N	M	L k	(J	-1	Н	G	F	Е	D C	В	А
Res	et 0x0	0000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1 1	. 1	1	1	1	1	1	1 1	1	. 1
Id	RW	Field	Value Id	V	alue	е						D	escr	ripti	ion																		
			Off	1								O	ff																				
Υ	W	S8RETENTION										Ke	eep	ret	ent	ion	on	RAI	√l se	cti	on S	8 w	her	RA	M s	ecti	on is	5					
												sv	witcl	hed	off	f																	
			Off	1								O	ff																				
Z	W	S9RETENTION										Κe	еер	ret	ent	ion	on	RAI	√l se	cti	on S	9 w	her	RA	M s	ecti	on is	5					
												sv	witcl	hed	off	f																	
			Off	1								Of	ff																				
а	W	S10RETENTION										Ke	eep	ret	ent	ion	on	RAI	√l se	cti	on S	10	whe	n R	AΜ	sect	ion	is					
													witcl	hed	off	f																	
			Off	1								Of																					
b	W	S11RETENTION											eep				on	RAI	√l se	ecti	on S	11	whe	n R	AΜ	sect	ion	is					
													witcl	hed	off	f																	
			Off	1								Of																					
С	W	S12RETENTION											eep				on	RAI	√l se	ecti	on S	12	whe	n R	AΜ	sect	ion	is					
													witcl	hed	off	f																	
			Off	1								Of																					
d	W	S13RETENTION											eep				on	RAI	√l se	ecti	on S	13	whe	n R	AM	sect	ion	is					
			0.00										witcl	hed	off	ŀ																	
	144	C4 4DETENTION	Off	1								Of									_												
е	W	S14RETENTION											eep				on	KAI	VI S	ecti	on S	14	whe	n R	AM	sect	ion	IS					
			011										witcl	hed	off	ľ																	
£	14/	CAEDETENTION	Off	1								01		rot	o n.t.			D A *	1 -		C	1 [- طيب	. P	A B A		lar	ic					
Т	W	S15RETENTION											eep				on	KAľ	VI SE	cti	on S	15	wne	n K	AIVI	seci	ion	15					
			Off	1								SV	vitcl	nea	on																		
			OII	1								U	H																				

16.9.22 RAM[3].POWER

Address offset: 0x930

RAM3 power control register

Bit r	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20) 19	1	8 1	7 1	5 1	5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U	Т	9	F	R C	Į F	P () N	1 1	ΛI	. K	J	-1	Н	G	F	Ε	D (В	A
Res	et OxC	0000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	C	0	0) 1	1 :	L 1	: ۱	1 1	l 1	1	1	1	1	1	1	1 1	L 1	. 1
Id	RW	Field	Value Id	Va	lue							De	scri	pti	on																			
Α	RW	SOPOWER										Kee	ep F	RAN	Λs	ect	ior	S0	ON	l Oi	r OF	Fir	ı Sy	ste	m O	Νn	nod	e.						
												RA	M s	ect	oi	ns a	ire	alw	ays	re	tair	ned	wh	ien	ON,	bu	t ca	n al:	so b	e				
												ret	aine	ed v	wh	ien	OF	F d	epe	nd	ent	on	the	e se	ttinį	ıi aş	s0	RET	ENT	ΓΙΟΝ	٧.			
												All	RAI	M s	ec	tior	าร เ	vill	be	OF	Fin	Sys	tei	n O	FF r	noc	le.							
			Off	0								Off	f																					
			On	1								On																						
В	RW	S1POWER										Kee	ep F	RAN	∕l s	ect	ior	S1	01	lo l	OF	Fir	ı Sy	ste	m O	N n	nod	e.						
												RA	M s	ect	oi	ns a	ire	alw	ays	re	tair	ned	wh	ien	ON,	bu	t ca	n al:	so b	e				
												ret	aine	ed v	wh	ien	OF	F d	epe	nd	ent	on	the	e se	ttinį	ıi aş	s S1	RET	ENT	ΓΙΟΝ	٧.			
												All	RAI	M s	ec	tior	าร เ	vill	be	OF	F in	Sys	tei	n O	FF r	noc	le.							
			Off	0								Off	f																					
			On	1								On																						
С	RW	S2POWER										Kee	ер Г	RAN	∕l s	ect	ior	S2	01	lo l	OF	Fir	ı Sy	ste	m O	Νn	nod	e.						
												RA	M s	ect	ioi	ns a	ire	alw	/ays	re	tair	ned	wh	ien	ON,	bu	t ca	n al:	so b	e				
												ret	aine	ed v	wh	ien	OF	F d	epe	nd	ent	on	the	e se	ttinį	ıi aş	n S2	RET	ENT	ΓΙΟΝ	٧.			
												All	RAI	M s	ec	tior	าร เ	vill	be	OF	F in	Sys	tei	n O	FF r	noc	le.							
			Off	0								Off	f																					
			On	1								On																						
D	RW	S3POWER										Kee	ер Ғ	RAN	∕l s	ect	ior	S3	ON	l Oi	r OF	Fir	ı Sy	ste	m O	Νn	nod	e.						



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Reset 0x0000FFFF		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1
ld RW Field	Value Id Off	Value RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off
	On	1 On
E RW S4POWER		Keep RAM section S4 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode.
	Off	0 Off
	On	1 On
F RW SSPOWER	Off On	RAM section S5 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S5RETENTION. All RAM sections will be OFF in System OFF mode. O Off On
G RW S6POWER	Oli	Keep RAM section S6 ON or OFF in System ON mode.
	Off On	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SGRETENTION. All RAM sections will be OFF in System OFF mode. Off On
H RW S7POWER	011	Keep RAM section S7 ON or OFF in System ON mode.
	Off On	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION. All RAM sections will be OFF in System OFF mode. Off On
I RW S8POWER		Keep RAM section S8 ON or OFF in System ON mode.
	Off	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. Off
I DW CODOWED	On	1 On
J RW S9POWER	Off On	RAM section S9 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. O Off On
K RW S10POWER	-	Keep RAM section S10 ON or OFF in System ON mode.
	Off On	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. 0 Off 1 On
L RW S11POWER	Oil	Keep RAM section S11 ON or OFF in System ON mode.
211.000		RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in



Bit r	numb	er		31 3	0 29	28 2	7 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x(0000FFFF		0 0	0	0 (0	0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 &$
Id	RW	Field	Value Id	Valu	e				Description
									S11RETENTION. All RAM sections will be OFF in System OFF
			Off	0					mode. Off
			On	1					On
М	RW	S12POWER	Oli	_					Keep RAM section S12 ON or OFF in System ON mode.
									RAM sections are always retained when ON, but can
									also be retained when OFF dependent on the settings in
									S12RETENTION. All RAM sections will be OFF in System OFF
									mode.
			Off	0					Off
			On	1					On
N	RW	S13POWER							Keep RAM section S13 ON or OFF in System ON mode.
									RAM sections are always retained when ON, but can
									also be retained when OFF dependent on the settings in
									S13RETENTION. All RAM sections will be OFF in System OFF
			Off	0					mode. Off
			On	1					On
0	RW	S14POWER							Keep RAM section S14 ON or OFF in System ON mode.
									RAM sections are always retained when ON, but can
									also be retained when OFF dependent on the settings in
									S14RETENTION. All RAM sections will be OFF in System OFF
									mode.
			Off	0					Off
_	5111		On	1					On
Р	KW	S15POWER							Keep RAM section S15 ON or OFF in System ON mode.
									RAM sections are always retained when ON, but can
									also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF
									mode.
			Off	0					Off
			On	1					On
Q	RW	SORETENTION							Keep retention on RAM section S0 when RAM section is in OFF
			Off	0					Off
P	DIA	CIDETENTION	On	1					On Keen retention on PAM section S1 when PAM section is in OFF
R	KW	S1RETENTION	Off	0					Keep retention on RAM section S1 when RAM section is in OFF Off
			On	1					On
S	RW	S2RETENTION							Keep retention on RAM section S2 when RAM section is in OFF
			Off	0					Off
			On	1					On
Т	RW	S3RETENTION	255						Keep retention on RAM section S3 when RAM section is in OFF
			Off	0					Off
U	R\M/	S4RETENTION	On	1					On Keep retention on RAM section S4 when RAM section is in OFF
-			Off	0					Off
			On	1					On
٧	RW	SSRETENTION							Keep retention on RAM section S5 when RAM section is in OFF
			Off	0					Off
			On	1					On
W	RW	S6RETENTION	Off	0					Keep retention on RAM section S6 when RAM section is in OFF
			Off On	0					Off On
			OII	1					OII



Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x0000FFFF		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1
ld	RW Field	Value Id	Value Description
Χ	RW S7RETENTION		Keep retention on RAM section S7 when RAM section is in OFF
		Off	0 Off
		On	1 On
Υ	RW S8RETENTION		Keep retention on RAM section S8 when RAM section is in OFF
		Off	0 Off
		On	1 On
Z	RW S9RETENTION		Keep retention on RAM section S9 when RAM section is in OFF
		Off	0 Off
		On	1 On
а	RW S10RETENTION		Keep retention on RAM section S10 when RAM section is in OFF
		Off	0 Off
		On	1 On
b	RW S11RETENTION		Keep retention on RAM section S11 when RAM section is in OFF
		Off	0 Off
		On	1 On
С	RW S12RETENTION		Keep retention on RAM section S12 when RAM section is in OFF
		Off	0 Off
		On	1 On
d	RW S13RETENTION		Keep retention on RAM section S13 when RAM section is in OFF
		Off	0 Off
		On	1 On
е	RW S14RETENTION		Keep retention on RAM section S14 when RAM section is in OFF
		Off	0 Off
		On	1 On
f	RW S15RETENTION		Keep retention on RAM section S15 when RAM section is in OFF
		Off	0 Off
		On	1 On

16.9.23 RAM[3].POWERSET

Address offset: 0x934

RAM3 power control set register

Id fedcbaZYXWVUTSR	Q P O N M L K J I H G F E D C B A
Reset 0x0000FFFF 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id Value Description	
A W SOPOWER Keep RAM section SO o	f RAM3 on or off in System ON mode
On 1 On	
B W S1POWER Keep RAM section S1 o	f RAM3 on or off in System ON mode
On 1 On	
C W S2POWER Keep RAM section S2 o	f RAM3 on or off in System ON mode
On 1 On	
D W S3POWER Keep RAM section S3 o	f RAM3 on or off in System ON mode
On 1 On	
E W S4POWER Keep RAM section S4 o	f RAM3 on or off in System ON mode
On 1 On	
F W S5POWER Keep RAM section S5 o	f RAM3 on or off in System ON mode
On 1 On	
G W S6POWER Keep RAM section S6 o	f RAM3 on or off in System ON mode
On 1 On	
H W S7POWER Keep RAM section S7 o	f RAM3 on or off in System ON mode
On 1 On	



Bit	numb	er		31 30	29 28 2	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
		0000FFFF				0 0	0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW W	Field S8POWER	Value Id	Value				Description Keep RAM section S8 of RAM3 on or off in System ON mode
'	VV	SOFOWER	On	1				On
J	W	S9POWER		_				Keep RAM section S9 of RAM3 on or off in System ON mode
			On	1				On
K	W	S10POWER						Keep RAM section S10 of RAM3 on or off in System ON mode
			On	1				On
L	W	S11POWER	On	1				Keep RAM section S11 of RAM3 on or off in System ON mode On
М	W	S12POWER	.	-				Keep RAM section S12 of RAM3 on or off in System ON mode
			On	1				On
N	W	S13POWER						Keep RAM section S13 of RAM3 on or off in System ON mode
			On	1				On
0	W	S14POWER						Keep RAM section S14 of RAM3 on or off in System ON mode
Р	W	S15POWER	On	1				On Keep RAM section S15 of RAM3 on or off in System ON mode
r	VV	SISPOWER	On	1				On
Q	W	SORETENTION	.	-				Keep retention on RAM section SO when RAM section is
								switched off
			On	1				On
R	W	S1RETENTION						Keep retention on RAM section S1 when RAM section is
								switched off
S	\A/	CODETENTION	On	1				On Voca retartion on DAM section C2 when DAM section is
3	W	S2RETENTION						Keep retention on RAM section S2 when RAM section is switched off
			On	1				On .
Т	W	S3RETENTION						Keep retention on RAM section S3 when RAM section is
								switched off
			On	1				On
U	W	S4RETENTION						Keep retention on RAM section S4 when RAM section is
			0					switched off
V	W	SSRETENTION	On	1				On Keep retention on RAM section S5 when RAM section is
·		5511212111011						switched off
			On	1				On
W	W	S6RETENTION						Keep retention on RAM section S6 when RAM section is
								switched off
,,		CARETENIA	On	1				On
Х	W	S7RETENTION						Keep retention on RAM section S7 when RAM section is switched off
			On	1				On
Υ	W	S8RETENTION		-				Keep retention on RAM section S8 when RAM section is
								switched off
			On	1				On
Z	W	S9RETENTION						Keep retention on RAM section S9 when RAM section is
								switched off
2	14/	SIGNETENTION	On	1				On Keen retention on PAM section S10 when PAM section is
а	W	S10RETENTION						Keep retention on RAM section S10 when RAM section is switched off
			On	1				On
b	W	S11RETENTION						Keep retention on RAM section S11 when RAM section is
								switched off
			On	1				On
С	W	S12RETENTION						Keep retention on RAM section S12 when RAM section is
			On	1				switched off
			On	1				On



Bitı	numbe	er		31	. 30	29	28	27	26	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4 3	3 2	1	0
Id				f	е	d	С	b	а	Z	Y	Х	W	٧	U	Т	S	R	Q	Р	О	Ν 1	ΛL	. K	J	1	Н	G	F	Е [С	В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1 1	. 1	1	1	1	1	1	1 1	l 1	1	1
Id	RW	Field	Value Id	Va	lue							D	escri	iptio	on																		
d	W	S13RETENTION										Κe	еері	rete	ntio	on c	on F	RAN	1 se	ctic	on S	13 ر	vhe	n RA	M s	ecti	on	is					
												sv	vitch	ned	off																		
			On	1								O	n																				
е	W	S14RETENTION										Κe	еері	rete	ntio	on c	on F	RAN	1 se	ctic	on S	14 v	vhe	n RA	M s	ecti	on	is					
												sv	vitch	ned	off																		
			On	1								O	n																				
f	W	S15RETENTION										Κe	еері	rete	ntio	on c	on F	RAN	1 se	ctic	on S	ا 15	vhe	n RA	M s	ecti	on	is					
												sv	vitch	ned	off																		
			On	1								O	n																				

16.9.24 RAM[3].POWERCLR

Address offset: 0x938

RAM3 power control clear register

Bit n	umbe	er		31 30	29 2	8 27	7 26	25 24	1 23	3 22 2	1 2	0 1	9 1	3 17	7 16	15	14	13	12 1	11 10	9	8	7	6	5 4	1 3	2	1
Id				f e	d (c b	а	Z Y	Χ	W V	/ ι	J	ΓS	R	Q	Р	О	N	М	L K	J	1	Н	G	F E	D	С	В
Rese	t 0x0	000FFFF		0 0	0 (0 0	0	0 0	0	0 0) (0	0	0	0	1	1	1	1	1 1	1	1	1	1	1 1	l 1	1	1
Id	RW	Field	Value Id	Value	<u>:</u>				De	escript	tior	ı																
Α	W	SOPOWER							Ke	ep RA	M	sec	tion	S0	of F	RAM	3 о	n oı	off	in Sy	ste	m O	N m	ode	:			
			Off	1					Of	ff																		
В	W	S1POWER							Ke	ep RA	M	sec	tion	S1	of F	RAM	3 o	n oı	off	in Sy	ste	m O	N m	ode	•			
			Off	1					Of	ff																		
С	W	S2POWER								ep RA	M	sec	tion	S2	of F	RAM	3 o	n oı	off	in Sy	ste	m O	N m	ode				
			Off	1					Of						_													
D	W	S3POWER								eep RA	M	sec	tion	S 3	of F	RAM	13 o	n oı	off	in Sy	/ste	m O	N m	ode	:			
_		CAROLLER	Off	1					Of													_						
E	W	S4POWER	Off	1					Ke Of	eep RA	AIVI	sec	tion	54	OT F	KAIV	3 0	n oı	оп	ın Sy	/ste	m O	N M	oae	:			
F	W	S5POWER	Oli							eep RA	M	sec	tion	\$5	of F	εΔΙΛ	13 n	n nı	off	in Sv	ıste	m O	Nm	ode				
•	••	331 OWER	Off	1					Of			300		33	0		50	0.	011	5,	Jec	0		ouc				
G	W	S6POWER								ep RA	M	sec	tion	S6	of F	RAM	3 o	n oı	off	in Sy	/ste	m O	N m	ode				
			Off	1					Of	ff										·								
Н	W	S7POWER							Ke	ep RA	M	sec	tion	S7	of F	RAM	3 o	n oı	off	in Sy	ste	m O	N m	ode	:			
			Off	1					Of	ff																		
I	W	S8POWER							Ke	ep RA	M	sec	tion	S8	of F	RAM	3 о	n oı	off	in Sy	ste	m O	N m	ode	:			
			Off	1					Of	ff																		
J	W	S9POWER								ep RA	M	sec	tion	S 9	of F	RAM	3 o	n oı	off	in Sy	ste	m O	N m	ode	:			
			Off	1					Of	ff																		
K	W	S10POWER								ep RA	M	sec	tion	S1(0 of	RAI	M3	on o	or of	f in S	Syst	em () NC	noc	le			
		2440.000	Off	1					Of											·								
L	W	S11POWER	Off	1					Ke Of	eep RA	AIVI	sec	tion	511	T Of	KAI	VI3	on o	or of	T IN S	yst	em (ו אכ	noc	ie			
N 4	14/	C12DOWED	Oπ	1									+:	C11	2 of	DAI	.42			f : (a ma 1	- NI -		la.			
M	W	S12POWER	Off	1					Of	eep RA ff	AIVI	3 C C	นบท	314	∠ Uſ	nΑl	VI3	UII (וט וע	1 111 3	yst	e111 (ו מוכ	1100	ie			
N	W	S13POWER	<u></u>							ep RA	M	sec	tion	S13	3 of	RAI	VI3	on (or of	f in ^c	Svst	em (י מכ	mod	le			
			Off	1					Of				,								,50							
О	W	S14POWER								ep RA	M	sec	tion	S14	4 of	RAI	M3	on o	or of	f in S	Syst	em (ON I	noc	le			
			Off	1					Of	ff																		
Р	W	S15POWER							Ke	ep RA	M	sec	tion	S15	5 of	RAI	M3	on o	or of	f in S	Syst	em () NC	noc	le			
			Off	1					Of	ff																		
Q	W	SORETENTION							Ke	ep ret	ten	tior	n on	RA	M s	ecti	on S	50 v	vher	RAN	vi se	ctio	n is					
									SW	vitche	d o	ff																



Bit	numb	er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					/XWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x0	0000FFFF			0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
			Off	1	Off
R	W	S1RETENTION			Keep retention on RAM section S1 when RAM section is
					switched off
			Off	1	Off
S	W	S2RETENTION			Keep retention on RAM section S2 when RAM section is
					switched off
_			Off	1	Off
Т	W	S3RETENTION			Keep retention on RAM section S3 when RAM section is
			Off	1	switched off Off
U	W	S4RETENTION	Oli	1	Keep retention on RAM section S4 when RAM section is
					switched off
			Off	1	Off
٧	W	SSRETENTION			Keep retention on RAM section S5 when RAM section is
					switched off
			Off	1	Off
W	W	S6RETENTION			Keep retention on RAM section S6 when RAM section is
					switched off
			Off	1	Off
Х	W	S7RETENTION			Keep retention on RAM section S7 when RAM section is
			Off	1	switched off Off
Υ	W	S8RETENTION	OII	1	Keep retention on RAM section S8 when RAM section is
'	VV	SORETENTION			switched off
			Off	1	Off
Z	W	S9RETENTION			Keep retention on RAM section S9 when RAM section is
					switched off
			Off	1	Off
a	W	S10RETENTION			Keep retention on RAM section S10 when RAM section is
					switched off
			Off	1	Off
b	W	S11RETENTION			Keep retention on RAM section S11 when RAM section is
			Off	1	switched off
С	W	S12RETENTION	Off	1	Off Keep retention on RAM section S12 when RAM section is
·	vV	SIZICILIVIION			switched off
			Off	1	Off
d	W	S13RETENTION			Keep retention on RAM section S13 when RAM section is
					switched off
			Off	1	Off
е	W	S14RETENTION			Keep retention on RAM section S14 when RAM section is
					switched off
			Off	1	Off
f	W	S15RETENTION			Keep retention on RAM section S15 when RAM section is
			011		switched off
			Off	1	Off

16.9.25 RAM[4].POWER

Address offset: 0x940

RAM4 power control register



Bit numbe	r		31 30 29 28 2	27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			f e d c	b a Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00	000FFFF		0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
	Field	Value Id	Value		Description
A RW	SOPOWER				RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode.
		Off	0		Off
		On	1		On
B RW	S1POWER	Off On	0 1		Reep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off On
C RW	S2POWER				Keep RAM section S2 ON or OFF in System ON mode.
		Off On	0 1		RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION. All RAM sections will be OFF in System OFF mode. Off On
D RW	S3POWER				Keep RAM section S3 ON or OFF in System ON mode.
		Off On	0		RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off On
E RW	S4POWER				Keep RAM section S4 ON or OFF in System ON mode.
		Off On	0 1		RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off On
F RW	S5POWER				Keep RAM section S5 ON or OFF in System ON mode.
		Off On	0		RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SSRETENTION. All RAM sections will be OFF in System OFF mode. Off On
G RW	S6POWER				Keep RAM section S6 ON or OFF in System ON mode.
		Off On	0		RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S6RETENTION. All RAM sections will be OFF in System OFF mode. Off On
H RW	S7POWER				Keep RAM section S7 ON or OFF in System ON mode.
		Off On	0		RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION. All RAM sections will be OFF in System OFF mode. Off On
I RW	S8POWER				Keep RAM section S8 ON or OFF in System ON mode.



	number			4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld D	-+ 0-00005555			X W V U T S R Q P O N M L K J I H G F E D C B A
Id	et 0x0000FFFF RW Field	Value Id	Value	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
		Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. Off
J	RW S9POWER	On	1	On Keep RAM section S9 ON or OFF in System ON mode.
•	NW 337 GWEN	Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. Off
		On	1	On
К	RW S10POWER	Off	0	RAM sections 310 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. Off
	RW S11POWER	On	1	On Keep RAM section S11 ON or OFF in System ON mode.
_	NW 31170WEN	Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S11RETENTION. All RAM sections will be OFF in System OFF mode. Off On
М	RW S12POWER	Oli	1	Keep RAM section S12 ON or OFF in System ON mode.
		Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. Off
N	RW S13POWER	On	1	On Keep RAM section S13 ON or OFF in System ON mode.
		Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode. Off On
0	RW S14POWER			Keep RAM section S14 ON or OFF in System ON mode.
		Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S14RETENTION. All RAM sections will be OFF in System OFF mode. Off On
P	RW S15POWER	Off	0	Keep RAM section S15 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF mode. Off



Bit r	numbe	er		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id					2 Y X W V U T S R Q P O N M L K J I H G F E D C B
	et 0x0	000FFFF			0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
			On	1	On
Q	RW	SORETENTION			Keep retention on RAM section SO when RAM section is in OFF
			Off	0	Off
			On	1	On
R	RW	S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
			Off	0	Off
			On	1	On
S	RW	S2RETENTION			Keep retention on RAM section S2 when RAM section is in OFF
			Off	0	Off
			On	1	On
Т	RW	S3RETENTION			Keep retention on RAM section S3 when RAM section is in OFF
			Off	0	Off
			On	1	On
U	RW	S4RETENTION			Keep retention on RAM section S4 when RAM section is in OFF
			Off	0	Off
			On	1	On
V	RW	SSRETENTION			Keep retention on RAM section S5 when RAM section is in OFF
			Off	0	Off
			On	1	On
W	RW	S6RETENTION			Keep retention on RAM section S6 when RAM section is in OFF
			Off	0	Off
			On	1	On
Χ	RW	S7RETENTION			Keep retention on RAM section S7 when RAM section is in OFF
			Off	0	Off
			On	1	On
Υ	RW	S8RETENTION			Keep retention on RAM section S8 when RAM section is in OFF
			Off	0	Off
			On	1	On
Z	RW	S9RETENTION			Keep retention on RAM section S9 when RAM section is in OFF
			Off	0	Off
			On	1	On
a	RW	S10RETENTION			Keep retention on RAM section S10 when RAM section is in OFF
			Off	0	Off
			On	1	On
b	RW	S11RETENTION			Keep retention on RAM section S11 when RAM section is in OFF
			Off	0	Off
			On	1	On
С	RW	S12RETENTION			Keep retention on RAM section S12 when RAM section is in OFF
			Off	0	Off
			On	1	On
d	RW	S13RETENTION			Keep retention on RAM section S13 when RAM section is in OFF
			Off	0	Off
			On	1	On
e	RW	S14RETENTION			Keep retention on RAM section S14 when RAM section is in OFF
			Off	0	Off
			On	1	On
f	RW	S15RETENTION			Keep retention on RAM section S15 when RAM section is in OFF
			Off	0	Off
			On	1	On

16.9.26 RAM[4].POWERSET

Address offset: 0x944

RAM4 power control set register



Bit r	numbe	er			5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
	et Ox0	0000FFFF			0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	W	SOPOWER			Keep RAM section S0 of RAM4 on or off in System ON mode
			On	1	On
В	W	S1POWER			Keep RAM section S1 of RAM4 on or off in System ON mode
			On	1	On
С	W	S2POWER			Keep RAM section S2 of RAM4 on or off in System ON mode
_		COROLLER	On	1	On "Control of Control
D	W	S3POWER	On	1	Keep RAM section S3 of RAM4 on or off in System ON mode
E	w	S4POWER	OII	1	On Keep RAM section S4 of RAM4 on or off in System ON mode
-	••	341 OWEN	On	1	On
F	W	S5POWER			Keep RAM section S5 of RAM4 on or off in System ON mode
			On	1	On
G	W	S6POWER			Keep RAM section S6 of RAM4 on or off in System ON mode
			On	1	On
Н	W	S7POWER			Keep RAM section S7 of RAM4 on or off in System ON mode
			On	1	On
I	W	S8POWER			Keep RAM section S8 of RAM4 on or off in System ON mode
			On	1	On
J	W	S9POWER			Keep RAM section S9 of RAM4 on or off in System ON mode
K	W	S10POWER	On	1	On Voor DAM section C10 of DAMA on or off in Custom ON mode
K	VV	STOPOWER	On	1	Keep RAM section S10 of RAM4 on or off in System ON mode On
L	W	S11POWER	- Cil	•	Keep RAM section S11 of RAM4 on or off in System ON mode
			On	1	On
М	W	S12POWER			Keep RAM section S12 of RAM4 on or off in System ON mode
			On	1	On
N	W	S13POWER			Keep RAM section S13 of RAM4 on or off in System ON mode
			On	1	On
0	W	S14POWER			Keep RAM section S14 of RAM4 on or off in System ON mode
			On	1	On
Р	W	S15POWER			Keep RAM section S15 of RAM4 on or off in System ON mode
0	\A/	CODETENTION	On	1	On Keen retention on DAM section CO when DAM section is
Q	W	SORETENTION			Keep retention on RAM section SO when RAM section is switched off
			On	1	On
R	W	S1RETENTION	- Cil	•	Keep retention on RAM section S1 when RAM section is
					switched off
			On	1	On
S	W	S2RETENTION			Keep retention on RAM section S2 when RAM section is
					switched off
			On	1	On
Т	W	S3RETENTION			Keep retention on RAM section S3 when RAM section is
					switched off
		CARETENTION	On	1	On Control of the Con
U	W	S4RETENTION			Keep retention on RAM section S4 when RAM section is
			On	1	switched off On
V	W	S5RETENTION	OII	1	On Keep retention on RAM section S5 when RAM section is
•	,,	232.2			switched off
			On	1	On
W	W	S6RETENTION			Keep retention on RAM section S6 when RAM section is
					switched off
			On	1	On



Bit r	numb	er		31	30	29 2	28 2	7 26	5 25	5 24	2	3 22 21 20	19	18 17	7 16	15	14	13	12 :	11 10	9	8	7	6	5	4	3	2 :	1 0
Id				f	е	d	c l	b a	Z	<u>'</u> Y)	W V U	Т	S R	Q	P	0	N	M	L K	J	1	Н	G	F	Ε	D	C E	3 A
Res	et 0x0	0000FFFF		0	0	0	0 (0 0	0	0	(0 0 0	0	0 0	0	1	1	1	1	1 1	1	1	1	1	1	1	1	1 1	l 1
Id	RW	Field	Value Id	Va	lue						D	escription																	
X	W	S7RETENTION	On	1							S	eep retention witched off n		n RA	ιM s	ecti	on S	57 w	her	n RAI	VI se	ectic	n is	•					
Υ	W	S8RETENTION	On	1							S	eep retention witched off n		n RA	M s	ecti	on S	8 w	her	n RAI	VI se	ectic	n is	•					
Z	W	S9RETENTION	On	1							S	eep retention witched off n		n RA	M s	ecti	on S	9 w	her	n RAI	VI se	ectic	n is	•					
a	W	S10RETENTION	On	1							S	eep retentio witched off n		n RA	M s	ecti	on S	10 ·	whe	en RA	AM s	sect	ion	is					
b	W	S11RETENTION	On	1							S	eep retention witched off		n RA	ιM s	ecti	on S	11	whe	en RA	AM s	sect	ion	is					
С	W	S12RETENTION	On	1							S	eep retention witched off		n RA	M s	ecti	on S	12	whe	en RA	AM s	sect	ion	is					
d	W	S13RETENTION	On	1							S	eep retention witched off		n RA	ιM s	ecti	on S	13	whe	en RA	AM s	sect	ion	is					
е	W	S14RETENTION	On	1							S	eep retention witched off		n RA	M s	ecti	on S	14	whe	en RA	AM s	sect	ion	is					
f	W	S15RETENTION	On	1							K	eep retention witched off		n RA	M s	ecti	on S	15	whe	en RA	AM s	sect	ion	is					

16.9.27 RAM[4].POWERCLR

Address offset: 0x948

RAM4 power control clear register

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23 :	22 2	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 -	4 3	2	1	0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	V	U	Т	S	R	Q	Р	О	N	М	L	K	J	1	Н	G	F	E D	С	В	Α
Res	et OxO	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	otic	on																			
Α	W	SOPOWER										Kee	p R	ΑN	1 se	cti	on !	S0 (of R	kΑN	14 c	n c	r of	ff in	Sys	ster	n O	N m	ode	e				
			Off	1								Off																						
В	W	S1POWER										Kee	p R	ΑN	1 se	cti	on !	S1 (of R	kΑN	14 c	n c	r of	ff in	Sys	ster	n O	N m	ode	9				
			Off	1								Off																						
С	W	S2POWER										Kee	p R	ΑN	1 se	cti	on !	S2 (of R	kΑN	14 c	n c	r of	ff in	Sys	ster	n O	N m	ode	e				
			Off	1								Off																						
D	W	S3POWER										Kee	p R	ΑN	1 se	cti	on !	S3 (of R	kΑN	14 c	n c	r of	ff in	Sys	ster	n O	N m	ode	9				
			Off	1								Off																						
E	W	S4POWER										Kee	p R	ΑN	1 se	cti	on S	S4 (of R	ΑN	14 c	n c	r of	ff in	Sys	ster	n O	N m	ode	9				
			Off	1								Off																						
F	W	S5POWER										Kee	p R	ΑN	1 se	cti	on !	S5 (of R	ΑN	14 c	n c	r of	ff in	Sys	ster	n O	N m	ode	9				
			Off	1								Off																						
G	W	S6POWER										Kee	p R	ΑN	1 se	cti	on !	S6 (of R	kΑN	14 c	n c	r of	ff in	Sys	ster	n O	N m	ode	9				
			Off	1								Off																						
Н	W	S7POWER										Kee	p R	ΑN	1 se	cti	on !	S7 (of R	AN	14 c	n c	r of	ff in	Sys	ster	n O	N m	ode	9				
			Off	1								Off																						



Bit r	numbe	er		31 30	29 28 2	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								X W V U T S R Q P O N M L K J I H G F E D C B A
		000FFFF			0 0	0 0	0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW W	Field S8POWER	Value Id	Value				Description Keep RAM section S8 of RAM4 on or off in System ON mode
•	VV	SOFOWER	Off	1				Off
J	W	S9POWER						Keep RAM section S9 of RAM4 on or off in System ON mode
			Off	1				Off
K	W	S10POWER						Keep RAM section S10 of RAM4 on or off in System ON mode
			Off	1				Off
L	W	S11POWER	Off	1				Keep RAM section S11 of RAM4 on or off in System ON mode
М	w	S12POWER	Oil	1				Off Keep RAM section S12 of RAM4 on or off in System ON mode
			Off	1				Off
N	W	S13POWER						Keep RAM section S13 of RAM4 on or off in System ON mode
			Off	1				Off
0	W	S14POWER						Keep RAM section S14 of RAM4 on or off in System ON mode
-		CAEDOWED	Off	1				Off
Р	W	S15POWER	Off	1				Keep RAM section S15 of RAM4 on or off in System ON mode Off
Q	W	SORETENTION	Oli	1				Keep retention on RAM section SO when RAM section is
-								switched off
			Off	1				Off
R	W	S1RETENTION						Keep retention on RAM section S1 when RAM section is
								switched off
	14/	CARETENTION	Off	1				Off
S	W	S2RETENTION						Keep retention on RAM section S2 when RAM section is switched off
			Off	1				Off
Т	W	S3RETENTION						Keep retention on RAM section S3 when RAM section is
								switched off
			Off	1				Off
U	W	S4RETENTION						Keep retention on RAM section S4 when RAM section is
			Off	1				switched off Off
V	W	SSRETENTION	Oli	_				Keep retention on RAM section S5 when RAM section is
								switched off
			Off	1				Off
W	W	S6RETENTION						Keep retention on RAM section S6 when RAM section is
								switched off
V	14/	CZDETENTION	Off	1				Off
Χ	W	S7RETENTION						Keep retention on RAM section S7 when RAM section is switched off
			Off	1				Off
Υ	W	S8RETENTION						Keep retention on RAM section S8 when RAM section is
								switched off
			Off	1				Off
Z	W	S9RETENTION						Keep retention on RAM section S9 when RAM section is
			Off	1				switched off Off
a	w	S10RETENTION	Oil	1				Keep retention on RAM section S10 when RAM section is
-								switched off
			Off	1				Off
b	W	S11RETENTION						Keep retention on RAM section S11 when RAM section is
								switched off
	147	C12DETENTION	Off	1				Off Voor retention on PAM section \$12 when PAM section is
С	W	S12RETENTION						Keep retention on RAM section S12 when RAM section is switched off
			Off	1				Off



Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22 2	21	20	19	18	17	16	15	14 :	13 1	.2 1	1 10) S	9 8	8 7	6	5	4	3	2 :	1 0
Id				f	е	d	С	b	а	Z	Υ	Х	W	٧	U	Т	S	R	Q	Р	0	1 N	VI	_ K	J		I F	G	F	Ε	D	C E	ВА
Rese	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1 :	l 1	. 1	ι :	1 1	1	1	1	1	1 1	1 1
Id	RW	Field	Value Id	Va	lue							De	scrip	otic	on																		
d	W	S13RETENTION											ep re			n c	on F	RAN	l se	ctic	n S	13 ر	vhe	n RA	٩M	se	ctio	ı is					
			Off	1								sw Off	itche f	ed	off																		
е	W	S14RETENTION											ep re			n c	on F	RAN	l se	ctic	n S	14 v	vhe	n RA	٩M	se	ctio	n is					
												SW	itche	ed	off																		
			Off	1								Off	f																				
f	W	S15RETENTION										Ke	ep re	ete	ntic	n c	on F	RAN	1 se	ctic	n S	15 ر	vhe	n RA	٩M	se	ctio	ı is					
												sw	itche	ed	off																		
			Off	1								Off	f																				

16.9.28 RAM[5].POWER

Address offset: 0x950

RAM5 power control register

Bit number			31 3	0 29	9 28 :	27 26	5 25 2	24 2	23 22	21	20	19	18	17 1	16	15 1	4 1	3 12	2 11	10	9	8	7 6	5	4	3	2	1
Id			f e	e d	С	b a	Z	Υ)	x w	٧	U	Т	S	R	Q	Р (1 C	N N	1 L	K	J	I E	1 0	i F	Ε	D	C I	В
Reset 0x0000	OFFFF		0 (0	0	0 0	0	0 (0 0	0	0	0	0	0	0	1 :	1 :	1 1	. 1	1	1	1 :	1 1	. 1	1	1	1	1
ld RW Fid	eld	Value Id	Valu	e				C	Descr	iptio	on																	
A RW SO	POWER							K	Сеер	RAN	∕l se	ectic	on S	60 O	Νo	r OF	F ir	n Sys	sten	n ON	l mo	ode.						
								R	RAM :	sect	ion	s ar	e al	lway	s r	etair	ned	whe	en C	N, b	out o	can a	also	be				
								r	etain	ed v	whe	en O	FF	dep	end	dent	on	the	sett	ings	in	SORE	ETEN	NTIC	N.			
								Δ	All RA	M s	ect	ions	s wi	II be	01	FF in	Sy	sten	n OF	F mo	ode							
		Off	0					C	Off																			
		On	1					C	On																			
B RW S1	LPOWER							K	Сеер	RAN	∕l se	ectic	on S	51 0	N o	or OF	F ir	n Sys	sten	n ON	l mo	ode.						
								R	RAM :	sect	ion	s ar	e al	lway	s r	etair	ned	whe	en C	N, b	out (can a	also	be				
								r	etain	ed v	whe	en O	FF	dep	end	dent	on	the	sett	ings	in	S1RE	ETEN	NTIC	N.			
								Δ	All RA	M s	ect	ions	wi	II be	01	FF in	Sy	sten	n OF	F mo	ode							
		Off	0					C	Off																			
		On	1					C	On																			
C RW S2	POWER							K	Сеер	RAN	∕l se	ectic	on S	S2 O	N o	or OF	F ir	n Sys	sten	n ON	l mo	ode.						
								R	RAM :	sect	ion	s ar	e al	lway	s r	etair	ned	wh	en C	N, b	out (can a	also	be				
								r	etain	ed v	whe	en O	FF	dep	end	dent	on	the	sett	ings	in	S2RE	ETE	NTIC	N.			
								Δ	All RA	M s	ect	ions	s wi	II be	OI	FF in	Sy	sten	n OF	F mo	ode							
		Off	0					C	Off																			
		On	1						On																			
D RW S3	BPOWER							K	Сеер	RAN	∕l se	ectic	on S	3 0	N o	or OF	F ir	n Sys	sten	n ON	l mo	ode.						
								R	RAM :	sect	ion	s ar	e al	lway	s r	etair	ned	wh	en C	N, b	out (can a	also	be				
								r	etain	ed v	whe	en O	FF	dep	end	dent	on	the	sett	ings	in :	S3RE	ETE	NTIC	N.			
									All RA	M s	ect	ions	s wi	II be	Ol	FF in	Sy	sten	n OF	F mo	ode							
		Off	0					C	Off																			
		On	1						On																			
E RW S4	1POWER							K	(eep	RAN	∕l se	ectic	on S	64 0	N o	or OF	F ir	n Sys	sten	i ON	l mo	ode.						
								R	RAM :	sect	ion	s ar	e al	lway	s r	etaiı	ned	wh	en C	N, b	ut (can a	also	be				
								r	etain	ed v	whe	en O)FF	dep	end	dent	on	the	sett	ings	in :	S4RE	ETE	NTIC	N.			
									All RA	M s	ect	ions	s wi	II be	OI	FF in	Sy	sten	n OF	F mo	ode							
		Off	0						Off																			
	-0014/50	On	1						On ,								. . .			٠								
F RW S5	SPOWER							K	Сеер	KΑÑ	VI SE	ectic	on S	5 0	N o	or OF	-F ir	n Sys	sten	i ON	I mo	ode.						
								R	RAM :	sect	ion	s ar	e al	lway	s r	etair	ned	whe	en C	N, b	out (can a	also	be				
									etain											_			ETE	NTIC	N.			
								Δ	All RA	M s	ect	ions	wi	II be	OI	FF in	Sy	sten	n OF	F mo	ode							



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZY	XWVUTSRQPONMLKJIHGFEDCBA
Reset 0x0000FFFF			0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value	Description Off
	Off On	0	Off On
G RW S6POWER	3 11	-	Keep RAM section S6 ON or OFF in System ON mode.
	Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SGRETENTION. All RAM sections will be OFF in System OFF mode. Off
	On	1	On
H RW S7POWER	Off	0	Keep RAM section S7 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION. All RAM sections will be OFF in System OFF mode. Off
	On	1	On
I RW S8POWER	Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. Off On
J RW S9POWER			Keep RAM section S9 ON or OFF in System ON mode.
	Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. Off
K RW S10POWER	On	1	On Keen BAM section \$10 ON or OFF in System ON mode
K RW S10POWER	Off	0	RAM section S10 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. Off
	On	1	On
L RW S11POWER	Off On	0 1	Keep RAM section S11 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S11RETENTION. All RAM sections will be OFF in System OFF mode. Off On
M RW S12POWER			Keep RAM section S12 ON or OFF in System ON mode.
	Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. Off On
N RW S13POWER	·		Keep RAM section S13 ON or OFF in System ON mode.
			RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode.



Bit r	numbe	r		31 30	29 2	28 27	7 26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d	c b	a	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	000FFFF		0 0	0 (0 0	0	0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 1 \ 1 \ $
ld	RW	Field	Value Id	Value	:				Description
			Off	0					Off
			On	1					On
0	RW	S14POWER							Keep RAM section S14 ON or OFF in System ON mode.
									RAM sections are always retained when ON, but can
									also be retained when OFF dependent on the settings in
									S14RETENTION. All RAM sections will be OFF in System OFF
									mode.
			Off	0					Off
			On	1					On
P	RW	S15POWER							Keep RAM section S15 ON or OFF in System ON mode.
									RAM sections are always retained when ON, but can
									also be retained when OFF dependent on the settings in
									S15RETENTION. All RAM sections will be OFF in System OFF
									mode.
			Off	0					Off
			On	1					On
Q	RW	SORETENTION							Keep retention on RAM section SO when RAM section is in OFF
			Off	0					Off
			On	1					On
R	RW	S1RETENTION							Keep retention on RAM section S1 when RAM section is in OFF
			Off	0					Off
			On	1					On
S	RW	S2RETENTION							Keep retention on RAM section S2 when RAM section is in OFF
			Off	0					Off
_	DVA	CORFTENTION	On	1					On
Т	KW	S3RETENTION	Off	0					Keep retention on RAM section S3 when RAM section is in OFF Off
			On	1					On
U	R\M/	S4RETENTION	Oll	1					Keep retention on RAM section S4 when RAM section is in OFF
Ü	1100	3-KETEIVIIOIV	Off	0					Off
			On	1					On
٧	RW	S5RETENTION							Keep retention on RAM section S5 when RAM section is in OFF
			Off	0					Off
			On	1					On
W	RW	S6RETENTION							Keep retention on RAM section S6 when RAM section is in OFF
			Off	0					Off
			On	1					On
Χ	RW	S7RETENTION							Keep retention on RAM section S7 when RAM section is in OFF
			Off	0					Off
			On	1					On
Υ	RW	S8RETENTION							Keep retention on RAM section S8 when RAM section is in OFF
			Off	0					Off
-	D	CODETENTION	On	1					On
Z	RW	S9RETENTION	0#	0					Keep retention on RAM section S9 when RAM section is in OFF
			Off	0					Off
2	D/V/	S10RETENTION	On	1					On Keen retention on RAM section \$10 when RAM section is in OFF
a	IVVV	J-ONE I LINTION	Off	0					Keep retention on RAM section S10 when RAM section is in OFF Off
			On	1					On
b	RW	S11RETENTION		•					Keep retention on RAM section S11 when RAM section is in OFF
~			Off	0					Off
			On	1					On
С	RW	S12RETENTION							Keep retention on RAM section S12 when RAM section is in OFF
			Off	0					Off



Bit r	numbe	r		31	30	29	28 2	27 :	26 2	25 2	4 2	3 22	21	20	19	18	17	16	15 :	14 1	.3 12	2 11	10	9	8	7 (6 5	4	3	2 :	1 0
Id				f	e	d	С	b	а	Z '	Y X	W	٧	U	Т	S	R	Q	Р	0 1	N M	l L	K	J	1 1	4 (3 F	Ε	D	C E	3 A
Res	et 0x0	000FFFF		0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	1	1	1 1	1	1	1	1	1 :	1 1	. 1	1	1 1	l 1
Id	RW	Field	Value Id	Val	lue						D	escri	iptio	on																	
			On	1							0	n																			
d	RW	S13RETENTION									K	еер	rete	entic	on c	on R	RAN	l se	ctio	n S:	L3 w	hen	RAI	VI s	ectic	n is	in	OFF			
			Off	0							0	ff																			
			On	1							0	n																			
e	RW	S14RETENTION									K	еер	rete	ntio	on c	n F	RAN	1 se	ctio	n S	L4 w	hen	RAI	VI s	ectio	n is	in	OFF			
			Off	0							0	ff																			
			On	1							0	n																			
f	RW	S15RETENTION									K	еер	rete	entic	on c	on R	RAN	l se	ctio	n S:	L5 w	hen	RAI	VI s	ectic	n is	in	OFF			
			Off	0							0	ff																			
			On	1							0	n																			

16.9.29 RAM[5].POWERSET

Address offset: 0x954

RAM5 power control set register

Bit r	numb	er		3:	1 30	29	28 2	7 26	25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f	е	d	c b	а	ΖY	'X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et Ox(0000FFFF		0	0	0	0 0	0	0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	V	alue					Description
Α	W	SOPOWER								Keep RAM section SO of RAM5 on or off in System ON mode
			On	1						On
В	W	S1POWER								Keep RAM section S1 of RAM5 on or off in System ON mode
			On	1						On
С	W	S2POWER								Keep RAM section S2 of RAM5 on or off in System ON mode
			On	1						On
D	W	S3POWER								Keep RAM section S3 of RAM5 on or off in System ON mode
			On	1						On
Ε	W	S4POWER								Keep RAM section S4 of RAM5 on or off in System ON mode
			On	1						On
F	W	S5POWER								Keep RAM section S5 of RAM5 on or off in System ON mode
			On	1						On
G	W	S6POWER								Keep RAM section S6 of RAM5 on or off in System ON mode
			On	1						On
Н	W	S7POWER								Keep RAM section S7 of RAM5 on or off in System ON mode
			On	1						On
I	W	S8POWER								Keep RAM section S8 of RAM5 on or off in System ON mode
			On	1						On
J	W	S9POWER								Keep RAM section S9 of RAM5 on or off in System ON mode
			On	1						On
K	W	S10POWER								Keep RAM section S10 of RAM5 on or off in System ON mode
			On	1						On
L	W	S11POWER								Keep RAM section S11 of RAM5 on or off in System ON mode
			On	1						On
M	W	S12POWER	_							Keep RAM section S12 of RAM5 on or off in System ON mode
			On	1						On
N	W	S13POWER	_							Keep RAM section S13 of RAM5 on or off in System ON mode
			On	1						On Control of Control
0	W	S14POWER	_							Keep RAM section S14 of RAM5 on or off in System ON mode
			On	1						On
Р	W	S15POWER	_							Keep RAM section S15 of RAM5 on or off in System ON mode
			On	1						On



Bit r	numbe	er		31 30	29 28	27 26	25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id								Y X W V U T S R Q P O N M L K J I H G F E D C B
Res	et 0x0	000FFFF						0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value				Description
Q	W	SORETENTION	_	_				Keep retention on RAM section S0 when RAM section is switched off
	14/	CARETENTION	On	1				On
R	W	S1RETENTION	On	1				Keep retention on RAM section S1 when RAM section is switched off On
S	W	S2RETENTION						Keep retention on RAM section S2 when RAM section is switched off
			On	1				On
Т	W	S3RETENTION	On	1				Keep retention on RAM section S3 when RAM section is switched off On
U	W	S4RETENTION	On	1				Keep retention on RAM section S4 when RAM section is switched off On
V	W	SSRETENTION	On	1				Keep retention on RAM section S5 when RAM section is switched off On
W	W	S6RETENTION						Keep retention on RAM section S6 when RAM section is switched off
			On	1				On
X	W	S7RETENTION	On	1				Keep retention on RAM section S7 when RAM section is switched off On
Υ	W	S8RETENTION	On	1				Keep retention on RAM section S8 when RAM section is switched off On
Z	W	S9RETENTION						Keep retention on RAM section S9 when RAM section is switched off
a	W	S10RETENTION	On	1				On Keep retention on RAM section S10 when RAM section is switched off
			On	1				On
b	W	S11RETENTION	On	1				Keep retention on RAM section S11 when RAM section is switched off On
С	W	S12RETENTION	_					Keep retention on RAM section S12 when RAM section is switched off
d	W	S13RETENTION	On	1				On Keep retention on RAM section S13 when RAM section is switched off
			On	1				On
е	W	S14RETENTION	On	1				Keep retention on RAM section S14 when RAM section is switched off On
f	W	S15RETENTION	On	1				Keep retention on RAM section S15 when RAM section is switched off
			On	1				On

16.9.30 RAM[5].POWERCLR

Address offset: 0x958

RAM5 power control clear register



Bit r	numb	er		31 30 29	28 2	7 26 :	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e d	c b	а	Z Y	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Res	et 0x0	0000FFFF		0 0 0	0 0	0	0 0	0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
Id		Field	Value Id	Value				Description
Α	W	SOPOWER	Off	1				Keep RAM section SO of RAM5 on or off in System ON mode Off
В	W	S1POWER	Off	1				Keep RAM section S1 of RAM5 on or off in System ON mode Off
С	W	S2POWER	Off	1				Keep RAM section S2 of RAM5 on or off in System ON mode Off
D	W	S3POWER	Off	1				Keep RAM section S3 of RAM5 on or off in System ON mode Off
Ε	W	S4POWER	Off	1				Keep RAM section S4 of RAM5 on or off in System ON mode Off
F	W	S5POWER	Off	1				Keep RAM section S5 of RAM5 on or off in System ON mode Off
G	W	S6POWER	Off	1				Keep RAM section S6 of RAM5 on or off in System ON mode Off
Н	W	S7POWER	Off	1				Keep RAM section S7 of RAM5 on or off in System ON mode Off
I	W	S8POWER	Off	1				Keep RAM section S8 of RAM5 on or off in System ON mode Off
J	W	S9POWER	Off	1				Keep RAM section S9 of RAM5 on or off in System ON mode Off
K	W	S10POWER	Off					Keep RAM section S10 of RAM5 on or off in System ON mode Off
L	W	S11POWER		1				Keep RAM section S11 of RAM5 on or off in System ON mode
М	W	S12POWER	Off	1				Off Keep RAM section S12 of RAM5 on or off in System ON mode
N	W	S13POWER	Off	1				Off Keep RAM section S13 of RAM5 on or off in System ON mode
0	W	S14POWER	Off	1				Off Keep RAM section S14 of RAM5 on or off in System ON mode
Р	W	S15POWER	Off	1				Off Keep RAM section S15 of RAM5 on or off in System ON mode
Q	W	SORETENTION	Off	1				Off Keep retention on RAM section S0 when RAM section is
			Off	1				switched off Off
R	W	S1RETENTION						Keep retention on RAM section S1 when RAM section is switched off
			Off	1				Off
S	W	S2RETENTION	Off	1				Keep retention on RAM section S2 when RAM section is switched off Off
Т	W	S3RETENTION		1				Keep retention on RAM section S3 when RAM section is switched off
U	W	S4RETENTION	Off	1				Off Keep retention on RAM section S4 when RAM section is
			Off	1				switched off Off
V	W	SSRETENTION						Keep retention on RAM section S5 when RAM section is switched off
w	W	S6RETENTION	Off	1				Off Keep retention on RAM section S6 when RAM section is
			Off	1				switched off Off
Х	W	S7RETENTION						Keep retention on RAM section S7 when RAM section is switched off



Bit	numb	er		3:	1 30	29	28	27	26	25	24	23	3 22	2 21	. 20	19	18	17	16	15	14	13	12 1	.1 1	0 9	8	7	6	5	4	3 2	2 1	. 0
Id				f	е	d	С	b	а	Z	Υ	Х	W	/ V	U	Т	S	R	Q	Р	О	N	M	L k	(J	-1	Н	G	F	Е	D C	В	А
Res	et 0x0	0000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1 1	. 1	1	1	1	1	1	1 1	1	. 1
Id	RW	Field	Value Id	V	alue	е						D	escr	ripti	ion																		
			Off	1								O	ff																				
Υ	W	S8RETENTION										Ke	eep	ret	ent	ion	on	RAI	√l se	cti	on S	8 w	her	RA	M s	ecti	on is	5					
												sv	witcl	hed	off	f																	
			Off	1								O	ff																				
Z	W	S9RETENTION										Ke	еер	ret	ent	ion	on	RAI	√l se	cti	on S	9 w	her	RA	M s	ecti	on is	5					
												sv	witcl	hed	off	f																	
			Off	1								Of	ff																				
а	W	S10RETENTION										Ke	eep	ret	ent	ion	on	RAI	√l se	cti	on S	10	whe	n R	AΜ	sect	ion	is					
													witcl	hed	off	f																	
			Off	1								Of																					
b	W	S11RETENTION											eep				on	RAI	√l se	ecti	on S	11	whe	n R	AΜ	sect	ion	is					
													witcl	hed	off	f																	
			Off	1								Of																					
С	W	S12RETENTION											eep				on	RAI	√l se	ecti	on S	12	whe	n R	AΜ	sect	ion	is					
													witcl	hed	off	f																	
			Off	1								Of																					
d	W	S13RETENTION											eep				on	RAI	√l se	ecti	on S	13	whe	n R	AM	sect	ion	is					
			0.00										witcl	hed	off	ŀ																	
	144	C4 4DETENTION	Off	1								Of									_												
е	W	S14RETENTION											eep				on	KAI	VI S	ecti	on S	14	whe	n R	AM	sect	ion	IS					
			011										witcl	hed	off	ľ																	
£	14/	CAEDETENTION	Off	1								01		rot	o n.t.			D A *	1 -		C	1 [- طيب	. P	A B A		lar	ic					
Т	W	S15RETENTION											eep				on	KAľ	VI SE	cti	on S	15	wne	n K	AIVI	seci	ion	15					
			Off	1								SV	vitcl	nea	on																		
			OII	1								U	H																				

16.9.31 RAM[6].POWER

Address offset: 0x960

RAM6 power control register

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	1:	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4 3	3 2	1	0
Id				f	е	d	С	b	а	Z	Υ	Х	W١	V	U	Т	S	R	Q	Р	0	N	М	L	K	J	ī	Н	G	F	E C) С	В	Α
Res	et OxC	0000FFFF		0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1
Id	RW	Field	Value Id	Va	lue							De	scrip	tio	on																			
Α	RW	SOPOWER										Kee	ep RA	١M	1 se	ectio	on:	S0 (NC	or	OFF	in	Syst	em	ON	l m	ode							
												RA	M se	cti	ion:	s ar	e a	lwa	iys	ret	aine	ed v	vher	n 0	N, b	ut	can	als	o be	2				
												ret	ained	d w	vhe	en C	OFF	de	per	ıde	nt c	n t	he s	etti	ings	in	SOR	ETE	NT	ION	١.			
												All	RAM	l se	ecti	ions	s w	ill b	e C	FF	in S	syst	em	OFI	F m	ode	١.							
			Off	0								Off	f																					
			On	1								On																						
В	RW	S1POWER										Kee	ep RA	١M	1 se	ectio	on:	S1 (NC	or	OFF	in	Syst	em	ON	l m	ode							
												RA	M se	cti	ion	s ar	e a	lwa	ivs	ret	aine	n h	vher	n Ω	N h	nut	can	als	o be	2				
													aineo																		١.			
													RAM												_									
			Off	0								Off	f																					
			On	1								On																						
С	RW	S2POWER										Kee	ep RA	١M	1 se	ectio	on:	S2 (ON	or	OFF	in	Syst	em	ON	l m	ode							
												RΔ	M se	cti	ion	car		lsa/s	avc	rot:	aine	ad v	vhor	۰.	N h	ı ıt	can	alc	n he	_				
													aine																					
													RAM						•						_									
			Off	0								Off										,,,,												
			On	1								On																						
D	RW	S3POWER										Kee	ep RA	١M	1 se	ectio	on:	S3 (NC	or	OFF	in	Syst	em	ON	l m	ode.							
																							•											



Bit number			4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x0000FFFF Id RW Field	Value Id	Value	Description
	Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off On
E RW S4POWER			Keep RAM section S4 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode.
	Off On	0	Off On
F RW S5POWER	Off On	0	Keep RAM section S5 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S5RETENTION. All RAM sections will be OFF in System OFF mode. Off On
G RW S6POWER	Off On	0	Keep RAM section S6 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SGRETENTION. All RAM sections will be OFF in System OFF mode. Off On
H RW S7POWER	Off On	0	Keep RAM section S7 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION. All RAM sections will be OFF in System OFF mode. Off On
I RW S8POWER	Off On	0	Keep RAM section S8 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. Off On
J RW S9POWER	Off On	0 1	Keep RAM section S9 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. Off On
K RW S10POWER	Off	0	Keep RAM section S10 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. Off
L RW S11POWER	On	1	On Keep RAM section S11 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in



Bit r	numb	er		31 3	0 29	28 2	7 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x(0000FFFF		0 0	0	0 (0	0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 &$
Id	RW	Field	Value Id	Valu	e				Description
									S11RETENTION. All RAM sections will be OFF in System OFF
			Off	0					mode. Off
			On	1					On
М	RW	S12POWER	Oli	_					Keep RAM section S12 ON or OFF in System ON mode.
									RAM sections are always retained when ON, but can
									also be retained when OFF dependent on the settings in
									S12RETENTION. All RAM sections will be OFF in System OFF
									mode.
			Off	0					Off
			On	1					On
N	RW	S13POWER							Keep RAM section S13 ON or OFF in System ON mode.
									RAM sections are always retained when ON, but can
									also be retained when OFF dependent on the settings in
									S13RETENTION. All RAM sections will be OFF in System OFF
			Off	0					mode. Off
			On	1					On
0	RW	S14POWER							Keep RAM section S14 ON or OFF in System ON mode.
									RAM sections are always retained when ON, but can
									also be retained when OFF dependent on the settings in
									S14RETENTION. All RAM sections will be OFF in System OFF
									mode.
			Off	0					Off
_	5111		On	1					On
Р	RW	S15POWER							Keep RAM section S15 ON or OFF in System ON mode.
									RAM sections are always retained when ON, but can
									also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF
									mode.
			Off	0					Off
			On	1					On
Q	RW	SORETENTION							Keep retention on RAM section S0 when RAM section is in OFF
			Off	0					Off
P	DIA	CIDETENTION	On	1					On Keen retention on PAM section S1 when PAM section is in OFF
R	KW	S1RETENTION	Off	0					Keep retention on RAM section S1 when RAM section is in OFF Off
			On	1					On
S	RW	S2RETENTION							Keep retention on RAM section S2 when RAM section is in OFF
			Off	0					Off
			On	1					On
Т	RW	S3RETENTION	255						Keep retention on RAM section S3 when RAM section is in OFF
			Off	0					Off
U	R\M/	S4RETENTION	On	1					On Keep retention on RAM section S4 when RAM section is in OFF
-			Off	0					Off
			On	1					On
٧	RW	SSRETENTION							Keep retention on RAM section S5 when RAM section is in OFF
			Off	0					Off
			On	1					On
W	RW	S6RETENTION	Off	0					Keep retention on RAM section S6 when RAM section is in OFF
			Off On	0					Off On
			OII	1					OII



Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x0000FFFF		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1
ld	RW Field	Value Id	Value Description
Χ	RW S7RETENTION		Keep retention on RAM section S7 when RAM section is in OFF
		Off	0 Off
		On	1 On
Υ	RW S8RETENTION		Keep retention on RAM section S8 when RAM section is in OFF
		Off	0 Off
		On	1 On
Z	RW S9RETENTION		Keep retention on RAM section S9 when RAM section is in OFF
		Off	0 Off
		On	1 On
а	RW S10RETENTION		Keep retention on RAM section S10 when RAM section is in OFF
		Off	0 Off
		On	1 On
b	RW S11RETENTION		Keep retention on RAM section S11 when RAM section is in OFF
		Off	0 Off
		On	1 On
С	RW S12RETENTION		Keep retention on RAM section S12 when RAM section is in OFF
		Off	0 Off
		On	1 On
d	RW S13RETENTION		Keep retention on RAM section S13 when RAM section is in OFF
		Off	0 Off
		On	1 On
е	RW S14RETENTION		Keep retention on RAM section S14 when RAM section is in OFF
		Off	0 Off
		On	1 On
f	RW S15RETENTION		Keep retention on RAM section S15 when RAM section is in OFF
		Off	0 Off
		On	1 On

16.9.32 RAM[6].POWERSET

Address offset: 0x964

RAM6 power control set register

Bit r	numbe	er		31	30	29 :	28 2	27 :	26 2	25 :	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4 3	3 2	1	0
Id				f	e	d	С	b	a i	Z	Υ	Χ	W	٧	U	Т	S	R	Q	Р	0	N	М	L	K	J	1	Н	G	F	ЕΩ) C	В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1 :	l 1	1	1
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	on																			
Α	W	SOPOWER										Kee	p F	RAN	∕l se	ecti	on !	S0 (of R	ΑN	16 c	n c	or o	ff in	Sy	ster	n O	Νn	nod	e				
			On	1								On																						
В	W	S1POWER										Kee	p F	RAN	∕l se	ecti	on !	S1 (of R	ΑN	16 c	n c	r o	ff in	Sy	ster	n O	Νn	nod	e				
			On	1								On																						
С	W	S2POWER										Kee	p F	RAN	∕l se	ecti	on S	S2 (of R	ΑN	16 c	n c	or o	ff in	Sy	ster	n O	Νn	nod	e				
			On	1								On																						
D	W	S3POWER										Kee	p F	RAN	∕l se	ecti	on !	S3 (of R	AN	16 c	n c	r o	ff in	Sy	ster	n O	Νn	nod	e				
			On	1								On																						
Ε	W	S4POWER										Kee	p F	RAN	∕l se	ecti	on !	S4 (of R	ΑN	16 c	n c	r o	ff in	Sy	ster	n O	Νn	nod	e				
			On	1								On																						
F	W	S5POWER										Kee	p F	RAN	∕l se	ecti	on S	S5 (of R	ΑN	16 c	n c	or o	ff in	Sy	ster	n O	Νn	nod	e				
			On	1								On																						
G	W	S6POWER										Kee	p F	RAN	∕l se	ecti	on !	S6 (of R	ΑN	16 c	n c	r o	ff in	Sy	ster	n O	Νn	nod	e				
			On	1								On																						
Н	W	S7POWER										Kee	p F	RAN	∕l se	ecti	on !	S7 (of R	AN	16 c	n c	or o	ff in	Sy	ster	n O	N n	nod	e				
			On	1								On																						



Bit	numb	er		31 30	29 28 2	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
		0000FFFF			0 0	0 0	0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW W	Field S8POWER	Value Id	Value				Description Keep RAM section S8 of RAM6 on or off in System ON mode
'	VV	SOPOWER	On	1				On
J	W	S9POWER		_				Keep RAM section S9 of RAM6 on or off in System ON mode
			On	1				On
K	W	S10POWER						Keep RAM section S10 of RAM6 on or off in System ON mode
			On	1				On
L	W	S11POWER	On	1				Keep RAM section S11 of RAM6 on or off in System ON mode On
М	W	S12POWER						Keep RAM section S12 of RAM6 on or off in System ON mode
			On	1				On
N	W	S13POWER						Keep RAM section S13 of RAM6 on or off in System ON mode
			On	1				On
0	W	S14POWER						Keep RAM section S14 of RAM6 on or off in System ON mode
Р	W	S15POWER	On	1				On Keep RAM section S15 of RAM6 on or off in System ON mode
r	VV	SISFOWER	On	1				On
Q	W	SORETENTION						Keep retention on RAM section S0 when RAM section is
								switched off
			On	1				On
R	W	S1RETENTION						Keep retention on RAM section S1 when RAM section is
								switched off
S	W	S2RETENTION	On	1				On Keep retention on RAM section S2 when RAM section is
3	VV	SZKETENTION						switched off
			On	1				On
Т	W	S3RETENTION						Keep retention on RAM section S3 when RAM section is
								switched off
			On	1				On
U	W	S4RETENTION						Keep retention on RAM section S4 when RAM section is
			On	1				switched off On
V	W	S5RETENTION	Oli	1				Keep retention on RAM section S5 when RAM section is
								switched off
			On	1				On
W	W	S6RETENTION						Keep retention on RAM section S6 when RAM section is
								switched off
V	144	CADETENTION	On	1				On Voca retention on DAM section 57 when DAM section is
X	W	S7RETENTION						Keep retention on RAM section S7 when RAM section is switched off
			On	1				On
Υ	W	S8RETENTION						Keep retention on RAM section S8 when RAM section is
								switched off
			On	1				On
Z	W	S9RETENTION						Keep retention on RAM section S9 when RAM section is
			00	1				switched off
a	W	S10RETENTION	On	1				On Keep retention on RAM section S10 when RAM section is
u	٧٧	J20NETENTION						switched off
			On	1				On
b	W	S11RETENTION						Keep retention on RAM section S11 when RAM section is
								switched off
			On	1				On
С	W	S12RETENTION						Keep retention on RAM section S12 when RAM section is
			On	1				switched off On
			OII	1				OII



Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 1	2 1	1 1	0 9	8	7	6	5	4	3 2	2 1	0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U	Т	S	R	Q	Р	О	Ν 1	ΛI	_ k	J	- 1	Н	G	F	Ε	D (В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1 1	L 1	. 1	1	. 1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	lue							De	scrip	otic	on																		
d	W	S13RETENTION										Ke	ep r	ete	ntic	n c	on R	RAN	1 se	ctic	on S	13 ر	vhe	n R	٩M	sec	tior	is					
												sw	itch	ed (off																		
			On	1								On																					
е	W	S14RETENTION										Ke	ep re	ete	ntic	n c	on F	RAN	1 se	ctic	on S	14 v	vhe	n R	٩M	sec	tior	is					
												sw	itch	ed (off																		
			On	1								On																					
f	W	S15RETENTION										Ke	ep re	ete	ntic	n c	on R	RAN	1 se	ctic	on S	ا 15	vhe	n R	٩M	sec	tior	is					
												sw	itch	ed (off																		
			On	1								On																					

16.9.33 RAM[6].POWERCLR

Address offset: 0x968

RAM6 power control clear register

Bit r	numb	er		31 30	29 2	8 27	26	25 24	1 23 2	22 21	. 20	19	18	17	16 1	15 1	4 13	3 12	11	10	9	8	7 (5	4	3 2	! 1	0
Id				f e	d c	b	а	Z Y	Х١	w v	U	Т	S	R	Q	P C	N	М	L	K	J	1	Н	i F	Ε	D C	В	Α
Res	et 0x0	0000FFFF		0 0	0 0	0	0	0 0	0	0 0	0	0	0	0	0	1 1	. 1	1	1	1	1	1	1 :	. 1	1	1 1	. 1	1
Id	RW	Field	Value Id	Value	:				Des	cripti	on																	
Α	W	SOPOWER							Kee	p RAI	VI se	ecti	on S	50 o	f RA	M6	on (or o	ff in	Sys	ten	10 r	l mo	de				
			Off	1					Off																			
В	W	S1POWER							Kee	p RAI	VI se	ecti	on S	51 o	f RA	M6	on (or o	ff in	Sys	ten	10 r	l mo	de				
			Off	1					Off																			
С	W	S2POWER							Kee	p RAI	M se	ecti	on S	52 o	f RA	M6	on (or o	ff in	Sys	ten	10	l mo	de				
			Off	1					Off																			
D	W	S3POWER								p RAI	M se	ecti	on S	53 o	f RA	M6	on (or o	ff in	Sys	ten	10	l mo	de				
			Off	1					Off																			
E	W	S4POWER								p RAI	M se	ecti	on S	54 o	f RA	M6	on (or o	ff in	Sys	ten	1 ON	۱ m	de				
_		25001150	Off	1					Off					-					· ·	_								
F	W	S5POWER	0#	4						p RAI	VI S	ecti	on S	o5 0	t RA	MM6	on (or o	ff in	Sys	ten	ı Or	N mo	ode				
_	14/	CCDOWED	Off	1					Off	- DAI	14.5	o oti			f D A	NAC			ee :	Cur	+	. 01	Lma	. da				
G	W	S6POWER	Off	1					Off	p RAI	VI SE	ecu	011 3	0 0	I KA	NIVIO	OH	טו ט	11 111	Sys	ten	ı Or	N IIII	oue				
Н	W	S7POWER	Oli	1						p RAI	\/ c4	octi	on (57 o	fRΔ	M6	on (or o	ff in	Sve	ton	. ON	J m	ahr				
	**	371 OWER	Off	1					Off	PINAI	VI 30	ccii	011.	,, 0	1 11/-	NIVIO	OII	01 0		Jys	CCII	101	V 1110	,uc				
1	W	S8POWER	5	-						p RAI	VI se	ecti	on S	58 o	f RA	M6	on (or o	ff in	Svs	ten	10 r	l mo	de				
			Off	1					Off											,								
J	W	S9POWER							Kee	p RAI	VI se	ecti	on S	59 o	f RA	M6	on (or o	ff in	Sys	ten	10 r	l mo	de				
			Off	1					Off																			
K	W	S10POWER							Kee	p RAI	VI se	ecti	on S	510	of R	AM	5 on	or	off i	n Sy	/ste	m C	N n	ode				
			Off	1					Off																			
L	W	S11POWER							Kee	p RAI	M se	ecti	on S	511	of R	AM	5 on	or	off i	n Sy	/ste	m C	N n	ode				
			Off	1					Off																			
М	W	S12POWER							Kee	p RAI	M se	ecti	on S	512	of R	AM	5 on	or	off i	n Sy	/ste	m C	N n	ode				
			Off	1					Off																			
N	W	S13POWER								p RAI	VI se	ecti	on S	513	of R	AM	5 on	or	off i	n Sy	/ste	m C	N n	ode				
			Off	1					Off																			
0	W	S14POWER								p RAI	M se	ecti	on S	514	of R	AM	5 on	or	off i	n Sy	/ste	m C	N n	ode				
			Off	1					Off								_		••									
Р	W	S15POWER	0"							p RAI	VI S	ecti	on S	515	of R	MA	o on	or	otf i	n Sy	/ste	m C	N n	ode				
_	14/	CODETENTION	Off	1					Off																			
Q	W	SORETENTION								p rete			on I	ΚΑΙV	se	ctioi	1 50	whe	en R	AM	sec	TIOI	1 IS					
									swit	ched	ott																	



Bit r	iumbe	er		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				fedcba	Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et OxC	0000FFFF		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
			Off	1	Off
R	W	S1RETENTION			Keep retention on RAM section S1 when RAM section is
					switched off
			Off	1	Off
S	W	S2RETENTION			Keep retention on RAM section S2 when RAM section is
			0"	4	switched off
т.	\A/	S3RETENTION	Off	1	Off
T	W	SSKETENTION			Keep retention on RAM section S3 when RAM section is switched off
			Off	1	Off
U	w	S4RETENTION	OII	•	Keep retention on RAM section S4 when RAM section is
		o merenion			switched off
			Off	1	Off
٧	W	S5RETENTION			Keep retention on RAM section S5 when RAM section is
					switched off
			Off	1	Off
W	W	S6RETENTION			Keep retention on RAM section S6 when RAM section is
					switched off
			Off	1	Off
Х	W	S7RETENTION			Keep retention on RAM section S7 when RAM section is
					switched off
			Off	1	Off
Υ	W	S8RETENTION			Keep retention on RAM section S8 when RAM section is
			Off	1	switched off Off
Z	W	S9RETENTION	OII	1	Keep retention on RAM section S9 when RAM section is
_	••	SSKETERVIION			switched off
			Off	1	Off
а	W	S10RETENTION			Keep retention on RAM section S10 when RAM section is
					switched off
			Off	1	Off
b	W	S11RETENTION			Keep retention on RAM section S11 when RAM section is
					switched off
			Off	1	Off
С	W	S12RETENTION			Keep retention on RAM section S12 when RAM section is
					switched off
	14.	CARDETENTION	Off	1	Off
d	W	S13RETENTION			Keep retention on RAM section S13 when RAM section is
			Off	1	switched off Off
e	W	S14RETENTION	Oli	1	Keep retention on RAM section S14 when RAM section is
		52 THE LEWITON			switched off
			Off	1	Off
f	W	S15RETENTION	-		Keep retention on RAM section S15 when RAM section is
					switched off
			Off	1	Off

16.9.34 RAM[7].POWER

Address offset: 0x970

RAM7 power control register



Bitı	number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Res	set 0x0000FFFF	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1
Id	RW Field Value Id	Value Description
Α	RW SOPOWER	RAM sections OON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode.
	Off	0 Off
В	On RW S1POWER	1 On
В	Off On	Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off On
С	RW S2POWER	Keep RAM section S2 ON or OFF in System ON mode.
	Off On	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION. All RAM sections will be OFF in System OFF mode. Off On
D	RW S3POWER	Keep RAM section S3 ON or OFF in System ON mode.
	Off On	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. O Off On
E	RW S4POWER	Keep RAM section S4 ON or OFF in System ON mode.
	Off On	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off On
F	RW S5POWER	Keep RAM section S5 ON or OFF in System ON mode.
	Off	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SSRETENTION. All RAM sections will be OFF in System OFF mode. Off
G	On RW S6POWER	1 On Keep RAM section S6 ON or OFF in System ON mode.
3	Off On	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S6RETENTION. All RAM sections will be OFF in System OFF mode. Off On
Н	RW S7POWER	Keep RAM section S7 ON or OFF in System ON mode.
	Off On	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION. All RAM sections will be OFF in System OFF mode. Off On
I	RW S8POWER	Keep RAM section S8 ON or OFF in System ON mode.



Bit n	umber		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			f e d c b a Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
	et 0x0000FFFF RW Field	Value Id		
ld	rvv riela	Off	0	Description RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. Off
J	RW S9POWER	On	1	On Keep RAM section S9 ON or OFF in System ON mode.
	33.6.1.2	Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. Off
K	RW S10POWER	On	1	On Keep RAM section S10 ON or OFF in System ON mode.
K	NW SIDOWLK	Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. Off On
L	RW S11POWER	OII .	1	Keep RAM section S11 ON or OFF in System ON mode.
		Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S11RETENTION. All RAM sections will be OFF in System OFF mode. Off On
М	RW S12POWER		•	Keep RAM section S12 ON or OFF in System ON mode.
		Off On	0 1	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. Off On
N	RW S13POWER			Keep RAM section S13 ON or OFF in System ON mode.
		Off On	0 1	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode. Off On
0	RW S14POWER	Off	0	Keep RAM section S14 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S14RETENTION. All RAM sections will be OFF in System OFF mode. Off
		On	1	On
P	RW S15POWER	Off	0	Keep RAM section S15 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S15RETENTION. All RAM sections will be OFF in System OFF mode. Off
		OII	U	UII



Bit n	iumbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				fedcbaZY	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0	000FFFF		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
			On	1	On
Q	RW	SORETENTION			Keep retention on RAM section S0 when RAM section is in OFF
			Off	0	Off
			On	1	On
R	RW	S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
			Off	0	Off
			On	1	On
S	RW	S2RETENTION			Keep retention on RAM section S2 when RAM section is in OFF
			Off	0	Off
			On	1	On
Т	RW	S3RETENTION			Keep retention on RAM section S3 when RAM section is in OFF
			Off	0	Off
			On	1	On
U	RW	S4RETENTION			Keep retention on RAM section S4 when RAM section is in OFF
			Off	0	Off
			On	1	On
V	RW	SSRETENTION			Keep retention on RAM section S5 when RAM section is in OFF
			Off	0	Off
			On	1	On
W	RW	S6RETENTION			Keep retention on RAM section S6 when RAM section is in OFF
			Off	0	Off
			On	1	On
Х	RW	S7RETENTION			Keep retention on RAM section S7 when RAM section is in OFF
			Off	0	Off
			On	1	On Control of the Con
Υ	RW	S8RETENTION	011		Keep retention on RAM section S8 when RAM section is in OFF
			Off	0	Off
-	DVA	CORFTENTION	On	1	On
Z	KW	S9RETENTION	011		Keep retention on RAM section S9 when RAM section is in OFF
			Off	0	Off
	D\A/	CAODETENTION	On	1	On Keen retention on DAM section \$10 when DAM section is in OFF
а	KVV	S10RETENTION	Off	0	Keep retention on RAM section S10 when RAM section is in OFF
					Off On
h	D\A/	C11DETENTION	On	1	
b	I VV	S11RETENTION	Off	0	Keep retention on RAM section S11 when RAM section is in OFF Off
			On	1	On
С	R/V/	S12RETENTION	Oil	1	Keep retention on RAM section S12 when RAM section is in OFF
C	11.44	JIZINET EINTI OIN	Off	0	Off
			On	1	On
d	RW/	S13RETENTION		•	Keep retention on RAM section S13 when RAM section is in OFF
ŭ		J.J. LIVIIOIV	Off	0	Off
			On	1	On
e	B/v/	S14RETENTION		-	Keep retention on RAM section S14 when RAM section is in OFF
е	IVVV	214IVETEINTION	Off	0	Off
			On	1	On
f	B/v/	S15RETENTION	OII	1	Keep retention on RAM section S15 when RAM section is in OFF
	IVV	313IKLI LIVII OIV	Off	0	Off
			On	1	On
			OII .	-	VIII

16.9.35 RAM[7].POWERSET

Address offset: 0x974

RAM7 power control set register



Bit n	umbe	er		31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et OxC	0000FFFF		0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	W	SOPOWER			Keep RAM section SO of RAM7 on or off in System ON mode
			On	1	On
В	W	S1POWER			Keep RAM section S1 of RAM7 on or off in System ON mode
_		CAROLLER	On	1	On Control of the Con
С	W	S2POWER	00	1	Keep RAM section S2 of RAM7 on or off in System ON mode
D	W	S3POWER	On	1	On Keep RAM section S3 of RAM7 on or off in System ON mode
	vv	33FOWER	On	1	On
E	W	S4POWER	.	-	Keep RAM section S4 of RAM7 on or off in System ON mode
			On	1	On
F	W	S5POWER			Keep RAM section S5 of RAM7 on or off in System ON mode
			On	1	On
G	W	S6POWER			Keep RAM section S6 of RAM7 on or off in System ON mode
			On	1	On
Н	W	S7POWER			Keep RAM section S7 of RAM7 on or off in System ON mode
			On	1	On
I	W	S8POWER			Keep RAM section S8 of RAM7 on or off in System ON mode
			On	1	On
J	W	S9POWER			Keep RAM section S9 of RAM7 on or off in System ON mode
			On	1	On
K	W	S10POWER			Keep RAM section S10 of RAM7 on or off in System ON mode
			On	1	On State of the Control of the Contr
L	W	S11POWER	0-	4	Keep RAM section S11 of RAM7 on or off in System ON mode
N 4	14/	C12DOWED	On	1	On Keep DAM section \$12 of DAM7 on or off in Sustam ON mode
M	W	S12POWER	On	1	Keep RAM section S12 of RAM7 on or off in System ON mode On
N	W	S13POWER	OII	1	Keep RAM section S13 of RAM7 on or off in System ON mode
	••	3131 0 WER	On	1	On
0	W	S14POWER			Keep RAM section S14 of RAM7 on or off in System ON mode
			On	1	On
Р	W	S15POWER			Keep RAM section S15 of RAM7 on or off in System ON mode
			On	1	On
Q	W	SORETENTION			Keep retention on RAM section SO when RAM section is
					switched off
			On	1	On
R	W	S1RETENTION			Keep retention on RAM section S1 when RAM section is
			_		switched off
		CORFTENITION	On	1	On
S	W	S2RETENTION			Keep retention on RAM section S2 when RAM section is
			On	1	switched off On
Т	W	S3RETENTION	UII	1	On Keep retention on RAM section S3 when RAM section is
'	VV	SUCCEPTION			switched off
			On	1	On
U	w	S4RETENTION			Keep retention on RAM section S4 when RAM section is
		-			switched off
			On	1	On
٧	W	SSRETENTION			Keep retention on RAM section S5 when RAM section is
					switched off
			On	1	On
W	W	S6RETENTION			Keep retention on RAM section S6 when RAM section is
					switched off
			On	1	On



Bit r	numb	er		31	. 30	29	28 2	27 26	6 25	5 24	2	3 22 2	1 2	20 1	9 1	8 1	7 1	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id				f	е	d	С	b a	Z	Y	>	(W)	V	U T	Г :	S F	R C	Į P	0	Ν	М	L	K	J	1	Н	G	F	Ε	D (C E	8 A
Res	et 0x0	0000FFFF		0	0	0	0	0 0	0	0	C	0 0	0	0 0) (0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1
Id	RW	Field	Value Id	Va	lue						D	escrip	tio	n																		
X	W	S7RETENTION										eep re			no r	n RA	M.	ect	ion	S7 ۱	whe	en R	ΑN	l se	ctio	n is						
			On	1)n																				
Y	W	S8RETENTION										eep re witche			10 1	n RA	M.	ect	ion	S8 \	whe	en R	ΑN	l se	ctio	n is						
			On	1)n	uc	,,,																		
Z	W	S9RETENTION										eep re			io r	n RA	M s	ect	ion	S9 \	whe	en R	ΑN	l se	ctio	n is						
			On	1								witche In	u c	ווכ																		
а	W	S10RETENTION										eep re			no r	n RA	M.	ect	ion	S10	wł	nen	RAI	M s	ecti	on i	s					
			On	1							_	witche In	d c	off																		
b	W	S11RETENTION									K	eep re	ter	ntior	io r	n RA	Ms	ect	ion	S11	. wł	nen	RAI	M s	ecti	on i	S					
												witche	d c	off																		
			On	1)n																				
С	W	S12RETENTION										eep re witche			10 1	1 KA	AIVI S	sect	ion	S12	wr	nen	KAI	VI S	ecti	on i	S					
			On	1)n																				
d	W	S13RETENTION									K	eep re	ter	ntior	no r	n RA	M.	ect	ion	S13	wł	nen	RAI	M s	ecti	on i	s					
												witche	d c	off																		
0	W	S14RETENTION	On	1								n eep re	+01	ation		. DA		oct	ion	C1 /	l	200	DΛI	\1 c	octi.	on i						
е	VV	314RETEINTION										witche			1 01	INA	(IVI S	eci	1011	314	· vvi	lell	NΑI	VI S	ecu	UIII	5					
			On	1							0	n																				
f	W	S15RETENTION										eep re			io r	n RA	M s	ect	ion	S15	wł	nen	RAI	M s	ecti	on i	S					
			0.5	1								witche	d c	off																		
			On	1							U)n																				

16.9.36 RAM[7].POWERCLR

Address offset: 0x978

RAM7 power control clear register

	11 10	9 8	3 7	6	5	4 3	2	1 0
Id fedcbaZYXWVUTSRQPONMI	L K	J I	I H	G	F	E D	С	ВА
Reset 0x0000FFFF 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1	1 1	1 1	1	1	1 1	1	1 1
Id RW Field Value Description								
A W SOPOWER Keep RAM section SO of RAM7 on or off	in Sys	stem	ON	mod	le			
Off 1 Off								
B W S1POWER Keep RAM section S1 of RAM7 on or off	in Sys	stem	ON	mod	le			
Off 1 Off								
C W S2POWER Keep RAM section S2 of RAM7 on or off	in Sys	stem	ON	mod	le			
Off 1 Off								
D W S3POWER Keep RAM section S3 of RAM7 on or off	f in Sys	stem	ON	mod	le			
Off 1 Off								
E W S4POWER Keep RAM section S4 of RAM7 on or off	f in Sys	stem	ON	mod	le			
Off 1 Off								
F W S5POWER Keep RAM section S5 of RAM7 on or off	f in Sys	stem	ON	mod	le			
Off 1 Off								
G W S6POWER Keep RAM section S6 of RAM7 on or off	f in Sys	stem	ON	mod	le			
Off 1 Off								
H W S7POWER Keep RAM section S7 of RAM7 on or off	f in Sys	stem	ON	mod	le			
Off 1 Off								



Bit	numb	er		31 30	29 28 2	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
		0000FFFF			0 0	0 0	0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW W	Field S8POWER	Value Id	Value				Description Keep RAM section S8 of RAM7 on or off in System ON mode
'	VV	SOPOWER	Off	1				Off
J	W	S9POWER		_				Keep RAM section S9 of RAM7 on or off in System ON mode
			Off	1				Off
K	W	S10POWER						Keep RAM section S10 of RAM7 on or off in System ON mode
			Off	1				Off
L	W	S11POWER	Off	1				Keep RAM section S11 of RAM7 on or off in System ON mode Off
М	W	S12POWER	5	-				Keep RAM section S12 of RAM7 on or off in System ON mode
			Off	1				Off
N	W	S13POWER						Keep RAM section S13 of RAM7 on or off in System ON mode
			Off	1				Off
0	W	S14POWER						Keep RAM section S14 of RAM7 on or off in System ON mode
Р	14/	CAEDOWED	Off	1				Off
Р	W	S15POWER	Off	1				Keep RAM section S15 of RAM7 on or off in System ON mode Off
Q	W	SORETENTION	OII	-				Keep retention on RAM section SO when RAM section is
-								switched off
			Off	1				Off
R	W	S1RETENTION						Keep retention on RAM section S1 when RAM section is
								switched off
			Off	1				Off
S	W	S2RETENTION						Keep retention on RAM section S2 when RAM section is switched off
			Off	1				Off
Т	W	S3RETENTION		_				Keep retention on RAM section S3 when RAM section is
								switched off
			Off	1				Off
U	W	S4RETENTION						Keep retention on RAM section S4 when RAM section is
								switched off
\/	W	S5RETENTION	Off	1				Off Keep retention on RAM section S5 when RAM section is
V	VV	SSKETEINTION						switched off
			Off	1				Off
W	W	S6RETENTION						Keep retention on RAM section S6 when RAM section is
								switched off
			Off	1				Off
X	W	S7RETENTION						Keep retention on RAM section S7 when RAM section is
			Off	1				switched off
Υ	W	S8RETENTION	Off	1				Off Keep retention on RAM section S8 when RAM section is
	••	23						switched off
			Off	1				Off
Z	W	S9RETENTION						Keep retention on RAM section S9 when RAM section is
								switched off
			Off	1				Off
а	W	S10RETENTION						Keep retention on RAM section S10 when RAM section is
			Off	1				switched off Off
b	W	S11RETENTION	J.,	_				Keep retention on RAM section S11 when RAM section is
								switched off
			Off	1				Off
С	W	S12RETENTION						Keep retention on RAM section S12 when RAM section is
								switched off
			Off	1				Off



Bit r	numbe	er		31	. 30	29	28	27	26	5 25	5 24	1 23	22	21	20	19 :	18 :	17 1	.6 1	.5 1	L4 1	.3 12	2 11	10	9	8	7	6	5 4	1 3	2	1	0
Id				f	е	d	С	b	а	Z	Υ	Х	W	٧	U	Т	S	R (Q I	Р	0 1	N N	l L	K	J	1	Н	G	F E	D	С	В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 :	1	1	1 1	1	1	1	1	1	1	1 1	. 1	1	1	1
Id	RW	Field	Value Id	Va	lue	:						De	escri	ptic	on																		
d	W	S13RETENTION											ep r vitch			n o	n R	AM	sec	tio	n Sí	L3 w	hen	RAI	M se	ectio	on i	S					
			Off	1								Of	f																				
е	W	S14RETENTION											ep r vitch			n o	n R	AM	sec	tio	n S:	L4 w	hen	RAI	M se	ectio	on i	S					
			Off	1								Of	f																				
f	W	S15RETENTION										Ke	ep r	ete	ntio	n o	n R	AM	sec	tio	n S:	L5 w	hen	RAI	M se	ectio	on i	S					
												SV	vitch	ed	off																		
			Off	1								Of	f																				

16.9.37 RAM[8].POWER

Address offset: 0x980

RAM8 power control register

Review	Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
RW SUPOWER SUPOWER RAM sections are always retained when OFF in System ON mode. RAM sections are always retained when OFF in System OFF mode. RAM sections are always retained when OFF in System OFF mode. RAM sections are always retained when OFF in System OFF mode. RAM sections will be OFF in System OFF mode. RAM sections will be OFF in System OFF mode. RAM sections are always retained when OFF mode. RAM sections are always retained when OFF mode. RAM sections are always retained when OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System OFF mode. RAM sections will be OFF in System OFF mode. RAM sections are always retained when OFF dependent on the settings in SIRETENTION. All RAM sections are always retained when OFF mode. RAM sections are always retained when OFF in System OFF mode. RAM sections are always retained when OFF mode. RAM sections will be OFF in System OFF mode. RAM sections will be OFF in System	d		fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
RAW SOPOWER RW SOPOWER RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode. Off 0 0 Off On 1 On RW SIPOWER RM SIPOWER RW SIPOWER RW SIPOWER RM SIPOWER RW SIPOWER RW SIPOWER RM SIPOWER RW SIPOW	Reset 0x0000FFFF		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1
RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode. Off 0 0 Off On 1 0 On B RW SIPOWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System OFF mode. Off 0 0 Off On 1 On C RW SIPOWER Keep RAM section S2 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System ON mode. RAM sections are always retained when OFF dependent on the settings in SIRETENTION. All RAM sections are always retained when OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On RW SSPOWER Keep RAM section swill be OFF in System OFF mode. Off On 0 Off On 1 On RW SSPOWER Keep RAM section SS ON or OFF in System ON mode.	d RW Field	Value Id	Value Description
retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On ERW SIPOWER OFF OO O	RW SOPOWER		Keep RAM section SO ON or OFF in System ON mode.
All RAM sections will be OFF in System OFF mode. Off On 1 On RAM Sections are always retained when ON, but can also be retained when OFF in System OFF mode. Off 0 Off On 1 On RAM Sections will be OFF in System OFF mode. RAM sections will be OFF in System ON mode. RAM sections will be OFF in System ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 On RAM Sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 On RAM Sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 On RAM Sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 On Keep RAM section S5 ON or OFF in System OFF mode.			RAM sections are always retained when ON, but can also be
Off On 1 On STANDER RAM Section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM Sections will be OFF in System OFF mode. Off On 1 On Keep RAM section S2 ON or OFF in System OFF mode. Off On 1 On Keep RAM section S2 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On Off On 1 On Off			retained when OFF dependent on the settings in SORETENTION.
RW SIPOWER RW SIPOWER RW SIPOWER RW SIPOWER RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System OFF mode. Off 0 0 OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System OFF mode. Off 0 0 OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System OFF mode. On 1 On RW SIPOWER RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System OFF mode. Off 0 0 OFF On 1 On RW SIPOWER RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SIRETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System OFF mode. Off 0 OFF ON 1 ON REEP RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SIRETENTION. All RAM sections are always retained when OFF mode. Off 0 OFF ON 1 ON REEP RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SIRETENTION. All RAM sections are always retained when OFF mode. Off 0 OFF ON 1 ON REEP RAM sections will be OFF in System OFF mode. Off 0 OFF ON 1 OFF O			All RAM sections will be OFF in System OFF mode.
Rep RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 OFF 0 OFF 0 OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 OFF 0 OFF dependent on the settings in S1RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 OFF RW S3POWER RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 ON REEP RAM sections APON OFF In System OFF mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 ON RAM Sections S5 ON or OFF in System OFF mode.		Off	0 Off
RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System OFF mode. Off 0 0 0ff On 1 0 On RW S2POWER		On	1 On
retained when OFF dependent on the settings in SIRETENTION. All RAM sections will be OFF in System OFF mode. Off 0 0 0 0ff On 1 0 On C RW S2POWER	B RW S1POWER		Keep RAM section S1 ON or OFF in System ON mode.
All RAM sections will be OFF in System OFF mode. Off On 1 On C RW SZPOWER Off On 1 On RAM sections 2 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SZRETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On RW SZPOWER FRAM SZPOWER OFF ON 1 ON All RAM sections 3 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SZRETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SZRETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On RAM SZPOWER RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SZRETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SZRETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SZRETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On FRAM SSPOWER Keep RAM sections SON or OFF in System OFF mode. Off On SZPOWER Keep RAM sections SON or OFF in System ON mode.			RAM sections are always retained when ON, but can also be
Off On 1 On Keep RAM section S2 ON or OFF in System ON mode. RAM S2POWER Off On 1 On Keep RAM section S2 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On Off RW S3POWER RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On E RW S4POWER RAM Sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On Keep RAM sections will be OFF in System OFF mode. Off On 1 On Keep RAM sections S5 ON or OFF in System ON mode.			retained when OFF dependent on the settings in S1RETENTION.
On 1 On Keep RAM section S2 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off 0 Off On 1 On RW S3POWER Keep RAM sections will be OFF in System OFF mode. Off 0 On 1 On RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 On E RW S4POWER Keep RAM section S4 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 Off On 0 Off On 1 On F RW S5POWER SEPOWER Keep RAM section S5 ON or OFF in System ON mode.			All RAM sections will be OFF in System OFF mode.
Keep RAM sections \$2 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in \$2RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 0 Off On 1 On RW S3POWER RAM sections 33 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in \$3RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in \$3RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 0 Off On 1 On E RW S4POWER RAM sections 40 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in \$4RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in \$4RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 On SERVING		Off	0 Off
RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S2RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 0 Off On 1 On RW S3POWER Keep RAM section S3 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 On E RW S4POWER Keep RAM section S4 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 On F RW S5POWER Keep RAM section S5 ON or OFF in System ON mode.		On	1 On
retained when OFF dependent on the settings in S2RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On RW S3POWER Fig. 3POWER Off On 1 RAM section S3 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On RAM Sections are always retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 REPROMER RAM Sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On FROM S5POWER REEPRAM Section S5 ON or OFF in System ON mode.	RW S2POWER		Keep RAM section S2 ON or OFF in System ON mode.
All RAM sections will be OFF in System OFF mode. Off On 1 On RW S3POWER FRAM S3POWER Off On 1 RW S3POWER All RAM section S3 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On Keep RAM sections will be OFF in System OFF mode. Off On 1 On RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 Or RAW S5POWER Keep RAM section S5 ON or OFF in System ON mode.			RAM sections are always retained when ON, but can also be
Off On 1 On RW S3POWER			retained when OFF dependent on the settings in S2RETENTION.
On RW S3POWER RAM section S3 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On E RW S4POWER RAW S4POWER RAM section S4 ON or OFF in System ON mode. RAM section S4 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On Keep RAM sections will be OFF in System OFF mode. Off On 1 On Keep RAM sections S5 ON or OFF in System ON mode.			All RAM sections will be OFF in System OFF mode.
RAM section S3 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On E RW S4POWER RAM Section S4 ON or OFF in System ON mode. RAM section S4 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off On 0 Off On 1 On Keep RAM section S5 ON or OFF in System ON mode.		Off	0 Off
RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On E RW S4POWER RW S4POWER RW S4POWER RAM section S4 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off On 0 Off On 0 F RW S5POWER RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off On 0 Keep RAM section S5 ON or OFF in System ON mode.		On	1 On
retained when OFF dependent on the settings in S3RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On E RW S4POWER FRW S4POWER Off On 1 Off Off On 1 Off Off Off Off Off Off Off Off Off	D RW S3POWER		Keep RAM section S3 ON or OFF in System ON mode.
All RAM sections will be OFF in System OFF mode. Off On 1 On E RW S4POWER FROM S4POWER OFF OFF OFF OFF OFF OFF OFF OFF OFF O			RAM sections are always retained when ON, but can also be
Off On 1 On ERW SAPOWER REGISTED AND SAPOWER REGIST			retained when OFF dependent on the settings in S3RETENTION.
On E RW SAPOWER F RW SSPOWER On Keep RAM section S4 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SARETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On Keep RAM section S5 ON or OFF in System ON mode.			
Keep RAM section S4 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On F RW SSPOWER Keep RAM section S5 ON or OFF in System ON mode.		Off	0 Off
RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On F RW SSPOWER Keep RAM section S5 ON or OFF in System ON mode.		On	
retained when OFF dependent on the settings in S4RETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On F RW SSPOWER REPRAM Section SS ON or OFF in System ON mode.	E RW S4POWER		Keep RAM section S4 ON or OFF in System ON mode.
All RAM sections will be OFF in System OFF mode. Off On 1 On F RW SSPOWER All RAM sections will be OFF in System OFF mode. Off Con Keep RAM section SS ON or OFF in System ON mode.			RAM sections are always retained when ON, but can also be
Off 0 Off On 1 On F RW S5POWER Keep RAM section S5 ON or OFF in System ON mode.			retained when OFF dependent on the settings in S4RETENTION.
On 1 On F RW SSPOWER Keep RAM section S5 ON or OFF in System ON mode.			·
F RW SSPOWER Keep RAM section S5 ON or OFF in System ON mode.			
	- DW 6505:::55	On	
RAM sections are always retained when ON, but can also be	- RW S5POWER		Keep RAM section S5 ON or OFF in System ON mode.
			RAM sections are always retained when ON, but can also be
retained when OFF dependent on the settings in S5RETENTION.			· · · · · · · · · · · · · · · · · · ·
All RAM sections will be OFF in System OFF mode.			All RAM sections will be OFF in System OFF mode.



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZY	XWVUTSRQPONMLKJIHGFEDCBA
Reset 0x0000FFFF			0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value	Description Off
	Off On	0	Off On
G RW S6POWER	3 11	-	Keep RAM section S6 ON or OFF in System ON mode.
	Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SGRETENTION. All RAM sections will be OFF in System OFF mode. Off
	On	1	On
H RW S7POWER	Off	0	Keep RAM section S7 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S7RETENTION. All RAM sections will be OFF in System OFF mode. Off
	On	1	On
I RW S8POWER	Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S8RETENTION. All RAM sections will be OFF in System OFF mode. Off On
J RW S9POWER			Keep RAM section S9 ON or OFF in System ON mode.
	Off	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S9RETENTION. All RAM sections will be OFF in System OFF mode. Off
K RW S10POWER	On	1	On Keen BAM section \$10 ON or OFF in System ON mode
K RW S10POWER	Off	0	RAM section S10 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S10RETENTION. All RAM sections will be OFF in System OFF mode. Off
	On	1	On
L RW S11POWER	Off On	0 1	Keep RAM section S11 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S11RETENTION. All RAM sections will be OFF in System OFF mode. Off On
M RW S12POWER			Keep RAM section S12 ON or OFF in System ON mode.
	Off On	0	RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S12RETENTION. All RAM sections will be OFF in System OFF mode. Off On
N RW S13POWER	·		Keep RAM section S13 ON or OFF in System ON mode.
			RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S13RETENTION. All RAM sections will be OFF in System OFF mode.



Fig.	Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
May Field Value by Value Value Value Chesription Or Or Or Or Or Or Or O						
OFF	Res	et 0x0	0000FFFF		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
No. No. STAPPOWER	Id	RW	Field	Value Id	Value	Description
New STAPPOWER				Off	0	Off
March Marc				On	1	On
A	0	RW	S14POWER			Keep RAM section S14 ON or OFF in System ON mode.
Part						RAM sections are always retained when ON, but can
Mathematical Content						also be retained when OFF dependent on the settings in
P						S14RETENTION. All RAM sections will be OFF in System OFF
P						
P						
RAM Sections are always retained when OR, but can also be retained when OR, but can also be retained when OR dependent on the settings in SISRETENTION. All RAM sections will be OFF in System OFF mode.		DIA	CAEDOWED	On	1	
also be retained when OFF dependent on the settings in SISRETENTION. All RAM sections will be OFF in System OFF mode. Off 0 0 Off 0 OF OF OF OFF OFF OFF OFF OFF OFF OFF	Р	KW	S15POWER			keep ram section S15 ON or OFF in System ON mode.
SISRETENTION: All RAM sections will be OFF in System OFF mode. Off						
Mode of the control o						
Company Comp						
New SORETENTION Constitution				Off	0	
Q RW SORETENTION Off 0 OFF						
Note	Q	RW	SORETENTION		-	
R	-			Off	0	·
New STRETENTION Constitution				On	1	On
New STRETENTION Constitution	R	RW	S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
S RW SZRETENTION Off 0 Off Of On 1 On T RW SJRETENTION Keep retention on RAM section SJ when RAM section is in OFF Off On Off U RW SARETENTION Keep retention on RAM section SJ when RAM section is in OFF Off On Off V RW SARETENTION Keep retention on RAM section SJ when RAM section is in OFF Off On Off V RW SARETENTION Keep retention on RAM section SJ when RAM section is in OFF Off On Off On 1 On X RW SARETENTION Keep retention on RAM section SG when RAM section is in OFF Off On Off Y RW SARETENTION Keep retention on RAM section SG when RAM section is in OFF Off O Off On 1 On Y RW SARETENTION Keep retention on RAM section SG when RAM section is in OFF				Off	0	Off
Off				On	1	On
No	S	RW	S2RETENTION			
T RW SARETENTION Off 0 OFF On 1 OFF On 0 OFF ON						
Off	т	D\A/	CODETENTION	On	1	
U RW SARETENTION Off 0 Off On 1 On Keep retention on RAM section S4 when RAM section is in OFF Off 0 Off On 1 On V RW SSRETENTION Off 0 Off On 1 On W RW SGRETENTION Off 0 Off On 1 On X RW SARETENTION Off 0 Off On 1 On X RW SARETENTION Off 0 Off On 1 On X RW SARETENTION Off 0 Off On 1 On X RW SARETENTION Off 0 Off On 1 On X RESPICIAL ON OFF Off 0 OFF ON 1 ON Keep retention on RAM section S6 when RAM section is in OFF Off On 1 ON X RW SARETENTION Off 0 Off On 1 ON X RW SARETENTION Off 0 Off ON 1 ON X RW SARETENTION Off 0 Off ON 1 ON X RESPICIAL ON OFF OFF OFF OFF OFF OFF OFF OFF OFF ON 1 ON X RESPICIAL ON X RESPICIAL ON X RESPICIAL ON X RESPICIAL ON X RESPICIAL ON X RESPICIAL ON X RW SARETENTION OFF OFF OFF ON 1 ON X RESPICIAL ON X RE	'	KVV	SSKETEINTION	Off	0	
V RW SERTENTION Off On 1 On Off	U	RW	S4RETENTION			
V RW STRETENTION Off O Off O Off				Off	0	Off
Off On 1 On Off On On W RW SGRETENTION				On	1	On
No	٧	RW	S5RETENTION			Keep retention on RAM section S5 when RAM section is in OFF
W RW SGRETENTION Off O Off O OFF On 1 ON X RW STRETENTION Off O OFF On 1 ON X RW STRETENTION Off O OFF On 1 ON X RW STRETENTION OFF OFF ON 1 ON X SRETENTION OFF ON 1 ON X SPRETENTION OFF ON 1 ON X SERPTENTION OFF ON 0 OF				Off		Off
Off On 1 On X RW STRETENTION				On	1	
Name	W	RW	S6RETENTION	011		·
X RW S7RETENTION Off Off On 1 On Y RW S8RETENTION Off On 1 On Keep retention on RAM section S7 when RAM section is in OFF Off On 0 Neep retention on RAM section S10 when RAM section is in OFF Off On 0 Off On 0 Neep retention on RAM section S11 when RAM section is in OFF Off On 0 Off On 0 Neep retention on RAM section S12 when RAM section is in OFF Off On 0 Neep retention on RAM section S12 when RAM section is in OFF						
V RW SRETENTION Ceep retention on RAM section S1 when RAM section is in OFF Off On 1 On Off Z RW SPRETENTION Keep retention on RAM section S9 when RAM section is in OFF Off On 1 On Off A RW SIORETENTION Keep retention on RAM section S10 when RAM section is in OFF Off On 1 On Off A RW SIORETENTION Keep retention on RAM section S10 when RAM section is in OFF Off On 1 On B RW SIIRETENTION Keep retention on RAM section S11 when RAM section is in OFF Off On 1 On C RW SI2RETENTION Keep retention on RAM section S12 when RAM section is in OFF	X	RW	SZRETENTION	Oli	1	
Y RW SBRETENTION On 1				Off	0	·
Off On 1 On CRAM section S9 when RAM section is in OFF Off On 0 Off On 1 On RW S9RETENTION Off O Off On 1 On RW S10RETENTION Off O Off On 1 On B RW S11RETENTION RECEIVED ON 1 ON RECEIVE ON 1 ON RECE						
Don 1 On Keep retention on RAM section S9 when RAM section is in OFF Off On 1 On Off On On Off On Of	Υ	RW	S8RETENTION			Keep retention on RAM section S8 when RAM section is in OFF
Z RW S9RETENTION Off Off On 1 On RW S10RETENTION FRW S10RETENTION Off On 1 On Keep retention on RAM section S9 when RAM section is in OFF Off Off On 1 On Keep retention on RAM section S10 when RAM section is in OFF Off On 1 On Keep retention on RAM section S10 when RAM section is in OFF Off On 0 Off On Keep retention on RAM section S11 when RAM section is in OFF Off Off On Off On Keep retention on RAM section S11 when RAM section is in OFF Off On Keep retention on RAM section S12 when RAM section is in OFF Keep retention on RAM section S12 when RAM section is in OFF				Off	0	Off
a RW S10RETENTION Congression of the congression of				On	1	On
a RW S10RETENTION Keep retention on RAM section S10 when RAM section is in OFF 0ff 0 Off 0n 1 On b RW S11RETENTION Keep retention on RAM section S11 when RAM section is in OFF 0ff 0 Off 0n 1 On c RW S12RETENTION Keep retention on RAM section S12 when RAM section is in OFF	Z	RW	S9RETENTION			·
a RW S10RETENTION Keep retention on RAM section S10 when RAM section is in OFF Off 0 Off On 1 On b RW S11RETENTION Keep retention on RAM section S11 when RAM section is in OFF Off 0 Off On 1 On c RW S12RETENTION Keep retention on RAM section S12 when RAM section is in OFF						
b RW S11RETENTION Keep retention on RAM section S11 when RAM section is in OFF c RW S12RETENTION Keep retention on RAM section S11 when RAM section is in OFF C RW S12RETENTION Keep retention on RAM section S12 when RAM section is in OFF		D\A/	STORETENTION	Un	1	
b RW S11RETENTION Keep retention on RAM section S11 when RAM section is in OFF Off O Off On On On c RW S12RETENTION Keep retention on RAM section S12 when RAM section is in OFF	d	ĸW	STORETEINTION	Off	0	
b RW S11RETENTION Keep retention on RAM section S11 when RAM section is in OFF Off 0 Off On 1 On c RW S12RETENTION Keep retention on RAM section S12 when RAM section is in OFF						
Off 0 Off On 1 On c RW S12RETENTION Keep retention on RAM section S12 when RAM section is in OFF	b	RW	S11RETENTION			
c RW S12RETENTION Keep retention on RAM section S12 when RAM section is in OFF				Off	0	·
·				On	1	On
Off 0 Off	С	RW	S12RETENTION			Keep retention on RAM section S12 when RAM section is in OFF
				Off	0	Off



Bit r	numbe	r		31	30	29	28 2	27 :	26 2	25 2	4 2	3 22	21	20	19	18	17	16	15 :	14 1	.3 12	2 11	10	9	8	7 (6 5	4	3	2 :	1 0
Id				f	e	d	С	b	а	Z '	Y X	W	٧	U	Т	S	R	Q	Р	0 1	N M	l L	K	J	1 1	4 (3 F	Ε	D	C E	3 A
Res	et 0x0	000FFFF		0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	1	1	1 1	1	1	1	1	1 :	1 1	. 1	1	1 1	l 1
Id	RW	Field	Value Id	Val	lue						D	escri	iptio	on																	
			On	1							0	n																			
d	RW	S13RETENTION									K	еер	rete	entic	on c	on R	RAN	l se	ctio	n S:	L3 w	hen	RAI	VI s	ectic	n is	in	OFF			
			Off	0							0	ff																			
			On	1							0	n																			
e	RW	S14RETENTION									K	еер	rete	ntio	on c	n F	RAN	1 se	ctio	n S	L4 w	hen	RAI	VI s	ectio	n is	in	OFF			
			Off	0							0	ff																			
			On	1							0	n																			
f	RW	S15RETENTION									K	еер	rete	ntio	on c	on R	RAN	l se	ctio	n S:	L5 w	hen	RAI	VI s	ectic	n is	in	OFF			
			Off	0							0	ff																			
			On	1							0	n																			

16.9.38 RAM[8].POWERSET

Address offset: 0x984

RAM8 power control set register

Bit r	numb	er		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				fedcbaZ	Y X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x(0000FFFF		0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 &$
Id	RW	Field	Value Id	Value	Description
Α	W	SOPOWER			Keep RAM section SO of RAM8 on or off in System ON mode
			On	1	On
В	W	S1POWER			Keep RAM section S1 of RAM8 on or off in System ON mode
			On	1	On
С	W	S2POWER			Keep RAM section S2 of RAM8 on or off in System ON mode
			On	1	On
D	W	S3POWER			Keep RAM section S3 of RAM8 on or off in System ON mode
			On	1	On
Ε	W	S4POWER			Keep RAM section S4 of RAM8 on or off in System ON mode
			On	1	On
F	W	S5POWER			Keep RAM section S5 of RAM8 on or off in System ON mode
			On	1	On
G	W	S6POWER			Keep RAM section S6 of RAM8 on or off in System ON mode
			On	1	On
Н	W	S7POWER			Keep RAM section S7 of RAM8 on or off in System ON mode
			On	1	On
ı	W	S8POWER			Keep RAM section S8 of RAM8 on or off in System ON mode
			On	1	On
J	W	S9POWER			Keep RAM section S9 of RAM8 on or off in System ON mode
			On	1	On
K	W	S10POWER	_		Keep RAM section S10 of RAM8 on or off in System ON mode
		244001150	On	1	On
L	W	S11POWER			Keep RAM section S11 of RAM8 on or off in System ON mode
	14/	C42DOWED	On	1	On
М	W	S12POWER	0.5	1	Keep RAM section S12 of RAM8 on or off in System ON mode
N	14/	C12DOWED	On	1	On Koop DAM section C12 of DAMS on or off in System ON mode
N	W	S13POWER	00	1	Keep RAM section S13 of RAM8 on or off in System ON mode
0	w	C14DOWED	On	1	On Koop PANA section \$14 of PANA? on or off in System ON mode.
U	vv	S14POWER	On	1	Keep RAM section S14 of RAM8 on or off in System ON mode On
Р	W	S15POWER	Oii	1	
۲	VV	SISPOWER	On	1	Keep RAM section S15 of RAM8 on or off in System ON mode On
			OII	1	Oil



Bit r	numbe	er		31 30	29 28	27 26	25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								XWVUTSRQPONMLKJIHGFEDCBA
Res	et OxC	000FFFF		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value				Description
Q	W	SORETENTION	0.	4				Keep retention on RAM section S0 when RAM section is switched off
D	14/	CARTENTION	On	1				On Keen retention on DAM costion S1 when DAM costion is
R	W	S1RETENTION	On	1				Keep retention on RAM section S1 when RAM section is switched off On
S	W	S2RETENTION						Keep retention on RAM section S2 when RAM section is switched off
			On	1				On
Т	W	S3RETENTION	On	1				Keep retention on RAM section S3 when RAM section is switched off On
U	W	S4RETENTION	0-	1				Keep retention on RAM section S4 when RAM section is switched off
V	W	SSRETENTION	On	1				On Keep retention on RAM section S5 when RAM section is switched off On
W	W	SGRETENTION						Keep retention on RAM section S6 when RAM section is switched off
			On	1				On
X	W	S7RETENTION	On	1				Keep retention on RAM section S7 when RAM section is switched off On
Υ	W	S8RETENTION	_					Keep retention on RAM section S8 when RAM section is switched off
Z	W	S9RETENTION	On	1				On Keep retention on RAM section S9 when RAM section is switched off On
а	W	S10RETENTION	On	1				Keep retention on RAM section S10 when RAM section is switched off On
b	W	S11RETENTION	On	1				Keep retention on RAM section S11 when RAM section is switched off On
С	W	S12RETENTION	On	1				Keep retention on RAM section S12 when RAM section is switched off On
d	W	S13RETENTION	On	1				Keep retention on RAM section S13 when RAM section is switched off On
е	W	S14RETENTION	On	1				Keep retention on RAM section S14 when RAM section is switched off On
f	W	S15RETENTION						Keep retention on RAM section S15 when RAM section is switched off
			On	1				On

16.9.39 RAM[8].POWERCLR

Address offset: 0x988

RAM8 power control clear register



Bit r	numb	er		31 30 2	29 28 2	27 26	5 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000FFFF		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
Id		Field	Value Id	Value				Description
Α	W	SOPOWER	Off	1				Keep RAM section S0 of RAM8 on or off in System ON mode Off
В	W	S1POWER	Off	1				Keep RAM section S1 of RAM8 on or off in System ON mode Off
С	W	S2POWER	Off	1				Keep RAM section S2 of RAM8 on or off in System ON mode Off
D	W	S3POWER	Off	1				Keep RAM section S3 of RAM8 on or off in System ON mode Off
E	W	S4POWER	Off	1				Keep RAM section S4 of RAM8 on or off in System ON mode Off
F	W	S5POWER	Off	1				Keep RAM section S5 of RAM8 on or off in System ON mode Off
G	W	S6POWER	Off	1				Keep RAM section S6 of RAM8 on or off in System ON mode Off
Н	W	S7POWER	Off	1				Keep RAM section S7 of RAM8 on or off in System ON mode Off
I	W	S8POWER	Off					Keep RAM section S8 of RAM8 on or off in System ON mode Off
J	W	S9POWER	Off	1				Keep RAM section S9 of RAM8 on or off in System ON mode Off
K	W	S10POWER	Off	1				Keep RAM section S10 of RAM8 on or off in System ON mode
L	W	S11POWER	Off	1				Off Keep RAM section S11 of RAM8 on or off in System ON mode
М	W	S12POWER		1				Off Keep RAM section S12 of RAM8 on or off in System ON mode
N	W	S13POWER	Off	1				Off Keep RAM section S13 of RAM8 on or off in System ON mode
0	W	S14POWER	Off	1				Off Keep RAM section S14 of RAM8 on or off in System ON mode
Р	W	S15POWER	Off	1				Off Keep RAM section S15 of RAM8 on or off in System ON mode
Q	W	SORETENTION	Off	1				Off Keep retention on RAM section S0 when RAM section is
			Off	1				switched off Off
R	W	S1RETENTION						Keep retention on RAM section S1 when RAM section is switched off
			Off	1				Off
S	W	S2RETENTION	011	4				Keep retention on RAM section S2 when RAM section is switched off
Т	W	S3RETENTION	Off	1				Off Keep retention on RAM section S3 when RAM section is switched off
U	W	S4RETENTION	Off	1				Off Keep retention on RAM section S4 when RAM section is
			Off	1				switched off Off
V	W	S5RETENTION	Off	1				Keep retention on RAM section S5 when RAM section is switched off Off
W	W	S6RETENTION	<u></u>	-				Keep retention on RAM section S6 when RAM section is switched off
			Off	1				Off
Х	W	S7RETENTION						Keep retention on RAM section S7 when RAM section is switched off



		er		31	. 30	29	28 .	2/2	b 2:	5 24	1 2:	3 22	21	20	19	TR	1/	16 .	15 .	L4 J	13 1	LZ 1	I 10	9	8	/	6	5	4 3	5 2	1	U
Id				f	е	d	С	b a	Z	. Y	Х	(W	/ V	U	Т	S	R	Q	Р	0 1	N N	M L	. K	J	1	Н	G	F	E C) С	В	Α
Reset	0x0	000FFFF		0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	1	1	1	1 1	. 1	1	1	1	1	1	1 1	l 1	1	1
ld I	RW	Field	Value Id	Va	lue						D	escr	ripti	on																		
			Off	1							0	ff																				
Υ \	W	S8RETENTION									K	eep	rete	enti	on (on F	RAN	l se	ctio	n S	8 w	hen	RAN	∕l se	ctio	n is						
											S۷	witch	hed	off	:																	
			Off	1							0	ff																				
Z \	W	S9RETENTION									K	еер	rete	enti	on (on F	RAN	l se	ctio	n S	9 w	hen	RAN	∕l se	ctio	n is						
											S۷	witch	hed	off																		
			Off	1							0	ff																				
a \	W	S10RETENTION									K	eep	rete	enti	on (on F	RAN	l se	ctio	n S:	10 v	whe	n RA	M s	ecti	on i	s					
											S۷	witch	hed	off	:																	
			Off	1							0	ff																				
b \	W	S11RETENTION									K	еер	rete	enti	on (on F	RAIV	l se	ctio	n S	11 v	whe	n RA	M s	ecti	on i	S					
											S۷	witch	hed	off																		
			Off	1							0	ff																				
c \	W	S12RETENTION									K	еер	rete	enti	on (on F	RAIV	se	ctio	n S	12 v	whe	n RA	M s	ecti	on i	S					
											S۷	witch	hed	off																		
			Off	1							0	ff																				
d \	W	S13RETENTION									K	eep	rete	enti	on (on F	RAN	l se	ctio	n S	13 v	whe	n RA	M s	ecti	on i	S					
											S۷	witch	hed	off																		
			Off	1							0	ff																				
e \	W	S14RETENTION									K	eep	rete	enti	on (on F	RAIV	se	ctio	n S:	14 v	whe	n RA	M s	ecti	on i	S					
											S۷	witch	hed	off																		
			Off	1							0	ff																				
f \	W	S15RETENTION									K	eep	rete	enti	on o	on F	RAN	se	ctio	n S	15 v	whe	n RA	M s	ecti	on i	S					
											SV	witch	hed	off																		
			Off	1							0	ff																				

16.10 Electrical specification

16.10.1 Regulator operating conditions

Description	Min.	Тур.	Max.	Units
VDD supply voltage needed during power-on reset.	1.75			V
VDD operating voltage.	1.7	3.0	3.6	V
VDDH operating voltage.	2.5	3.7	5.5	V
Voltage output on VDD when supplied from internal regulator	1.8		3.3	V
(REG0). Note: VDDH is the input to REG0.				
Current draw of external circuitry from VDD in High voltage			1	mA
mode (supply on VDDH) with EXTSUPPLY enabled in UICR,				
during System OFF.				
Current that can be drawn by external circuitry from VDD in		25		mA
High voltage mode (supply on VDDH) with EXTSUPPLY enabled				
in UICR, during System ON. ⁹				
Current draw from VDD in High voltage mode (supply on VDDH)			50	mA
of both external circuits and nRF device.				
Minimum difference between voltage supplied on VDDH pin	0.3			V
and voltage output on VDD pin.				
	VDD supply voltage needed during power-on reset. VDD operating voltage. VDDH operating voltage. Voltage output on VDD when supplied from internal regulator (REGO). Note: VDDH is the input to REGO. Current draw of external circuitry from VDD in High voltage mode (supply on VDDH) with EXTSUPPLY enabled in UICR, during System OFF. Current that can be drawn by external circuitry from VDD in High voltage mode (supply on VDDH) with EXTSUPPLY enabled in UICR, during System ON. Current draw from VDD in High voltage mode (supply on VDDH) of both external circuits and nRF device. Minimum difference between voltage supplied on VDDH pin	VDD supply voltage needed during power-on reset. 1.75 VDD operating voltage. 2.5 Voltage output on VDD when supplied from internal regulator (REGO). Note: VDDH is the input to REGO. Current draw of external circuitry from VDD in High voltage mode (supply on VDDH) with EXTSUPPLY enabled in UICR, during System OFF. Current that can be drawn by external circuitry from VDD in High voltage mode (supply on VDDH) with EXTSUPPLY enabled in UICR, during System ON. Current draw from VDD in High voltage mode (supply on VDDH) of both external circuits and nRF device. Minimum difference between voltage supplied on VDDH pin 1.75 1.75 1.75 1.75 1.75 1.75 1.86 1.86 1.86 1.87 1.88 1.89 1.80 1.8	VDD supply voltage needed during power-on reset. VDD operating voltage. 1.7 3.0 VDDH operating voltage. 2.5 3.7 Voltage output on VDD when supplied from internal regulator (REGO). Note: VDDH is the input to REGO. Current draw of external circuitry from VDD in High voltage mode (supply on VDDH) with EXTSUPPLY enabled in UICR, during System OFF. Current that can be drawn by external circuitry from VDD in High voltage mode (supply on VDDH) with EXTSUPPLY enabled in UICR, during System ON. Current draw from VDD in High voltage mode (supply on VDDH) of both external circuits and nRF device. Minimum difference between voltage supplied on VDDH pin 0.3	VDD supply voltage needed during power-on reset. VDD operating voltage. 1.7 3.0 3.6 VDDH operating voltage. 2.5 3.7 5.5 Voltage output on VDD when supplied from internal regulator (REGO). Note: VDDH is the input to REGO. Current draw of external circuitry from VDD in High voltage mode (supply on VDDH) with EXTSUPPLY enabled in UICR, during System OFF. Current that can be drawn by external circuitry from VDD in High voltage mode (supply on VDDH) with EXTSUPPLY enabled in UICR, during System ON.9 Current draw from VDD in High voltage mode (supply on VDDH) of both external circuits and nRF device. Minimum difference between voltage supplied on VDDH pin 1.75 1.75 1.75 1.8 2.5 3.7 5.5 1 1 1 1 1 1 1 1 1 1 1 1 1

⁹ The sum of nRF device load current and external circuit load current cannot exceed I_{REGO}; At high TX power settings or other operating modes of the nRF device where peak load current is high, the current available for external circuits may be less than I_{EX,ON} nominal.



16.10.2 Current consumption, sleep

Symbol	Description	Min.	Тур.	Max.	Units
I _{OFF,NV}	System OFF current, no RAM retention, Normal voltage mode		0.4		μΑ
	(supply on VDD)				
I _{ON,NV}	System ON base current, no RAM retention, Normal voltage		0.7		μΑ
	mode (supply on VDD)				
I _{OFF,HV}	System OFF current, no RAM retention, High voltage mode		0.4		μΑ
	(supply on VDDH)				
I _{ON,HV}	System ON base current, no RAM retention, High voltage mode		0.7		μΑ
	(supply on VDDH)				
I _{RAM}	Additional RAM retention current per 4 KB RAM section		30		nA

16.10.3 Device startup times

Symbol	Description	Min.	Тур.	Max.	Units
t _{POR}	Time in power-on reset after VDD reaches V,dd,start for all				
	supply voltages and temperatures. Dependent on supply rise				
	time.				
t _{POR,10μs}	VDD rise time 10 μs		1	10	ms
t _{POR,10ms}	VDD rise time 10 ms ¹⁰		9		ms
t _{POR,60ms}	VDD rise time 60 ms ¹⁰		23	110	ms
t _{RISE,REGOOUT}	REGO output (VDD) rise time after VDDH reaches minimum				
	VDDH supply voltage ¹⁰				
t _{RISE,REGOOUT,10μs}	VDDH rise time 10 μs^{10}		0.22	1.55	ms
t _{RISE,REGOOUT,10ms}	VDDH rise time 10 ms ¹⁰		5		ms
t _{RISE,REGOOUT,100ms}	VDDH rise time 100 ms ¹⁰	30	50	80	ms
t _{PINR}	If a GPIO pin is configured as reset, the maximum time taken				
	to pull up the pin and release reset after power-on reset.				
	Dependent on the pin capacitive load.				
t _{PINR,500nF}	500 nF capacitance at reset pin			32.5	ms
t _{PINR,10μ} F	10 μF capacitance at reset pin			650	ms
t _{R2ON}	Time from power-on reset to System ON				
t _{R2ON,NOTCONF}	If reset pin not configured.	tPOR			ms
t _{R2ON,CONF}	If reset pin configured.	tPOR +			ms
		tPINR			
t _{OFF2ON}	Time from OFF to CPU execute.		16.5		μs
t _{IDLE2CPU}	Time from IDLE to CPU execute.		3.0		μs
t _{EVTSET,CL1}	Time from HW event to PPI event in Constant Latency System		0.0625		μs
	ON mode.				
t _{EVTSET,CL0}	Time from HW event to PPI event in Low Power System ON		0.0625		μs
	mode				

16.10.4 Power fail comparator

Symbol	Description	Min.	Тур.	Max.	Units
$V_{POF,NV}$	Nominal power level warning thresholds (falling supply	1.7		2.8	V
	voltage) in Normal voltage mode (supply on VDD). Levels are				
	configurable between Min. and Max. in 100 mV increments.				
$V_{POF,HV}$	Nominal power level warning thresholds (falling supply voltage)	2.7		4.2	V
	in High voltage mode (supply on VDDH). Levels are configurable				
	in 100 mV increments.				
V _{POFTOL}	Threshold voltage tolerance (applies in both Normal voltage	-5		5	%
	mode and High voltage mode)				
$V_{POFHYST}$	Threshold voltage hysteresis (applies in both Normal voltage	40	50	60	mV
	mode and High voltage mode)				

¹⁰ See *Recommended operating conditions* on page 17 for more information.



Symbol	Description	Min.	Тур.	Max.	Units
V _{BOR,OFF}	Brownout reset voltage range System OFF mode. Brownout only	1.2		1.62	V
	applies to the voltage on VDD.				
V _{BOR,ON}	Brownout reset voltage range System ON mode. Brownout only	1.57	1.6	1.63	V
	applies to the voltage on VDD.				

16.10.5 USB operating conditions

Symbol	Description	Min.	Тур.	Max.	Units
V _{BUS}	Supply voltage on VBUS pin.	4.35	5	5.5	V
V_{DPDM}	Voltage on D+ and D- lines	VSS - 0	3	VUSB33	+ V
		V		0.3 V	

16.10.6 USB regulator specifications

Symbol	Description	Min.	Тур.	Max.	Units
I _{USB,QUIES}	USB regulator quiescence current drawn from Vbus (USBD		170		μΑ
	enabled).				
t _{USBPWRRDY}	Time from USB enabled to USBPWRRDY event triggered, V_{BUS}		1		ms
	supply provided.				
V _{USB33}	On voltage at the USB regulator output (DECUSB pin)	3.0	3.3	3.6	V
R _{SOURCE,VBUS}	Maximum source resistance on Vbus, incl. cable			2	Ω

16.10.7 VBUS detection specifications

Symbol	Description	Min.	Тур.	Max.	Units
V _{BUS,DETECT}	Voltage at which rising VBUS gets reported by USBDETECTED	3.45	4.01	4.26	V
V _{BUS,REMOVE}	Voltage at which decreasing VBUS gets reported by	3.1	3.61	3.84	V
	USBREMOVED				



17 CLOCK — Clock control

The clock control system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. Clock distribution is automated and grouped independently by module to limit current consumption in unused branches of the clock tree.

Listed here are the main features for CLOCK:

- 64 MHz on-chip oscillator
- 64 MHz crystal oscillator, using external 32 MHz crystal
- 32.768 kHz +/-500 ppm RC oscillator
- 32.768 kHz crystal oscillator, using external 32.768 kHz crystal
- · 32.768 kHz oscillator synthesized from 64 MHz oscillator
- Firmware (FW) override control of crystal oscillator activity for low latency start up
- Automatic internal oscillator and clock control, and distribution for ultra-low power

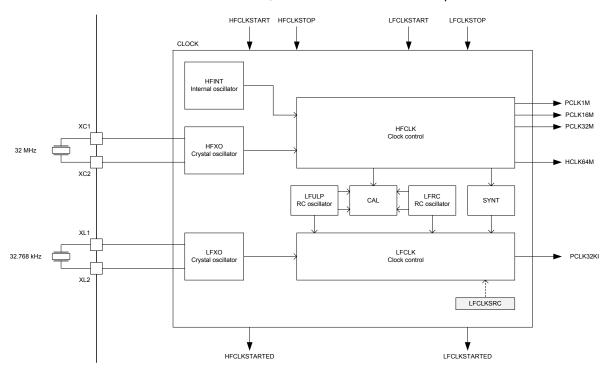


Figure 17: Clock control

17.1 HFCLK clock controller

The HFCLK clock controller provides the following clocks to the system.

- HCLK64M: 64 MHz CPU clock
- PCLK1M: 1 MHz peripheral clock
- PCLK16M: 16 MHz peripheral clock
- PCLK32M: 32 MHz peripheral clock

The HFCLK controller supports the following high frequency clock (HFCLK) sources:

- 64 MHz internal oscillator (HFINT)
- 64 MHz crystal oscillator (HFXO)

For illustration, see Figure 17: Clock control on page 141.



When the system requests one or more clocks from the HFCLK controller, the HFCLK controller will automatically provide them. If the system does not request any clocks provided by the HFCLK controller, the controller will enter a power saving mode.

These clocks are only available when the system is in ON mode. When the system enters ON mode, the internal oscillator (HFINT) clock source will automatically start to be able to provide the required HFCLK clock(s) for the system.

The HFINT will be used when HFCLK is requested and HFXO has not been started.

The HFXO is started by triggering the HFCLKSTART task and stopped by triggering the HFCLKSTOP task. When the HFCLKSTART task is triggered, the HFCLKSTARTED event is generated once the HFXO startup time has elapsed. The HFXO startup time is given as the sum of the following:

- HFXO power-up time, as specified in 64 MHz crystal oscillator (HFXO) on page 150.
- HFXO debounce time, as specified in the HFXODEBOUNCE on page 148 register.

The HFXO must be running to use the RADIO or the calibration mechanism associated with the 32.768 kHz RC oscillator.

17.1.1 64 MHz crystal oscillator (HFXO)

The 64 MHz crystal oscillator (HFXO) is controlled by a 32 MHz external crystal

The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet.

Figure 18: Circuit diagram of the 64 MHz crystal oscillator on page 142 shows how the 32 MHz crystal is connected to the 64 MHz crystal oscillator.

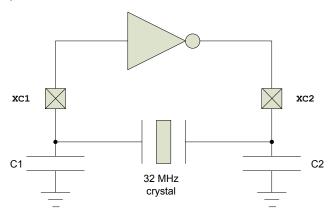


Figure 18: Circuit diagram of the 64 MHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{\left(C1' \cdot C2'\right)}{\left(C1' + C2'\right)}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

 $C2' = C2 + C_{pcb2} + C_{pin}$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. For more information, see *Reference circuitry* on page 688. C_{pcb1} and C_{pcb2} are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the xc1 and xc2 pins. See table *64 MHz crystal oscillator (HFXO)* on page 150. The load capacitors C1 and C2 should have the same value.



For reliable operation, the crystal load capacitance, shunt capacitance, equivalent series resistance, and drive level must comply with the specifications in table 64 MHz crystal oscillator (HFXO) on page 150. It is recommended to use a crystal with lower than maximum load capacitance and/or shunt capacitance. A low load capacitance will reduce both start up time and current consumption.

17.2 LFCLK clock controller

The system supports several low frequency clock sources.

As illustrated in *Figure 17: Clock control* on page 141, the system supports the following low frequency clock sources:

- 32.768 kHz RC oscillator (LFRC)
- 32.768 kHz crystal oscillator (LFXO)
- 32.768 kHz synthesized from HFCLK (LFSYNT)

The LFCLK clock controller and all of the LFCLK clock sources are always switched off when in OFF mode.

The LFCLK clock is started by first selecting the preferred clock source in register *LFCLKSRC* on page 148 and then triggering the LFCLKSTART task. If the LFXO is selected as the clock source, the LFCLK will initially start running from the 32.768 kHz LFRC while the LFXO is starting up and automatically switch to using the LFXO once this oscillator is running. The LFCLKSTARTED event will be generated when the LFXO has been started.

The LFCLK clock is stopped by triggering the LFCLKSTOP task.

The *LFCLKSRC* on page 148 register controls the clock source, and its allowed swing. The truth table for various situations is as follows:

Table 17: LFCLKSRC configuration depending on clock source

SRC	EXTERNAL	BYPASS	Comment
0	0	0	Normal operation, RC is source
0	0	1	DO NOT USE
0	1	Χ	DO NOT USE
1	0	0	Normal XTAL operation
1	1	0	Apply external low swing signal to XL1, ground XL2
1	1	1	Apply external full swing signal to XL1, leave XL2 grounded or unconnected
1	0	1	DO NOT USE
2	0	0	Normal operation, synth is source
2	0	1	DO NOT USE
2	1	Χ	DO NOT USE

It is not allowed to write to register *LFCLKSRC* on page 148 when the LFCLK is running.

A LFCLKSTOP task will stop the LFCLK oscillator. However, the LFCLKSTOP task can only be triggered after the STATE field in register *LFCLKSTAT* on page 147 indicates a 'LFCLK running' state.

The synthesized 32.768 kHz clock depends on the HFCLK to run. If high accuracy is required for the LFCLK running off the synthesized 32.768 kHz clock, the HFCLK must be generated from the HFCLK crystal oscillator.

17.2.1 32.768 kHz RC oscillator (LFRC)

The default source of the low frequency clock (LFCLK) is the 32.768 kHz RC oscillator (LFRC).

The LFRC oscillator has two modes of operation, that is normal and ultra-low power (ULP) mode, enabling the user to trade power consumption against accuracy of the clock. The mode/status of the LFRC is selected/read in the *LFRCMODE* on page 149 register. It is allowed to change LFRC mode when the LFRC oscillator is running.

The LFRC frequency will be affected by variation in temperature. The LFRC oscillator can be calibrated to improve accuracy by using the HFXO as a reference oscillator during calibration. The LFRC oscillator does not require additional external components.



17.2.2 Calibrating the 32.768 kHz RC oscillator

After any of the two 32.768 kHz RC oscillators are started and running, they can be calibrated by triggering the CAL task. The 32.768 kHz RC oscillator will then temporarily request the HFCLK to be used as a reference for the calibration.

A DONE event will be generated when calibration has finished. The calibration mechanism will only work as long as HFCLK is generated from the HFCLK crystal oscillator, it is therefore necessary to explicitly start this crystal oscillator before calibration can be started, see HFCLKSTART task.

It is not allowed to stop the LFRC or write to LFRCMODE on page 149 during an ongoing calibration.

17.2.3 Calibration timer

The calibration timer can be used to time the calibration interval of the 32.768 kHz RC oscillator.

The calibration timer is started by triggering the CTSTART task and stopped by triggering the CTSTOP task. The calibration timer will always start counting down from the value specified in CTIV and generate a CTTO timeout event when it reaches 0. The Calibration timer will stop by itself when it reaches 0.

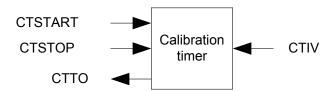


Figure 19: Calibration timer

Due to limitations in the calibration timer, only one task related to calibration, that is, CAL, CTSTART and CTSTOP, can be triggered for every period of LFCLK.

17.2.4 32.768 kHz crystal oscillator (LFXO)

For higher LFCLK accuracy (when better than +/- 500 ppm accuracy is required), the low frequency crystal oscillator (LFXO) must be used.

The following external clock sources are supported:

- Low swing clock signal applied to the XL1 pin. The XL2 pin shall then be grounded.
- Rail-to-rail clock signal applied to the XL1 pin. The XL2 pin shall then be grounded or left unconnected.

To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. *Figure 20: Circuit diagram of the 32.768 kHz crystal oscillator* on page 144 shows the LFXO circuitry.

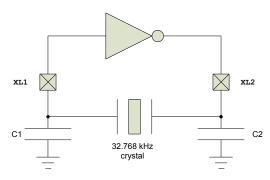


Figure 20: Circuit diagram of the 32.768 kHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:



$$CL = \frac{\left(C1' \cdot C2'\right)}{\left(C1' + C2'\right)}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

$$C2' = C2 + C_{pcb2} + C_{pin}$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_{pcb1} and C_{pcb2} are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the XC1 and XC2 pins (see *Low frequency crystal oscillator (LFXO)* on page 150). The load capacitors C1 and C2 should have the same value.

For more information, see Reference circuitry on page 688.

17.2.5 32.768 kHz synthesized from HFCLK (LFSYNT)

LFCLK can also be synthesized from the HFCLK clock source. The accuracy of LFCLK will then be the accuracy of the HFCLK.

Using the LFSYNT clock avoids the requirement for a 32.768 kHz crystal, but increases average power consumption as the HFCLK will need to be requested in the system.

17.3 Registers

Table 18: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40000000	CLOCK	CLOCK	Clock control		

Table 19: Register Overview

Register	Offset	Description	
TASKS_HFCLKSTART	0x000	Start HFCLK crystal oscillator	
TASKS_HFCLKSTOP	0x004	Stop HFCLK crystal oscillator	
TASKS_LFCLKSTART	0x008	Start LFCLK source	
TASKS_LFCLKSTOP	0x00C	Stop LFCLK source	
TASKS_CAL	0x010	Start calibration of LFRC or LFULP oscillator	
TASKS_CTSTART	0x014	Start calibration timer	
TASKS_CTSTOP	0x018	Stop calibration timer	
EVENTS_HFCLKSTARTED	0x100	HFCLK oscillator started	
EVENTS_LFCLKSTARTED	0x104	LFCLK started	
EVENTS_DONE	0x10C	Calibration of LFCLK RC oscillator complete event	
EVENTS_CTTO	0x110	Calibration timer timeout	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
HFCLKRUN	0x408	Status indicating that HFCLKSTART task has been triggered	
HFCLKSTAT	0x40C	HFCLK status	
LFCLKRUN	0x414	Status indicating that LFCLKSTART task has been triggered	
LFCLKSTAT	0x418	LFCLK status	
LFCLKSRCCOPY	0x41C	Copy of LFCLKSRC register, set when LFCLKSTART task was triggered	
LFCLKSRC	0x518	Clock source for the LFCLK	
HFXODEBOUNCE	0x528	HFXO debounce time. The HFXO is started by triggering the TASKS_HFCLKSTART task.	
CTIV	0x538	Calibration timer interval	Retained
TRACECONFIG	0x55C	Clocking options for the Trace Port debug interface	
LFRCMODE	0x5B4	LFRC mode configuration	



17.3.1 INTENSET

Address offset: 0x304

Enable interrupt

Bitı	number			31	30	29	28 2	7 26	25	24	23 2	22 2:	1 2	0 19	9 18	3 17	16	15	14 1	.3 1	.2 11	1 10	9	8	7	6 !	5 4	1 3	2	1)
Id																											0) С		В	4
Res	et 0x0000000	0		0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0 (0 0	0	0	0	כ
Id	RW Field		Value Id	Va	lue						Des	script	tion	1																	
Α	RW HFCLK	STARTED								,	Wri	ite '1	' to	Ena	ble	inte	erru	pt f	or H	FCL	.KST	ARTI	ED e	ever	nt						
										:	See	EVE	NTS	S_H	FCL	KSTA	ART	ED													
			Set	1							Ena	able																			
			Disabled	0							Rea	ad: Di	isab	oled																	
			Enabled	1							Rea	ad: Er	nab	led																	
В	RW LFCLK	STARTED								,	Wri	ite '1	' to	Ena	ble	inte	erru	pt f	or L	FCL	KSTA	ARTE	D e	ven	t						
										:	See	EVE	NTS	S_LF	CLF	STA	RT	D													
			Set	1							Ena	able																			
			Disabled	0							Rea	ad: Di	isab	oled																	
			Enabled	1						-	Rea	ad: Er	nab	led																	
С	RW DONE									,	Wri	ite '1	' to	Ena	ble	inte	erru	pt f	or D	ON	E ev	ent									
											See	EVE	NTS	S_D	ONI	Ē															
			Set	1							Ena	able																			
			Disabled	0							Rea	ad: Di	isab	oled																	
			Enabled	1							Rea	ad: Er	nab	led																	
D	RW CTTO									,	Wri	ite '1	' to	Ena	ble	inte	erru	pt f	or C	TTC	eve	ent									
										;	See	EVE	NTS	s_ <i>c</i> :	гто																
			Set	1							Ena	able																			
			Disabled	0							Rea	ad: Di	isab	oled																	
			Enabled	1							Rea	ad: Er	nab	led																	

17.3.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit	numbe	er		31 30 29	28 27	26 25	24 2	23 22	21 20	19 1	18 1	7 16	15 1	14 13	3 12	11 10	9	8	7	5 5	4	3	2 1	0
Id																					D	С	В	Α
Res	et 0x0	0000000		0 0 0	0 0	0 0	0 (0 0	0 0	0	0 (0 0	0	0 0	0	0 0	0	0	0	0 0	0	0 (0	0
Id	RW	Field	Value Id	Value			0	Descr	iption															
Α	RW	HFCLKSTARTED					٧	Vrite	'1' to	Disab	ole ii	nterr	upt f	or H	CLK	STAR	ΓED	ever	nt					
							c	oo F	VENTS	нес	יו עכ	TADT	ED											
			CI.							_111 C	LKS	IANI	LD											
			Clear	1				Disab																
			Disabled	0			R	Read:	Disab	led														
			Enabled	1			R	Read:	Enabl	ed														
В	RW	LFCLKSTARTED					٧	Vrite	'1' to	Disab	ole ii	nterr	upt f	or LF	CLKS	START	ED 6	even	t					
							ς	ee F	VENTS	LEC	I KST	TART	FD											
			Clear	1				Disab																
				_					: Disab															
			Disabled	0																				
			Enabled	1					Enabl															
С	RW	DONE					٧	Vrite	'1' to	Disab	ole ii	nterr	upt f	or D	ONE	event								
							S	see <i>E</i>	VENTS	_DOI	V <i>E</i>													
			Clear	1				Disab	le															
			Disabled	0			R	Read:	Disab	ed														
			Enabled	1					Enabl															
D	R\M/	СТТО		_					'1' to		رز مار	nterr	unt f	or C	TO 4	ovent								
0	1.00	CITO					V	viile	1 10	Disak	JIC II	itell	upti	or C	10 (LVCIIL								
							S	ee E	VENTS	CTT	0													



Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

17.3.3 HFCLKRUN

Address offset: 0x408

Status indicating that HFCLKSTART task has been triggered

Bitı	numbe	er		31 30	29	28	3 27	26	25	24	23 :	22 2	1 20	0 19	18	17	16	15	14 1	.3 1	2 11	10	9	8	7	6	5	4 3	2	1	0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Valu	е						Des	crip	tion	ı																	
Α	R	STATUS									HFC	CLKS	TAR	T ta	sk tı	rigg	ere	d or	not												
			NotTriggered	0							Tasl	k no	t tri	gger	ed																
			Triggered	1							Tasl	k trig	gger	ed																	

17.3.4 HFCLKSTAT

Address offset: 0x40C

HFCLK status

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					В
Re	set 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
Α	R	SRC			Source of HFCLK
			RC	0	64 MHz internal oscillator (HFINT)
			Xtal	1	64 MHz crystal oscillator (HFXO)
В	R	STATE			HFCLK state
			NotRunning	0	HFCLK not running
			Running	1	HFCLK running

17.3.5 LFCLKRUN

Address offset: 0x414

Status indicating that LFCLKSTART task has been triggered

Bit	numb	er		31 30	29	28 2	27 :	26 2	25 2	24 2	23 2	22 2	1 20	19	18	17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value							Des	crip	tion																		
Α	R	STATUS								L	_FCI	LKST	ART	tas	k tr	igg	ere	d or	no	t											
			NotTriggered	0						7	Гasl	c no	tri	gger	ed																
			Triggered	1						1	Гasl	c trig	ger	ed																	

17.3.6 LFCLKSTAT

Address offset: 0x418

LFCLK status

Bit r	iumbe	er		31	30 2	9 :	28 2	7 2	6 2	5 2	4 2	3 2	22 2	21 2	20 :	19 :	18 2	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																			В														,	4 А
Rese	et OxO	0000000		0	0	0	0 (0) () (0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						C	es	crip	otio	n																			
Α	R	SRC									S	oui	rce	of I	LFC	LK																		



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B A A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	RC	0	32.768 kHz RC oscillator
	Xtal	1	32.768 kHz crystal oscillator
	Synth	2	32.768 kHz synthesized from HFCLK
B R STATE			LFCLK state
	NotRunning	0	LFCLK not running
	Running	1	LFCLK running

17.3.7 LFCLKSRCCOPY

Address offset: 0x41C

Copy of LFCLKSRC register, set when LFCLKSTART task was triggered

Bit r	iumbe	er		3:	1 30	29	9 28	8 27	7 20	6 25	5 24	1 2	3 22	2 21	. 20	19	18	17	16	15	14	13	3 12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	2						D	esc	ript	ion																			
Α	R	SRC										С	lock	soı	ırce	•																		
			RC	0								3	2.76	8 k	Hz f	RC o	osci	llat	or															
			Xtal	1								3	2.76	8 k	Hz	rys	tal	osc	illa	tor														
			Synth	2								3	2.76	58 k	Hz s	synt	he	size	d fr	om	n HF	CLI	K											

17.3.8 LFCLKSRC

Address offset: 0x518

Clock source for the LFCLK

Bit r	numbe	er		31	30 2	9 2	8 27	7 2	6 25	5 2	4 23	22	21 2	0 1	19 1	8 :	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																	С	В														,	А А
Res	et 0x0	0000000		0	0 () (0 0) (0	C	0 0	0	0 (כ	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						De	scr	iptio	ı																			
Α	RW	SRC									Clo	ock	sour	e																			
			RC	0							32.	.76	8 kHz	RC	os	cilla	ato	r															
			Xtal	1							32.	.76	8 kHz	cr	ysta	Ιo	scil	lat	or														
			Synth	2							32.	.76	8 kHz	sy	nth	esi	zec	l fr	om	HF	CLK												
В	RW	BYPASS									Ena	able	e or c	lisa	ble	by	pas	ss c	of L	FCL	Кс	ryst	al d	osci	llate	or w	/ith	ext	err	al			
											clo	ck :	sourc	e																			
			Disabled	0							Dis	sabl	e (us	e v	vith	Xt	al c	r lo	ow-	SW	ng	ext	ern	al s	our	ce)							
			Enabled	1							Ena	able	e (use	e w	ith	rail	-to	-ra	il e	xte	rna	l so	urc	e)									
С	RW	EXTERNAL									Ena	able	e or c	lisa	ble	ex	ter	nal	so	urc	e fo	r L	FCL	K									
			Disabled	0							Dis	sabl	e ext	err	nal s	ou	rce	e (u	se	wit	h Xt	al)											
			Enabled	1							Ena	able	e use	of	ext	err	al	sοι	ırce	in	stea	ad o	of X	tal	(SR	C ne	ed	s to	be				
											set	t to	Xtal)																				

17.3.9 HFXODEBOUNCE

Address offset: 0x528

HFXO debounce time. The HFXO is started by triggering the TASKS_HFCLKSTART task.

The EVENTS_HFCLKSTARTED event is generated after the HFXO power up time + the HFXO debounce time has elapsed. It is not allowed to change the value of this register while the HFXO is starting.



Bit	numb	er		31	30 2	29 2	8 27	7 26	25	24 :	23 2	22 2	1 2	0 1	9 18	3 17	16	15	14	13 :	L2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																									Α	Α	Α	Α	АА	A	Α
Res	et 0x0	0000010		0	0	0 (0 0	0	0	0	0	0 (0 (0 (0	0	0	0	0	0	0 (0	0	0	0	0	0	1	0 0	0	0
Id	RW	Field	Value Id	Va	lue					ı	Des	crip	tio	n																	
Α	RW	HFXODEBOUNCE		0x0	010	xFF					HFX	O d	ebc	uno	e ti	me.	De	oou	nce	tim	e =	HFX	ODE	ВО	UN	CE *	16				
											IS.																				

17.3.10 CTIV (Retained)

Address offset: 0x538

This register is a retained register

Calibration timer interval

Bit	numbe	er		31	30	29	28 2	27 20	5 2	5 24	1 23	3 22	21	20	19 1	8 1	7 1	5 15	14	13	12	11 :	10	9	8	7	6 !	5 4	3	2	1	0
Id																											A A	4 Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	escri	ptic	on																		
Α	RW	CTIV									Ca	libr	atio	n tiı	ner	inte	rva	l in ı	mul	tipl	e of	0.2	5 se	COI	nds.	Ra	nge	:				_
											_						_															

0.25 seconds to 31.75 seconds.

17.3.11 TRACECONFIG

Address offset: 0x55C

Clocking options for the Trace Port debug interface

This register is a retained register. Reset behavior is the same as debug components.

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			в в
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW TRACEPORTSPEED			Speed of Trace Port clock. Note that the TRACECLK pin will
			output this clock divided by two.
	32MHz	0	32 MHz Trace Port clock (TRACECLK = 16 MHz)
	16MHz	1	16 MHz Trace Port clock (TRACECLK = 8 MHz)
	8MHz	2	8 MHz Trace Port clock (TRACECLK = 4 MHz)
	4MHz	3	4 MHz Trace Port clock (TRACECLK = 2 MHz)
B RW TRACEMUX			Pin multiplexing of trace signals. See pin assignment chapter for
			more details.
	GPIO	0	No trace signals routed to pins. All pins can be used as regular
			GPIOs.
	Serial	1	SWO trace signal routed to pin. Remaining pins can be used as
			regular GPIOs.
	Parallel	2	All trace signals (TRACECLK and TRACEDATA[n]) routed to pins.

17.3.12 LFRCMODE

Address offset: 0x5B4 LFRC mode configuration

Bit r	numbe	r		31	. 30	29	28	27 2	26 2	25 2	24 2	23 2	2 2	1 20	2 19	9 18	3 17	7 16	5 15	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		В																Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cript	ion	ı																			
Α	RW	MODE									9	Set I	FRC	m	ode																			
			Normal	0							1	Vori	mal	mo	de																			
			ULP	1							ι	Jltra	a-lov	v p	owe	er n	nod	e (l	JLP)														
В	RW	STATUS									A	Acti	ve LI	RC	mo	de.	. Th	is f	ield	is	rea	d on	ly.											
			Normal	0							1	Vori	mal	mo	de																			



Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Id			В			
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			
Id RW Field	Value Id	Value	Description			
	ULP	1	Ultra-low power mode (ULP)			

17.4 Electrical specification

17.4.1 64 MHz internal oscillator (HFINT)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_HFINT}	Nominal output frequency		64		MHz
f _{TOL_HFINT}	Frequency tolerance		±1.5	±8	%

17.4.2 64 MHz crystal oscillator (HFXO)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_HFXO}	Nominal output frequency		64		MHz
f_{XTAL_HFXO}	External crystal frequency		32		MHz
f_{TOL_HFXO}	Frequency tolerance requirement for 2.4 GHz proprietary radio			±60	ppm
	applications				
$f_{TOL_HFXO_BLE}$	Frequency tolerance requirement, Bluetooth low energy			±40	ppm
	applications				
C_{L_HFXO}	Load capacitance			12	pF
C _{0_HFXO}	Shunt capacitance			7	pF
R _{S_HFXO_7PF}	Equivalent series resistance C0 = 7 pF			60	ohm
R _{S_HFXO_5PF}	Equivalent series resistance C0 = 5 pF			60	ohm
R _{S_HFXO_3PF}	Equivalent series resistance C0 = 3 pF			100	ohm
P _{D_HFXO}	Drive level			100	μW
C _{PIN_HFXO}	Input capacitance XC1 and XC2		3		pF
I _{STBY_X32M}	Core standby current for various crystals				
I _{STBY_X32M_X0}	Epson TSX-3225		80		μΑ
I _{STBY_X32M_X1}	Epson FA-20H		72		μΑ
I _{STBY_X32M_X2}	Epson FA-128		70		μΑ
I _{STBY_X32M_X3}	NDK NX1612AA		136		μΑ
I _{STBY_X32M_X4}	NDK NX1210AB		143		μΑ
I _{START_X32M}	Average startup current for various crystals, first 1 ms				
I _{START_X32M_X0}	Epson TSX-3225		328		μΑ
I _{START_X32M_X1}	Epson FA-20H		363		μΑ
I _{START_X32M_X2}	Epson FA-128		396		μΑ
I _{START_X32M_X3}	NDK NX1612AA		783		μΑ
I _{START_X32M_X4}	NDK NX1210AB		833		μΑ
t _{POWER_X32M}	Power-up time				μs
t _{START_X32M}	Startup time for various crystals				
t _{START_X32M_X0}	Epson TSX-3225		304		μs
$t_{START_X32M_X1}$	Epson FA-20H		316		μs
t _{START_X32M_X2}	Epson FA-128		328		μs
t _{START_X32M_X3}	NDK NX1612AA				μs
t _{START_X32M_X4}	NDK NX1210AB				μs

17.4.3 Low frequency crystal oscillator (LFXO)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_LFXO}	Crystal frequency		32.768		kHz
f _{TOL_LFXO_BLE}	Frequency tolerance requirement for BLE stack			±500	ppm
f _{TOL_LFXO_ANT}	Frequency tolerance requirement for ANT stack			±50	ppm
C _{L_LFXO}	Load capacitance			12.5	pF



Symbol	Description	Min.	Тур.	Max.	Units
C _{0_LFXO}	Shunt capacitance			2	pF
R _{S_LFXO}	Equivalent series resistance			100	kohm
P _{D_LFXO}	Drive level			1	uW
C _{pin}	Input capacitance on XL1 and XL2 pads		4		pF
I _{LFXO}	Run current for 32.768 kHz crystal oscillator		0.23		μΑ
t _{START_LFXO}	Startup time for 32.768 kHz crystal oscillator		0.25		S

17.4.4 Low frequency RC oscillator (LFRC), Normal mode

Symbol	Description	Min.	Тур.	Max.	Units
f_{NOM_LFRC}	Nominal frequency		32.768		kHz
f _{TOL_LFRC}	Frequency tolerance, uncalibrated			±2.5	%
f _{TOL_CAL_LFRC}	Frequency tolerance after calibration ¹¹			±500	ppm
I _{LFRC}	Run current		0.7		μΑ
t _{START LFRC}	Startup time		1000		us

17.4.5 Low frequency RC oscillator (LFRC), Ultra-low power mode (ULP)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_LFULP}	Nominal frequency		32.768		kHz
f _{TOL_UNCAL_LFULP}	Frequency tolerance, uncalibrated			±7	%
f _{TOL_CAL_LFULP}	Frequency tolerance after calibration 12			±2000	ppm
I _{LFULP}	Run current		0.2		μΑ
t _{START_LFULP}	Startup time		1500		us

17.4.6 Synthesized low frequency clock (LFSYNT)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_LFSYNT}	Nominal frequency		32.768		kHz

Constant temperature within ± 0.5 °C and calibration performed at least every 8 seconds, defined as 3 sigma Constant temperature within ± 0.5 °C and calibration performed at least every 8 seconds, defined as 3 sigma



18 Power and clock management

Power and clock management in nRF52840 is optimized for ultra-low power applications.

The core of the power and clock management system is the Power Management Unit (PMU) illustrated in *Figure 21: Power Management Unit* on page 152.

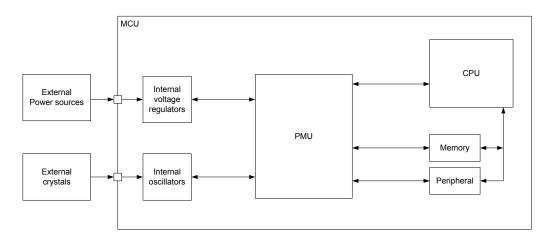


Figure 21: Power Management Unit

The user application is not required to actively control power and clock, since the PMU is able to automatically detect which resources are required by the different components in the system at any given time. The PMU will continuously optimize the system based on this information to achieve the lowest power consumption possible without user interaction.

18.1 Current consumption scenarios

As the system is being constantly tuned by the PMU, estimating the energy consumption of an application can be challenging if the designer is not able to do measurements on the hardware directly. To facilitate this process, there is a defined set of current consumption scenarios.

See *Electrical specification* on page 152 for application scenarios showing average current drawn from the VDD supply.

Each scenario specifies a set of active operations and conditions applying to the given scenario. *Table 20: Current consumption scenarios, common conditions* on page 152 shows the conditions used for a scenario unless otherwise is stated in the scenario description.

Table 20: Current consumption scenarios, common conditions

Condition	Value
VDD	3 V
Temperature	25°C
CPU	WFI/WFE sleep
Peripherals	All idle
Clock	Not running
Regulator	DC/DC

18.1.1 Electrical specification

Current consumption: Radio

Symbol	Description	Min.	Тур.	Max.	Units
I _{RADIO_TX0}	0 dBm TX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO		6.6		mA
I _{RADIO_TX1}	-40 dBm TX @ 1 Mb/s Bluetooth Low Energy mode, Clock =				mA
	HFXO				



Symbol	Description	Min.	Тур.	Max.	Units
I _{RADIO_RX0}	Radio RX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO		6.4		mA
I _{RADIO_RX1}	Radio RX @ 2 Mb/s Bluetooth Low Energy mode, Clock = HFXO,		11		mA
	Regulator = LDO				
I _{RADIO_RX2}	Radio RX @ 2 Mb/s Bluetooth Low Energy mode, Clock = HFXO,		12.6		mA
	Regulator = LDO				
I _{RADIO_RX2}	Radio RX @ 125 kb/s Bluetooth Low Energy mode, Clock =		10.9		mA
	HFXO, Regulator = LDO				

Current consumption: Radio protocol configurations

Symbol	Description	Min.	Тур.	Max.	Units
I _{SO}	CPU running CoreMark from Flash, Radio 0 dBm TX @ 1 Mb/s		9.1		mA
	Bluetooth Low Energy mode, Clock = HFXO, Cache enabled				
I _{S1}	CPU running CoreMark from Flash, Radio RX @ 1 Mb/s		8.9		mA
	Bluetooth Low Energy mode, Clock = HFXO, Cache enabled				
I _{S4}	CPU running CoreMark from Flash, Radio RX @ 1 Mb/s		7.5		mA
	Bluetooth Low Energy mode, Clock = HFXO, Cache enabled,				
	VDDH = 5V, REG0 out = 3V				

Current consumption: Ultra-low power

Symbol	Description	Min.	Тур.	Max.	Units
I _{ON_RAMOFF_EVENT}	System ON, No RAM retention, Wake on any event				μΑ
I _{ON_RAMON_EVENT}	System ON, Full RAM retention, Wake on any event				μΑ
I _{ON_RAMOFF_RTC}	System ON, No RAM retention, Wake on RTC (LFCLK = LFRC,		1.3		μΑ
	normal mode)				
I _{OFF_RAMOFF_RESET}	System OFF, No RAM retention, Wake on reset				μΑ
I _{OFF_RAMOFF_GPIO}	System OFF, No RAM retention, Wake on GPIO				μΑ
I _{OFF_RAMOFF_LPCOMP}	System OFF, No RAM retention, Wake on LPCOMP				μΑ
I _{OFF_RAMOFF_NFC}	System OFF, No RAM retention, Wake on NFC field				μΑ
I _{OFF_RAMON_RESET}	System OFF, Full RAM retention, Wake on reset				μΑ

Current consumption: Serial interfaces

Symbol	Description	Min.	Тур.	Max.	Units
I _{SPIM,IDLE}	SPIM Idle (enabled, no ongoing data transfer)				mA
I _{SPIM,ACTIVE}	SPIM R+W data transfer, 1 MHz SCK frequency, Clock = HFINT				mA
I _{SPIS,IDLE}	SPIS Idle (enabled, started, no activity on CSN, CLK, MISO or				mA
	MOSI)				
I _{SPIS,ACTIVE}	SPIS R+W data transfer, 1 MHz SCK frequency, Clock = HFINT				mA
I _{TWIM,IDLE}	TWIM Idle (enabled, no ongoing data transfer)				mA
I _{TWIM,ACTIVE}	SPIM data transfer @ 400 kb/s, Clock = HFINT				mA
I _{TWIS,IDLE}	SPIS Idle (enabled, no ongoing data transfer, PREPARETX and/or				mA
	PREPARERX tasks triggered)				
I _{TWIS,ACTIVE}	SPIM data transfer @ 400 kb/s, Clock = HFINT				mA

Current consumption: CPU

Symbol	Description	Min.	Тур.	Max.	Units
I _{CPU0}	CPU running from Flash, Clock = HFXO				mA
I _{CPU1}	CPU running from RAM, Clock = HFXO				mA
I _{CPU2}	CPU running from Flash, Clock = HFINT				mA



19 GPIO — General purpose input/output

The general purpose input/output pins (GPIOs) are grouped as one or more ports with each port having up to 32 GPIOs.

The number of ports and GPIOs per port might vary with product variant and package. Refer to *Registers* on page 156 and *Pin assignments* on page 13 for more information about the number of GPIOs that are supported.

GPIO has the following user-configurable features:

- Up to 32 GPIO pins per GPIO port
- · Configurable output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on state changes on any pin
- All pins can be used by the PPI task/event system
- One or more GPIO outputs can be controlled through PPI and GPIOTE channels
- All pins can be individually mapped to interface blocks for layout flexibility
- GPIO state changes captured on SENSE signal can be stored by LATCH register

The GPIO Port peripheral implements up to 32 pins, PIN0 through PIN31. Each of these pins can be individually configured in the PIN_CNF[n] registers (n=0..31).

The following parameters can be configured through these registers:

- Direction
- · Drive strength
- Enabling of pull-up and pull-down resistors
- Pin sensing
- · Input buffer disconnect
- Analog input (for selected pins)

The PIN_CNF registers are retained registers. See <u>POWER — Power supply</u> on page 66 chapter for more information about retained registers.

19.1 Pin configuration

Pins can be individually configured, through the SENSE field in the PIN_CNF[n] register, to detect either a high level or a low level on their input.

When the correct level is detected on any such configured pin, the sense mechanism will set the DETECT signal high. Each pin has a separate DETECT signal, and the default behaviour, as defined by the DETECTMODE register, is that the DETECT signal from all pins in the GPIO Port are combined into a common DETECT signal that is routed throughout the system, which then can be utilized by other peripherals, see *Figure 22: GPIO Port and the GPIO pin details* on page 155. This mechanism is functional in both ON and OFF mode.



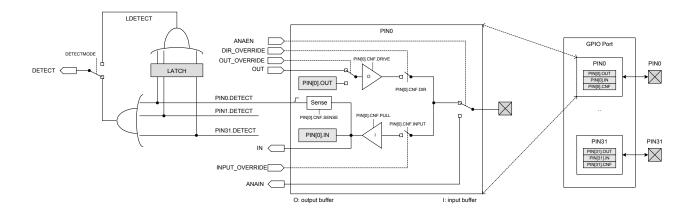


Figure 22: GPIO Port and the GPIO pin details

Figure 22: GPIO Port and the GPIO pin details on page 155 illustrates the GPIO port containing 32 individual pins, where PINO is illustrated in more detail as a reference. All the signals on the left side of the illustration are used by other peripherals in the system, and therefore, are not directly available to the CPU.

Make sure that a pin is in a level that cannot trigger the sense mechanism before enabling it. Detect will go high immediately if the sense condition configured in the PIN_CNF registers is met when the sense mechanism is enabled. This will trigger a PORT event if the DETECT signal was low before enabling the sense mechanism. See *GPIOTE* — *GPIO tasks and events* on page 200.

See the following peripherals for more information about how the DETECT signal is used:

- POWER: uses the DETECT signal to exit from System OFF.
- GPIOTE: uses the DETECT signal to generate the PORT event.

When a pin's PINx.DETECT signal goes high, a flag will be set in the LATCH register, e.g. when the PIN0.DETECT signal goes high, bit 0 in the LATCH register will be set to '1'.

The LATCH register will only be cleared if the CPU explicitly clears it by writing a '1' to the bit that shall be cleared, i.e. the LATCH register will not be affected by a PINx.DETECT signal being set low.

If the CPU performs a clear operation on a bit in the LATCH register when the associated PINx.DETECT signal is high, the bit in the LATCH register will not be cleared.

The LDETECT signal will be set high when one or more bits in the LATCH register are '1'. The LDETECT signal will be set low when all bits in the LATCH register are successfully cleared to '0'.

If one or more bits in the LATCH register are '1' after the CPU has performed a clear operation on the LATCH registers, a rising edge will be generated on the LDETECT signal, this is illustrated in *Figure 23: DETECT signal behavior* on page 156.

Important: The CPU can read the LATCH register at any time to check if a SENSE condition has been met on one or more of the the GPIO pins even if that condition is no longer met at the time the CPU queries the LATCH register. This mechanism will work even if the LDETECT signal is not used as the DETECT signal.

The LDETECT signal is by default not connected to the GPIO port's DETECT signal, but via the DETECTMODE register it is possible to change the behaviour of the GPIO port's DETECT signal from the default behaviour described above to instead be derived directly from the LDETECT signal, see *Figure 22: GPIO Port and the GPIO pin details* on page 155. *Figure 23: DETECT signal behavior* on page 156 illustrates the DETECT signals behaviour for these two alternatives.



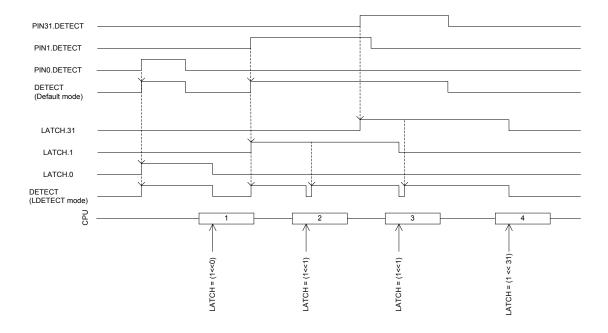


Figure 23: DETECT signal behavior

The input buffer of a GPIO pin can be disconnected from the pin to enable power savings when the pin is not used as an input, see *Figure 22: GPIO Port and the GPIO pin details* on page 155. Inputs must be connected in order to get a valid input value in the IN register and for the sense mechanism to get access to the pin.

Other peripherals in the system can attach themselves to GPIO pins and override their output value and configuration, or read their analog or digital input value, see *Figure 22: GPIO Port and the GPIO pin details* on page 155.

Selected pins also support analog input signals, see ANAIN in *Figure 22: GPIO Port and the GPIO pin details* on page 155. The assignment of the analog pins can be found in *Pin assignments* on page 13.

Important: When a pin is configured as digital input, care has been taken in the nRF52840 design to minimize increased current consumption when the input voltage is between V_{IL} and V_{IH} . However, it is a good practice to ensure that the external circuitry does not drive that pin to levels between V_{IL} and V_{IH} for a long period of time.

19.2 GPIO located near the RADIO

Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current close to the radio power supply and antenna pins.

Refer to *Pin assignments* on page 13 for recommended usage guidelines to maximize radio performance in an application.

19.3 Registers

Table 21: Instances

Base address	Peripheral	Instance	Description Configuration	
0x50000000	GPIO	GPIO	General purpose input and output	Deprecated
0x50000000	GPIO	P0	General purpose input and output, port 0 P0.00 to P0.31 implemented	
0x50000300	GPIO	P1	General purpose input and output, port 1 P1.00 to P1.15 implemented	



Table 22: Register Overview

Register	Offset	Description
OUT	0x504	Write GPIO port
OUTSET	0x508	Set individual bits in GPIO port
OUTCLR	0x50C	Clear individual bits in GPIO port
IN	0x510	Read GPIO port
DIR	0x514	Direction of GPIO pins
DIRSET	0x518	DIR set register
DIRCLR	0x51C	DIR clear register
LATCH	0x520	Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE
		registers
DETECTMODE	0x524	Select between default DETECT signal behaviour and LDETECT mode
PIN_CNF[0]	0x700	Configuration of GPIO pins
PIN_CNF[1]	0x704	Configuration of GPIO pins
PIN_CNF[2]	0x708	Configuration of GPIO pins
PIN_CNF[3]	0x70C	Configuration of GPIO pins
PIN_CNF[4]	0x710	Configuration of GPIO pins
PIN_CNF[5]	0x714	Configuration of GPIO pins
PIN_CNF[6]	0x718	Configuration of GPIO pins
PIN_CNF[7]	0x71C	Configuration of GPIO pins
PIN_CNF[8]	0x720	Configuration of GPIO pins
PIN_CNF[9]	0x724	Configuration of GPIO pins
PIN_CNF[10]	0x728	Configuration of GPIO pins
PIN_CNF[11]	0x72C	Configuration of GPIO pins
PIN_CNF[12]	0x730	Configuration of GPIO pins
PIN_CNF[13]	0x734	Configuration of GPIO pins
PIN_CNF[14]	0x738	Configuration of GPIO pins
PIN_CNF[15]	0x73C	Configuration of GPIO pins
PIN_CNF[16]	0x740	Configuration of GPIO pins
PIN_CNF[17]	0x744	Configuration of GPIO pins
PIN_CNF[18]	0x748	Configuration of GPIO pins
PIN_CNF[19]	0x74C	Configuration of GPIO pins
PIN_CNF[20]	0x750	Configuration of GPIO pins
PIN_CNF[21]	0x754	Configuration of GPIO pins
PIN_CNF[22]	0x758	Configuration of GPIO pins
PIN_CNF[23]	0x75C	Configuration of GPIO pins
PIN_CNF[24]	0x760	Configuration of GPIO pins
PIN_CNF[25]	0x764	Configuration of GPIO pins
PIN_CNF[26]	0x768	Configuration of GPIO pins
PIN_CNF[27]	0x76C	Configuration of GPIO pins
PIN_CNF[28]	0x770	Configuration of GPIO pins
PIN_CNF[29]	0x774	Configuration of GPIO pins
PIN_CNF[30]	0x778	Configuration of GPIO pins
PIN_CNF[31]	0x77C	Configuration of GPIO pins

19.3.1 OUT

Address offset: 0x504 Write GPIO port

Bit r	iumbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 :	20 :	19	18	17	16	15	14	13	12	11 1	LO	9	8	7	6	5	4	3 2	1	0
Id				f	е	d	С	b	а	Z	Υ	Х	W	V	U	Т	S	R	Q	Р	О	N	М	L	K	J	1 1	+ (G	F	Е	D C	В	Α
Rese	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scrip	otio	n																			
Α	RW	PIN0										Pin	n 0																					
			Low	0								Pin	driv	ver	is lo	wc																		
			High	1								Pin	driv	ver	is h	igh																		
В	RW	PIN1										Pin	1																					



Bit r	numbe	er		31 30	29 28	27	26 2	5 24	23	22 21	. 20	19	18 1	7 10	5 15	14	13 1	2 11	10	9	8 7	6	5	4	3 2	2 1	. 0
Id				f e	d c	b	a 2	<u> </u>	Х	w v	U	Т	S	R C	P	0	N N	1 L	K	J	I H	(i F	Ε	D (В	Α
Res	et 0x0	0000000		0 0	0 0	0	0 (0	0	0 0	0	0	0	0 0	0	0	0 (0	0	0	0 0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Value						scripti																	
			Low	0						drive																	
			High	1						drive	r is	high															
С	RW	PIN2	Low	0					Pin	ı 2 ı drivei	. i.	laur															
			High	1						ı drivei ı drivei																	
D	RW	PIN3	111611	-					Pin		1 13	шы															
			Low	0						drive	r is	low															
			High	1					Pin	drive	r is	high															
E	RW	PIN4							Pin	4																	
			Low	0					Pin	drive	r is	low															
			High	1					Pin	drive	r is	high															
F	RW	PIN5							Pin																		
			Low	0						drive																	
			High	1						drive	r is	high															
G	кW	PIN6	Low	0					Pin		. i	leve															
			Low	0						ı drivei ı drivei																	
Н	R\M/	PIN7	High	1					Pin		1 15	nign															
	11.00	11117	Low	0						ı , ı drivei	r is	low															
			High	1						drive																	
ı	RW	PIN8							Pin			Ü															
			Low	0					Pin	drive	r is	low															
			High	1					Pin	drive	r is	high															
J	RW	PIN9							Pin	9																	
			Low	0					Pin	drive	r is	low															
			High	1						drive	r is	high															
K	RW	PIN10		_						10																	
			Low	0						drive																	
L	D\A/	PIN11	High	1						ı drivei ı 11	rıs	nıgn															
-	IVV	LIMIT	Low	0						ı 11 ı drivei	r is	low															
			High	1						drive																	
М	RW	PIN12								12		Ü															
			Low	0					Pin	drive	r is	low															
			High	1					Pin	drive	r is	high															
N	RW	PIN13							Pin	13																	
			Low	0					Pin	drive	r is	low															
			High	1						drive	r is	high															
0	RW	PIN14	Low	0						14 . drivo	. :	la:															
			Low	0						drive																	
Р	RW/	PIN15	High	1						ı drivei ı 15	1 15	ıııgıı															
•	11.00	111123	Low	0						drive	r is	low															
			High	1						drive																	
Q	RW	PIN16								16		Ü															
			Low	0						drive	r is	low															
			High	1					Pin	drive	r is	high															
R	RW	PIN17							Pin	17																	
			Low	0					Pin	drive	r is	low															
			High	1						drive	r is	high															
S	RW	PIN18		_						18																	
			Low	0						drive																	
т	D\A/	DIN10	High	1						drive	r IS	nıgh															
Т	KVV	PIN19	Low	0						ı 19 ı drivei	r ic	low															
				J					- 41	. Grivel	. 13	.0 ٧٧															



Bit r	numbe	er		31 30	29	9 28	27	26	25	24	2	3 22 2	21	20 :	19	18 :	17 :	16	15	14 :	13 1	2 1	1 1	0 9) 8	3 7	6	5	4	3	2	1	0
Id				f e	d	С	b	а	Ζ	Υ	Х	(W	V	U	Т	S	R	Q	Р	О	N 1	И	LI	< J	ı	Н	G	i F	Ε	D	С	В	Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0) (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Value							D	escrip	tic	n																			
			High	1							Pi	in driv	er	is h	igh																		
U	RW	PIN20									Pi	in 20																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
٧	RW	PIN21									Pi	in 21																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
W	RW	PIN22									Pi	in 22																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
Χ	RW	PIN23									Pi	in 23																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
Υ	RW	PIN24									Pi	in 24																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
Z	RW	PIN25									Pi	in 25																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
а	RW	PIN26									Pi	in 26																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
b	RW	PIN27									Pi	in 27																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
С	RW	PIN28									Pi	in 28																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1								in driv	er	is h	igh																		
d	RW	PIN29									Pi	in 29																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
е	RW	PIN30										in 30																					
			Low	0								in driv																					
			High	1								in driv	er	is h	igh																		
f	RW	PIN31										in 31																					
			Low	0								in driv																					
			High	1							Pi	in driv	er	is h	igh																		

19.3.2 OUTSET

Address offset: 0x508

Set individual bits in GPIO port Read: reads value of OUT register.

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5 5 4 3 2 1 0
Id		fedcbaZYXWVUTSRQPONMLKJIH (F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0
Id RW Field	Value Id	Value Description	
A RW PINO		Pin 0	
	Low	0 Read: pin driver is low	
	High	1 Read: pin driver is high	
	Set	1 Write: writing a '1' sets the pin high; writing a '0' has no e	effect
B RW PIN1		Pin 1	
	Low	0 Read: pin driver is low	



Bit r	number			31 30	29 28	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x000	000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW F	Field	Value Id	Value				Description
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
С	RW F	PIN2	Loui	0				Pin 2
			Low High	0				Read: pin driver is low Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
D	RW F	PIN3		_				Pin 3
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Ε	RW F	PIN4						Pin 4
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
F	RW F	PIN5						Pin 5
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
G	RW F	DINE	Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect Pin 6
U	IVV F	- IIVO	Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Н	RW F	PIN7						Pin 7
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
I	RW F	PIN8						Pin 8
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
	DIA/ F	DINO	Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect Pin 9
J	RW F	PIN9	Low	0				Read: pin driver is low
			High	1				Read: pin driver is low
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
K	RW F	PIN10						Pin 10
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
L	RW F	PIN11						Pin 11
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
N 4	D\4/ 5	DIN12	Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
М	RW F	≺IINTZ	Low	0				Pin 12
			Low High	0				Read: pin driver is low Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
N	RW F	PIN13		•				Pin 13
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
0	RW F	PIN14						Pin 14
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Р	RW F	PIN15						Pin 15



Bit r	numbe	er		31 30	29 2	8 27	7 26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d d	c b	а	Z Y	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Res	et 0x0	0000000		0 0	0 (0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
0	D\A/	PIN16	Set	1					Write: writing a '1' sets the pin high; writing a '0' has no effect Pin 16
Q	KVV	LINTO	Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Set	1					Write: writing a '1' sets the pin high; writing a '0' has no effect
R	RW	PIN17							Pin 17
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Set	1					Write: writing a '1' sets the pin high; writing a '0' has no effect
S	RW	PIN18							Pin 18
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Set	1					Write: writing a '1' sets the pin high; writing a '0' has no effect
Т	RW	PIN19							Pin 19
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high Write: writing a '1' sets the pin high; writing a '0' has no effect
U	R\M	PIN20	Set	1					Pin 20
Ü	11.44	111120	Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Set	1					Write: writing a '1' sets the pin high; writing a '0' has no effect
٧	RW	PIN21							Pin 21
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Set	1					Write: writing a '1' sets the pin high; writing a '0' has no effect
W	RW	PIN22							Pin 22
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
V	DIA	DINI22	Set	1					Write: writing a '1' sets the pin high; writing a '0' has no effect
Χ	KVV	PIN23	Low	0					Pin 23 Read: pin driver is low
			High	1					Read: pin driver is high
			Set	1					Write: writing a '1' sets the pin high; writing a '0' has no effect
Υ	RW	PIN24							Pin 24
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Set	1					Write: writing a '1' sets the pin high; writing a '0' has no effect
Z	RW	PIN25							Pin 25
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Set	1					Write: writing a '1' sets the pin high; writing a '0' has no effect
а	ŔW	PIN26	Laur	0					Pin 26
			Low	0					Read: pin driver is low
			High Set	1					Read: pin driver is high Write: writing a '1' sets the pin high; writing a '0' has no effect
b	RW	PIN27							Pin 27
-			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Set	1					Write: writing a '1' sets the pin high; writing a '0' has no effect
С	RW	PIN28							Pin 28
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Set	1					Write: writing a '1' sets the pin high; writing a '0' has no effect



Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	7 16	5 1	5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0	ı
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U	Т	S	R	. a	Į P	C	1 (N N	1 L	. K	J	1	Н	G	F	Ε	D	С	ВА	l
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C) () () (0	0	0	0	0	0	0	0	0	0 0	l
Id	RW	Field	Value Id	Va	lue							De	scri	pti	on																				l
d	RW	PIN29										Pin	29																						ĺ
			Low	0								Rea	ad:	pin	dri	ive	ris	lov	v																
			High	1								Rea	ad:	pin	dri	ive	ris	hig	h																
			Set	1								Wr	ite	wr	itin	ng a	'1'	se	ts t	he	oin	hię	gh; v	writ	ing	a '0'	ha	s no	eff	ect					
е	RW	PIN30										Pin	30																						
			Low	0								Rea	ad:	pin	dri	ive	ris	lov	v																
			High	1								Rea	ad:	pin	dri	ive	ris	hig	h																
			Set	1								Wr	ite	wr	itin	ng a	'1'	se	ts t	he	oin	hig	gh; v	writ	ing	a ' 0'	ha	s no	eff	ect					
f	RW	PIN31										Pin	31																						
			Low	0								Rea	ad:	pin	dri	ive	ris	lov	v																
			High	1								Rea	ad:	pin	dri	ive	is	hig	h																
			Set	1								Wr	ite	wr	itin	ng a	'1'	se	ts t	he	oin	hig	gh; v	writ	ing	a '0'	ha	s no	eff	ect					

19.3.3 OUTCLR

Address offset: 0x50C

Clear individual bits in GPIO port Read: reads value of OUT register.

Bit r	numb	er		3	31 30	29	28	27	26	25	24	2	23 22 21 2	0 1	9 1	3 17	16	15	14	13	12	11	10	9	8	7	6 !	5 4	1 3	2	1	C
Id				f	е	d	С	b	а	Z	Υ	>	x w v	U 1	T 9	R	Q	Р	О	Ν	М	L	K	J	L	н	G I	FI	E C	С	В	1
Res	et Ox(0000000		C	0	0	0	0	0	0	0	C	0 0 0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	-
Id	RW	Field	Value Id	١	/alue	•						D	escriptio	n																		
Α	RW	PIN0										Р	in 0																			
			Low	C)							R	Read: pin o	drive	er is	low																
			High	1								R	Read: pin o	drive	er is	hig	h															
			Clear	1								٧	Vrite: writ	ing	a '1	' set	s th	ie p	in l	ow;	wr	itinį	ga'	0' h	nas r	10 6	ffe	ct				
В	RW	PIN1										Р	in 1																			
			Low	C)							R	Read: pin o	drive	er is	low																
			High	1								R	Read: pin o	drive	er is	hig	h															
			Clear	1								٧	Vrite: writ	ing	a '1	' set	s th	ie p	in l	ow;	wr	itin	ga'	0' h	nas r	10 6	ffe	ct				
С	RW	PIN2										Р	in 2																			
			Low	C)							R	Read: pin o	drive	er is	low																
			High	1								R	Read: pin o	drive	er is	hig	h															
			Clear	1								٧	Vrite: writ	ing	a '1	' set	s th	ie p	in l	ow;	wr	itin	ga'	0' h	nas r	10 6	ffe	ct				
D	RW	PIN3										Р	in 3																			
			Low	C)							R	Read: pin o	drive	er is	low																
			High	1								R	Read: pin o	drive	er is	hig	h															
			Clear	1								٧	Vrite: writ	ing	a '1	' set	s th	ie p	in l	ow;	wr	itinį	ga'	0' h	nas r	10 6	ffe	ct				
E	RW	PIN4										Р	in 4																			
			Low	C)							R	Read: pin o	drive	er is	low																
			High	1								R	Read: pin o	drive	er is	hig	h															
			Clear	1								٧	Vrite: writ	ing	a '1	' set	s th	ie p	in l	ow;	wr	itin	ga'	0' h	nas r	10 6	ffe	ct				
F	RW	PIN5										Р	in 5																			
			Low	()							R	Read: pin o	drive	er is	low																
			High	1								R	Read: pin o	drive	er is	hig	h															
			Clear	1								٧	Vrite: writ	ing	a '1	' set	s th	ie p	in l	ow;	wr	itinį	ga'	0' h	nas r	10 6	ffe	ct				
G	RW	PIN6										Р	in 6																			
			Low	()							R	Read: pin o	drive	er is	low																
			High	1								R	Read: pin o	drive	er is	hig	h															
			Clear	1								٧	Vrite: writ	ing	a '1	' set	s th	ie p	in l	ow;	wr	itinį	ga'	0' h	nas r	10 6	ffe	ct				
Н	RW	PIN7										Р	in 7																			
			Low	()							R	Read: pin o	drive	er is	low																
			High	1								R	Read: pin o	drive	er is	hig	h															



Bit n	umbe	er		31 30	29 28	27 2	6 25	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	a Z	(XWVUTSRQPONMLKJIHGFEDCBA
Rese	et 0x0	0000000		0 0	0 0	0 (0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
I	RW	PIN8		_				Pin 8
			Low	0				Read: pin driver is low
			High Clear	1				Read: pin driver is high Write: writing a '1' sets the pin low; writing a '0' has no effect
	RW	PIN9	Clear	1				Pin 9
,		11145	Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
K	RW	PIN10						Pin 10
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
L	RW	PIN11						Pin 11
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
	DVA	DINI4 2	Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
M	KVV	PIN12	Low	0				Pin 12 Read: pin driver is low
			High	1				Read: pin driver is low
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
N	RW	PIN13						Pin 13
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
0	RW	PIN14						Pin 14
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
-	DIA	DINIAE	Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
Р	KW	PIN15	Low	0				Pin 15
			Low High	1				Read: pin driver is low Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
Q	RW	PIN16		_				Pin 16
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
R	RW	PIN17						Pin 17
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
S	кW	PIN18	Low	0				Pin 18
			Low High	0				Read: pin driver is low Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
Т	RW	PIN19	5.541	•				Pin 19
		-	Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
U	RW	PIN20						Pin 20
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
V	RW	PIN21						Pin 21
			Low	0				Read: pin driver is low



DILL	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e d c b a Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
W	RW	PIN22			Pin 22
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
Χ	RW	PIN23			Pin 23
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
Υ	RW	PIN24			Pin 24
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
-	D)4/	DINIOS	Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
Z	KW	PIN25	La	0	Pin 25
			Low	0	Read: pin driver is low
			High Clear	1	Read: pin driver is high Write: writing a '1' sets the pin low; writing a '0' has no effect
a	D\A/	PIN26	Cledi	1	Pin 26
a	IVV	FINZO	Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
b	RW	PIN27			Pin 27
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
С	RW	PIN28			Pin 28
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
d	RW	PIN29			Pin 29
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
е	RW	PIN30			Pin 30
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
f	RW	PIN31			Pin 31
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect

19.3.4 IN

Address offset: 0x510 Read GPIO port

Bitı	numl	ber	•		31	L 30	29	28	27	26	25	24	23	22	21	20 1	19 :	18 1	17 1	16 1	15 :	14 1	.3 1	.2 1	1 1	9	8	7	6	5	4	3	2	1 0
Id					f	е	d	С	b	а	Z	Υ	Х	W	٧	U	Т	S	R	Q	Р	0	N I	И L	. k	J	-1	Н	G	F	Ε	D	С	ВА
Res	et 0>	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0
Id	RV	٧	Field	Value Id	Va	alue							De	scri	ptio	n																		
Α	R		PIN0										Pin	0																				
				Low	0								Pin	inp	ut i	s lo	w																	
				High	1								Pin	inp	ut i	s hi	gh																	



Bit r	numbe	er		31 30	29 2	8 27	' 26 2	25 24	1 23	22 21	20	19 1	8 17	16	15 1	14 13	3 12	11 :	10 9	8 (7	6 !	5 4	3	2	1 0
Id										W V																
Res	et 0x0	0000000		0 0	0 (0 0	0	0 0	0	0 0	0	0 (0 0	0	0	0 0	0	0	0 (0	0	0 (0 0	0	0	0 0
Id	RW	Field	Value Id	Value					De	scripti	on															
В	R	PIN1								n 1																
			Low	0						n input																
			High	1						n input	is h	nigh														
С	R	PIN2	Law	0						12	:- 1.															
			Low	0						n input n input																
D	R	PIN3	High	1						1 iliput 1 3	15 11	ııgıı														
		11145	Low	0						n input	is lo	οw														
			High	1						n input																
E	R	PIN4	-							n 4																
			Low	0					Pir	n input	is lo	ow														
			High	1					Pir	n input	is h	nigh														
F	R	PIN5							Pir	า 5																
			Low	0					Pir	n input	is lo	ow														
			High	1					Pir	n input	is h	nigh														
G	R	PIN6								า 6																
			Low	0						n input																
	_		High	1						n input –	is h	nigh														
Н	R	PIN7	Low	0						17	ia la															
			Low High	0						n input n input																
	R	PIN8	riigii	1						1 III put 1 8	13 11	iigii														
•		1110	Low	0						n input	is lo	οw														
			High	1						n input																
J	R	PIN9	-							1 9																
			Low	0					Pir	n input	is lo	ow														
			High	1					Pir	n input	is h	nigh														
K	R	PIN10							Pir	า 10																
			Low	0					Pir	n input	is lo	ow														
			High	1					Pir	n input	is h	nigh														
L	R	PIN11								า 11																
			Low	0						n input																
		DINI42	High	1						n input	is h	nigh														
М	R	PIN12	Low	0						n 12 n input	ic le	014														
			High	1						input input																
N	R	PIN13	111611	-						1 13	13 11															
			Low	0						n input	is lo	ow														
			High	1						n input																
0	R	PIN14								n 14																
			Low	0					Pir	n input	is lo	ow														
			High	1					Pir	n input	is h	nigh														
Р	R	PIN15							Pir	า 15																
			Low	0						n input																
			High	1						n input	is h	nigh														
Q	R	PIN16		_						n 16																
			Low	0						n input																
Р	P	PIN17	High	1						n input	is h	iigh														
R	R	FIIV1/	Low	0						n 17 n input	is la	OW/														
			High	1						input input																
S	R	PIN18		-						າ 18	.5 11	0''														
-		-	Low	0						n input	is lo	ow														
			High	1						n input																
Т	R	PIN19								n 19																



Bit r	iumbe	er		31 30	29	28	27	26	25 2	4 2	23 22 2	1 2	20 19	9 1	8 17	7 1	6 1	.5 1	4 1	3 12	2 13	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				f e	d	С	b	а	ΖY	,	x w v	V	U T	٠,	s R	. (Q	P	1 C	N N	1 L	K	J	1	н	G	F	Е	D (В	, Α
Rese	et 0x0	0000000		0 0	0	0	0	0	0 0)	0 0 (0	0 0) (0 0	(0 (0	0 (0 0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Value							Descrip	tio	n																		
			Low	0						F	Pin inpu	ut i:	s low	,																	
			High	1						F	Pin inpu	ut i	s hig	h																	
U	R	PIN20								F	Pin 20																				
			Low	0						F	Pin inpu	ut i	s low	,																	
			High	1						F	Pin inpu	ut i	s hig	h																	
٧	R	PIN21								F	Pin 21																				
			Low	0						F	Pin inpu	ut i	s low	,																	
			High	1						F	Pin inpu	ut i	s hig	h																	
W	R	PIN22								F	Pin 22																				
			Low	0						F	Pin inpu	ut i	s low	,																	
			High	1						F	Pin inpu	ut i	s hig	h																	
Χ	R	PIN23								F	Pin 23																				
			Low	0						F	Pin inpu	ut i	s low	,																	
			High	1						F	Pin inpu	ut i	s hig	h																	
Υ	R	PIN24								F	Pin 24																				
			Low	0						F	Pin inpu	ut i	s low	/																	
			High	1						F	Pin inpu	ut i	s hig	h																	
Z	R	PIN25								F	Pin 25																				
			Low	0						F	Pin inpu	ut i	s low	/																	
			High	1						F	Pin inpu	ut i	s hig	h																	
а	R	PIN26								F	Pin 26																				
			Low	0						F	Pin inpu	ut i	s low	/																	
			High	1						F	Pin inpu	ut i	s hig	h																	
b	R	PIN27								F	Pin 27																				
			Low	0						F	Pin inpu	ut i	s low	/																	
			High	1							Pin inpu	ut i	s hig	h																	
С	R	PIN28									Pin 28																				
			Low	0							Pin inpu																				
			High	1							Pin inpu	ut i	s hig	h																	
d	R	PIN29									Pin 29																				
			Low	0							Pin inpu																				
			High	1							Pin inpu	ıt i	s hig	h																	
е	R	PIN30									Pin 30																				
			Low	0							Pin inpu																				
			High	1							Pin inpu	ut i:	s hig	h																	
f	R	PIN31									Pin 31																				
			Low	0							Pin inpu																				
			High	1						F	Pin inpu	ut i	s hig	h																	

19.3.5 DIR

Address offset: 0x514 Direction of GPIO pins

Bit r	numbe	er		31	30	29	28	27	26 2	25	24 2	23 :	22 :	21 2	20 2	L9 1	.8 1	7 1	6 1	5 1	4 1	3 1	2 11	1 10	9	8	7	6	5	4	3	2	1 0
Id				f	е	d	С	b	a i	Z	Υ	X	W	V	U	Т :	S	R C	Ω	P (1 C	1 N	1 L	K	J	1	Н	G	F	Ε	D	С	ВА
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 () (0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	otio	n																		
Α	RW	PIN0									ı	Pin	0																				
			Input	0							ı	Pin	set	as i	npı	ut																	
			Output	1							1	Pin	set	as (out	put																	
В	RW	PIN1									ı	Pin	1																				
			Input	0							ı	Pin	set	as i	npı	ıt																	
			Output	1							ı	Pin	set	as (out	put																	
С	RW	PIN2									1	Pin	2																				



D.:				24.20	20.20	 	. 24	22 22 2	4 20	10.1	0 47	10	15.4	4.40	12.1	1 10	0	0 -	, ,		2 2	1
Bit r	iumbe	er ·						23 22 2 X W \														
	et 0x0	000000						0 0 0														
		Field	Value Id	Value				Descrip														
			Input	0				Pin set a		ut												
			Output	1				Pin set a	s out	put												
D	RW	PIN3						Pin 3														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	as out	put												
Ε	RW	PIN4						Pin 4														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	as out	put												
F	RW	PIN5						Pin 5														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	s out	put												
G	RW	PIN6						Pin 6														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	s out	put												
Н	RW	PIN7						Pin 7														
			Input	0				Pin set a														
			Output	1				Pin set a	as out	put												
I	RW	PIN8						Pin 8														
			Input	0				Pin set a														
	DIA	DINIO	Output	1				Pin set a	as out	put												
J	RW	PIN9		•				Pin 9														
			Input	0				Pin set a														
K	D\A/	PIN10	Output	1				Pin set a Pin 10	is out	put												
K	NVV	PINIO	Input	0				Pin set a	oc inn													
			Output	1				Pin set a														
L	RW	PIN11	Catput	•				Pin 11	is out	put												
-			Input	0				Pin set a	as inpi	ut												
			Output	1				Pin set a														
М	RW	PIN12	·					Pin 12														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	as out	put												
N	RW	PIN13						Pin 13														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	s out	put												
0	RW	PIN14						Pin 14														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	s out	put												
Р	RW	PIN15						Pin 15														
			Input	0				Pin set a														
			Output	1				Pin set a	s out	put												
Q	RW	PIN16						Pin 16	_													
			Input	0				Pin set a														
_			Output	1				Pin set a	s out	put												
R	KW	PIN17	Lament	0				Pin 17														
			Input	0				Pin set a														
c	DIA	DINI19	Output	1				Pin set a	is out	.put												
S	ĸw	PIN18	Innut	0				Pin 18	inn.	+												
			Input					Pin set a														
Т	B/V	PIN19	Output	1				Pin set a	is out	.µut												
	ΚVV	LINTA	Innut	0					ic inn	ut												
			Input Output	1				Pin set a														
U	B/V	PIN20	σαιραι	1				Pin set a	is out	.pul												
J	11.00		Input	0				Pin set a	ıç inn	ut												
			put	J					.5 mp	J.												



Bitı	numbe	er		31 30	29	28 2	27 26	25	24	23 2	22 21	20 1	9 18	3 17	16	15	14 1	3 12	11	10 9	9 8	3 7	6	5	4	3 2	1	0
Id				f e	d	С	b a	Z	Υ	Χ١	w v	U T	S	R	Q	Р	0 1	N M	L	Κ.	JI	Н	G	F	Е	D C	В	Α
Res	et 0x0	0000000		0 0	0	0	0 0	0	0	0	0 0	0 0	0	0	0	0	0 (0	0	0 (0 (0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value						Des	criptio	on																
			Output	1						Pin s	set as	outp	ut															
٧	RW	PIN21								Pin 2	21																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
W	RW	PIN22								Pin 2	22																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
Χ	RW	PIN23								Pin 2	23																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
Υ	RW	PIN24								Pin 2	24																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
Z	RW	PIN25								Pin 2	25																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
а	RW	PIN26								Pin 2	26																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
b	RW	PIN27								Pin 2	27																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
С	RW	PIN28								Pin 2	28																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
d	RW	PIN29								Pin 2	29																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
е	RW	PIN30								Pin 3	30																	
			Input	0						Pin	set as	inpu	t															
			Output	1						Pin	set as	outp	ut															
f	RW	PIN31								Pin 3	31																	
			Input	0						Pin	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															

19.3.6 DIRSET

Address offset: 0x518

DIR set register

Read: reads value of DIR register.

Bit	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x00000000		$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW Field	Value Id	Value Description
Α	RW PINO		Set as output pin 0
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
В	RW PIN1		Set as output pin 1
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
С	RW PIN2		Set as output pin 2



Bit r	iumbe	er		31 30	29 28	27 26	25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	ΖY	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0 0	0 (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value				Description
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
_		B.1.1.0	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
D	RW	PIN3		•				Set as output pin 3
			Input	0				Read: pin set as input
			Output Set	1				Read: pin set as output Write: writing a '1' sets pin to output; writing a '0' has no effect
E	RW/	PIN4	Jei	1				Set as output pin 4
-		11144	Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
F	RW	PIN5						Set as output pin 5
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
G	RW	PIN6						Set as output pin 6
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Н	RW	PIN7						Set as output pin 7
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
I	RW	PIN8						Set as output pin 8
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
		B.11.0	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
J	RW	PIN9		•				Set as output pin 9
			Input	0				Read: pin set as input
			Output Set	1				Read: pin set as output Write: writing a '1' sets pin to output; writing a '0' has no effect
K	R\M/	PIN10	Set	1				Set as output pin 10
K	IVV	FINIO	Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
L	RW	PIN11		_				Set as output pin 11
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
М	RW	PIN12						Set as output pin 12
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
N	RW	PIN13						Set as output pin 13
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
0	RW	PIN14						Set as output pin 14
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Р	RW	PIN15						Set as output pin 15
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect



Bit r	numbe	er		31 30	29 28 :	27 26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
Q	RW	PIN16						Set as output pin 16
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
R	RW	PIN17						Set as output pin 17
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
S	RW	PIN18						Set as output pin 18
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Т	RW	PIN19						Set as output pin 19
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
U	RW	PIN20						Set as output pin 20
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
V	RW	PIN21						Set as output pin 21
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
W	RW	PIN22						Set as output pin 22
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Х	RW	PIN23						Set as output pin 23
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Υ	RW	PIN24						Set as output pin 24
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Z	RW	PIN25						Set as output pin 25
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
а	RW	PIN26						Set as output pin 26
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
b	RW	PIN27						Set as output pin 27
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
С	RW	PIN28						Set as output pin 28
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
d	RW	PIN29						Set as output pin 29
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output



Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20 1	.9 1	.8 1	7 16	15	14	13	L2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id				f	e	d	С	b	а	Z	Υ	Χ	W	٧	U .	Т :	S F	Q	P	О	N	M	L K	J	1	Н	G	F	ЕΙ	ОС	В	Α
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue	!						De	scri	ptic	n																	
			Set	1								W	rite:	wri	ting	a ':	1' se	ts p	in to	ο οι	ıtpu	; w	ritin	g a '	0' ha	as n	o e	ffec	t			
е	RW	PIN30										Se	t as	out	put	pin	30															
			Input	0								Re	ad: ¡	pin	set a	as ii	npu	t														
			Output	1								Re	ad: ¡	pin	set a	as o	utp	ut														
			Set	1								W	rite:	wri	ting	a ':	1' se	ts p	in to	οι	ıtpu	; w	ritin	g a '	0' ha	as n	o e	ffec	t			
f	RW	PIN31										Se	t as	out	put	pin	31															
			Input	0								Re	ad: ¡	pin	set a	as ii	npu	t														
			Output	1								Re	ad: ¡	pin	set a	as o	utp	ut														
			Set	1								W	rite:	wri	ting	a ':	1' se	ts p	in to	οι	ıtpu	; w	ritin	g a '	0' ha	as n	o e	ffec	t			

19.3.7 DIRCLR

Address offset: 0x51C

DIR clear register

Read: reads value of DIR register.

Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
Α	RW PINO		Set as input pin 0
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
В	RW PIN1		Set as input pin 1
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
С	RW PIN2		Set as input pin 2
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
D	RW PIN3		Set as input pin 3
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
Е	RW PIN4		Set as input pin 4
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
F	RW PIN5		Set as input pin 5
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
G	RW PIN6		Set as input pin 6
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
Н	RW PIN7		Set as input pin 7
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
I	RW PIN8		Set as input pin 8
		Input	0 Read: pin set as input



Bit n	iumbe	r		31 30	29 28	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
J	RW	PIN9						Set as input pin 9
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
K	RW	PIN10						Set as input pin 10
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
L	RW	PIN11						Set as input pin 11
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
М	RW	PIN12		_				Set as input pin 12
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
	DIA	DINIA 2	Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
N	KVV	PIN13	la acce	0				Set as input pin 13
			Input	0				Read: pin set as input
			Output Clear	1				Read: pin set as output Write: writing a '1' sets pin to input; writing a '0' has no effect
0	D\A/	PIN14	Cledi	1				Set as input pin 14
U	IVV	FINIA	Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
Р	RW	PIN15	0.00.	_				Set as input pin 15
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
Q	RW	PIN16						Set as input pin 16
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
R	RW	PIN17						Set as input pin 17
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
S	RW	PIN18						Set as input pin 18
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
Т	RW	PIN19						Set as input pin 19
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
U	RW	PIN20		_				Set as input pin 20
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
	p	DINI24	Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
V	KW	PIN21	Toronto.	0				Set as input pin 21
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
\A/	DIA	DINI22	Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
W	ΝVV	PIN22						Set as input pin 22



Bit	number		31 30	29 2	3 2	7 26	25 2	24	23 22 21 20	0 19	18 17	' 16	5 15	14	13	12	11	10	9	8	7	6	5	4 3	3 2	1	. 0
Id			f e	d c	b	а	Z	Υ	x w v u	JΤ	S R	a	Р	С	N	М	L	K	J	Ĺ	Н	G	F	E C) (В	А
Res	set 0x00000000		0 0	0 0	O	0	0	0	0 0 0 0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW Field	Value Id	Value						Description	1																	
		Input	0						Read: pin se	et as i	nput																
		Output	1						Read: pin se	et as (outpu	ıt															
		Clear	1					,	Write: writi	ng a '	1' set	s p	in t	ni o	put	; w	ritir	ng a	'0'	has	no	effe	ct				
Χ	RW PIN23								Set as input	pin 2	23																
		Input	0						Read: pin se	et as i	nput																
		Output	1						Read: pin se	et as	outpu	ıt															
		Clear	1					,	Write: writi	ng a '	1' set	s p	in t	o ir	put	; w	ritir	ng a	'0'	has	no	effe	ct				
Υ	RW PIN24							:	Set as input	pin 2	24																
		Input	0						Read: pin se	et as i	nput																
		Output	1						Read: pin se	et as	outpu	ıt															
		Clear	1					,	Write: writi	ng a '	1' set	s p	in t	ni o	put	; w	ritir	ng a	'0'	has	no	effe	ct				
Z	RW PIN25								Set as input	pin 2	25																
		Input	0						Read: pin se	et as i	nput																
		Output	1						Read: pin se	et as	outpu	ıt															
		Clear	1					,	Write: writi	ng a '	1' set	s p	in t	o ir	put	; w	ritir	ng a	'0'	has	no	effe	ct				
а	RW PIN26							:	Set as input	pin 2	26																
		Input	0						Read: pin se	et as i	nput																
		Output	1						Read: pin se	et as	outpu	ıt															
		Clear	1						Write: writi	ng a '	1' set	s p	in t	ni o	put	; w	ritir	ng a	'0'	has	no	effe	ct				
b	RW PIN27							:	Set as input	pin 2	27																
		Input	0						Read: pin se	et as i	nput																
		Output	1						Read: pin se	et as	outpu	ıt															
		Clear	1					,	Write: writi	ng a '	1' set	s p	in t	ni o	put	; w	ritir	ng a	'0'	has	no	effe	ct				
С	RW PIN28								Set as input	pin 2	28																
		Input	0						Read: pin se	et as i	nput																
		Output	1						Read: pin se	et as	outpu	ıt															
		Clear	1					'	Write: writi	ng a '	1' set	s p	in t	ni o	put	; w	ritir	ng a	'0'	has	no	effe	ct				
d	RW PIN29								Set as input	pin 2	29																
		Input	0						Read: pin se	et as i	nput																
		Output	1						Read: pin se																		
		Clear	1						Write: writi	ng a '	1' set	s p	in t	o ir	put	; w	ritir	ng a	'0'	has	no	effe	ct				
е	RW PIN30								Set as input																		
		Input	0						Read: pin se		•																
		Output	1						Read: pin se																		
		Clear	1						Write: writi			s p	in t	ni o	put	; w	ritir	ng a	'0'	has	no	effe	ct				
f	RW PIN31								Set as input																		
		Input	0						Read: pin se																		
		Output	1						Read: pin se																		
		Clear	1						Write: writi	ng a '	1' set	s p	in t	ni o	put	; w	ritir	ng a	'0'	has	no	effe	ct				

19.3.8 LATCH

Address offset: 0x520

Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers

Bitı	numbe	er		31	. 30	29	28	27	26 2	25	24 2	23 :	22 2	21 2	0 1	.9 18	17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3 2	1	0
Id				f	е	d	С	b	а	Z	Υ	X	w '	Vι	J	T S	R	Q	Р	О	N	М	L I	(J	-1	Н	G	F	E I	0 0	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 0) (0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0 0	0	0
Id	RW	Field	Value Id	Va	llue						ı	Des	crip	tior	•																	
Α	RW	PIN0									9	Stat	us o	on w	he	ther	PIN	0 h	as n	net	crit	eria	set	in P	IN_	CNF	0.51	ENS	E			
											1	regi	ister	r. W	rite	'1'	o cl	ear														
			NotLatched	0							(Crit	eria	has	no	t be	en i	net														
			Latched	1							(Crit	eria	has	be	en r	net															
В	RW	PIN1									9	Stat	tus o	on w	he	ther	PIN	1 h	as n	net	crit	eria	set	in P	IN_	CNF	1.SI	ENS	E			
											ı	regi	ister	r. W	rite	'1'	o cl	ear														



Bitı	number	r		31 30	29 28	3 27	26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00	0000000		0 0	0 0	0	0 (0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	•				Description
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
С	RW	PIN2							Status on whether PIN2 has met criteria set in PIN_CNF2.SENSE
									register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
D	RW	PIN3							Status on whether PIN3 has met criteria set in PIN_CNF3.SENSE
				_					register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
_	D\A/	DINIA	Latched	1					Criteria has been met
E	RW	PIN4							Status on whether PIN4 has met criteria set in PIN_CNF4.SENSE
			NotLatched	0					register. Write '1' to clear. Criteria has not been met
			Latched	1					Criteria has been met
F	RW	PIN5	Laterica	_					Status on whether PIN5 has met criteria set in PIN_CNF5.SENSE
									register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
G	RW	PIN6							Status on whether PIN6 has met criteria set in PIN_CNF6.SENSE
									register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
Н	RW	PIN7							Status on whether PIN7 has met criteria set in PIN_CNF7.SENSE
									register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
I	RW	PIN8							Status on whether PIN8 has met criteria set in PIN_CNF8.SENSE
				_					register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
	D\A/	DINO	Latched	1					Criteria has been met
J	RW	PIN9							Status on whether PIN9 has met criteria set in PIN_CNF9.SENSE
			NotLatched	0					register. Write '1' to clear. Criteria has not been met
			Latched	1					Criteria has been met
K	RW	PIN10	Luterieu	-					Status on whether PIN10 has met criteria set in
									PIN_CNF10.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
L	RW	PIN11							Status on whether PIN11 has met criteria set in
									PIN_CNF11.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
M	RW	PIN12							Status on whether PIN12 has met criteria set in
									PIN_CNF12.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
N	RW	PIN13							Status on whether PIN13 has met criteria set in
									PIN_CNF13.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
0	RW	PIN14							Status on whether PIN14 has met criteria set in
			Not atched	0					PIN_CNF14.SENSE register. Write '1' to clear.
			NotLatched Latched	0					Criteria has not been met Criteria has been met
			Latched	1					Criteria nas peen met



Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e d c b a Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Р	RW	PIN15			Status on whether PIN15 has met criteria set in
					PIN_CNF15.SENSE register. Write '1' to clear.
			NotLatched	0	Criteria has not been met
	DIA	DINIAC	Latched	1	Criteria has been met
Q	RW	PIN16			Status on whether PIN16 has met criteria set in
			NotLatched	0	PIN_CNF16.SENSE register. Write '1' to clear. Criteria has not been met
			Latched	1	Criteria has been met
R	RW	PIN17	Laterica	-	Status on whether PIN17 has met criteria set in
					PIN_CNF17.SENSE register. Write '1' to clear.
			NotLatched	0	Criteria has not been met
			Latched	1	Criteria has been met
S	RW	PIN18			Status on whether PIN18 has met criteria set in
					PIN_CNF18.SENSE register. Write '1' to clear.
			NotLatched	0	Criteria has not been met
			Latched	1	Criteria has been met
Т	RW	PIN19			Status on whether PIN19 has met criteria set in
					PIN_CNF19.SENSE register. Write '1' to clear.
			NotLatched	0	Criteria has not been met
			Latched	1	Criteria has been met
U	RW	PIN20			Status on whether PIN20 has met criteria set in
					PIN_CNF20.SENSE register. Write '1' to clear.
			NotLatched	0	Criteria has not been met
.,	DVA	DINI24	Latched	1	Criteria has been met
V	KVV	PIN21			Status on whether PIN21 has met criteria set in
			NotLatched	0	PIN_CNF21.SENSE register. Write '1' to clear. Criteria has not been met
			Latched	1	Criteria has been met
W	RW	PIN22	Laterica	-	Status on whether PIN22 has met criteria set in
••					PIN CNF22.SENSE register. Write '1' to clear.
			NotLatched	0	Criteria has not been met
			Latched	1	Criteria has been met
Χ	RW	PIN23			Status on whether PIN23 has met criteria set in
					PIN_CNF23.SENSE register. Write '1' to clear.
			NotLatched	0	Criteria has not been met
			Latched	1	Criteria has been met
Υ	RW	PIN24			Status on whether PIN24 has met criteria set in
					PIN_CNF24.SENSE register. Write '1' to clear.
			NotLatched	0	Criteria has not been met
			Latched	1	Criteria has been met
Z	RW	PIN25			Status on whether PIN25 has met criteria set in
			Night stab.	0	PIN_CNF25.SENSE register. Write '1' to clear.
			NotLatched	0	Criteria has not been met
_	DVA	DINIAC	Latched	1	Criteria has been met
а	ΚW	PIN26			Status on whether PIN26 has met criteria set in PIN_CNF26.SENSE register. Write '1' to clear.
			NotLatched	0	Criteria has not been met
			Latched	1	Criteria has been met
b	RW	PIN27		-	Status on whether PIN27 has met criteria set in
					PIN_CNF27.SENSE register. Write '1' to clear.
			NotLatched	0	Criteria has not been met
			Latched	1	Criteria has been met
С	RW	PIN28			Status on whether PIN28 has met criteria set in
					PIN_CNF28.SENSE register. Write '1' to clear.
			NotLatched	0	Criteria has not been met



Bit number		31	30 29	28 2	7 26	25 2	4 23	22 21	20 1	19 18	3 17	16	15 1	4 13	12	11 1	0 9	8	7	6 5	5 4	3	2 :	L 0
Id		f	e d	c b	а	ΖY	′ X	w v	U	T S	R	Q	P (O N	М	L k	J	1	Н	G F	E	D	C E	3 A
Reset 0x0000	0000	0	0 0	0 0	0	0 (0	0 0	0	0 0	0	0	0 (0 0	0	0 0	0	0	0	0 0	0	0	0 (0
Id RW Fie	ld Value Id	Va	lue				Des	cription	on															
	Latched	1					Crit	eria h	as be	een r	net													
d RW PIN	N29						Sta	tus on	whe	ether	PIN	29 h	as n	net o	rite	ria se	t in							
							PIN	_CNF2	29.SE	NSE	regi	ster	. Wr	ite '	l' to	clear								
	NotLatche	d 0					Crit	eria h	as no	ot be	en n	net												
	Latched	1					Crit	eria h	as be	een r	net													
e RW PIN	130						Sta	tus on	whe	ether	PIN	30 h	as n	net o	rite	ria se	t in							
							PIN	_CNF3	30.SE	NSE	regi	ster	. Wr	ite '	l' to	clear								
	NotLatche	d 0					Crit	eria h	as no	ot be	en n	net												
	Latched	1					Crit	eria h	as be	een r	net													
f RW PIN	N31						Sta	tus on	whe	ether	PIN	31 h	as n	net o	rite	ria se	t in							
							PIN	_CNF3	31.SE	NSE	regi	ster	. Wr	ite '	l' to	clear								
	NotLatche	d 0					Crit	eria h	as no	ot be	en n	net												
	Latched	1					Crit	eria h	as be	een r	net													

19.3.9 DETECTMODE

Address offset: 0x524

Select between default DETECT signal behaviour and LDETECT mode

Bit	numbe	er		3	1 30	29	28	3 27	26	5 25	5 24	23	22	21	20	19 1	18 1	17 1	6 1	L5 1	.4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1	0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0 () (0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	'alue	2						De	scri	ptio	n																			
Α	RW	DETECTMODE										Sel	ect	bet	wee	en d	lefa	ult	DE1	TEC	T si	gna	be	havi	our	and	l LD	ETE	ECT					
												mc	ode																					
			Default	0								DE	TEC	T di	rec	tly c	oni	nect	ted	to	PIN	DE.	ΓEC	T sig	nals	;								
			LDETECT	1								Us	e th	e la	tch	ed L	DE.	TEC	T b	eha	vio	ur												

19.3.10 PIN_CNF[0]

Address offset: 0x700

Configuration of GPIO pins

Rit r	numb	er		31	30	29	28 °	77 .	26.3	25 1	24	23 2	2 2	1 20	19	1.8	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4 3	2	1 (
Id	Idilib			51	50	23	20 .	_, .	202			25 2			, 13	, 10		E	13		15 1			D	_		Ŭ	J			В /
	at Ove	00000002		0	0	0	0	0	^	^	^			_	۸	۰	٥	۸	^	_		0 0		0	0	^	0	0	0 0		1 (
			Value Id	_	ŭ	U	U	U	U	U	U	D			U	U	U	U	U	Ü	U		, 0	U	U	U	U	U		Ü	_ '
ld		Field	value id	Va	lue							Desc																			
Α	RW	DIR										Pin o								_	ster	as D	IR re	egist	er						
			Input	0								Conf	figui	e p	in a	s ar	ı in	put	pin												
			Output	1								Conf	figur	e p	in a	s ar	า ดเ	ıtpu	t pi	n											
В	RW	INPUT										Coni	nect	or	disc	onr	nec	t inp	ut	buf	fer										
			Connect	0								Coni	nect	inp	ut k	ouff	er														
			Disconnect	1								Disc	onn	ect i	inpı	ut b	uff	er													
С	RW	PULL										Pull	con	figu	rati	on															
			Disabled	0								No p	ull																		
			Pulldown	1								Pull	dow	n o	n pi	in															
			Pullup	3								Pull	up c	n p	in																
D	RW	DRIVE										Driv	е со	nfig	ura	tior	า														
			S0S1	0								Stan	dar	'0' b	, sta	and	ard	'1'													
			H0S1	1								High	dri	/e '()', s	tan	dar	d '1	•												
			SOH1	2								Stan	dar	'0' b	, hi	gh d	driv	e '1													
			H0H1	3								High	dri	/e '()', h	igh	'dr	ive	1"												
			D0S1	4								Disc	onn	ect	'0' s	tan	daı	d '1	' (n	orn	nally	use	d for	wii	ed-	or					
												conr	nect	ions	5)																



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

19.3.11 PIN_CNF[1]

Address offset: 0x704

Configuration of GPIO pins

Bit nur	mbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E D D D C C B
Reset (0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld R	RW	Field	Value Id	Value	Description
A R	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
B R	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
C R	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D R	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			D0S1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E R	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

19.3.12 PIN_CNF[2]

Address offset: 0x708

Configuration of GPIO pins



Bit r	numbe	er		31	30 2	29 28	27	26 2	25 24	1 23	3 22 2	21 20	19	18	17	16 :	15	14 1	.3 1	12 1	.1 1) 9	8	7	6	5	4	3 2	1	0
Id															Ε	Е					0	D	D					c c	В	Α
Res	et OxC	0000002		0	0 (0 0	0	0	0 0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	1	0
Id	RW	Field	Value Id	Val	ue					D	escrip	otion																		
Α	RW	DIR								Pi	in dire	ectio	n. Sa	me	phy	/sica	al r	egis	er	as I	OIR 1	egi	ster							
			Input	0						Co	onfigu	ıre p	in as	an	inp	ut p	in													
			Output	1						Co	onfigu	ıre p	in as	an	out	put	pir	1												
В	RW	INPUT								Co	onne	ct or	disco	nne	ect i	inpı	ut b	uffe	er											
			Connect	0						Co	onne	t inp	ut b	uffe	r															
			Disconnect	1						Di	iscon	nect	inpu	bu	ffe	r														
С	RW	PULL								Pι	ull co	nfigu	ratio	n																
			Disabled	0						N	o pull																			
			Pulldown	1						Pι	ull do	wn o	n pir	ı																
			Pullup	3						Pι	ull up	on p	in																	
D	RW	DRIVE								Dı	rive c	onfig	urati	on																
			S0S1	0						St	tanda	rd '0'	', sta	nda	rd '	1'														
			H0S1	1						Hi	igh dr	ive '	0', sta	and	ard	'1'														
			S0H1	2						St	tanda	rd '0'	', hig	h dr	ive	'1'														
			H0H1	3						Hi	igh dr	ive '	0', hi	gh '	driv	/e '1	L''													
			DOS1	4						Di	iscon	nect	'0' st	and	lard	l '1'	(nc	rma	ally	use	d fo	r w	ired	l-or						
										CC	onnec	tions	5)																	
			D0H1	5							iscon			igh	driv	ve ':	1' (ı	norr	nall	ly u	sed	for	wire	ed-o	r					
			S0D1	6							tanda		•			+ 141	1/0	o w.o.o	alls		~ d f			4	٦					
			3001	ь							onnec			JOIII	nec	ιı	(11)	OTTI	ally	us	eu ii	JI W	vire	J-dii	u					
			H0D1	7						Hi	igh dr	ive '	0', di:	1002	nne	ct ':	1' (ı	norr	nall	ly u	sed	for	wire	ed-a	nd					
										cc	onnec	tions	5)																	
Е	RW	SENSE								Pi	in sen	sing	mecl	nan	ism															
			Disabled	0						Di	isable	d																		
			High	2						Se	ense f	or hi	gh le	vel																
			Low	3						Se	ense f	or lo	w le	/el																

19.3.13 PIN_CNF[3]

Address offset: 0x70C Configuration of GPIO pins

ССВА
0 0 1 0



Bit number		31 3	30 29	28	8 27	7 26	25	24	23	22 2	21 2	0 1	9 18	3 17	16	15	14 1	.3 12	2 11	10	9	8	7	6 5	5 4	3	2	1	0
Id														Ε	Ε					D	D	D				С	С	В	Α
Reset 0x00000002		0 (0 0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0 0	0	0	0	0 ()	0 (0	0	0	1	0
ld RW Field	Value Id	Valu	ıe						Des	scrip	tior	1																	
	D0H1	5							Disc	con	nect	'0',	hig	h dr	ive	'1' (nori	nally	use	d fo	r w	ired	-or						
									con	nnec	tion	s)																	
	SOD1	6							Star	nda	rd '0)'. d	isco	nne	ct '1	l' (n	orm	ally	usec	for	wii	ed-	anc	ı					
									con	nnec	tion	s)																	
	H0D1	7							Higl	gh dr	ive '	0',	disc	onn	ect '	'1' (nori	nally	use	d fo	r w	ired	-an	d					
									con	nnec	tion	s)																	
E RW SENSE									Pin	sen	sing	me	echa	nisn	n														
	Disabled	0							Disa	able	d																		
	High	2							Sen	nse f	or h	igh	leve	el															
	Low	3							Sen	nse f	or lo	ow l	eve	I															

19.3.14 PIN_CNF[4]

Address offset: 0x710

Configuration of GPIO pins

	<u> </u>		
Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E E D D D C C B A
Reset 0x00000002		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
ld RW Field	Value Id	Value	Description
A RW DIR			Pin direction. Same physical register as DIR register
	Input	0	Configure pin as an input pin
	Output	1	Configure pin as an output pin
B RW INPUT			Connect or disconnect input buffer
	Connect	0	Connect input buffer
	Disconnect	1	Disconnect input buffer
C RW PULL			Pull configuration
	Disabled	0	No pull
	Pulldown	1	Pull down on pin
	Pullup	3	Pull up on pin
D RW DRIVE			Drive configuration
	S0S1	0	Standard '0', standard '1'
	H0S1	1	High drive '0', standard '1'
	SOH1	2	Standard '0', high drive '1'
	H0H1	3	High drive '0', high 'drive '1"
	D0S1	4	Disconnect '0' standard '1' (normally used for wired-or
			connections)
	D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or connections)
	SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
	11004	-	connections)
	H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
F DW CENCE			connections)
E RW SENSE	Disabled	0	Pin sensing mechanism
	Disabled	0	Disabled
	High	2	Sense for law level
	Low	3	Sense for low level

19.3.15 PIN_CNF[5]

Address offset: 0x714

Configuration of GPIO pins



Bit	number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E E DDD CCBA
Res	et 0x00000002		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW DIR			Pin direction. Same physical register as DIR register
		Input	0	Configure pin as an input pin
		Output	1	Configure pin as an output pin
В	RW INPUT			Connect or disconnect input buffer
		Connect	0	Connect input buffer
		Disconnect	1	Disconnect input buffer
С	RW PULL			Pull configuration
		Disabled	0	No pull
		Pulldown	1	Pull down on pin
		Pullup	3	Pull up on pin
D	RW DRIVE			Drive configuration
		S0S1	0	Standard '0', standard '1'
		H0S1	1	High drive '0', standard '1'
		S0H1	2	Standard '0', high drive '1'
		H0H1	3	High drive '0', high 'drive '1"
		D0S1	4	Disconnect '0' standard '1' (normally used for wired-or
				connections)
		D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
				connections)
		S0D1	6	Standard '0'. disconnect '1' (normally used for wired-and
				connections)
		H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
				connections)
Ε	RW SENSE			Pin sensing mechanism
		Disabled	0	Disabled
		High	2	Sense for high level
		Low	3	Sense for low level

19.3.16 PIN_CNF[6]

Address offset: 0x718

Configuration of GPIO pins

Bit r	num	her			21	30	29	28 °	77 -	26 2	5 2	1 2:	3 22	21	20	19	1Ω	17	16	15	1/1	12 1	2 1	1 10) Q	8	7	6	5	1	3 :	2 1	0
Id	Iuiii	ibci			51	50	25	20 1	_ , ,	20 2	.5 2	7 2.	J	. 21	20	13	10	Ε		15.	14	13 1	1		D		,	Ü	5		о. С (3 A
	· ·	00	000002		0	_	_	0	0					_	_	_	_	_	_	_	_	0	n (0	0	0	0	_			. 0
					_		U	U	U	0 (, (, ,	, 0	U	U	U	U	U	U	U	U	U	, (י י	U	U	U	U	U	U	U	, 1	U
ld	RV	N	Field	Value Id	Va	lue						D	escr	iptio	on																		
Α	RV	Ν	DIR									Pi	in di	rect	ion	. Sa	me	ph	ysic	al r	egis	ter	as C	IR r	egis	ter							
				Input	0							Co	onfi	gure	pir	n as	an	inp	ut p	oin													
				Output	1							Co	onfi	gure	pir	n as	an	out	tpu	t pir	1												
В	RV	Ν	INPUT									Co	onn	ect o	or d	isco	nn	ect	inp	ut b	uff	er											
				Connect	0							Co	onn	ect i	npu	ıt b	uffe	er															
				Disconnect	1							Di	isco	nne	ct ir	าрน	t bı	uffe	r														
С	RV	Ν	PULL									Pι	ull c	onfi	gura	atio	n																
				Disabled	0							N	о рі	ıll																			
				Pulldown	1							Pι	ull d	owr	on	pir	1																
				Pullup	3							Pι	ull u	p or	niq r	n																	
D	RV	Ν	DRIVE									D	rive	con	figu	ırat	ion																
				S0S1	0							St	and	lard	'0',	sta	nda	ard	'1'														
				H0S1	1							Hi	igh (drive	e '0'	', st	and	larc	i '1'														
				S0H1	2							St	and	lard	'0',	hig	h d	rive	'1'														
				H0H1	3							Hi	igh (drive	e '0'	', hi	gh '	'dri	ve '	1''													
				DOS1	4							Di	isco	nne	ct 'C)' st	and	dard	d '1'	(nc	rm	ally	use	d fo	r wi	red-	or						
												cc	onne	ectic	ns)																		



Bit number		31 30 29 28	27 26 25	5 24	23 22 2	21 20	19 1	8 17	16	15 1	.4 13	12 1	1 10	9	8	7	6 5	5 4	3	2 1	. 0
Id								Е	Ε				D	D	D				С	СВ	Α
Reset 0x00000002		0 0 0 0	0 0 0	0	0 0	0 0	0 (0	0	0 (0 0	0	0 0	0	0	0	0 0	0	0	0 1	. 0
ld RW Field	Value Id	Value			Descrip	otion															
	D0H1	5			Discon	nect '	0', hi	gh dr	ive '	1' (n	orma	ally u	sed f	or w	/ired	-or					
					connec	tions)														
	SOD1	6			Standa	rd '0'.	. disc	onne	ct '1	.' (nc	rmal	ly us	ed fo	r wi	red-	and					
					connec	tions)														
	H0D1	7			High dr	rive '0)', dis	conn	ect '	1' (n	orma	ally u	sed f	or w	vired	l-an	d				
					connec	tions)														
E RW SENSE					Pin sen	nsing r	mech	anisr	n												
	Disabled	0			Disable	ed															
	High	2			Sense f	for hig	gh lev	el													
	Low	3			Sense f	for lov	w leve	el													

19.3.17 PIN_CNF[7]

Address offset: 0x71C

Configuration of GPIO pins

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		E E DDD CCB
Reset 0x00000002		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW DIR		Pin direction. Same physical register as DIR register
	Input	0 Configure pin as an input pin
	Output	1 Configure pin as an output pin
B RW INPUT		Connect or disconnect input buffer
	Connect	0 Connect input buffer
	Disconnect	1 Disconnect input buffer
C RW PULL		Pull configuration
	Disabled	0 No pull
	Pulldown	1 Pull down on pin
	Pullup	3 Pull up on pin
D RW DRIVE		Drive configuration
	S0S1	0 Standard '0', standard '1'
	H0S1	1 High drive '0', standard '1'
	S0H1	2 Standard '0', high drive '1'
	H0H1	3 High drive '0', high 'drive '1"
	DOS1	4 Disconnect '0' standard '1' (normally used for wired-or
		connections)
	D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
		connections)
	SOD1	6 Standard '0'. disconnect '1' (normally used for wired-and
		connections)
	H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
	Disabled	0 Disabled
	High	2 Sense for high level
	Low	3 Sense for low level

19.3.18 PIN_CNF[8]

Address offset: 0x720



Bit	number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E E DDD CCBA
Res	et 0x00000002		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW DIR			Pin direction. Same physical register as DIR register
		Input	0	Configure pin as an input pin
		Output	1	Configure pin as an output pin
В	RW INPUT			Connect or disconnect input buffer
		Connect	0	Connect input buffer
		Disconnect	1	Disconnect input buffer
С	RW PULL			Pull configuration
		Disabled	0	No pull
		Pulldown	1	Pull down on pin
		Pullup	3	Pull up on pin
D	RW DRIVE			Drive configuration
		SOS1	0	Standard '0', standard '1'
		H0S1	1	High drive '0', standard '1'
		S0H1	2	Standard '0', high drive '1'
		H0H1	3	High drive '0', high 'drive '1"
		DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
				connections)
		D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
				connections)
		SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
				connections)
		H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
				connections)
Ε	RW SENSE			Pin sensing mechanism
		Disabled	0	Disabled
		High	2	Sense for high level
		Low	3	Sense for low level

19.3.19 PIN_CNF[9]

Address offset: 0x724

Bit r	num	her			21	30	29	28 -	77 -	26 2	5 2	1 2:	2 22	21	20	19 1	12	17	16	15 1	1/1 1	3 1	2 1	1 10	a	8	7	6	5	1	3 :) 1	0
Id	Iuiii	ibci			51	50	25.	20 1	_ , ,	20 2	.5 2	7 2.	<i>3</i>	. 21	20	15.		Ε		13.		.5 1.	۷ 1.		D	_	,	Ü	5		C (. O
	· ·	00	000002		0	_	_	^	0					_	_	_	_	_	_	_	_	0 0			0	0	٥	0	0	_	0 (. 0
					_		U	U	U	0 (, (, ,	U	·	U	U	U	U	U	U	U	U	, ,	U	U	U	U	U	U	U	0 (, 1	U
ld	RV	N	Field	Value Id	Va	lue						D	escr	iptio	on																		
Α	RV	Ν	DIR									Pi	n di	rect	ion.	Sar	ne	phy	/sic	al re	gis	ter a	s D	IR re	egist	er							
				Input	0							Co	onfi	gure	pin	as	an	inp	ut p	oin													
				Output	1							Co	onfi	gure	pin	as	an	out	put	pin	ı												
В	RV	Ν	INPUT									Co	onne	ect c	or di	isco	nne	ect	inp	ut b	uff	er											
				Connect	0							Co	onne	ect i	npu	t bu	ıffe	r															
				Disconnect	1							Di	isco	nne	ct in	put	bu	ıffeı	r														
С	RV	Ν	PULL									Pι	ull c	onfi	gura	atio	า																
				Disabled	0							N	о рі	ıll																			
				Pulldown	1							Pι	ull d	own	on	pin																	
				Pullup	3							Pι	ull u	p or	pir	ı																	
D	RV	Ν	DRIVE									D	rive	con	figu	rati	on																
				S0S1	0							St	and	ard	'0',	star	nda	rd '	1'														
				H0S1	1							Hi	igh (drive	e '0'	, sta	ınd	ard	'1'														
				S0H1	2							St	and	ard	'0',	high	n dr	rive	'1'														
				H0H1	3							Hi	igh (drive	0'	, hig	gh '	driv	/e '1	L"													
				DOS1	4							Di	isco	nne	ct '0)' sta	and	lard	1'1'	(no	rm	ally ı	use	d for	wii	ed-	or						
												cc	onne	ectio	ns)																		



Bit number		31 3	30 29	28	8 27	26	25	24	23 2	2 21	20	19	18 :	17 1	16 1	L5 1	4 13	3 12	11	10	9	8	7 (5 5	5 4	3	2	1	0
Id														Е	E					D	D	D				С	С	В	Α
Reset 0x00000002		0 (0 0	0	0	0	0	0	0 0	0 0	0	0	0	0	0 (0 (0 0	0	0	0	0	0 () (0 (0	0	0	1	0
ld RW Field	Value Id	Valu	ıe						Desc	ripti	on																		
	D0H1	5							Disco	onne	ct '(0', h	igh	driv	⁄e '1	L' (n	orm	ally	use	d fo	r w	ired	or						
									conn	nectio	ons))																	
	SOD1	6						:	Stan	dard	'0'.	disc	oni	nect	t '1'	(nc	rma	lly u	sed	for	iiw	ed-	nd						
									conn	nectio	ons))																	
	H0D1	7							High	driv	e '0	', dis	cor	nne	ct '1	L' (n	orm	ally	use	d fo	r w	ired	an	d					
									conn	nectio	ons))																	
E RW SENSE									Pin s	ensii	ng n	necł	nani	sm															
	Disabled	0							Disal	bled																			
	High	2						:	Sens	e for	hig	gh le	vel																
	Low	3						:	Sens	e for	lov	v lev	el																

19.3.20 PIN_CNF[10]

Address offset: 0x728

Configuration of GPIO pins

Bit nu	mbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Reset	0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld I	RW	Field	Value Id	Value	Description
A I	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В І	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
C I	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D I	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			D0S1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E I	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

19.3.21 PIN_CNF[11]

Address offset: 0x72C



Bit r	numbe	er		31	30 2	29 28	27	26 2	25 24	4 23	3 22	21 2	0 1	9 18	17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3 2	1	0
Id															Ε	Ε					[) [D					c c	В	Α
Res	et OxC	0000002		0	0 (0 0	0	0	0 0	0	0	0 (0 0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0 0	1	0
Id	RW	Field	Value Id	Val	ue					D	escri	ptior	n																	
Α	RW	DIR								Pi	in dii	ectio	n. S	ame	e ph	iysic	cal ı	regis	ster	as	DIR	regi	ster							
			Input	0						Co	onfig	ure p	oin a	as ar	n inp	out	pin													
			Output	1						Co	onfig	ure p	oin a	as ar	n ou	itpu	t pi	n												
В	RW	INPUT								Co	onne	ct or	dis	conr	nect	inp	ut	buff	er											
			Connect	0						Co	onne	ct in	put	buff	er															
			Disconnect	1						Di	iscor	nect	inp	ut b	uffe	er														
С	RW	PULL								Pι	ull co	nfigu	urat	ion																
			Disabled	0						N	lo pu	II																		
			Pulldown	1						Pι	ull d	own o	on p	in																
			Pullup	3						Pι	ull u	on p	pin																	
D	RW	DRIVE								D	rive	confi	gura	atior	1															
			S0S1	0						St	tand	ard 'C)', st	and	ard	'1'														
			HOS1	1						Hi	igh c	rive '	'0', s	stan	dar	d '1'	•													
			S0H1	2						St	tand	ard 'C)', h	igh c	driv	e '1'	'													
			H0H1	3						Hi	igh c	rive '	'0', I	nigh	'dri	ive '	1"													
			DOS1	4						Di	iscor	nect	'0'	stan	dar	d '1	' (n	orm	ally	/ us	ed fo	or w	/ired	l-or						
										cc	onne	ction	ıs)																	
			D0H1	5								nect ction		higł	n dr	ive	'1' ((nor	ma	lly ι	ısed	for	wir	ed-o	r					
			S0D1	6								ard 'C	•			a+ 11	11/-		المد		. a d f			4	ام					
			3001	О								ction		iscoi	ine	CL J	L (I	10111	Idli	y us	eu i	OI V	vire	u-ai	ıu					
			H0D1	7						Hi	igh c	rive '	'0', d	disco	onn	ect '	'1' (nor	ma	lly ι	ısed	for	wir	ed-a	nd					
										cc	onne	ction	ıs)																	
Е	RW	SENSE								Pi	in se	nsing	me	cha	nisn	n														
			Disabled	0						Di	isabl	ed																		
			High	2						Se	ense	for h	igh	leve	el															
			Low	3						Se	ense	for lo	ow I	evel																

19.3.22 PIN_CNF[12]

Address offset: 0x730 Configuration of GPIO pins

numb	er		31	. 30	29	28	27	26 2	25 :	24	23 2	22	21 :	20	19 1	18 :	17 :	16	15 1	.4 :	13 :	12 :	l1 1	0 9	8	7	6	5	4	3	2	1 (
																	Е	E					1) [D					С	C I	ВА
et 0x(00000002		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1 (
RW	Field	Value Id	Va	lue							Des	cri	ptio	n																		
RW	DIR										Pin	dir	ecti	on.	Sar	ne	phy	sic	al re	gis	ter	as	DIR	regi	ster							
		Input	0								Con	fig	ure	pin	as	an i	inpı	ut p	in													
		Output	1								Con	fig	ure	pin	as	an (out	put	pin													
RW	INPUT										Con	ne	ct o	r di	sco	nne	ect i	np	ut b	uff	er											
		Connect	0								Con	ne	ct ir	npu	t bu	ffe	r															
		Disconnect	1								Disc	on	nec	t in	put	bu	ffer															
RW	PULL										Pull	со	nfig	gura	tioi	1																
		Disabled	0								No p	pul	I																			
		Pulldown	1								Pull	do	wn	on	pin																	
		Pullup	3								Pull	up	on	pir	1																	
RW	DRIVE										Driv	e c	onf	igu	rati	on																
		S0S1	0							:	Star	nda	rd '	0',	star	ıda	rd '	1'														
		H0S1	1								High	n d	rive	'0'	, sta	nd	ard	'1'														
		S0H1	2							:	Star	nda	rd '	0',	high	dr	ive	'1'														
		H0H1	3								High	n di	rive	'0'	, hig	h 'd	driv	e '1	L''													
		DOS1	4								Disc	on	nec	t '0	' sta	nd	ard	'1'	(no	rm	ally	use	ed f	or w	ired	l-or						
											con	nor	rtio	ns)																		
	RW RW	RW Field RW DIR RW INPUT RW PULL RW DRIVE	RW Field Value Id RW DIR Input Output RW INPUT Connect Disconnect RW PULL Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 HOH1	RW Field Value Id Val	RW Field Value Id Val	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3 THE SOH1 2 HOH1 3 TO T	RW Field Value Id Id Id Value Id Id Id Value Id	RW Field Value Id Val	RW Field Value Id Value Id Value Id Value Id RW DIR RW INPUT Connect Disconnect 1 RW PULL PULL Disabled O Pulldown 1 Pullup 3 RW DRIVE SOS1 O HOS1 SOH1 SOH1 SOH1 SOH1 SOH1 SOH1 SOH1 SOH1	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3 DOS1 4	RW Field Value Id Value RW DIR Input Output 1 Connect Disconnect Disconnect Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 SOH1 SOH1 SOH1 SOH1 SOS1 HOHI DISCON SON OUTPUT	RW Field Value Id Value	RW Field Value Id Val	RW Field Value Id Value	RW Field Value Id Val	RW Field Value Id Value Valu	RW Field Value Id Value	RW Field Value Market Pin direction. Same physical	RW Field Value Id Value Pin direction. Same physical reference Pin d	RW Field Value Id Value Pin direction. Same physical register	RW Field Value Id Value Id Value Id Description Pin direction. Same physical register	RW Field Value Id Value Valu	RW Field Value Id Value Pin direction. Same physical register as DIR	RW Field	RW Field Value Id Value	RW Field Value Id Value Id Pin direction. Same physical register as DIR regist	RW Field Value Id Pind irection. Same physical register as DIR register NPUT	RW Field Value Id Value	RW Field Value Id Value Valu	NPUT	RW Field Value Id Value Valu



Bit number		31 3	30 29	28	8 27	26	25	24	23 2	2 21	20	19	18 :	17 1	16 1	L5 1	4 13	3 12	11	10	9	8	7 (5 5	5 4	3	2	1	0
Id														Е	E					D	D	D				С	С	В	Α
Reset 0x00000002		0 (0 0	0	0	0	0	0	0 0	0 0	0	0	0	0	0 (0 (0 0	0	0	0	0	0 () (0 (0	0	0	1	0
ld RW Field	Value Id	Valu	ıe						Desc	ripti	on																		
	D0H1	5							Disco	onne	ct '(0', h	igh	driv	⁄e '1	L' (n	orm	ally	use	d fo	r w	ired	or						
									conn	nectio	ons))																	
	SOD1	6						:	Stan	dard	'0'.	disc	oni	nect	t '1'	(nc	rma	lly u	sed	for	iiw	ed-	nd						
									conn	nectio	ons))																	
	H0D1	7							High	driv	e '0	', dis	cor	nne	ct '1	L' (n	orm	ally	use	d fo	r w	ired	an	d					
									conn	nectio	ons))																	
E RW SENSE									Pin s	ensii	ng n	necł	nani	sm															
	Disabled	0							Disal	bled																			
	High	2						:	Sens	e for	hig	gh le	vel																
	Low	3						:	Sens	e for	lov	v lev	el																

19.3.23 PIN_CNF[13]

Address offset: 0x734

Configuration of GPIO pins

Bit n	umbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Rese	t 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

19.3.24 PIN_CNF[14]

Address offset: 0x738



Bit r	numbe	er		31 3	0 29	28	27 2	6 25	5 24	23	22 2	21 20	0 19	18	17	16	15	14 1	.3 1	2 13	1 10	9	8	7	6	5 4	1 3	2	1	0
Id															Ε	Ε					D	D	D				С	С	В	Α
Res	et OxC	00000002		0 (0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0 0	0	1	0
Id	RW	Field	Value Id	Valu	e					De	escrip	tion	l																	
Α	RW	DIR								Pir	n dire	ctio	n. S	ame	e ph	iysic	al r	egist	er a	as D	IR re	egist	er							
			Input	0						Со	nfigu	ıre p	in a	s an	inp	out	pin													
			Output	1						Со	nfigu	ıre p	in a	s an	ou	tpu	t pi	n												
В	RW	INPUT								Со	nnec	t or	disc	onn	nect	inp	ut l	ouffe	er											
			Connect	0						Со	nnec	t inp	out b	ouff	er															
			Disconnect	1						Dis	sconr	nect	inpı	ut b	uffe	er														
С	RW	PULL								Pu	ıll cor	nfigu	rati	on																
			Disabled	0						No	pull																			
			Pulldown	1						Pu	ıll dov	wn o	n pi	n																
			Pullup	3						Pu	ıll up	on p	in																	
D	RW	DRIVE								Dri	ive co	onfig	gura	tion	1															
			S0S1	0						Sta	andaı	rd '0	', sta	anda	ard	'1'														
			H0S1	1						Hig	gh dr	ive '	0', s	tano	dard	d '1'														
			S0H1	2						Sta	andaı	rd '0	', hi	gh d	irive	e '1'														
			H0H1	3						Hig	gh dr	ive '	0', h	igh	'dri	ve '	1''													
			DOS1	4						Dis	sconr	nect	'0' s	tan	dar	d '1	' (n	orma	ally	used	d for	vii	ed-	or						
										COI	nnec	tions	s)																	
			D0H1	5						Dis	sconr	nect	'0',	high	n dri	ive '	'1' (norn	nall	y us	ed f	or w	/ire	d-or						
										COI	nnec	tions	s)																	
			SOD1	6						Sta	andaı	rd '0	'. di	scor	nne	ct '1	L' (n	orm	ally	use	d fo	r wi	red	and	i					
										COI	nnec	tions	s)																	
			H0D1	7						Hig	gh dr	ive '	0', d	isco	onne	ect '	'1' (norn	nall	y us	ed f	or w	/ire	d-an	ıd					
										COI	nnec	tions	s)																	
Ε	RW	SENSE									n sen	-	me	char	nisn	n														
			Disabled	0							sable																			
			High	2						Sei	nse f	or hi	igh I	eve	1															
			Low	3						Sei	nse f	or lo	w le	evel																

19.3.25 PIN_CNF[15]

Address offset: 0x73C Configuration of GPIO pins

ССВА
0 0 1 0



Bit number	31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
S0D1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

19.3.26 PIN_CNF[16]

Address offset: 0x740

Configuration of GPIO pins

Bit nu	umbe	er		31 30 29 28	27 26 2	25 24	23 2	2 21 2	0 19 1	18 1	7 16	15	14 1	3 12	11 1	10 9	8	7	6	5 4	3	2	1 (
Id										E	ЕЕ					D C	D				С	С	B A
Rese	t 0x0	0000002		0 0 0 0	0 0	0 0	0 0	0 0	0 0	0 (0 0	0	0 (0 0	0	0 0	0	0	0	0 0	0	0	1 (
Id	RW	Field	Value Id	Value			Desc	ription	n														
Α	RW	DIR					Pin d	directio	n. Sar	ne p	hysi	cal r	egist	er as	DIR	regi	ster						
			Input	0			Conf	figure p	oin as	an ir	nput	pin											
			Output	1			Conf	figure p	oin as	an o	utpu	ut pir	า										
В	RW	INPUT					Conn	nect or	disco	nne	ct in	put b	ouffe	r									
			Connect	0			Conn	nect in	put bu	ıffer													
			Disconnect	1			Disco	onnect	input	buf	fer												
С	RW	PULL					Pull	configu	uration	ı													
			Disabled	0			No p	ull															
			Pulldown	1			Pull	down	on pin														
			Pullup	3			Pull ເ	up on I	pin														
D	RW	DRIVE					Drive	e confi	gurati	on													
			S0S1	0			Stan	dard '0)', star	ndar	d '1'												
			H0S1	1			High	drive	'0', sta	nda	rd '1	L '											
			S0H1	2			Stan	dard '0)', high	dri	ve '1	L'											
			H0H1	3			High	drive	'0', hig	gh 'd	rive	'1"											
			DOS1	4			Disco	onnect	'0' sta	anda	ard ':	1' (no	orma	lly us	sed f	or w	ired	or					
							conn	nection	ıs)														
			D0H1	5			Disco	onnect	'0', hi	gh c	lrive	'1' (norn	nally	used	for	wire	d-or					
							conn	nection	ıs)														
			SOD1	6			Stand	dard 'C)'. disc	onn	ect '	1' (n	orma	ally u	sed	for v	vired	-and	t				
							conn	nection	ıs)														
			H0D1	7			High	drive	'0', dis	con	nect	'1' (norn	nally	used	for	wire	d-ar	nd				
							conn	nection	ıs)														
E	RW	SENSE					Pin s	ensing	mech	anis	sm												
			Disabled	0			Disab	bled															
			High	2			Sens	e for h	igh le	vel													
			Low	3			Sens	e for lo	ow lev	el													

19.3.27 PIN_CNF[17]

Address offset: 0x744



Bit	number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E E DDD CCBA
Res	et 0x00000002		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW DIR			Pin direction. Same physical register as DIR register
		Input	0	Configure pin as an input pin
		Output	1	Configure pin as an output pin
В	RW INPUT			Connect or disconnect input buffer
		Connect	0	Connect input buffer
		Disconnect	1	Disconnect input buffer
С	RW PULL			Pull configuration
		Disabled	0	No pull
		Pulldown	1	Pull down on pin
		Pullup	3	Pull up on pin
D	RW DRIVE			Drive configuration
		SOS1	0	Standard '0', standard '1'
		H0S1	1	High drive '0', standard '1'
		S0H1	2	Standard '0', high drive '1'
		H0H1	3	High drive '0', high 'drive '1"
		DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
				connections)
		D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
				connections)
		SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
				connections)
		H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
				connections)
Ε	RW SENSE			Pin sensing mechanism
		Disabled	0	Disabled
		High	2	Sense for high level
		Low	3	Sense for low level

19.3.28 PIN_CNF[18]

Address offset: 0x748
Configuration of GPIO pins

Bit r	iumbe	er		31	30	29	28 2	27 2	26 2	5 24	4 23	22	21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																	Ε	Ε					D	D	D				(СС	: В	Α
Rese	et OxC	0000002		0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 0) 1	0
Id	RW	Field	Value Id	Va	llue						De	scr	ipti	on																		
Α	RW	DIR									Pin	n di	rect	tion	. Sa	ne	ph	ysic	al r	egis	ter	as [IR r	egis	ter							
			Input	0							Co	nfig	gure	e pir	n as	an	inp	ut	oin													
			Output	1							Co	nfig	gure	e pir	n as	an	ou	tpu	t pir	ı												
В	RW	INPUT									Co	nne	ect (or d	lisco	nn	ect	inp	ut k	ouff	er											
			Connect	0							Co	nne	ect i	inpu	ut bu	ıffe	er															
			Disconnect	1							Dis	co	nne	ct ii	nput	: bu	ıffe	r														
С	RW	PULL									Pul	II c	onfi	gur	atio	n																
			Disabled	0							No	pι	ıll																			
			Pulldown	1							Pul	ll d	owr	n or	n pin																	
			Pullup	3							Pul	ll u	no q	n pi	n																	
D	RW	DRIVE									Dri	ive	con	figu	ırati	on																
			S0S1	0							Sta	and	lard	'0',	stai	nda	ırd	'1'														
			H0S1	1							Hig	gh d	driv	e '0	', sta	and	larc	i '1'														
			SOH1	2							Sta	and	lard	'0',	hig	n dı	rive	'1'														
			H0H1	3							Hig	gh d	driv	e '0	', hi	gh '	dri	ve '	1''													
			DOS1	4							Dis	co	nne	ct '(O' st	anc	dar	d '1'	(no	orm	ally	use	d fo	r wi	red-	or						
											100	nne	ectio	ons))																	



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

19.3.29 PIN_CNF[19]

Address offset: 0x74C

Configuration of GPIO pins

	<u> </u>		
Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E E D D D C C B A
Reset 0x00000002		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW DIR			Pin direction. Same physical register as DIR register
	Input	0	Configure pin as an input pin
	Output	1	Configure pin as an output pin
B RW INPUT			Connect or disconnect input buffer
	Connect	0	Connect input buffer
	Disconnect	1	Disconnect input buffer
C RW PULL			Pull configuration
	Disabled	0	No pull
	Pulldown	1	Pull down on pin
	Pullup	3	Pull up on pin
D RW DRIVE			Drive configuration
	S0S1	0	Standard '0', standard '1'
	H0S1	1	High drive '0', standard '1'
	SOH1	2	Standard '0', high drive '1'
	H0H1	3	High drive '0', high 'drive '1"
	DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
			connections)
	D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or connections)
	SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
	11004	_	connections)
	H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
F DW CENCE			connections)
E RW SENSE	Disabled	0	Pin sensing mechanism
	Disabled	0	Disabled
	High	2	Sense for high level
	Low	3	Sense for low level

19.3.30 PIN_CNF[20]

Address offset: 0x750



Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E D D D C C B A
Res	et 0x0	0000002		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

19.3.31 PIN_CNF[21]

Address offset: 0x754

ССВА
0 0 1 0



Bit number		31 3	30 29	28	8 27	26	25	24	23 2	2 21	20	19	18 :	17 1	16 1	L5 1	4 13	3 12	11	10	9	8	7 (5 5	5 4	3	2	1	0
Id														Е	E					D	D	D				С	С	В	Α
Reset 0x00000002		0 (0 0	0	0	0	0	0	0 0	0 0	0	0	0	0	0 (0 (0 0	0	0	0	0	0 () (0 (0	0	0	1	0
ld RW Field	Value Id	Valu	ıe						Desc	ripti	on																		
	D0H1	5							Disco	onne	ct '(0', h	igh	driv	⁄e '1	L' (n	orm	ally	use	d fo	r w	ired	or						
									conn	nectio	ons))																	
	SOD1	6						:	Stan	dard	'0'.	disc	oni	nect	t '1'	(nc	rma	lly u	sed	for	iiw	ed-	nd						
									conn	nectio	ons))																	
	H0D1	7							High	driv	e '0	', dis	cor	nne	ct '1	L' (n	orm	ally	use	d fo	r w	ired	an	d					
									conn	nectio	ons))																	
E RW SENSE									Pin s	ensii	ng n	necł	nani	sm															
	Disabled	0							Disal	bled																			
	High	2						:	Sens	e for	hig	gh le	vel																
	Low	3						:	Sens	e for	lov	v lev	el																

19.3.32 PIN_CNF[22]

Address offset: 0x758

Configuration of GPIO pins

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		E E DDD CCB
Reset 0x00000002		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW DIR		Pin direction. Same physical register as DIR register
	Input	0 Configure pin as an input pin
	Output	1 Configure pin as an output pin
B RW INPUT		Connect or disconnect input buffer
	Connect	0 Connect input buffer
	Disconnect	1 Disconnect input buffer
C RW PULL		Pull configuration
	Disabled	0 No pull
	Pulldown	1 Pull down on pin
	Pullup	3 Pull up on pin
D RW DRIVE		Drive configuration
	S0S1	0 Standard '0', standard '1'
	H0S1	1 High drive '0', standard '1'
	S0H1	2 Standard '0', high drive '1'
	H0H1	3 High drive '0', high 'drive '1"
	DOS1	4 Disconnect '0' standard '1' (normally used for wired-or
		connections)
	D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
		connections)
	SOD1	6 Standard '0'. disconnect '1' (normally used for wired-and
		connections)
	H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
	Disabled	0 Disabled
	High	2 Sense for high level
	Low	3 Sense for low level

19.3.33 PIN_CNF[23]

Address offset: 0x75C



Reset 0x00000002	Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value Id Value Description A RW DIR Input 0 Configure pin as an input pin B RW INPUT Connect Connect or disconnect input buffer C Connect Disconnect Disconnect input buffer C RW PULL Pull configuration Pull pollown 1 Pull configuration D Pull upon pin Pull upon pin Pull upon pin Pull upon pin SSS1 SSS1 SSS1 HOS1 1 High drive "0", standard "1" SOH1 2 Standard "0", high drive "1" HOH1 3 High drive "0", high drive "1" HOH1 3 High drive "0", high drive "1" (normally used for wired-or connections) DOH1 5 Disconnect "0" standard "1" (normally used for wired-or connections) E RW ENSE High drive "0", high drive "1" (normally used for wired-and connections) F Pull to the pull to	Id					E E DDD CCBA
A RW DIR	Res	et 0x0	0000002		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Input	Id	RW	Field	Value Id	Value	Description
B RW INPUT Connect Connect of disconnect input buffer Connect place input buffer Disconnect input buffer Pull configuration Disabled Pulldown Pullup Pu	Α	RW	DIR			Pin direction. Same physical register as DIR register
B RW INPUT Connect Connect Connect Connect input buffer Disconnect Disco				Input	0	Configure pin as an input pin
Connect Disconnect 0 Connect input buffer Disconnect input buffer Disconnect input buffer Pull configuration C RW PULL Pull Pull Pull Pull Pull Pull Pull Pu				Output	1	Configure pin as an output pin
C RW PULL Pullonfiguration Disabled 0 No pull Onfiguration Pullon Pull down on pin Pullup 3 Pull up on pin Drive configuration Drive configuration Drive configuration SoS1 0 Standard '1' Standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' H0H1 3 High drive '0', high drive '1' H0H1 3 Disconnect '0' standard '1' (normally used for wired-or connections) Disconnect '0', high drive '1' (normally used for wired-or connections) Disconnect '1' (normally used for wired-and connect '1' (normally used for wired-and connections) E RW SENSE Pissel Obisabled 0 Disabled	В	RW	INPUT			Connect or disconnect input buffer
C RW PULL Disabled 0 No pull Pull down on pin Pullup 3 Pull up on pin D RW DRIVE SOS1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' HOH1 3 High drive '0', high drive '1" DOS1 4 Disconnect '0', high drive '1' DOS1 5 Standard '1' (normally used for wired-or connections) SOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) FOR DISSONSE RW SENSE Disabled 0 Disabled Pull own on pin Pull up				Connect	0	Connect input buffer
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin Drive configuration Drive configuration SoS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				Disconnect	1	Disconnect input buffer
Pulldown 1 Pulldown on pin Pullup 3 Pull up on pin D RW DRIVE Drive configuration SOS1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled	С	RW	PULL			Pull configuration
Pullup 3 Pullup on pin Drive configuration Standard '0', standard '1' H0S1 1 High drive '0', standard '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-and connections) For a standard '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled Disabled Disabled Disabled Disabled				Disabled	0	No pull
D RW DRIVE SOS1 O Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1" DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled				Pulldown	1	Pull down on pin
SOS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1" DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled O Disabled				Pullup	3	Pull up on pin
H0S1 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1" D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled	D	RW	DRIVE			Drive configuration
SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high 'drive '1" DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				SOS1	0	Standard '0', standard '1'
H0H1 3 High drive '0', high 'drive '1" D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				H0S1	1	High drive '0', standard '1'
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				S0H1	2	Standard '0', high drive '1'
connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled O Disabled				H0H1	3	High drive '0', high 'drive '1"
DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled						connections)
S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled						connections)
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled						connections)
E RW SENSE Pin sensing mechanism Disabled 0 Disabled				H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
Disabled 0 Disabled						connections)
	Е	RW	SENSE			Pin sensing mechanism
High 2 Sense for high level				Disabled	0	Disabled
riigii 2 Scrisc for ingritever				High	2	Sense for high level
Low 3 Sense for low level				Low	3	Sense for low level

19.3.34 PIN_CNF[24]

Address offset: 0x760 Configuration of GPIO pins

Bit r	iumbe	er		31	30	29	28 2	27 2	26 2	5 24	4 23	22	21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																	Ε	Ε					D	D	D				(СС	: В	Α
Rese	et OxC	0000002		0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 0) 1	0
Id	RW	Field	Value Id	Va	llue						De	scr	ipti	on																		
Α	RW	DIR									Pin	n di	rect	tion	. Sa	ne	ph	ysic	al r	egis	ter	as [IR r	egis	ter							
			Input	0							Co	nfig	gure	e pir	n as	an	inp	ut	oin													
			Output	1							Co	nfig	gure	e pir	n as	an	ou	tpu	t pir	ı												
В	RW	INPUT									Co	nne	ect (or d	lisco	nn	ect	inp	ut k	ouff	er											
			Connect	0							Co	nne	ect i	inpu	ut bu	ıffe	er															
			Disconnect	1							Dis	co	nne	ct ii	nput	: bu	ıffe	r														
С	RW	PULL									Pul	II c	onfi	gur	atio	n																
			Disabled	0							No	pι	ıll																			
			Pulldown	1							Pul	ll d	owr	n or	n pin																	
			Pullup	3							Pul	ll u	no q	n pi	n																	
D	RW	DRIVE									Dri	ive	con	figu	ırati	on																
			S0S1	0							Sta	and	lard	'0',	stai	nda	ırd	'1'														
			H0S1	1							Hig	gh d	driv	e '0	', sta	and	larc	i '1'														
			SOH1	2							Sta	and	lard	'0',	hig	n dı	rive	'1'														
			H0H1	3							Hig	gh d	driv	e '0	', hi	gh '	dri	ve '	1''													
			DOS1	4							Dis	co	nne	ct '(O' st	anc	dar	d '1'	(no	orm	ally	use	d fo	r wi	red-	or						
											100	nne	ectio	ons))																	



Bit number		31 3	30 29	28	8 27	26	25	24	23 2	2 21	20	19	18 :	17 1	16 1	L5 1	4 13	3 12	11	10	9	8	7 (5 5	5 4	3	2	1	0
Id														Е	E					D	D	D				С	С	В	Α
Reset 0x00000002		0 (0 0	0	0	0	0	0	0 0	0 0	0	0	0	0	0 (0 (0 0	0	0	0	0	0 () (0 (0	0	0	1	0
ld RW Field	Value Id	Valu	ıe						Desc	ripti	on																		
	D0H1	5							Disco	onne	ct '(0', h	igh	driv	⁄e '1	L' (n	orm	ally	use	d fo	r w	ired	or						
									conn	nectio	ons))																	
	SOD1	6						:	Stan	dard	'0'.	disc	oni	nect	t '1'	(nc	rma	lly u	sed	for	iiw	ed-	nd						
									conn	nectio	ons))																	
	H0D1	7							High	driv	e '0	', dis	cor	nne	ct '1	L' (n	orm	ally	use	d fo	r w	ired	an	d					
									conn	nectio	ons))																	
E RW SENSE									Pin s	ensii	ng n	necł	nani	sm															
	Disabled	0							Disal	bled																			
	High	2						:	Sens	e for	hig	gh le	vel																
	Low	3						:	Sens	e for	lov	v lev	el																

19.3.35 PIN_CNF[25]

Address offset: 0x764

Configuration of GPIO pins

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		E E DDD CCB
Reset 0x00000002		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW DIR		Pin direction. Same physical register as DIR register
	Input	0 Configure pin as an input pin
	Output	1 Configure pin as an output pin
B RW INPUT		Connect or disconnect input buffer
	Connect	0 Connect input buffer
	Disconnect	1 Disconnect input buffer
C RW PULL		Pull configuration
	Disabled	0 No pull
	Pulldown	1 Pull down on pin
	Pullup	3 Pull up on pin
D RW DRIVE		Drive configuration
	S0S1	0 Standard '0', standard '1'
	H0S1	1 High drive '0', standard '1'
	S0H1	2 Standard '0', high drive '1'
	H0H1	3 High drive '0', high 'drive '1"
	DOS1	4 Disconnect '0' standard '1' (normally used for wired-or
		connections)
	D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
		connections)
	SOD1	6 Standard '0'. disconnect '1' (normally used for wired-and
		connections)
	H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
	Disabled	0 Disabled
	High	2 Sense for high level
	Low	3 Sense for low level

19.3.36 PIN_CNF[26]

Address offset: 0x768



Reset 0x00000002	Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value Id Value Description A RW DIR Input 0 Configure pin as an input pin B RW INPUT Connect Connect or disconnect input buffer C Connect Disconnect Disconnect input buffer C RW PULL Pull configuration Pull pollown 1 Pull configuration D Pull upon pin Pull upon pin Pull upon pin Pull upon pin SSS1 SSS1 SSS1 HOS1 1 High drive "0", standard "1" SOH1 2 Standard "0", high drive "1" HOH1 3 High drive "0", high drive "1" HOH1 3 High drive "0", high drive "1" (normally used for wired-or connections) DOH1 5 Disconnect "0" standard "1" (normally used for wired-or connections) E RW ENSE High drive "0", high drive "1" (normally used for wired-and connections) F Pull to the pull to	Id					E E DDD CCBA
A RW DIR	Res	et 0x0	0000002		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Input	Id	RW	Field	Value Id	Value	Description
B RW INPUT Connect Connect of disconnect input buffer Connect place input buffer Disconnect input buffer Pull configuration Disabled Pulldown Pullup Pu	Α	RW	DIR			Pin direction. Same physical register as DIR register
B RW INPUT Connect Connect Connect Connect input buffer Disconnect Disco				Input	0	Configure pin as an input pin
Connect Disconnect 0 Connect input buffer Disconnect input buffer Disconnect input buffer Pull configuration C RW PULL Pull Pull Pull Pull Pull Pull Pull Pu				Output	1	Configure pin as an output pin
C RW PULL Pullonfiguration Disabled 0 No pull Onfiguration Pullon Pull down on pin Pullup 3 Pull up on pin Drive configuration Drive configuration Drive configuration SoS1 0 Standard '1' Standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' H0H1 3 High drive '0', high drive '1' H0H1 3 Disconnect '0' standard '1' (normally used for wired-or connections) Disconnect '0', high drive '1' (normally used for wired-or connections) Disconnect '1' (normally used for wired-and connect '1' (normally used for wired-and connections) E RW SENSE Pissel Obisabled 0 Disabled	В	RW	INPUT			Connect or disconnect input buffer
C RW PULL Disabled 0 No pull Pull down on pin Pullup 3 Pull up on pin D RW DRIVE SOS1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' HOH1 3 High drive '0', high drive '1" DOS1 4 Disconnect '0', high drive '1' DOS1 5 Standard '1' (normally used for wired-or connections) SOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) FOR DISSONSE RW SENSE Disabled 0 Disabled Pull own on pin Pull up				Connect	0	Connect input buffer
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin Drive configuration Drive configuration SoS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				Disconnect	1	Disconnect input buffer
Pulldown 1 Pulldown on pin Pullup 3 Pull up on pin D RW DRIVE Drive configuration SOS1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled	С	RW	PULL			Pull configuration
Pullup 3 Pullup on pin Drive configuration Standard '0', standard '1' H0S1 1 High drive '0', standard '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-and connections) For a standard '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled Disabled Disabled Disabled Disabled				Disabled	0	No pull
D RW DRIVE SOS1 O Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1" DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled				Pulldown	1	Pull down on pin
SOS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1" DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled O Disabled				Pullup	3	Pull up on pin
H0S1 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1" D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled	D	RW	DRIVE			Drive configuration
SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high 'drive '1" DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				SOS1	0	Standard '0', standard '1'
H0H1 3 High drive '0', high 'drive '1" D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				H0S1	1	High drive '0', standard '1'
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				S0H1	2	Standard '0', high drive '1'
connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled O Disabled				H0H1	3	High drive '0', high 'drive '1"
DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled						connections)
S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled						connections)
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled						connections)
E RW SENSE Pin sensing mechanism Disabled 0 Disabled				H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
Disabled 0 Disabled						connections)
	Е	RW	SENSE			Pin sensing mechanism
High 2 Sense for high level				Disabled	0	Disabled
riigii 2 Scrise for ingrirever				High	2	Sense for high level
Low 3 Sense for low level				Low	3	Sense for low level

19.3.37 PIN_CNF[27]

Address offset: 0x76C Configuration of GPIO pins

Bit r	num	her			21	30	29	28 -	77 -	26 2	5 2	1 2:	2 22	21	20	19 1	12	17	16	15 1	1/1 1	3 1	2 1	1 10	a	8	7	6	5	1	3 :) 1	0
Id	Iuiii	ibci			51	50	25.	20 1	_ , ,	20 2	.5 2	7 2.	<i>3</i>	. 21	20	15.		Ε		15.		.5 1.	۷ 1.		D	_	,	Ü	5		C (. O
	· ·	00	000002		0	_	_	^	0					_	_	_	_	_	_	_	_	0 0			0	0	٥	0	0	_	0 (. 0
					_		U	U	U	0 (, (, ,	U	·	U	U	U	U	U	U	U	U	, ,	U	U	U	U	U	U	U	0 (, 1	U
ld	RV	N	Field	Value Id	Va	lue						D	escr	iptio	on																		
Α	RV	Ν	DIR									Pi	n di	rect	ion.	Sar	ne	phy	/sic	al re	gis	ter a	s D	IR re	egist	er							
				Input	0							Co	onfi	gure	pin	as	an	inp	ut p	oin													
				Output	1							Co	onfi	gure	pin	as	an	out	put	pin	ı												
В	RV	Ν	INPUT									Co	onne	ect c	or di	isco	nne	ect	inp	ut b	uff	er											
				Connect	0							Co	onne	ect i	npu	t bu	ıffe	r															
				Disconnect	1							Di	isco	nne	ct in	put	bu	ıffeı	r														
С	RV	Ν	PULL									Pι	ull c	onfi	gura	atio	า																
				Disabled	0							N	о рі	ıll																			
				Pulldown	1							Pι	ull d	own	on	pin																	
				Pullup	3							Pι	ull u	p or	pir	ı																	
D	RV	Ν	DRIVE									D	rive	con	figu	rati	on																
				S0S1	0							St	and	ard	'0',	star	nda	rd '	1'														
				H0S1	1							Hi	igh (drive	e '0'	, sta	ınd	ard	'1'														
				S0H1	2							St	and	ard	'0',	high	n dr	rive	'1'														
				H0H1	3							Hi	igh (drive	0'	, hig	gh '	driv	/e '1	L"													
				DOS1	4							Di	isco	nne	ct '0)' sta	and	lard	1'1'	(no	rm	ally ı	use	d for	wii	ed-	or						
												cc	onne	ectio	ns)																		



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	E E DDD CCBA
Reset 0x00000002	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value Description
D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
	connections)
SOD1	6 Standard '0'. disconnect '1' (normally used for wired-and
	connections)
H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
	connections)
E RW SENSE	Pin sensing mechanism
Disabled	0 Disabled
High	2 Sense for high level
Low	3 Sense for low level

19.3.38 PIN_CNF[28]

Address offset: 0x770

Configuration of GPIO pins

Bit r	iumbe	r		31 30	29	28 2	7 26	25	24 2	23	22 21	20	19	18	17	16	15	14	13	12	11 1	.0 9	8	7	6	5	4	3 2	2 1	. 0
Id															Ε	Ε					1) C	D D					C (С В	3 A
Rese	et 0x0	0000002		0 0	0	0 (0 0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 () 1	. 0
Id	RW	Field	Value Id	Value	•					Des	scripti	on																		
Α	RW	DIR							F	Pin	direc	tioi	n. Sa	me	e ph	nysi	cal	regi	ister	as	DIR	reg	istei	•						
			Input	0					(Cor	nfigure	e pi	in a	ar	inį	put	pin													
			Output	1					(Cor	nfigure	e pi	in a	ar	า อน	ıtpı	ıt p	in												
В	RW	INPUT							(Cor	nnect	or	disc	onr	nect	t inp	put	buf	fer											
			Connect	0					(Cor	nnect	inp	ut b	uff	er															
			Disconnect	1					[Dis	conne	ct	inpu	ıt b	uffe	er														
С	RW	PULL							F	Pul	II confi	gu	ratio	on																
			Disabled	0					1	No	pull																			
			Pulldown	1					F	Pul	II dow	n o	n pi	n																
			Pullup	3					F	Pul	ll up o	n p	in																	
D	RW	DRIVE							[Dri	ive cor	ıfig	ura	ior	1															
			S0S1	0					9	Sta	andard	'0'	, sta	ınd	ard	'1'														
			H0S1	1					ŀ	Hig	gh driv	e '()', st	an	dar	d '1	.'													
			S0H1	2					9	Sta	andard	'0'	, hig	gh c	driv	e '1														
			H0H1	3					ŀ	Hig	gh driv	e '()', h	igh	'dr	ive	'1"													
			DOS1	4					[Dis	conne	ct	'0' s	tan	dar	d '1	L' (n	orn	nally	us	ed f	or v	vire	d-or						
									C	con	nnecti	ons	5)																	
			D0H1	5					[Dis	conne	ct	'0', I	nigh	n dr	ive	'1'	(no	rmal	lyι	ısed	for	wir	ed-d	or					
									C	con	nnecti	ons	5)																	
			SOD1	6					9	Sta	andard	'0'	. dis	COI	nne	ct '	1' (ı	nori	mally	/ us	sed t	or	wire	d-ar	nd					
									C	con	nnecti	ons	5)																	
			H0D1	7					ŀ	Hig	gh driv	e '()', d	isco	onn	ect	'1'	(no	rmal	lyι	ısed	for	wir	ed-a	nd					
									(con	nnecti	ons	5)																	
E	RW	SENSE									sensi	ng	med	ha	nisr	n														
			Disabled	0					[Dis	abled																			
			High	2					9	Ser	nse for	· hi	gh l	eve	el															
			Low	3					9	Ser	nse for	· lo	w le	vel																

19.3.39 PIN_CNF[29]

Address offset: 0x774



Bit r	numbe	er		31 3	0 29	28	27 2	6 25	5 24	23	22 2	21 20	0 19	18	17	16	15	14 1	.3 1	2 13	1 10	9	8	7	6	5 4	1 3	2	1	0
Id															Ε	Ε					D	D	D				С	С	В	Α
Res	et OxC	00000002		0 (0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0 0	0	1	0
Id	RW	Field	Value Id	Valu	e					De	escrip	tion	l																	
Α	RW	DIR								Pir	n dire	ctio	n. S	ame	e ph	iysic	al r	egist	er a	as D	IR re	egist	er							
			Input	0						Со	nfigu	ıre p	in a	s an	inp	out	pin													
			Output	1						Со	nfigu	ıre p	in a	s an	ou	tpu	t pi	n												
В	RW	INPUT								Со	nnec	t or	disc	onn	nect	inp	ut l	ouffe	er											
			Connect	0						Со	nnec	t inp	out b	ouff	er															
			Disconnect	1						Dis	sconr	nect	inpı	ut b	uffe	er														
С	RW	PULL								Pu	ıll cor	nfigu	rati	on																
			Disabled	0						No	pull																			
			Pulldown	1						Pu	ıll dov	wn o	n pi	n																
			Pullup	3						Pu	ıll up	on p	in																	
D	RW	DRIVE								Dri	ive co	onfig	gura	tion	1															
			S0S1	0						Sta	andaı	rd '0	', sta	anda	ard	'1'														
			H0S1	1						Hig	gh dr	ive '	0', s	tano	dard	d '1'														
			S0H1	2						Sta	andaı	rd '0	', hi	gh d	irive	e '1'														
			H0H1	3						Hig	gh dr	ive '	0', h	igh	'dri	ve '	1''													
			DOS1	4						Dis	sconr	nect	'0' s	tan	dar	d '1	' (n	orma	ally	used	d for	vir	ed-	or						
										COI	nnec	tions	s)																	
			D0H1	5						Dis	sconr	nect	'0',	high	n dri	ive '	'1' (norn	nall	y us	ed f	or w	/ire	d-or						
										COI	nnec	tions	s)																	
			SOD1	6						Sta	andaı	rd '0	'. di	scor	nne	ct '1	L' (n	orm	ally	use	d fo	r wi	red	and	i					
										COI	nnec	tions	s)																	
			H0D1	7						Hig	gh dr	ive '	0', d	isco	onne	ect '	'1' (norn	nall	y us	ed f	or w	/ire	d-an	ıd					
										COI	nnec	tions	s)																	
Ε	RW	SENSE									n sen	-	me	char	nisn	n														
			Disabled	0							sable																			
			High	2						Sei	nse f	or hi	igh I	eve	1															
			Low	3						Sei	nse f	or lo	w le	evel																

19.3.40 PIN_CNF[30]

Address offset: 0x778 Configuration of GPIO pins

numb	er		31	. 30	29	28	27	26 2	25 :	24	23 2	22	21 :	20	19 1	18 :	17 :	16	15 1	.4 :	13 :	12 :	l1 1	0 9	8	7	6	5	4	3	2	1 (
																	Е	E					1) [D					С	C I	ВА
et 0x(00000002		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1 (
RW	Field	Value Id	Va	lue							Des	cri	ptio	n																		
RW	DIR										Pin	dir	ecti	on.	Sar	ne	phy	sic	al re	gis	ter	as	DIR	regi	ster							
		Input	0								Con	fig	ure	pin	as	an i	inpı	ut p	in													
		Output	1								Con	fig	ure	pin	as	an (out	put	pin													
RW	INPUT										Con	ne	ct o	r di	sco	nne	ect i	np	ut b	uff	er											
		Connect	0								Con	ne	ct ir	npu	t bu	ffe	r															
		Disconnect	1								Disc	on	nec	t in	put	bu	ffer															
RW	PULL										Pull	со	nfig	gura	tioi	1																
		Disabled	0								No p	pul	I																			
		Pulldown	1								Pull	do	wn	on	pin																	
		Pullup	3								Pull	up	on	pir	1																	
RW	DRIVE										Driv	e c	onf	igu	rati	on																
		S0S1	0							:	Star	nda	rd '	0',	star	ıda	rd '	1'														
		H0S1	1								High	n d	rive	'0'	, sta	nd	ard	'1'														
		S0H1	2							:	Star	nda	rd '	0',	high	dr	ive	'1'														
		H0H1	3								High	n di	rive	'0'	, hig	h 'd	driv	e '1	L''													
		DOS1	4								Disc	on	nec	t '0	' sta	nd	ard	'1'	(no	rm	ally	use	ed f	or w	ired	l-or						
											con	nor	rtio	ns)																		
	RW RW	RW Field RW DIR RW INPUT RW PULL RW DRIVE	RW Field Value Id RW DIR Input Output RW INPUT Connect Disconnect RW PULL Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 HOH1	RW Field Value Id Val	RW Field Value Id Val	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3 THE SOH1 2 HOH1 3 TO T	RW Field Value Id Id Id Value Id Id Id Value Id	RW Field Value Id Val	RW Field Value Id Value Id Value Id Value Id RW DIR RW INPUT Connect Disconnect 1 RW PULL PULL Disabled O Pulldown 1 Pullup 3 RW DRIVE SOS1 O HOS1 SOH1 SOH1 SOH1 SOH1 SOH1 SOH1 SOH1 SOH1	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3 DOS1 4	RW Field Value Id Value RW DIR Input Output 1 Connect Disconnect Disconnect Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 SOH1 SOH1 SOH1 SOH1 SOS1 HOHI DISCON SON OUTPUT	RW Field Value Id Value	RW Field Value Id Val	RW Field Value Id Value	RW Field Value Id Val	RW Field Value Id Value Valu	RW Field Value Id Value	RW Field Value Market Pin direction. Same physical	RW Field Value Id Value Pin direction. Same physical reference Pin d	RW Field Value Id Value Pin direction. Same physical register	RW Field Value Id Value Id Value Id Description Pin direction. Same physical register	RW Field Value Id Value Valu	RW Field Value Id Value Pin direction. Same physical register as DIR	RW Field	RW Field Value Id Value	RW Field Value Id Value Id Pin direction. Same physical register as DIR regist	RW Field Value Id Pind irection. Same physical register as DIR register NPUT	RW Field Value Id Value	RW Field Value Id Value Valu	NPUT	RW Field Value Id Value Valu



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

19.3.41 PIN_CNF[31]

Address offset: 0x77C

Configuration of GPIO pins

	<u> </u>		
Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E E D D D C C B A
Reset 0x00000002		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW DIR			Pin direction. Same physical register as DIR register
	Input	0	Configure pin as an input pin
	Output	1	Configure pin as an output pin
B RW INPUT			Connect or disconnect input buffer
	Connect	0	Connect input buffer
	Disconnect	1	Disconnect input buffer
C RW PULL			Pull configuration
	Disabled	0	No pull
	Pulldown	1	Pull down on pin
	Pullup	3	Pull up on pin
D RW DRIVE			Drive configuration
	S0S1	0	Standard '0', standard '1'
	H0S1	1	High drive '0', standard '1'
	SOH1	2	Standard '0', high drive '1'
	H0H1	3	High drive '0', high 'drive '1"
	DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
			connections)
	D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or connections)
	SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
	11004	_	connections)
	H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
F DW CENCE			connections)
E RW SENSE	Disabled	0	Pin sensing mechanism
	Disabled	0	Disabled
	High	2	Sense for high level
	Low	3	Sense for low level

19.4 Electrical specification

19.4.1 GPIO Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
V _{IH}	Input high voltage	0.7 x VD	D	VDD	V



Symbol	Description	Min.	Тур.	Max.	Units
V _{IL}	Input low voltage	VSS		0.3 x VDI	O V
V _{OH,SD}	Output high voltage, standard drive, 0.5 mA, VDD ≥1.7	VDD-0.4		VDD	V
V _{OH,HDH}	Output high voltage, high drive, 5 mA, VDD >= 2.7 V	VDD-0.4		VDD	V
V _{OH,HDL}	Output high voltage, high drive, 3 mA, VDD >= 1.7 V	VDD-0.4		VDD	V
V _{OL,SD}	Output low voltage, standard drive, 0.5 mA, VDD ≥1.7	VSS		VSS+0.4	V
V _{OL,HDH}	Output low voltage, high drive, 5 mA, VDD >= 2.7 V	VSS		VSS+0.4	V
V _{OL,HDL}	Output low voltage, high drive, 3 mA, VDD >= 1.7 V	VSS		VSS+0.4	V
I _{OL,SD}	Current at VSS+0.4 V, output set low, standard drive, VDD ≥1.7	1	2	4	mA
I _{OL,HDH}	Current at VSS+0.4 V, output set low, high drive, VDD >= 2.7 V	6	10	15	mA
I _{OL,HDL}	Current at VSS+0.4 V, output set low, high drive, VDD >= 1.7 V	3			mA
I _{OH,SD}	Current at VDD-0.4 V, output set high, standard drive, VDD ≥1.7	1	2	4	mA
I _{OH,HDH}	Current at VDD-0.4 V, output set high, high drive, VDD >= 2.7 V	6	9	14	mA
I _{OH,HDL}	Current at VDD-0.4 V, output set high, high drive, VDD >= 1.7 V	3			mA
t _{RF,15pF}	Rise/fall time, standard drive mode, 10-90%, 15 pF load ¹		9		ns
t _{RF,25pF}	Rise/fall time, standard drive mode, 10-90%, 25 pF load ¹		13		ns
t _{RF,50pF}	Rise/fall time, standard drive mode, 10-90%, 50 pF load ¹		25		ns
t _{HRF,15pF}	Rise/Fall time, high drive mode, 10-90%, 15 pF load ¹		4		ns
t _{HRF,25pF}	Rise/Fall time, high drive mode, 10-90%, 25 pF load ¹		5		ns
t _{HRF,50pF}	Rise/Fall time, high drive mode, 10-90%, 50 pF load ¹		8		ns
R _{PU}	Pull-up resistance	11	13	16	kΩ
R _{PD}	Pull-down resistance	11	13	16	kΩ
C _{PAD}	Pad capacitance		3		pF
C _{PAD_NFC}	Pad capacitance on NFC pads		4		pF
I _{NFC_LEAK}	Leakage current between NFC pads when driven to different		1	4	μΑ
	states				

The current drawn from the battery when GPIO is active as an output is calculated as follows:

 I_{GPIO} = V_{DD} C_{load} f

 C_{load} being the load capacitance and "f" is the switching frequency.

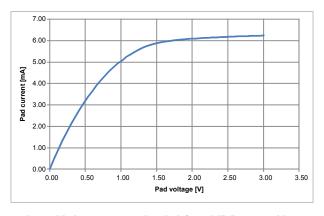


Figure 24: GPIO drive strength vs Voltage, standard drive, VDD = 3.0 V

¹ Rise and fall times based on simulations



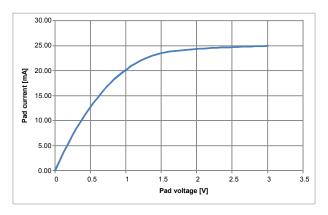


Figure 25: GPIO drive strength vs Voltage, high drive, VDD = 3.0 V

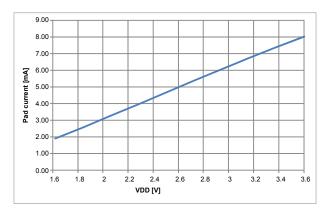


Figure 26: Max sink current vs Voltage, standard drive

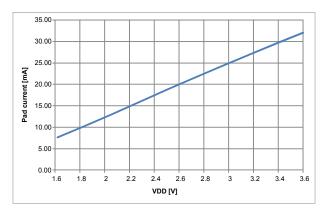


Figure 27: Max sink current vs Voltage, high drive

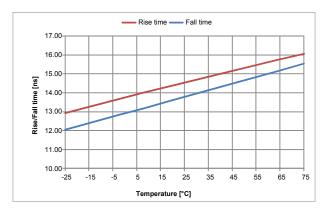


Figure 28: Rise and fall time vs Temperature, 10%-90%, 25pF load capacitance, VDD = 3.0 V



20 GPIOTE — GPIO tasks and events

The GPIO tasks and events (GPIOTE) module provides functionality for accessing GPIO pins using tasks and events. Each GPIOTE channel can be assigned to one pin.

A GPIOTE block enables GPIOs to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system. Low power detection of pin state changes is possible when in System ON or System OFF.

Table 23: GPIOTE properties

Instance	Number of GPIOTE channels
GPIOTE	8

Up to three tasks can be used in each GPIOTE channel for performing write operations to a pin. Two tasks are fixed (SET and CLR), and one (OUT) is configurable to perform following operations:

- Set
- Clear
- Toggle

An event can be generated in each GPIOTE channel from one of the following input conditions:

- · Rising edge
- Falling edge
- · Any change

20.1 Pin events and tasks

The GPIOTE module has a number of tasks and events that can be configured to operate on individual GPIO pins.

The tasks (SET[n], CLR[n] and OUT[n]) can be used for writing to individual pins, and the events (IN[n]) can be generated from changes occurring at the inputs of individual pins.

The SET task will set the pin selected in CONFIG[n].PSEL to high.

The CLR task will set the pin low.

The effect of the OUT task on the pin is configurable in CONFIG[n].POLARITY, and can either set the pin high, set it low, or toggle it.

The tasks and events are configured using the CONFIG[n] registers. Every set of SET, CLR and OUT[n] tasks and IN[n] events has one CONFIG[n] register associated with it.

As long as a SET[n], CLR[n] and OUT[n] task or an IN[n] event is configured to control a pin **n**, the pin's output value will only be updated by the GPIOTE module. The pin's output value as specified in the GPIO will therefore be ignored as long as the pin is controlled by GPIOTE. Attempting to write a pin as a normal GPIO pin will have no effect. When the GPIOTE is disconnected from a pin, see MODE field in CONFIG[n] register, the associated pin will get the output and configuration values specified in the GPIO module.

When conflicting tasks are triggered simultaneously (i.e. during the same clock cycle) in one channel, the precedence of the tasks will be as described in *Table 24: Task priorities* on page 200.

Table 24: Task priorities

Priority	Task
1	OUT
2	CLR
2	CET



When setting the CONFIG[n] registers, MODE=Disabled does not have the same effect as MODE=Task and POLARITY=None. In the latter case, a CLR or SET task occurring at the exact same time as OUT will end up with no change on the pin, according to the priorities described in the table above.

When a GPIOTE channel is configured to operate on a pin as a task, the initial value of that pin is configured in the OUTINIT field of CONFIG[n].

20.2 Port event

PORT is an event that can be generated from multiple input pins using the GPIO DETECT signal.

The event will be generated on the rising edge of the DETECT signal. See *GPIO* — *General purpose input/output* on page 154 for more information about the DETECT signal.

Putting the system into System ON IDLE while DETECT is high will not cause DETECT to wake the system up again. Make sure to clear all DETECT sources before entering sleep. If the LATCH register is used as a source, if any bit in LATCH is still high after clearing all or part of the register (for instance due to one of the PINx.DETECT signal still high), a new rising edge will be generated on DETECT, see *Pin configuration* on page 154.

Trying to put the system to System OFF while DETECT is high will cause a wakeup from System OFF reset.

This feature is always enabled although the peripheral itself appears to be IDLE, that is, no clocks or other power intensive infrastructure have to be requested to keep this feature enabled. This feature can therefore be used to wake up the CPU from a WFI or WFE type sleep in System ON with all peripherals and the CPU idle, that is, lowest power consumption in System ON mode.

In order to prevent spurious interrupts from the PORT event while configuring the sources, the user shall first disable interrupts on the PORT event (through INTENCLR.PORT), then configure the sources (PIN_CNF[n].SENSE), clear any potential event that could have occurred during configuration (write '1' to EVENTS_PORT), and finally enable interrupts (through INTENSET.PORT).

20.3 Tasks and events pin configuration

Each GPIOTE channel is associated with one physical GPIO pin through the CONFIG.PSEL field.

When Event mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an input, overriding the DIR setting in GPIO. Similarly, when Task mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an output overriding the DIR setting and OUT value in GPIO. When Disabled is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will use its configuration from the PIN[n].CNF registers in GPIO.

Only one GPIOTE channel can be assigned to one physical pin. Failing to do so may result in unpredictable behavior.

20.4 Registers

Table 25: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40006000	GPIOTE	GPIOTE	GPIO tasks and events	

Table 26: Register Overview

Register	Offset	Description
TASKS_OUT[0]	0x000	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is configured in
		CONFIG[0].POLARITY.
TASKS_OUT[1]	0x004	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is configured in
		CONFIG[1].POLARITY.



TASKS_OUT[3] 0x008 Task for writing to pin specified in CONFIG[2].PSEL Action on pin is configured in CONFIG[3].POLARITY. TASKS_OUT[4] 0x000 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is configured in CONFIG[3].POLARITY. TASKS_OUT[4] 0x001 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is configured in CONFIG[7].PSEL Action on pin is to set it high. TASKS_OUT[7] 0x012 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[7] 0x038 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[7] 0x038 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_CRITIO 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_CRITIO 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_CRITIO 0x040 Task for writing to pin spec	Register	Offset	Description
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TASKS_OUT[3] bibOC Task for writing to pin specified in CONFIG[3].PSEL Action on pin is configured in CONFIG[3].POLARITY. TASKS_OUT[5] bibO14 Task for writing to pin specified in CONFIG[4].PSEL Action on pin is configured in CONFIG[5].POLARITY. TASKS_OUT[5] bibO14 Task for writing to pin specified in CONFIG[5].PSEL Action on pin is configured in CONFIG[6].PSEL Action on pin is configured in CONFIG[7].PSEL Action on pin is to set it high. TASKS_OUT[7] bibO12 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[1] bibO34 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[1] bibO34 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[8] bibO35 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[8] bibO36 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[8] bibO38 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[8] bibO38 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[8] bibO38 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CER[8] bibO39 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CER[8] bibO39 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CER[8] bibO39 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CER[8] bibO39 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it how. TASKS_CER[8] bibO39 Task for writing to pin specified	1/13/13_001[2]	0,000	
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TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it low. TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[7].PSEL Action on pin is to set it low. EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[6] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[2]	0x068	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it low.
TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[3]	0x06C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low.
TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[4]	0x070	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it low.
TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[5]	0x074	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low.
EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[6]	0x078	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low.
EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[7]	0x07C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low.
EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[0]	0x100	Event generated from pin specified in CONFIG[0].PSEL
EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[1]	0x104	Event generated from pin specified in CONFIG[1].PSEL
EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[2]	0x108	Event generated from pin specified in CONFIG[2].PSEL
EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[3]	0x10C	Event generated from pin specified in CONFIG[3].PSEL
EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[4]	0x110	Event generated from pin specified in CONFIG[4].PSEL
EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[5]	0x114	Event generated from pin specified in CONFIG[5].PSEL
EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[6]	0x118	Event generated from pin specified in CONFIG[6].PSEL
INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[7]	0x11C	Event generated from pin specified in CONFIG[7].PSEL
INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_PORT	0x17C	Event generated from multiple input GPIO pins with SENSE mechanism enabled
CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	INTENSET	0x304	Enable interrupt
CONFIG[1] Ox514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] Ox518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] Ox51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] Ox520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] Ox524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	INTENCLR	0x308	Disable interrupt
CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	CONFIG[0]	0x510	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	CONFIG[1]	0x514	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	CONFIG[2]	0x518	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	CONFIG[3]	0x51C	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
	CONFIG[4]	0x520	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	CONFIG[5]	0x524	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
• • • • • • • • • • • • • • • • • • • •	CONFIG[6]	0x528	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[7] 0x52C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	CONFIG[7]	0x52C	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

20.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		31 3	30 29	28	27 2	26 2	5 2	4 2	3 22	2 21	L 20	19	18	17	16	15	14	13	12 :	11 1	9	8	7	6	5	4	3	2	1 0
Id		1																					Н	G	F	Ε	D	С	ВА
Reset 0x00000000		0	0 0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id RW Field	Value Id	Valu	ıe					D	esc	ripti	ion																		

Write '1' to Enable interrupt for IN[0] event



Bit r	number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			1	H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
				See EVENTS_IN[0]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW IN1			Write '1' to Enable interrupt for IN[1] event
				See EVENTS_IN[1]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW IN2			Write '1' to Enable interrupt for IN[2] event
				See EVENTS_IN[2]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW IN3			Write '1' to Enable interrupt for IN[3] event
				See EVENTS_IN[3]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E	RW IN4			Write '1' to Enable interrupt for IN[4] event
		Set	1	See EVENTS_IN[4] Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW IN5	Endoica	-	Write '1' to Enable interrupt for IN[5] event
				See EVENTS_IN[5]
		Set	1	Enable
		Disabled	0	Read: Disabled
_	DIA/ INC	Enabled	1	Read: Enabled Write '1' to Enable interrupt for IN[6] event
G	RW IN6			
				See EVENTS_IN[6]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW IN7			Write '1' to Enable interrupt for IN[7] event
				See EVENTS_IN[7]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
I	RW PORT			Write '1' to Enable interrupt for PORT event
				See EVENTS_PORT
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

20.4.2 INTENCLR

Address offset: 0x308

Disable interrupt



Bit	numb	er		31 30	29	28 :	27 2	6 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				1						H G F E D C B A
Res	et 0x0	0000000		0 0	0	0	0 () (0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value						Description
Α	RW	INO								Write '1' to Disable interrupt for IN[0] event See EVENTS_IN[0]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
В	RW	IN1								Write '1' to Disable interrupt for IN[1] event
			a.							See EVENTS_IN[1]
			Clear	1						Disable
			Disabled	0						Read: Disabled
_	D\A/	INIO	Enabled	1						Read: Enabled
С	KVV	IN2								Write '1' to Disable interrupt for IN[2] event See EVENTS_IN[2]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
D	RW	IN3								Write '1' to Disable interrupt for IN[3] event
										See EVENTS_IN[3]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Ε	RW	IN4								Write '1' to Disable interrupt for IN[4] event
										See EVENTS_IN[4]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
F	RW	IN5								Write '1' to Disable interrupt for IN[5] event
										See EVENTS_IN[5]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
G	RW	IN6								Write '1' to Disable interrupt for IN[6] event
										See EVENTS_IN[6]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Н	RW	IN7								Write '1' to Disable interrupt for IN[7] event See EVENTS IN[7]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
ı	RW	PORT								Write '1' to Disable interrupt for PORT event
										See EVENTS_PORT
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled

20.4.3 CONFIG[0]

Address offset: 0x510



Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E DD CBBBB AA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	MODE			Mode
			Disabled	0	Disabled. Pin specified by PSEL will not be acquired by the
					GPIOTE module.
			Event	1	Event mode
					The pin specified by PSEL will be configured as an input and the
					IN[n] event will be generated if operation specified in POLARITY
					occurs on the pin.
			Task	3	Task mode
					The GPIO specified by PSEL will be configured as an output and
					triggering the SET[n], CLR[n] or OUT[n] task will perform the
					operation specified by POLARITY on the pin. When enabled as a
					task the GPIOTE module will acquire the pin and the pin can no
					longer be written as a regular output pin from the GPIO module.
В	RW	PSEL		[031]	GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
					and IN[n] event
С	RW	PORT		[01]	Port number
D	RW	POLARITY			When In task mode: Operation to be performed on output
					when OUT[n] task is triggered. When In event mode: Operation
					on input that shall trigger IN[n] event.
			None	0	Task mode: No effect on pin from OUT[n] task. Event mode: no
					IN[n] event generated on pin activity.
			LoToHi	1	Task mode: Set pin from OUT[n] task. Event mode: Generate
					IN[n] event when rising edge on pin.
			HiToLo	2	Task mode: Clear pin from OUT[n] task. Event mode: Generate
			TI-	2	IN[n] event when falling edge on pin.
			Toggle	3	Task mode: Toggle pin from OUT[n]. Event mode: Generate
E	R\M	OUTINIT			IN[n] when any change on pin. When in task mode: Initial value of the output when the GPIOTE
E	I VV	OUTINIT			channel is configured. When in event mode: No effect.
			Low	0	Task mode: Initial value of pin before task triggering is low
			High	1	Task mode: Initial value of pin before task triggering is low
			'''b''	-	rask mode. Initial value of pin before task triggering is night

20.4.4 CONFIG[1]

Address offset: 0x514

	_																																		
Bitı	numbe	er		3	1 30	29	28	27	26	25	24	23	22 :	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															Ε			D	D			С	В	В	В	В	В							Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	alue							Des	cri	otic	n																				
Α	RW	MODE										Мо	de																						
			Disabled	0								Disa	able	ed.	Pin	spe	ecif	ied	by	PSI	EL١	will	not	be	aco	quir	ed l	by 1	the						
												GPI	ОТЕ	E m	odı	ıle.																			
			Event	1								Eve	nt r	noc	de																				
												The	pir	ı sp	eci	fied	d by	/ PS	EL	wil	l be	e co	nfig	gure	ed a	ıs aı	n in	put	an	d th	ne				
												IN[r	ո] e	ver	nt w	ill l	oe g	gen	era	ited	l if	оре	erat	ion	spe	ecifi	ed i	in P	OL	٩RI	ΤY				
												осс	urs	on	the	piı	n.																		
			Task	3								Tas	k m	ode	е																				
												The	GP	PIO.	spe	cifi	ed	by	PSI	Lw	/ill	be	con	figu	ırec	l as	an	out	put	an	d				
												trig	ger	ing	the	SE	T[r	1], (CLR	[n]	or	OU.	T[n]] ta:	sk v	vill p	erf	orr	n th	ie					
												ope	rat	ion	spe	ecif	ied	by	PC	LAF	RIT	Y oı	n th	ер	in. ۱	Whe	en e	ena	ble	d as	a				



Bit	numb	er		31 30	29	28	27 2	26 2	5 24	4 23	3 22	2 21	20	19	18	17	16	15	14 1	L3 1	12 1	1 10	9	8	7	6	5 4	4 3	3 2	1	0
Id													Ε			D	D			С	ВЕ	В	В	В						Α	Α
Res	et 0x0	00000000		0 0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Value	•					D	esc	ripti	on																		
										ta	isk 1	the (GPI	OTE	E m	odu	le v	vill a	icqu	ire	the	pin a	nd	the	pir	ca	n no				
										lo	nge	er be	e w	ritte	en a	ıs a	reg	ular	out	put	pin	fror	n th	ie G	PIO	mo	dul	е.			
В	RW	PSEL		[031	.]					GI	PIO	nur	nbe	er a	sso	ciat	ed v	vith	SE1	[n]	, CLI	R[n]	and	OL	JT[n] ta	sks				
										ar	nd I	N[n]] ev	/ent	t																
С	RW	PORT		[01]						Po	ort	num	ıbe	r																	
D	RW	POLARITY								W	/he	n In	tas	k m	ode	e: O	per	atio	n to	be	per	form	ed	on	out	put					
										W	her	n OU	JT[r	n] ta	ask	is tr	igge	erec	. W	hen	In e	even	t m	ode	: 0	oera	tior	1			
										or	n in	put	tha	at sh	nall	trig	ger	IN[ı	n] ev	/en	t.										
			None	0						Ta	ask	mod	de:	No	eff	ect o	on p	in f	rom	OL	JT[n] tas	k. E	ven	t m	ode	: no				
										IN	l[n]	eve	nt	gen	era	ted	on	pin	acti	vity											
			LoToHi	1						Ta	ask	mod	de:	Set	pin	fro	m (UT	[n] t	ask	. Eve	ent r	noc	le: 0	Gen	erat	te				
										IN	l[n]	eve	nt	whe	en r	isin	g e	lge	on p	in.											
			HiToLo	2								mod							-	-		ven	m	ode	: Ge	enei	rate				
												eve					-	-													
			Toggle	3								mod		_						n].	Evei	nt m	ode	e: G	ene	rate	9				
												whe				-		•													
Ε	RW	OUTINIT										n in										•				e GF	PIOT	E			
												nel i			-																
			Low	0								mod												_							
			High	1						Ta	ask	mod	de:	Init	ial v	/alu	e o	fpir	be	ore	tas	k triį	gge	ring	is h	nigh					

20.4.5 CONFIG[2]

Address offset: 0x518

Bit r	iumbe	er		31	. 30	29	28 2	27 2	6 25	5 24	1 23	22 2	21 2	0 19	18	17	16	15 1	L4 1	3 1	2 11	10	9	8	7	6 5	4	3	2	1 0
Id													E			D	D		(С В	В	В	В	В					,	А А
Res	et 0x0	0000000		0	0	0	0	0 (0 0	0	0	0	0 0	0 0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						Des	scrip	otion	1																
Α	RW	MODE									Мо	ode																		
			Disabled	0							Dis	able	d. P	in sp	oeci	fied	by	PSEI	wil	l no	t be	acq	uire	ed b	y th	е				
											GPI	IOTE	mo	dule	2.															
			Event	1							Eve	ent n	node	e																
											The	e pin	spe	ecifie	ed b	y PS	SEL 1	will l	oe c	onfi	gure	ed a	s an	inp	ut a	and t	he			
											IN[n] e	vent	will	be	gen	era	ted i	if op	era	tion	spe	cifie	ed in	PC	LAR	ITY			
											occ	curs	on t	he p	in.															
			Task	3							Tas	sk m	ode																	
											The	e GP	IO s	peci	fied	by	PSE	L wi	ll be	COI	nfigu	ıred	as a	an o	utp	ut a	nd			
											trig	ggeri	ing t	he S	ET[n], (CLR[n] o	r Ol	JT[r] ta	sk w	ill p	erfo	rm	the				
											оре	erati	ion s	pec	ified	d by	РО	LARI	TY c	n tl	he p	in. V	Vhe	n er	nab	led a	is a			
											tas	k the	e GP	TOI	E m	odu	le w	ill a	cqui	ire t	he p	oin a	nd 1	the _l	oin	can	no			
											lon	iger	be w	vritt	en a	is a	reg	ılar	out	out	pin	from	the	e GP	Oli	mod	lule.			
В	RW	PSEL		[0	31]						GPI	IO n	umb	er a	SSO	ciate	ed v	vith	SET	[n],	CLR	[n] a	ınd	OUT	[n]	tasl	(S			
											and	d IN[[n] e	ven	t															
С	RW	PORT		[0	1]						Por	rt nu	ımbe	er																
D	RW	POLARITY									Wh	nen I	n ta	sk m	node	e: O	per	atio	n to	be	perf	orm	ed o	on o	utp	ut				
											wh	en C	TUC	[n] ta	ask	is tr	igge	red	. Wł	nen	In e	vent	mc	de:	Op	erat	ion			
											on	inpu	ıt th	at sl	nall	trig	ger	IN[n] ev	ent										
			None	0								sk m										task	. Ev	ent	mc	de:	no			
											-	n] e		-																
			LoToHi	1								sk m						-	-		Eve	nt m	ode	e: G	ene	rate				
											IN[n] e	vent	wh	en r	isin	g ec	lge o	n p	in.										



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E DD CBBBB AA
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
		IN[n] event when falling edge on pin.
	Toggle	Task mode: Toggle pin from OUT[n]. Event mode: Generate
		IN[n] when any change on pin.
E RW OUTINIT		When in task mode: Initial value of the output when the GPIOTE
		channel is configured. When in event mode: No effect.
	Low	0 Task mode: Initial value of pin before task triggering is low
	High	1 Task mode: Initial value of pin before task triggering is high

20.4.6 CONFIG[3]

Address offset: 0x51C

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

State Stat	Ç 1,		-		-													
Reset 0.00000000 Value V	Bit number	31	1 30 29 28 27 26	5 25 24 2	23 22 21 20	19 18	17 16	6 15 1	4 13	12 1	11 10	9 8	7	6	5	4 3	2	1 0
Note	Id				Е		D D)	С	В	ВВ	ВВ						A A
A RW MODE Disabled 0 Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module. Event 1 Event mode The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin. Task 3 Task mode The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. B RW PSEL	Reset 0x00000000	0	0 0 0 0 0	000	0 0 0 0	0 0	0 0	0 (0 0	0 (0 0	0 0	0	0	0	0 0	0	0 0
Part	Id RW Field Valu	ue Id V	alue	C	Description													
GPIOTE module. Event 1 Event mode The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin. Task 3 Task mode The GPIO specified by PSEL will be configured as an input and the operation specified in POLARITY occurs on the pin. Task 5 Task mode The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. B RW PSEL [0.31] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event C RW PORT [0.1] Port number D RW POLARITY When an interval is a sequence of the performed on output when OUT[n] task is triggered. When in event mode: Operation on input that shall trigger IN[n] event. None 0 Task mode: Operation to be performed on output when OUT[n] task. Event mode: Operation on IN[n] event generated on pin activity. LOTOHI 1 Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. HITOLO 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] event when falling edge on pin. When in task mode initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low	A RW MODE			N	Лode													
Event mode The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin. Task Task Task Task B RW PSEL C RW PORT D RW POLARITY None None LOTOHI LOTOHI LOTOHI 1 1 2 2 3 3 4 3 4 3 4 3 4 3 4 3 4 3 4 3 4 3	Disa	abled 0		0	Disabled. Pii	n specif	fied by	y PSEL	ı lliw.	not b	e acq	uired	by t	he				
The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin. Task Task Task as Task mode The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. B RW PSEL [031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event C RW PORT [01] Port number When in task mode: Operation to be performed on output when OUT[n] task is triggered. When in event mode: Operation on input that shall trigger IN[n] event. None O Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event when GPIOT[n] event when falling edge on pin. Toggle Toggle Task mode: Clear pin from OUT[n]. Event mode: Generate IN[n] event when falling edge on pin. Toggle Task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low O Task mode: Initial value of pin before task triggering is low				G	SPIOTE mod	dule.												
IN[n] event will be generated if operation specified in POLARITY occurs on the pin. Task Task node The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. B RW PSEL [031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event D RW PORT [01] Port number When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. None O Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. HITOLO Toggle Toggle Toggle Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low O Task mode: Initial value of pin before task triggering is low	Ever	nt 1		E	vent mode													
occurs on the pin. Task				Т	he pin spec	cified by	y PSEL	L will b	oe cor	nfigu	red a	s an ir	put	and	the	9		
Task Mode The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. B RW PSEL [031]				II	N[n] event	will be a	gener	ated i	f ope	ratio	n spe	cified	in P	OLA	RIT	Y		
The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. B RW PSEL [0.31]				O	occurs on th	ne pin.												
triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. B RW PSEL [031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event and IN[n] event C RW PORT [01] Port number D RW POLARITY When in task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. None 0 Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. LoTOHi 1 Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. HITOLO 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When any change on pin. LoW 0 Task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.	Task	k 3		Т	ask mode													
operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. B RW PSEL [031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event C RW PORT [01] Port number When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. None 0 Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. LOTOHI 1 Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. Toggle 3 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low				Т	he GPIO sp	ecified	by PS	EL wil	l be c	onfig	gured	as an	out	put	and			
task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. B RW PSEL [031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event C RW PORT [01] Port number When In task mode: Operation to be performed on output when OUT[n] task is triggered. When in event mode: Operation on input that shall trigger IN[n] event. None O Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. LoToHi 1 Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. HITOLO 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.				t	riggering th	ne SET[r	n], CLF	R[n] or	r OUT	[n] t	ask w	ill per	forn	n the	e			
B RW PSEL [031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event				O	peration sp	pecified	by Po	OLARI	TY on	the	pin. V	Vhen	enal	bled	las	а		
B RW PSEL [031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event C RW PORT [01] Port number When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. None 0 Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. LoToHi 1 Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. HiToLo 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low				t	ask the GPI	OTE mo	odule	will a	cquire	e the	pin a	nd th	e pir	n car	n no)		
and IN[n] event C RW PORT [01] Port number When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. None 0 Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. LoTOHi 1 Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. HiToLo 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low				lo	onger be w	ritten a	s a re	gular	outpu	ut pir	n from	the (GPIC) mo	dul	e.		
C RW PORT [01] Port number When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. None 0 Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. LoToHi 1 Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. HiToLo 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low	B RW PSEL	[0)31]	G	GPIO numbe	er assoc	ciated	with:	SET[n	1], CL	R[n] a	nd O	UT[r] ta	sks			
D RW POLARITY When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. None O Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. LoToHi 1 Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. HiToLo 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low				a	ınd IN[n] ev	ent												
when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event. None 0 Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. LoToHi 1 Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. HiToLo 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low	C RW PORT	[0)1]	P	ort numbe	r												
on input that shall trigger IN[n] event. None 0 Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. LoToHi 1 Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. HiToLo 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low	D RW POLARITY			٧	When In tas	k mode	e: Ope	eration	to b	e per	rform	ed on	out	put				
None 0 Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity. LoToHi 1 Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. HiToLo 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low				V	vhen OUT[r	n] task i	s trigg	gered.	Whe	n In	event	mod	e: 0	pera	oite	n		
IN[n] event generated on pin activity. LoToHi 1 Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. HiToLo 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low				0	on input tha	t shall t	trigge	r IN[n] ever	nt.								
LoToHi 1 Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin. HiToLo 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low	Non	ne 0		Т	ask mode:	No effe	ect on	pin fr	om O	UT[n	n] tasl	. Eve	nt m	ode	: no)		
IN[n] event when rising edge on pin. HiToLo 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low				II	N[n] event	generat	ted or	n pin a	ctivit	y.								
HiToLo 2 Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin. Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low	LoTo	oHi 1				•		_	-		ent n	node:	Gen	erat	te			
Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low								•										
Toggle 3 Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low	HiTo	oLo 2									Event	mod	e: G	ener	rate			
IN[n] when any change on pin. E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low								_										
E RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low	Togg	gle 3					•			. Eve	nt mo	ode: G	iene	rate	2			
channel is configured. When in event mode: No effect. Low 0 Task mode: Initial value of pin before task triggering is low	5 DW OUTDUT					•	-	•						-		_		
Low 0 Task mode: Initial value of pin before task triggering is low	E RW OUTINIT										•			e GF	TOI	E		
		_				-												
High 1 Task mode: Initial value of pin before task triggering is high											_	_	_					
	High	л 1		Т	ask mode:	initial v	alue (ot pin	petor	re tas	sk trig	gerin	g is h	ııgh				

20.4.7 CONFIG[4]

Address offset: 0x520



Bit number	31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E DD CBBBB AA
Reset 0x00000000	0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field Value Id	Value	Description
A RW MODE		Mode
Disabled	0	Disabled. Pin specified by PSEL will not be acquired by the
		GPIOTE module.
Event	1	Event mode
		The pin specified by PSEL will be configured as an input and the
		IN[n] event will be generated if operation specified in POLARITY
		occurs on the pin.
Task	3	Task mode
		The GPIO specified by PSEL will be configured as an output and
		triggering the SET[n], CLR[n] or OUT[n] task will perform the
		operation specified by POLARITY on the pin. When enabled as a
		task the GPIOTE module will acquire the pin and the pin can no
		longer be written as a regular output pin from the GPIO module.
B RW PSEL	[031]	GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
		and IN[n] event
C RW PORT	[01]	Port number
D RW POLARITY		When In task mode: Operation to be performed on output
		when OUT[n] task is triggered. When In event mode: Operation
		on input that shall trigger IN[n] event.
None	0	Task mode: No effect on pin from OUT[n] task. Event mode: no
		IN[n] event generated on pin activity.
LoToHi	1	Task mode: Set pin from OUT[n] task. Event mode: Generate
	_	IN[n] event when rising edge on pin.
HiToLo	2	Task mode: Clear pin from OUT[n] task. Event mode: Generate
	2	IN[n] event when falling edge on pin.
Toggle	3	Task mode: Toggle pin from OUT[n]. Event mode: Generate
E RW OUTINIT		IN[n] when any change on pin.
E RW OUTINIT		When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.
Low	0	Task mode: Initial value of pin before task triggering is low
	1	Task mode: Initial value of pin before task triggering is low Task mode: Initial value of pin before task triggering is high
High	1	rask mode. midal value of pin before task triggering is nigh

20.4.8 CONFIG[5]

Address offset: 0x524

	_																																		
Bit r	numbe	r		31	30 2	9 2	28 2	7 2	26 2	25 2	24	23 :	22 2	21 2	20 1	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															Ε			D	D			С	В	В	В	В	В							Α	Α
Rese	et 0x0	0000000		0	0 ()	0 (0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Val	ue							Des	crip	tio	n																				
Α	RW	MODE										Мо	de																						
			Disabled	0								Disa	ble	d. F	in:	spe	ecif	ied	by	PSE	Lν	vill	not	be	acc	quire	ed l	by 1	the						
												GPI	OTE	mo	odu	ıle.																			
			Event	1								Eve	nt m	nod	le																				
												The	pin	spe	ecif	fied	d by	/ PS	EL	will	be	co	nfig	gure	d a	s ar	ı inı	put	an	d tł	ne				
												IN[r	ı] ev	/en	t w	ill k	oe g	gen	era	ted	lif	оре	rat	ion	spe	cifie	ed i	n P	OL	ARI	TY				
												occ	urs (on t	the	pir	n.																		
			Task	3								Tasl	c mo	ode																					
												The	GPI	IO s	ne	cifi	ed	hv	PSF	l w	/ill l	he c	on	figu	red	las	an i	out	nut	t an	Н				
													gerii											-					•		_				
												-	ratio	-			-														s a				
												- 100			- 10 -			-,	. •					- p.											



Bitı	number			31 30 2	29 28	27 20	5 25	24 2	3 22	2 21	20	19 1	8 17	7 16	15	14 1	.3 12	2 11	10	9	3 7	6	5	4	3 2	2 1	. 0
Id											Ε		D	D			СВ	В	В	В	3					Α	A
Res	et 0x000	000000		0 0	0 0	0 0	0	0 0	0	0 0	0	0 (0 0	0	0	0	0 0	0	0	0	0 0	0	0	0	0 (0	0
Id	RW F	ield	Value Id	Value				D	esc	riptio	on																
								ta	ask 1	the G	PIO	TE n	nodı	ıle v	will a	acqu	ire t	he p	oin a	nd t	ne p	in c	an n	0			
								lo	onge	er be	wri	tten	as a	reg	gular	out	put	oin	from	the	GPI	O m	odu	le.			
В	RW P	SEL		[031]				G	PIO) num	nber	asso	ociat	ted	with	SET	[n],	CLR	[n] a	nd ()UT	n] t	asks				
								aı	nd I	IN[n]	eve	nt															
С	RW P	PORT		[01]				P	ort	numl	ber																
D	RW P	POLARITY						W	Vhe	n In t	ask	mod	de: C	per	ratio	n to	be p	erf	orm	ed o	n ou	tpu	t				
								w	her	n OU	T[n]	task	is t	rigg	erec	l. W	nen	n e	vent	mo	de: 0	Dpe	ratio	n			
								0	n in	nput t	hat	shal	l trig	gger	IN[n] ev	ent.										
			None	0				Ta	ask	mod	e: N	lo ef	fect	on	pin f	rom	OU.	Γ[n]	task	. Ev	ent r	noc	le: n	0			
								IN	V[n]] ever	nt ge	ener	ated	on	pin	acti	/ity.										
			LoToHi	1				Ta	ask	mod	e: S	et pi	n fro	om (OUT	[n] t	ask.	Eve	nt m	ode	: Ge	ner	ate				
								IN	V[n]] ever	nt w	hen	risir	ng e	dge	on p	in.										
			HiToLo	2				Ta	ask	mod	e: C	lear	pin 1	fron	n Ol	JT[n]	tas	k. E	vent	mo	de: 0	en	erate	9			
] ever				_	-												
			Toggle	3						mod		-				-	n]. E	ven	t mo	de:	Gen	era	te				
] whe			_		•												
Е	RW C	DUTINIT								n in t									•				SPIO	TE			
										inel is		·															
			Low	0						mod					•				-	_	-						
			High	1				Ta	ask	mod	e: Ir	nitial	valu	ue o	f pir	n bef	ore	task	trig	geri	ng is	hig	h				

20.4.9 CONFIG[6]

Address offset: 0x528

Bit n	umbe	er		31	. 30	29	28	27	26 2	25 2	24 23	3 22	2 21	20	19	18	17	16	15 1	4 1	3 1	2 1	1 10	9	8	7	6 !	5 4	3	2	1 0
Id														Ε			D	D		(C E	3 B	В	В	В						А А
Rese	t 0x0	0000000		0	0	0	0	0	0 (0	0 0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0 (0 0	0	0	0 0
Id	RW	Field	Value Id	Va	alue						D	esci	ripti	on																	
Α	RW	MODE									M	1ode	e																		
			Disabled	0							D	isab	oled.	Pir	ı spe	cifi	ied	by F	PSEL	wil	l nc	t be	e acc	quir	ed b	y th	ie				
											G	PIO	TE m	nod	lule.																
			Event	1							E۱	vent	t mo	de																	
											TI	he p	oin s	pec	ified	l by	/ PSI	EL v	vill b	e c	onf	igur	ed a	s ar	ı inp	ut a	and	the			
											IN	N[n]	eve	nt v	will b	e g	gene	erat	ed i	f op	era	tior	spe	cifi	ed ii	n PC	DLAI	RITY			
											0	ccur	rs on	th	e pir	١.															
			Task	3							Ta	ask	mod	le																	
											TI	he G	GPIO	sp	ecifi	ed I	by F	SEI	. wil	l be	co	nfig	ured	las	an c	outp	ut a	ınd			
											tr	rigge	ering	th	e SE	T[n], C	LR[ı	n] or	οι	JT[r	ı] ta	sk w	/ill p	erfo	orm	the				
											O	pera	ation	sp	ecif	ed	by I	POL	.ARI	TY c	n t	he p	in. ۱	Nhe	en e	nab	led	as a			
											ta	ask t	the G	GPI	OTE	mo	dul	e w	ill ac	qui	re t	he	pin a	nd	the	pin	can	no			
											lo	onge	er be	wr	rittei	n as	s a r	egu	ılar d	outp	out	pin	fron	n th	e G	PIO	mo	dule.			
В	RW	PSEL		[0	31]						G	PIO	nun	nbe	er as	soc	iate	d w	ith s	SET	[n],	CLF	(n)	and	ΟU	T[n]	tas	ks			
											aı	nd I	N[n]	ev	ent																
С	RW	PORT		[0	1]						Po	ort ı	num	ber	r																
D	RW	POLARITY									W	√her	n In t	tasl	k mo	de	: Op	era	tion	to	be	per	orm	ed	on c	utp	ut				
											w	hen	n OU	T[n	ı] tas	k is	s tri	gge	red.	Wh	ien	In e	ven	t m	ode	Ор	era	ion			
											OI	n in	put t	tha	t sha	ıll t	rigg	er I	N[n]	ev	ent										
			None	0									mod					•				•	tas	k. E	vent	mo	de:	no			
													eve		•																
			LoToHi	1									mod						-	-		Eve	ent r	nod	e: G	ene	rate	9			
											IN	N[n]	eve	nt v	whe	n ris	sing	ed	ge o	n p	in.										



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E DD CBBBB AA
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
		IN[n] event when falling edge on pin.
	Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate
		IN[n] when any change on pin.
E RW OUTINIT		When in task mode: Initial value of the output when the GPIOTE
		channel is configured. When in event mode: No effect.
	Low	0 Task mode: Initial value of pin before task triggering is low
	High	Task mode: Initial value of pin before task triggering is high

20.4.10 CONFIG[7]

Address offset: 0x52C

		•		•	•																						
Bitı	numbe	er		31	30 2	9 28	27 26	25 2	4 23	22 21	20	19 1	8 17	7 16	15 3	L4 1	3 12	11	10	9 8	3 7	7 6	5	4	3	2	1 0
Id											Ε		D	D		(В	В	В	ВЕ	3						A A
Res	et 0x0	0000000		0	0 (0 0	0 0	0 0	0 0	0 0	0	0 (0	0	0	0 0	0	0	0	0 () (0	0	0	0	0	0 0
ld	RW	Field	Value Id	Va	lue				Des	scriptio	on																
Α	RW	MODE							Мо	ode																	
			Disabled	0						abled. IOTE m			ifie	d by	PSEI	_wil	l not	be	acq	uire	d by	the					
			Event	1						ent mo																	
									IN[e pin sp n] ever curs on	nt w	vill be	e ge				_				•						
			Task	3					Tas	sk mod	e																
										e GPIO	•							-						nd			
									оре	eration	spe	ecifie	d b	/ PC	LARI	TY c	n th	e pi	n. W	/hen	en	able	d a	s a			
									tas	k the G	SPIC	TE n	nod	ıle v	vill a	cqui	ire th	ie p	in a	nd th	ne p	in c	an r	10			
									lon	ger be	wri	tten	as a	reg	ular	out	out p	in f	rom	the	GP	IO m	nod	ule.			
В	RW	PSEL		[0.	.31]				GPI	IO nun	nbei	asso	ocia	ted	with	SET	[n], (CLR[n] a	nd C	UT	[n] t	ask	S			
									and	d IN[n]	eve	nt															
С	RW	PORT		[0.	.1]				Por	rt num	ber																
D	RW	POLARITY							Wh	nen In t	task	mod	le: C	per	atio	ı to	be p	erfo	orme	ed o	n oı	ıtpu	t				
									wh	en OU	T[n]	task	is t	rigg	ered	. Wh	nen li	n ev	ent	mod	de:	Оре	rati	on			
									on	input t	that	shal	l trig	gger	IN[n] ev	ent.										
			None	0					Tas	sk mod	e: N	lo ef	fect	on	oin fi	om	OUT	[n]	task	. Eve	ent	mod	le: r	10			
									IN[n] eve	nt g	ener	ated	lon	pin a	activ	ity.										
			LoToHi	1					Tas	sk mod	e: S	et pi	n fro	om (]TUC	n] ta	ask. E	ver	nt m	ode	: Ge	ner	ate				
									IN[n] eve	nt w	hen	risir	ng e	dge d	n p	in.										
			HiToLo	2					Tas	sk mod	e: C	lear	pin	fron	า	T[n]	task	. Ev	ent	mod	le: 0	Gen	erat	:e			
									IN[n] eve	nt w	hen	falli	ng e	dge	on p	oin.										
			Toggle	3					Tas	sk mod	e: T	oggl	e piı	n fro	m O	ı]TU	n]. Ev	/ent	t mo	de:	Ger	era	te				
									IN[n] whe	en a	ny ch	nang	e oı	n pin												
Ε	RW	OUTINIT							Wh	nen in t	task	mod	le: I	nitia	l val	ue o	f the	ou	tput	whe	en t	he C	SPIC	OTE			
									cha	annel is	s co	nfigu	red	. Wł	nen i	ı ev	ent r	nod	le: N	lo ef	fect	t.					
			Low	0					Tas	sk mod	e: Ir	nitial	valı	ıe o	f pin	bef	ore t	ask	trig	gerir	ng is	lov	,				
			High	1					Tas	sk mod	e: Ir	nitial	valı	ue o	f pin	bef	ore t	ask	trig	gerir	ng is	hig	h				
																			_			_					



20.5 Electrical specification

20.5.1 GPIOTE Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{GPIOTE,IN}	Run current with 1 or more GPIOTE active channels in Input				μΑ
	mode, System On Idle				
I _{GPIOTE,OUT}	Run current with 1 or more GPIOTE active channels in Output				μΑ
	mode, System On Idle				
I _{GPIOTE,IDLE}	Run current when all channels in Idle mode.				μΑ



21 PPI — Programmable peripheral interconnect

The Programmable peripheral interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. The PPI allows precise synchronization between peripherals when real-time application constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

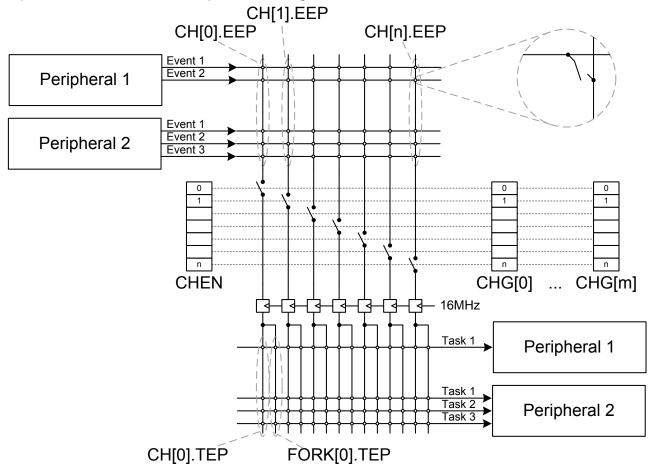


Figure 29: PPI block diagram

The PPI system has, in addition to the fully programmable peripheral interconnections, a set of channels where the event end point (EEP) and task end points (TEP) are fixed in hardware. These fixed channels can be individually enabled, disabled, or added to PPI channel groups in the same way as ordinary PPI channels.

Table 27: Configurable and fixed PPI channels

Instance	Channel	Number of channels	Number of groups
PPI	0-19	20	6
PPI (fixed)	20-31	12	

The PPI provides a mechanism to automatically trigger a task in one peripheral as a result of an event occurring in another peripheral. A task is connected to an event through a PPI channel. The PPI channel is composed of three end point registers, one EEP and two TEPs. A peripheral task is connected to a TEP using the address of the task register associated with the task. Similarly, a peripheral event is connected to an EEP using the address of the event register associated with the event.

On each PPI channel, the signals are synchronized to the 16 MHz clock, to avoid any internal violation of setup and hold timings. As a consequence, events that are synchronous to the 16 MHz clock will be delayed by one clock period, while other asynchronous events will be delayed by up to one 16 MHz clock period.



Note that shortcuts (as defined in the SHORTS register in each peripheral) are not affected by this 16 MHz synchronization, and are therefore not delayed.

Each TEP implements a fork mechanism that enables a second task to be triggered at the same time as the task specified in the TEP is triggered. This second task is configured in the task end point register in the FORK registers groups, e.g. FORK.TEP[0] is associated with PPI channel CH[0].

There are two ways of enabling and disabling PPI channels:

- Enable or disable PPI channels individually using the CHEN, CHENSET, and CHENCLR registers.
- Enable or disable PPI channels in PPI channel groups through the groups' ENABLE and DISABLE tasks. Prior to these tasks being triggered, the PPI channel group must be configured to define which PPI channels belongs to which groups.

Note that when a channel belongs to two groups m and n, and CHG[m].EN and CHG[n].DIS occur simultaneously (m and n can be equal or different), EN on that channel has priority.

PPI tasks (for example, CHG[0].EN) can be triggered through the PPI like any other task, which means they can be hooked up to a PPI channel as a TEP. One event can trigger multiple tasks by using multiple channels and one task can be triggered by multiple events in the same way.

21.1 Pre-programmed channels

Some of the PPI channels are pre-programmed. These channels cannot be configured by the CPU, but can be added to groups and enabled and disabled like the general purpose PPI channels. The FORK TEP for these channels are still programmable and can be used by the application.

For a list of pre-programmed PPI channels, see the table below.

Table 28: Pre-programmed channels

Channel	EEP	TEP
20	TIMERO->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
21	TIMERO->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
22	TIMERO->EVENTS_COMPARE[1]	RADIO->TASKS_DISABLE
23	RADIO->EVENTS_BCMATCH	AAR->TASKS_START
24	RADIO->EVENTS_READY	CCM->TASKS_KSGEN
25	RADIO->EVENTS_ADDRESS	CCM->TASKS_CRYPT
26	RADIO->EVENTS_ADDRESS	TIMERO->TASKS_CAPTURE[1]
27	RADIO->EVENTS_END	TIMERO->TASKS_CAPTURE[2]
28	RTCO->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
29	RTC0->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
30	RTCO->EVENTS_COMPARE[0]	TIMERO->TASKS_CLEAR
31	RTCO->EVENTS_COMPARE[0]	TIMERO->TASKS_START

21.2 Registers

Table 29: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001F000	PPI	PPI	Programmable peripheral interconnect	

Table 30: Register Overview

Register	Offset	Description
TASKS_CHG[0].EN	0x000	Enable channel group 0
TASKS_CHG[0].DIS	0x004	Disable channel group 0
TASKS_CHG[1].EN	0x008	Enable channel group 1
TASKS_CHG[1].DIS	0x00C	Disable channel group 1
TASKS_CHG[2].EN	0x010	Enable channel group 2
TASKS_CHG[2].DIS	0x014	Disable channel group 2
TASKS_CHG[3].EN	0x018	Enable channel group 3
TASKS_CHG[3].DIS	0x01C	Disable channel group 3
TASKS_CHG[4].EN	0x020	Enable channel group 4



Register	Offset	Description
TASKS_CHG[4].DIS	0x024	Disable channel group 4
TASKS_CHG[5].EN	0x028	Enable channel group 5
TASKS_CHG[5].DIS	0x02C	Disable channel group 5
CHEN	0x500	Channel enable register
CHENSET	0x504	Channel enable set register
CHENCLR	0x508	Channel enable clear register
CH[0].EEP	0x510	Channel 0 event end-point
CH[0].TEP	0x514	Channel 0 task end-point
CH[1].EEP	0x518	Channel 1 event end-point
CH[1].TEP	0x51C	Channel 1 task end-point
CH[2].EEP	0x520	Channel 2 event end-point
CH[2].TEP	0x524	Channel 2 task end-point
CH[3].EEP	0x528	Channel 3 event end-point
CH[3].TEP	0x52C	Channel 3 task end-point
CH[4].EEP	0x530	Channel 4 event end-point
CH[4].TEP	0x534	Channel 4 task end-point
CH[5].EEP	0x538	Channel 5 event end-point
CH[5].TEP	0x53C	Channel 5 task end-point
CH[6].EEP	0x540	Channel 6 event end-point
CH[6].TEP	0x544	Channel 6 task end-point
CH[7].EEP	0x548	Channel 7 event end-point
CH[7].TEP	0x54C	Channel 7 task end-point
CH[8].EEP	0x550	Channel 8 event end-point
CH[8].TEP	0x554	Channel 8 task end-point
CH[9].EEP	0x558	Channel 9 event end-point
CH[9].TEP	0x55C	Channel 9 task end-point
CH[10].EEP	0x560	Channel 10 event end-point
CH[10].TEP	0x564	Channel 10 task end-point Channel 10 task end-point
CH[11].EEP	0x568	Channel 11 event end-point
CH[11].TEP	0x56C	Channel 11 task end-point Channel 11 task end-point
CH[12].EEP	0x50C 0x570	Channel 12 event end-point
CH[12].TEP	0x574	Channel 12 task end-point Channel 12 task end-point
CH[13].EEP	0x574	Channel 13 event end-point
CH[13].TEP	0x576	Channel 13 task end-point Channel 13 task end-point
CH[14].EEP	0x580	Channel 14 event end-point
CH[14].TEP	0x580	Channel 14 task end-point
CH[15].EEP	0x584 0x588	Channel 15 event end-point
CH[15].TEP	0x58C	Channel 15 task end-point Channel 15 task end-point
CH[16].EEP	0x590	Channel 16 event end-point
CH[16].TEP	0x590 0x594	Channel 16 task end-point Channel 16 task end-point
CH[17].EEP	0x594 0x598	Channel 17 event end-point
CH[17].EEP	0x598 0x59C	Channel 17 task end-point Channel 17 task end-point
CH[18].EEP	0x59C 0x5A0	Channel 18 event end-point
CH[18].TEP	0x5A0	Channel 18 task end-point
CH[19].EEP	0x5A4 0x5A8	Channel 19 event end-point
CH[19].TEP	0x5A6	Channel 19 task end-point Channel 19 task end-point
CHG[0]	0x800	Channel group 1
CHG[1]	0x804	Channel group 2
CHG[2]	0x808	Channel group 2
CHG[3]	0x80C	Channel group 4
CHG[4]	0x810	Channel group 5
CHG[5]	0x814	Channel group 5
FORK[0].TEP	0x910	Channel 0 task end-point
FORK[1].TEP	0x914	Channel 1 task end-point
FORK[2].TEP	0x918	Channel 2 task end-point
FORK[3].TEP	0x91C	Channel 3 task end-point
FORK[4].TEP	0x920	Channel 4 task end-point
FORK[5].TEP	0x924	Channel 5 task end-point



Register	Offset	Description	
FORK[6].TEP	0x928	Channel 6 task end-point	
FORK[7].TEP	0x92C	Channel 7 task end-point	
FORK[8].TEP	0x930	Channel 8 task end-point	
FORK[9].TEP	0x934	Channel 9 task end-point	
FORK[10].TEP	0x938	Channel 10 task end-point	
FORK[11].TEP	0x93C	Channel 11 task end-point	
FORK[12].TEP	0x940	Channel 12 task end-point	
FORK[13].TEP	0x944	Channel 13 task end-point	
FORK[14].TEP	0x948	Channel 14 task end-point	
FORK[15].TEP	0x94C	Channel 15 task end-point	
FORK[16].TEP	0x950	Channel 16 task end-point	
FORK[17].TEP	0x954	Channel 17 task end-point	
FORK[18].TEP	0x958	Channel 18 task end-point	
FORK[19].TEP	0x95C	Channel 19 task end-point	
FORK[20].TEP	0x960	Channel 20 task end-point	
FORK[21].TEP	0x964	Channel 21 task end-point	
FORK[22].TEP	0x968	Channel 22 task end-point	
FORK[23].TEP	0x96C	Channel 23 task end-point	
FORK[24].TEP	0x970	Channel 24 task end-point	
FORK[25].TEP	0x974	Channel 25 task end-point	
FORK[26].TEP	0x978	Channel 26 task end-point	
FORK[27].TEP	0x97C	Channel 27 task end-point	
FORK[28].TEP	0x980	Channel 28 task end-point	
FORK[29].TEP	0x984	Channel 29 task end-point	
FORK[30].TEP	0x988	Channel 30 task end-point	
FORK[31].TEP	0x98C	Channel 31 task end-point	

21.2.1 CHEN

Address offset: 0x500 Channel enable register

	numb	er					28 2																			7	-	_	4 3	2	1	Э
Id				f	е	d	c I	b a	a Z	<u> </u>	X	W	V	U	Т	S	R	Q	Р	0	Ν 1	ΛI	_ K	J	1	Н	G	F	E D	С	В	A
Res	et 0x(0000000		0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0 0	0	0	0
Id	RW	Field	Value Id	V	alue						De	escri	ipti	on																		
Α	RW	CH0									En	nable	e or	r di	sab	le c	har	inel	0													
			Disabled	0							Di	isabl	e c	har	nnel																	
			Enabled	1							Er	nable	e ch	nan	nel																	
В	RW	CH1									En	nable	e or	r di	sab	le c	har	nel	1													
			Disabled	0							Di	isabl	e c	har	nnel																	
			Enabled	1							En	nable	e ch	nan	nel																	
С	RW	CH2									En	nable	e or	r di	sab	le c	har	inel	2													
			Disabled	0							Di	isabl	e c	har	nnel																	
			Enabled	1							En	nable	e ch	nan	nel																	
D	RW	CH3									En	nable	e or	r di	sab	le c	har	nel	3													
			Disabled	0							Di	isabl	e c	har	nnel																	
			Enabled	1							En	nable	e ch	nan	nel																	
Е	RW	CH4									Er	nable	e or	r di	sab	le c	har	nel	4													
			Disabled	0							Di	isabl	e c	har	nnel																	
			Enabled	1							En	nable	e ch	nan	nel																	
F	RW	CH5									En	nable	e or	r di	sab	le c	har	inel	5													
			Disabled	0							Di	isabl	e c	har	nnel																	
			Enabled	1							En	nable	e ch	nan	nel																	
G	RW	CH6									En	nable	e or	r di	sab	le c	har	nel	6													
			Disabled	0							Di	isabl	e c	har	nnel																	
			Enabled	1							En	nable	e ch	nan	nel																	
Н	RW	CH7									Er	nable	e or	r di	sab	le c	har	nel	7													



Bit r	iumbe	er		31 30	29 28	27 2	6 25	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id				f e	d c	b a	a Z	Y X W V U T S R Q P O N M L K J I H G F E D C B
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value				Description
			Disabled	0				Disable channel
			Enabled	1				Enable channel
I	RW	CH8						Enable or disable channel 8
			Disabled	0				Disable channel
			Enabled	1				Enable channel
J	RW	CH9						Enable or disable channel 9
			Disabled	0				Disable channel
			Enabled	1				Enable channel
K	RW	CH10						Enable or disable channel 10
			Disabled	0				Disable channel
			Enabled	1				Enable channel
L	RW	CH11						Enable or disable channel 11
			Disabled	0				Disable channel
			Enabled	1				Enable channel
М	RW	CH12						Enable or disable channel 12
			Disabled	0				Disable channel
			Enabled	1				Enable channel
N	RW	CH13						Enable or disable channel 13
			Disabled	0				Disable channel
			Enabled	1				Enable channel
0	RW	CH14						Enable or disable channel 14
			Disabled	0				Disable channel
			Enabled	1				Enable channel
Р	RW	CH15						Enable or disable channel 15
			Disabled	0				Disable channel
			Enabled	1				Enable channel
Q	RW	CH16						Enable or disable channel 16
			Disabled	0				Disable channel
			Enabled	1				Enable channel
R	RW	CH17						Enable or disable channel 17
			Disabled	0				Disable channel
			Enabled	1				Enable channel
S	RW	CH18		_				Enable or disable channel 18
			Disabled	0				Disable channel
_	5111	01140	Enabled	1				Enable channel
Т	RW	CH19	5					Enable or disable channel 19
			Disabled	0				Disable channel
	D)A/	CH20	Enabled	1				Enable channel
U	KVV	CH20	Disabled	0				Enable or disable channel 20
			Disabled	0				Disable channel
.,	D)A/	CH24	Enabled	1				Enable channel
V	KW	CH21	Disabled	0				Enable or disable channel 21
			Disabled	0				Disable channel
	DIA	cuaa	Enabled	1				Enable channel
W	KW	CH22	Disabled	0				Enable or disable channel 22
			Disabled	0				Disable channel
v	DIA	CH33	Enabled	1				Enable channel
Х	KW	CH23	Disabled	0				Enable or disable channel 23
			Disabled	0				Disable channel
.,	B	CUDA	Enabled	1				Enable channel
Υ	кW	CH24	D: 11 1	•				Enable or disable channel 24
			Disabled	0				Disable channel
			Enabled	1				Enable channel
_			Z. Tablea	_				5 II II II I I I I I I I I I I I I I I
Z	RW	CH25	Disabled	0				Enable or disable channel 25 Disable channel



Bitı	numbe	er		31 30	29 2	8 27 :	26 2	5 24	1 23	22 2	21 2	20 19	9 1	8 17	16	15	14 1	3 12	2 11	10	9	8	7	6 5	5 4	3	2	1 0
Id				f e	d c	b	a Z	2 Y	Χ	W '	V	U T	- 5	R	Q	Р	0 1	N N	1 L	K	J	1 1	4 (G F	E	D	С	ВА
Res	et 0x0	0000000		0 0	0 0	0	0 0	0	0	0 (0	0 0) (0	0	0	0 (0 0	0	0	0	0 ()	0 0	0	0	0	0 0
Id	RW	Field	Value Id	Value					De	escrip	tio	n																
			Enabled	1					En	able	cha	nne	I															
а	RW	CH26							En	able	or (disak	ole	char	nnel	26												
			Disabled	0					Dis	sable	ch	anne	el															
			Enabled	1					En	able	cha	nne	I															
b	RW	CH27							En	able	or (disak	ole	char	nnel	27												
			Disabled	0					Dis	sable	ch	anne	el															
			Enabled	1					En	able	cha	nne	I															
С	RW	CH28							En	able	or (disak	ole	char	nnel	28												
			Disabled	0					Dis	sable	ch	anne	el															
			Enabled	1					En	able	cha	nne	I															
d	RW	CH29							En	able	or (disak	ole	char	nnel	29												
			Disabled	0					Dis	sable	ch	anne	el															
			Enabled	1					En	able	cha	nne	I															
е	RW	CH30							En	able	or (disak	ole	char	nnel	30												
			Disabled	0					Dis	sable	ch	anne	el															
			Enabled	1					En	able	cha	nne	I															
f	RW	CH31							En	able	or (disab	ole	char	nnel	31												
			Disabled	0					Dis	sable	ch	anne	el															
			Enabled	1					En	able	cha	nne	I															

21.2.2 CHENSET

Address offset: 0x504

Channel enable set register

Read: reads value of CH{i} field in CHEN register.

Rit	numbe	er er		31 :	30.2	9 28	27.2	6.2	5 24	1 2:	3 22	21 2	0 19	18	3 17	16	15	14 1	3 12	11	1 10	9	8	7	6 5	4	3	2	1 0
Id	iidiiib.	-1				d c																					_		
	et OxO	0000000			0 (0 0																
Id		Field	Value Id	Valu							escri													_			Ť		
A	RW	CH0										•	enab	le s	set r	egis	ter	Wri	ting	'0'	has	no e	effe	ct					
			Disabled	0									nnel			_			. 0										
			Enabled	1						Re	ead:	char	nnel e	ena	bled	ł													
			Set	1						W	/rite:	Ena	ble c	har	nnel														
В	RW	CH1								Cl	hann	el 1	enab	le s	set r	egis	ster.	Wri	ting	'0'	has	no e	effe	ct					
			Disabled	0						Re	ead:	char	nnel	disa	ble	ď			Ĭ										
			Enabled	1						Re	ead:	char	nnel e	ena	bled	ł													
			Set	1						W	/rite:	Ena	ble c	har	nnel														
С	RW	CH2								Cl	hann	el 2	enab	le s	set r	egis	ster	Wri	ting	'0'	has	no e	effe	ct					
			Disabled	0						Re	ead:	char	nnel	disa	ble	t													
			Enabled	1						Re	ead:	char	nnel e	ena	bled	ł													
			Set	1						W	/rite:	Ena	ble c	har	nnel														
D	RW	CH3								Cl	hann	el 3	enab	le s	set r	egis	ster.	Wri	ting	'0'	has	no e	effe	ct					
			Disabled	0						Re	ead:	char	nel	disa	ble	t													
			Enabled	1						Re	ead:	char	nnel e	ena	bled	i													
			Set	1						W	/rite:	Ena	ble c	har	nnel														
Ε	RW	CH4								Cl	hann	el 4	enab	le s	set r	egis	ster	Wri	ting	'0'	has	no e	effe	ct					
			Disabled	0						Re	ead:	char	nnel	disa	ble	t													
			Enabled	1						Re	ead:	char	nnel e	ena	bled	ł													
			Set	1						W	/rite:	Ena	ble c	har	nnel														
F	RW	CH5								Cl	hann	el 5	enab	le s	set r	egis	ster.	Wri	ting	'0'	has	no e	effe	ct					
			Disabled	0						Re	ead:	char	nnel	disa	ble	t													
			Enabled	1						Re	ead:	char	nnel e	ena	bled	ł													
			Set	1						W	/rite:	Ena	ble c	har	nnel														



Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCB
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
G	RW CH6		Channel 6 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Н	RW CH7		Channel 7 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
	DW CHO	Set	1 Write: Enable channel
I	RW CH8	Disabled	Channel 8 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
	RW CH9	Set	1 Write: Enable channel
J	KW CH9	Disabled	Channel 9 enable set register. Writing '0' has no effect O Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
K	RW CH10	361	Channel 10 enable set register. Writing '0' has no effect
K	KW CHIO	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
L	RW CH11	361	Channel 11 enable set register. Writing '0' has no effect
•	KW CHII	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
М	RW CH12		Channel 12 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
N	RW CH13		Channel 13 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
0	RW CH14		Channel 14 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Р	RW CH15		Channel 15 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Q	RW CH16		Channel 16 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
R	RW CH17		Channel 17 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
S	RW CH18		Channel 18 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Т	RW CH19		Channel 19 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled



Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCE	ВА
Rese	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
Id	RW Field	Value Id	Value Description	
		Set	1 Write: Enable channel	
U	RW CH20		Channel 20 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
٧	RW CH21		Channel 21 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
W	RW CH22		Channel 22 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
Χ	RW CH23		Channel 23 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
Υ	RW CH24		Channel 24 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
Z	RW CH25		Channel 25 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
а	RW CH26		Channel 26 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
b	RW CH27		Channel 27 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
C	RW CH28		Channel 28 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
d	RW CH29		Channel 29 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
е	RW CH30		Channel 30 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
f	RW CH31		Channel 31 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	

21.2.3 CHENCLR

Address offset: 0x508

Channel enable clear register



Read: reads value of CH(i) field in CHEN register.

		.,	
Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Res	set 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
Α	RW CH0		Channel 0 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
В	RW CH1		Channel 1 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
С	RW CH2		Channel 2 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
D	RW CH3	Cicui	Channel 3 enable clear register. Writing '0' has no effect
	KW CHS	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
_	Dist. Cit.	Clear	1 Write: disable channel
E	RW CH4	Dissipled	Channel 4 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
_		Clear	1 Write: disable channel
F	RW CH5		Channel 5 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
G	RW CH6		Channel 6 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
Н	RW CH7		Channel 7 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
I	RW CH8		Channel 8 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
J	RW CH9		Channel 9 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
K	RW CH10		Channel 10 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
L	RW CH11		Channel 11 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
М	RW CH12		Channel 12 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
N	RW CH13	Cicai	Channel 13 enable clear register. Writing '0' has no effect
N	IVAN CI172		Chamier 15 enable clear register. Wilting O has no enect



Bit r	number			31 30	29 28	27 26	5 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0000	00000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Fie	eld	Value Id	Value				Description
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
0	RW CH	114						Channel 14 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
Р	RW CH	H15						Channel 15 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
Q	RW CH	116						Channel 16 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
R	RW CH	117						Channel 17 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
S	RW CH	118						Channel 18 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
Т	RW CH	119						Channel 19 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
U	RW CH	120	5					Channel 20 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
.,	D)4/ C)	124	Clear	1				Write: disable channel
V	RW CH	121	D: 11 1	•				Channel 21 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
14/	DIA/ CI	122	Clear	1				Write: disable channel
W	RW CH	122	Disabled	0				Channel 22 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled Read: channel enabled
			Enabled	1				Write: disable channel
v	RW CH	122	Clear	1				Channel 23 enable clear register. Writing '0' has no effect
Х	KW CH	123	Disabled	0				Read: channel disabled
								Read: channel enabled
			Enabled	1				
V	DIA/ CII	124	Clear	1				Write: disable channel
Υ	RW CH	124	Disabled	0				Channel 24 enable clear register. Writing '0' has no effect
			Disabled					Read: channel disabled
			Enabled	1				Read: channel enabled
7	RW CH	125	Clear	1				Write: disable channel Channel 25 enable clear register. Writing '0' has no effect
Z	NVV CH	12.3	Disabled	0				Channel 25 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
	DIA C	126	Clear	1				Write: disable channel Channel 26 anable clear register. Writing 101 has no offert
а	RW CH	120	Disabled	0				Channel 26 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel



Bit r	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZY	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
b	RW CH27			Channel 27 enable clear register. Writing '0' has no effect
		Disabled	0	Read: channel disabled
		Enabled	1	Read: channel enabled
		Clear	1	Write: disable channel
С	RW CH28			Channel 28 enable clear register. Writing '0' has no effect
		Disabled	0	Read: channel disabled
		Enabled	1	Read: channel enabled
		Clear	1	Write: disable channel
d	RW CH29			Channel 29 enable clear register. Writing '0' has no effect
		Disabled	0	Read: channel disabled
		Enabled	1	Read: channel enabled
		Clear	1	Write: disable channel
e	RW CH30			Channel 30 enable clear register. Writing '0' has no effect
		Disabled	0	Read: channel disabled
		Enabled	1	Read: channel enabled
		Clear	1	Write: disable channel
f	RW CH31			Channel 31 enable clear register. Writing '0' has no effect
		Disabled	0	Read: channel disabled
		Enabled	1	Read: channel enabled
		Clear	1	Write: disable channel
f	RW CH31	Enabled	1	Read: channel disabled Read: channel enabled

21.2.4 CH[0].EEP

Address offset: 0x510

Channel 0 event end-point

Bit nu	ımbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A	Δ	Α	Α
Reset	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α	RW	EEP										Poi	nte	r to	ev	ent	reg	giste	er. /	Acc	ept	s or	ıly a	add	ress	ses	to i	regi	ste	rs					Т

from the Event group.

21.2.5 CH[0].TEP

Address offset: 0x514 Channel 0 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 :	19 1	8 1	7 1	6 1	5 14	4 13	3 12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	Δ Α	Α Α	. Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	ΑА	A	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	TEP										Poi	nter	to	tas	k re	gist	er.	Acc	ept	s or	ıly a	ddr	esse	es t	o re	gis	ters					

from the Task group.

21.2.6 CH[1].EEP

Address offset: 0x518
Channel 1 event end-point



Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 1	16 1	15 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	EEP										Poi	nte	r to	ev	ent	reg	iste	r. A	cce	pts	only	ado	dres	ses	to	reg	iste	rs				
												fro	m tl	he l	Eve	nt g	rou	p.															

21.2.7 CH[1].TEP

Address offset: 0x51C Channel 1 task end-point

Bit r	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21 :	20 :	19 1	18 1	7 1	16 1	5 1	4 1	3 12	11	10	9	8	7	6	5	4	3	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α /	Δ ,	A A	Α Α	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α /	A A	АА
Res	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 () (0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							Des	scri	ptio	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	egist	er.	Acc	ept	10 2	nly a	ddr	ess	es t	o re	egis	ters	5				
												froi	m tl	he T	ask	gro	oup.																

21.2.8 CH[2].EEP

Address offset: 0x520

Channel 2 event end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	L4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Δ Α	Δ Δ	ι A	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	EEP										Poi	nte	r to	ev	ent	reg	iste	er. A	Acce	pts	onl	y ac	ldre	sse	s to	reg	iste	rs				
												fro	m tl	he I	Eve	nt g	rou	p.															

21.2.9 CH[2].TEP

Address offset: 0x524 Channel 2 task end-point

Bit r	iumbe	er		3	1 3	0 2	9 2	28 :	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2	1 0
Id				Α	. 4		4	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α,	А А
Res	et OxC	0000000		0	O) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	٧	alu	е							De	scr	ipti	on																			
Α	RW	TEP											Ро	inte	er to	o ta	sk r	egi	ster	. A	cce	ots	only	y ac	dre	sse	s to	o re	gis	ters	;				
													fro	m	the	Tas	k g	rou	p.																

21.2.10 CH[3].EEP

Address offset: 0x528

Channel 3 event end-point

Bit number	31 30 29	28 27 26 25 24 23	22 21 20 19 18 17 1	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id	A A A	A A A A A A	A A A A A A	A A A A A A A	
Reset 0x00000000	0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field Value	e Id Value	De	scription		
A RW EEP		Poi	inter to event registe	r. Accepts only addresse	es to registers

from the Event group.

21.2.11 CH[3].TEP

Address offset: 0x52C Channel 3 task end-point



Bit r	numl	ber			31	. 30	29	28	27	7 26	25	24	23	22	21	20 :	19	18 1	17 1	16 1	15 :	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (,
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	A A	
Res	et Ox	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 (,
Id	RV	V	Field	Value Id	Va	lue							De	scri	ptic	n																				l
Α	RV	٧ .	TEP										Poi	nte	r to	tas	k re	gist	ter.	Ac	сер	ts (only	/ ac	ldre	esse	es to	o re	gis	ters	5					
													fro	m tl	he 1	Task	gr	guc																		

21.2.12 CH[4].EEP

Address offset: 0x530

Channel 4 event end-point

Bitı	numb	er		31	. 30	29	28	8 2	7 2	26 2	25 :	24	23	22 :	21 :	20	19	18 :	17 :	16	15 :	14	13	12 :	11	10	9	8	7	6	5	4	3	2	1 (í
Id				Α	Α	Α	Α		Δ ,	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Ĺ
Res	et Ox(0000000		0	0	0	0	(0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (
Id	RW	Field	Value Id	Va	alue	•							Des	cri	otio	n																				ı
Α	RW	EEP											Poi	ntei	r to	eve	ent	reg	iste	r. A	\cce	pts	on	ıly a	dd	res	ses	to	reg	iste	rs					
													froi	n th	ne E	vei	nt g	rou	p.																	

21.2.13 CH[4].TEP

Address offset: 0x534 Channel 4 task end-point

Bit r	numbe	er		31	. 30	29	28	3 2	7 26	25	24	23	3 22	21	20	19	18	17	16	15	14	13 :	12 :	11 :	10	9	8	7	6	5	4	3	2	1)
Id				Α	Α	Α	Α	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A.	Α .	Α
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	Va	lue	:						De	escr	ipti	on																				ı
Α	RW	TEP										Pc	ointe	er to	o ta	sk r	egis	ster	. Ac	cep	ots o	nly	ad	dre	sse	s t	o re	gis	ters	5					
												fro	om 1	the	Tas	k gr	oup	ο.																	

21.2.14 CH[5].EEP

Address offset: 0x538

Channel 5 event end-point

Bit r	numb	er		31	. 30	29	28	27	26	25	24	23 :	22 2	1 20	19	18	17	16 1	L5 1	4 1	3 12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	Α	Α	Α	A	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α /	4 Δ	А
Res	et Ox(0000000		0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	ion																		
													ср																			
Α	RW	EEP											nter			reg	iste	er. A	cce	pts	only	add	res	ses	to ı	regi	iste	ers				

21.2.15 CH[5].TEP

Address offset: 0x53C Channel 5 task end-point

Bit r	numbe	er		31	30	29	28	27 :	26 :	25 :	24	23 2	22 2	1 2	0 19	18	3 17	16	15	14	13	12	11 :	LO	9	8	7	6	5	4	3 2	1	0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	А А	Α	Α	Α	Α	Α	Α	Α	Α	A.	Α	Α	Α	Α	Α	Α	A A	. 4	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tior	1																		
Α	RW	TEP										Poir	nter	to t	task	reg	iste	r. A	cce	pts	only	y ac	ldre	sse	s to	re	gist	ers					

from the Task group.

21.2.16 CH[6].EEP

Address offset: 0x540

Channel 6 event end-point



Bit r	umb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15	14 1	.3 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	A	Α /	А А	Α	Α	Α	Α	Α.	Д Д	A	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Res	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	crip	tio	n																	
Α	RW	EEP										Poi	nter	to	even	t re	gist	er. /	Acce	epts	only	y ad	dres	sses	to	reg	iste	rs				
												fro	m th	ie E	vent	gro	up.															

21.2.17 CH[6].TEP

Address offset: 0x544 Channel 6 task end-point

Bit r	umber		31	30	29	28	3 2	7 2	6 2	25 2	24 2	23 :	22 :	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id			Α	Α	Α	Α	Δ	\ <i>A</i>	4	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	A A
Res	et 0x00000000		0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW Field	Value Id	Va	lue							ı	Des	crip	otic	n																			
Α	RW TEP										ı	io	ntei	· to	tas	k re	egis	ster	r. A	cce	pts	onl	y a	ddr	ess	es t	o re	egis	ters	5				
											f	ror	n th	ne 1	asl	gr	OIII	n																

21.2.18 CH[7].EEP

Address offset: 0x548

Channel 7 event end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	L4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Δ Α	Δ Δ	ι A	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	EEP										Poi	nte	r to	ev	ent	reg	iste	er. A	Acce	pts	onl	y ac	ldre	sse	s to	reg	iste	rs				
												fro	m tl	he I	Eve	nt g	rou	p.															

21.2.19 CH[7].TEP

Address offset: 0x54C Channel 7 task end-point

Bit nu	ımbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 :	L8 1	7 1	6 1	.5 1	4 1	.3 1	.2 :	11 1	LO	9	8	7	6	5	4	3 2	2 1	0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	Δ ,	4 /	Δ ,	۱ ۸	Δ.	Д	Д	Α	Α	Α	Α	Α	Α	Α	A A	A A	A A
Rese	t 0x0	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 () (0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	TEP										Poi	inte	r to	tas	k re	gist	er.	Acc	ept	s o	nly	ad	dre	sse	s to	o re	gist	ters					
												fro	m t	he 1	Task	gr	nun																	

21.2.20 CH[8].EEP

Address offset: 0x550

Channel 8 event end-point

Bit number	31 30 29	28 27 26 25 24 23	22 21 20 19 18 17 1	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id	A A A	A A A A A A	A A A A A A	A A A A A A A	
Reset 0x00000000	0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field Value	e Id Value	De	scription		
A RW EEP		Poi	inter to event registe	r. Accepts only addresse	es to registers

from the Event group.

21.2.21 CH[8].TEP

Address offset: 0x554 Channel 8 task end-point



Bit r	nur	nbe	r		31	30	29	28	27	26	25	24	23	22	21	20 :	19 1	18 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α /	Δ Α	Α Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	A A
Res	et (0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	R	w	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	R	W	TEP										Ро	inte	r to	tas	k re	gist	er.	Acc	ept	on	ly a	ddr	ess	es t	o re	gis	ters					
													fro	m tl	he 1	Гask	gro	oup.																

21.2.22 CH[9].EEP

Address offset: 0x558

Channel 9 event end-point

Bit r	nun	nbe	r		31	30	29	28	3 27	7 26	25	24	23	22	21 :	20 1	.9 1	8 17	7 16	5 15	14	13	12	11 1	.0	9	8 7	7 6	5	4	3	2	1	0
Id					Α	Α	Α	Α	А	A	Α	Α	Α	Α	Α	Α.	Δ ,	Α Α	. A	Α	Α	Α	Α	Α.	Α,	Δ.	4 Α	\ <i>A</i>	A	. A	Α	Α	Α	Α
Res	et (0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0
Id	R	w	Field	Value Id	Va	lue							De	scri	ptio	n																		
Α	R	W	EEP										Poi	inte	r to	eve	nt r	egis	ter.	Acc	ept	10 2:	nly a	ıddı	ess	es 1	o re	egis	ters					_
													fro	m tl	he E	ver	t gr	oup																

21.2.23 CH[9].TEP

Address offset: 0x55C Channel 9 task end-point

Bit r	numbe	er		31	. 30	29	28	3 2	7 26	25	24	23	3 22	21	20	19	18	17	16	15	14	13 :	12 :	11 :	10	9	8	7	6	5	4	3	2	1)
Id				Α	Α	Α	Α	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A.	Α .	Α
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	Va	lue	:						De	escr	ipti	on																				ı
Α	RW	TEP										Pc	ointe	er to	o ta	sk r	egis	ster	. Ac	cep	ots o	nly	ad	dre	sse	s t	o re	gis	ters	5					
												fro	om 1	the	Tas	k gr	oup	ο.																	

21.2.24 CH[10].EEP

Address offset: 0x560

Channel 10 event end-point

Bit	number		31 30 29 2	28 27 26	25 2	24 23	22 21	20 19	18 1	7 16	15	14 13	3 12	11 10	9	8	7	6	5	4	3 2	1	0
Id			A A A A	A A A	A	А А	A A	A A	A A	А А	Α	ΑА	А	A A	Α	Α	Α	Α	Α	Α	A A	Α	Α
Res	et 0x00000000	0 0 0 0	0 0 0	0 (0 0	0 0	0 0	0 (0 0	0	0 0	0	0 0	0	0	0	0	0	0	0 0	0	0	
Id	DW 5: 11	Value Id	Value			n-																	
	RW Field	value lu	value			De	script	on															
A	RW EEP	value lu	value				•	on o ever	t regi	ster.	Acc	epts	only	addre	sses	s to	reg	iste	ers				

21.2.25 CH[10].TEP

Address offset: 0x564

Channel 10 task end-point

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW TEP	Pointer to task register. Accepts only addresses to registers

from the Task group.

21.2.26 CH[11].EEP

Address offset: 0x568

Channel 11 event end-point



Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	otic	n																			
Α	RW	EEP										Poi	nte	r to	ev	ent	reg	giste	er.	Acc	ept	S O	nly	ado	dres	ses	to	reg	iste	ers				

from the Event group.

21.2.27 CH[11].TEP

Address offset: 0x56C

Channel 11 task end-point

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15 :	L4 1	3 12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 A	Α	Α	Α	Α	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	4 A	А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio																		
		riciu											,cp	LiUi	•																	
Α		TEP													task	regi	ster	. Ac	сер	ts o	nly a	ddre	esse	s to	re	gist	ters	s				

21.2.28 CH[12].EEP

Address offset: 0x570

Channel 12 event end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21 :	20 :	19 1	18 1	7 1	6 15	5 14	4 13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ /	4 A	. 4	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ,	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	scrip	otio	n																		
Α	RW	EEP										Poi	ntei	r to	eve	ent	regi	ste	r. Ac	cep	ots c	nly	ado	ires	ses	to	reg	iste	ers				
												froi	m th	ne F	ver	nt g	rout	1															

21.2.29 CH[12].TEP

Address offset: 0x574

Channel 12 task end-point

Bit	numb	er		3	1 30	29	28	3 27	7 26	25	24	23	22 2	21 2	0 19	9 18	3 17	16	15	14	13	L2 1	.1 1	0 9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	. A	A	Α	Α	Α	Α	Α .	А А	Α	Α	Α	Α	Α	Α	Α .	4 Δ	A	A	. A	Α	Α	Α	A A	A 4	A A
Res	et 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	V	alue	•						De	scrip	otio	n																	
Δ	D۱۸	' TEP										Poi	inter	r to	task	reg	iste	r A	ccer	nts (only	ad	dres	ses	to i	regi	ster	'S				
, ,	11.00	ILF														6	iste		0001		····,		u. co	505		-0						

21.2.30 CH[13].EEP

Address offset: 0x578

Channel 13 event end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW EEP		Pointer to event register. Accepts only addresses to registers

from the Event group.

21.2.31 CH[13].TEP

Address offset: 0x57C

Channel 13 task end-point



Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15 :	L4 1	3 12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 A	Α	Α	Α	Α	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	4 A	А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio																		
		riciu											,cp	LiUi	•																	
Α		TEP													task	regi	ster	. Ac	сер	ts o	nly a	ddre	esse	s to	re	gist	ters	s				

21.2.32 CH[14].EEP

Address offset: 0x580

Channel 14 event end-point

Bitı	numbe	er		3:	1 30	29	2	8 2	7 2	26 2	25	24	23	22 :	21 2	20 :	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1)
Id				Α	Α	Α	. 4	۱ ۸	4 /	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A.
Res	et 0x0	0000000		0	0	0	0) (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	,
Id	RW	Field	Value Id	V	alue	•							Des	cri	otio	n																				ı
Α	RW	EEP											Poi	ntei	to	eve	ent	reg	iste	er. A	Acc	ept	s oı	nly	ado	Ires	ses	to ı	egi	iste	rs					7
													froi	n th	ne F	ver	nt ø	roi	ın																	

21.2.33 CH[14].TEP

Address offset: 0x584

Channel 14 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	.9 1	l8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ,	A A	A /	A A	. Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Α Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	TEP										Poi	nter	to	tasl	k re	gist	er.	Acc	ept	on	y a	ddre	sse	s to	re	gist	ers	5				
												froi	n th	ne T	ask	gro	oup.																

21.2.34 CH[15].EEP

Address offset: 0x588

Channel 15 event end-point

Bit	number		31 30 29 2	28 27 26	25 2	24 23	22 21	20 19	18 1	7 16	15	14 13	3 12	11 10	9	8	7	6	5	4	3 2	1	0
Id			A A A A	A A A	A	А А	A A	A A	A A	А А	Α	ΑА	А	A A	Α	Α	Α	Α	Α	Α	A A	Α	Α
Res	et 0x00000000		0 0 0 0	0 0 0	0 (0 0	0 0	0 0	0 (0 0	0	0 0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id	DW 5: 11	Value Id	Value			n-																	
	RW Field	value lu	value			De	script	on															
A	RW EEP	value lu	value				•	on o ever	t regi	ster.	Acc	epts	only	addre	sses	s to	reg	iste	ers				

21.2.35 CH[15].TEP

Address offset: 0x58C

Channel 15 task end-point

Bitı	numbe	r		31	30	29	28	27	26	25	24	23	22	21 :	20 1	.9 1	8 1	7 1	6 1	5 14	4 1	3 12	2 1:	10	9	8	7	6	5	4	3	2	1 0	
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ,	A A	۸ 4	Α Α			. Α	. A	. A	Α	Α	Α	Α	Α	Α	A	Δ,	А А	
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0) (0	0	0	0	0	0	0	0	0	0	0 (0 0	
Id	RW	Field	Value Id	Va	lue							De	cri	otio	n																			
Α	RW	TEP										Poi	nte	r to	tas	k re	gist	er.	Acc	ept	s o	ıly a	add	ress	es 1	to re	egis	ter	s					

from the Task group.

21.2.36 CH[16].EEP

Address offset: 0x590

Channel 16 event end-point



Bit r	umb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15	14 1	.3 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	A	Α /	А А	Α	Α	Α	Α	Α.	Д Д	A	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Res	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	crip	tio	n																	
Α	RW	EEP										Poi	nter	to	even	t re	gist	er. /	Acce	epts	only	y ad	dres	sses	to	reg	iste	rs				
												fro	m th	ie E	vent	gro	up.															

21.2.37 CH[16].TEP

Address offset: 0x594

Channel 16 task end-point

Bit r	nur	nbe	r		31	30	29	28	27	26	25	24	23	22	21	20 :	19 1	18 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α /	4 4	Α Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	A A
Res	et (0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	R	w	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	R	W	TEP										Ро	inte	r to	tas	k re	gist	er.	Acc	ept	on	ly a	ddr	ess	es t	o re	gis	ters					
													fro	m tl	he 1	Гask	gro	oup.																

21.2.38 CH[17].EEP

Address offset: 0x598

Channel 17 event end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21 :	20 :	19 1	18 1	7 1	6 15	5 14	4 13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ /	4 A	. 4	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ,	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	scrip	otio	n																		
Α	RW	EEP										Poi	ntei	r to	eve	ent	regi	ste	r. Ac	cep	ots c	nly	ado	ires	ses	to	reg	iste	ers				
												froi	m th	ne F	ver	nt g	rout	1															

21.2.39 CH[17].TEP

Address offset: 0x59C

Channel 17 task end-point

Bit r	iumb	er			31	1 30	29	2	8 2	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 :	1 ()
Id					Α	Α	Α	A	Δ.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۸ ۸	4 Α	
Rese	et Ox	000	00000		0	0	0	C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 ()
Id	RW	Fi	ield	Value Id	Va	alue	•							De	scr	ipti	on																				l
Α	RW	' TI	EP											Ро	int	er t	o ta	sk r	egi	ster	. A	cce	pts	on	ly a	ddr	esse	es to	o re	gis	ters	;					
														fro	m	the	Tas	kσ	rou	n																	

21.2.40 CH[18].EEP

Address offset: 0x5A0

Channel 18 event end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW EEP		Pointer to event register. Accepts only addresses to registers

from the Event group.

21.2.41 CH[18].TEP

Address offset: 0x5A4 Channel 18 task end-point



Bit r	numbe	r		31	30	29	28	27	26	25	24	23	22	21	20 :	19	18 1	17 1	16 1	L5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	Δ Α	λ Δ	. 4	A	Α	Α	Α	Α	Α	Α	A	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							De	cri	otic	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	egis	ter.	Aco	cept	ts o	nly	add	ress	es t	to re	egis	ter	5				

from the Task group.

from the Event group.

21.2.42 CH[19].EEP

Address offset: 0x5A8

Channel 19 event end-point

Bit nun	mber		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 1	16 1	15 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α ,	Δ Α	A	Α	Α	Α	Α	Α	Α	Α	Α.	А А	A	Α
Reset (0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0	0	0
ld R	RW Field	Value Id	Va	lue							De	scri	ptic	on																		
A R	RW EEP										Ро	nte	r to	ev	ent	reg	iste	r. A	cce	pts	only	ad	dres	ses	to	reg	iste	rs				

21.2.43 CH[19].TEP

Address offset: 0x5AC Channel 19 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	4 А
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	TEP										Ро	inte	r to	tas	k re	egis	ter	. Ac	cep	ots	onl	y a	ddr	ess	es t	o re	egis	ters	5				
												fro	m t	he -	Task	gr	our	o.																

21.2.44 CHG[0]

Address offset: 0x800 Channel group 0

Bit r	numbe	er		31	30	29	28	27	26	25	5 2	24 2	23 2	22	21	20	19	18	17	7 10	5 1	5 1	4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3	2	1	0
Id				f	е	d	С	b	а	Z	١	Υ :	X١	W	٧	U	Т	S	R	. C	Į F	, ()	N N	/ I	_ K	J	-1	Н	G	F	Ε	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	(0	0	0	0	0	0	0	0	0	C) ()	0 () (0 0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue	:						0	Des	cri	ipti	on																				
Α	RW	CH0										I	ncli	ud	e o	r ex	κclι	ıde	ch	anr	el	0														
			Excluded	0								Е	xcl	lud	le																					
			Included	1								I	ncli	ud	e																					
В	RW	CH1										I	ncli	ud	e o	r ex	κclι	ıde	ch	anr	el:	1														
			Excluded	0								Е	Excl	lud	le																					
			Included	1								I	ncli	ud	е																					
С	RW	CH2										I	ncli	ud	e o	r ex	κclι	ıde	ch	anr	el:	2														
			Excluded	0								Е	xcl	lud	le																					
			Included	1								I	ncli	ud	e																					
D	RW	CH3										- I	ncli	ud	e o	r ex	κclι	ıde	ch	anr	el:	3														
			Excluded	0								E	Excl	lud	le																					
			Included	1								I	ncli	ud	e																					
E	RW	CH4										I	ncli	ud	e o	r ex	κclι	ıde	ch	anr	el -	4														
			Excluded	0								Е	Excl	lud	le																					
			Included	1								I	ncli	ud	e																					
F	RW	CH5										I	ncli	ud	e o	r ex	κclι	ıde	ch	anr	el!	5														
			Excluded	0								E	Excl	lud	le																					
			Included	1								- I	ncli	ud	e																					
G	RW	CH6										I	ncli	ud	e o	r ex	κclι	ıde	ch	anr	el	6														



Di+ w	مامس	\-		21 20	20.20	27.20	25.24	12 22 24 2	00 10 1	0 17	16 15	14 12	12 11	10 0	0	7 /	~ F	1	2 2	1 0
Id	iumbe	er						23 22 21 2 X W V I												
	et OxO	0000000						0 0 0 0												
		Field	Value Id	Value				Description												
			Excluded	0				Exclude												
			Included	1				Include												
Н	RW	CH7						Include or	exclud	e chai	nnel 7									
			Excluded	0				Exclude												
			Included	1				Include												
I	RW	CH8						Include or	exclud	e chai	nnel 8									
			Excluded	0				Exclude												
			Included	1				Include												
J	RW	СН9						Include or	exclud	e chai	nnel 9									
			Excluded	0				Exclude												
			Included	1				Include												
K	RW	CH10						Include or	exclud	e chai	nnel 10	0								
			Excluded	0				Exclude												
	Dist	CU11	Included	1				Include												
L	KW	CH11	Evaluded	0				Include or	exclud	e chai	inel 1	Ţ								
			Excluded Included	0				Exclude Include												
М	D\A/	CH12	included	1				Include or	ovelud	o chai	nnal 1	,								
IVI	I VV	CHIZ	Excluded	0				Exclude	exciuu	e ciiai	illei 1.	2								
			Included	1				Include												
N	RW	CH13	o.uucu	_				Include or	exclud	e chai	nnel 1	3								
			Excluded	0				Exclude												
			Included	1				Include												
0	RW	CH14						Include or	exclud	e chai	nnel 1	4								
			Excluded	0				Exclude												
			Included	1				Include												
Р	RW	CH15						Include or	exclud	e chai	nnel 1	5								
			Excluded	0				Exclude												
			Included	1				Include												
Q	RW	CH16						Include or	exclud	e chai	nnel 1	6								
			Excluded	0				Exclude												
			Included	1				Include												
R	RW	CH17						Include or	exclud	e chai	nnel 1	7								
			Excluded	0				Exclude												
	DIA	CUAO	Included	1				Include				_								
S	KVV	CH18	Evaludad	0				Include or	exclud	e cnai	inei 1	5								
			Excluded Included	1				Exclude Include												
Т	RW	CH19	included	_				Include or	exclud	e chai	nnel 1	9								
			Excluded	0				Exclude												
			Included	1				Include												
U	RW	CH20						Include or	exclud	e chai	nnel 20	0								
			Excluded	0				Exclude												
			Included	1				Include												
V	RW	CH21						Include or	exclud	e chai	nnel 2	1								
			Excluded	0				Exclude												
			Included	1				Include												
W	RW	CH22						Include or	exclud	e chai	nnel 2	2								
			Excluded	0				Exclude												
			Included	1				Include												
Х	RW	CH23						Include or	exclud	e chai	nnel 2	3								
			Excluded	0				Exclude												
			Included	1				Include												
Υ	кW	CH24	Frielinde d	0				Include or	exclud	e chai	nnel 2	4								
			Excluded	0				Exclude												



Bi	t num	nbe	r		31 3	0 2	9 28	27 2	6 2	5 24	23	22 :	21 2	0 19	18	17	16 1	5 14	13	12 1	1 10	9	8	7 6	5	4	3	2 1	. 0
Id					f e	e d	d c	b a	a Z	<u> </u>	Χ	W	νι	J T	S	R	Q F	0	N	M L	. K	J	L	1 (i F	Ε	D	СВ	8 A
R	eset 0)x00	000000		0 (0 (0 0	0 () (0	0	0	0 (0	0	0	0 0	0	0	0 0	0	0	0 () (0	0	0	0 0	0
Id	R	w	Field	Value Id	Valu	ie					De	scrip	otior	1															
				Included	1						Inc	clude	:																
Z	R۱	W	CH25								Inc	clude	ore	exclu	ide (char	nel :	25											
				Excluded	0						Exc	clude	9																
				Included	1						Inc	clude	:																
а	R۱	W	CH26								Inc	clude	ore	exclu	ide (char	nel:	26											
				Excluded	0						Exc	clude	9																
				Included	1						Inc	clude	:																
b	R۱	W	CH27								Inc	clude	ore	exclu	ide (char	nel:	27											
				Excluded	0						Exc	clude	9																
				Included	1						Inc	clude	:																
С	R۱	W	CH28								Inc	clude	ore	exclu	ide (char	nel:	28											
				Excluded	0						Exc	clude	e																
				Included	1						Inc	clude	:																
d	R۱	W	CH29								Inc	clude	ore	exclu	ide (char	nel:	29											
				Excluded	0						Exc	clude	9																
				Included	1						Inc	clude	•																
е	R۱	W	CH30								Inc	clude	ore	exclu	ide (char	nel	30											
				Excluded	0						Exc	clude	9																
				Included	1						Inc	clude																	
f	R۱	W	CH31								Inc	clude	ore	exclu	ide (char	nel	31											
				Excluded	0						Exc	clude	2																
				Included	1						Inc	clude	:																

21.2.45 CHG[1]

Address offset: 0x804

Channel group 1

Bit	numbe	er		31	30	29	28	27	26	25	5 24	2:	3 2	22 21	1 2	0 1	9 1	8	17	16	15	14	13 1	12 1	1 10) 9	8	7	6	5	4	3 2	1	0
Id														W V																				
	et 0x0	0000000												0 0																				
Id		Field	Value Id	Va	lue							D	es	cript	ioi	n																		
Α	RW	CH0												ude (lud	e c	har	nne	10													
			Excluded	0								E>	xcl	ude																				
			Included	1								In	ıclı	ude																				
В	RW	CH1										In	ıclı	ude (or	excl	lud	e c	har	nne	11													
			Excluded	0								E>	xcl	ude																				
			Included	1								In	ıclı	ude																				
С	RW	CH2										In	ıclı	ude (or	excl	lud	e c	har	nne	12													
			Excluded	0								E>	xcl	ude																				
			Included	1								In	ıclı	ude																				
D	RW	СНЗ										ln	ıclı	ude (or	excl	lud	e c	har	nne	13													
			Excluded	0								E>	xcl	ude																				
			Included	1								In	ıclı	ude																				
Ε	RW	CH4										In	ıclı	ude (or	excl	lud	e c	har	nne	۱4													
			Excluded	0								E>	xcl	ude																				
			Included	1								In	ıclı	ude																				
F	RW	CH5										In	ıclı	ude (or	excl	lud	e c	har	nne	15													
			Excluded	0								E>	xcl	ude																				
			Included	1								In	ıclı	ude																				
G	RW	CH6										In	ıclı	ude (or	excl	lud	e c	har	ne	۱6													
			Excluded	0								E>	xcl	ude																				
			Included	1								In	ıclı	ude																				
Н	RW	CH7										In	ıclı	ude (or	excl	lud	e c	har	nne	17													
			Excluded	0								Ex	xcl	ude																				



	umbe	er						4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								'XWVUTSRQPONMLKJIHGFEDCBA
		0000000			0 0	0	0 0	
ld	RW	Field	Value Id	Value				Description
			Included	1				Include
I	RW	CH8						Include or exclude channel 8
			Excluded	0				Exclude
			Included	1				Include
J	RW	CH9						Include or exclude channel 9
			Excluded	0				Exclude
			Included	1				Include
K	RW	CH10						Include or exclude channel 10
			Excluded	0				Exclude
			Included	1				Include
L	RW	CH11						Include or exclude channel 11
			Excluded	0				Exclude
			Included	1				Include
М	RW	CH12						Include or exclude channel 12
			Excluded	0				Exclude
			Included	1				Include
N	RW	CH13						Include or exclude channel 13
			Excluded	0				Exclude
			Included	1				Include
0	RW	CH14						Include or exclude channel 14
			Excluded	0				Exclude
			Included	1				Include
Р	RW	CH15						Include or exclude channel 15
			Excluded	0				Exclude
			Included	1				Include
Q	RW	CH16						Include or exclude channel 16
			Excluded	0				Exclude
			Included	1				Include
R	RW	CH17						Include or exclude channel 17
			Excluded	0				Exclude
			Included	1				Include
S	RW	CH18						Include or exclude channel 18
			Excluded	0				Exclude
			Included	1				Include
Т	RW	CH19						Include or exclude channel 19
			Excluded	0				Exclude
			Included	1				Include
U	RW	CH20						Include or exclude channel 20
			Excluded	0				Exclude
			Included	1				Include
V	RW	CH21						Include or exclude channel 21
			Excluded	0				Exclude
			Included	1				Include
w	RW	CH22						Include or exclude channel 22
			Excluded	0				Exclude
			Included	1				Include
Х	RW	CH23						Include or exclude channel 23
			Excluded	0				Exclude
			Included	1				Include
Υ	RW	CH24						Include or exclude channel 24
			Excluded	0				Exclude
			Included	1				Include
Z	RW	CH25						Include or exclude channel 25
			Excluded	0				Exclude
			Included	1				Include



Bit	numbe	er		31	30	29 2	28 2	7 26	25	24	23	22	21 2	20 1	9 1	8 17	7 16	5 15	14	13	12	11 1	0 9	8	7	6	5	4	3 2	1	0
Id				f	е	d	c b	а	Z	Υ	Χ	W	٧	U 1	Г :	S R	. a	P	0	N	М	L k	J	-1	Н	G	F	Ε	D C	В	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Val	lue						De	escri	otio	n																	
а	RW	CH26									Inc	clude	or	excl	lud	e ch	ann	el 2	6												
			Excluded	0							Ex	clud	е																		
			Included	1							Inc	clude	9																		
b	RW	CH27									Inc	clude	or	excl	lud	e ch	ann	el 2	7												
			Excluded	0							Ex	clud	е																		
			Included	1							Inc	clude	9																		
С	RW	CH28									Inc	clude	or	excl	lud	e ch	ann	el 2	8												
			Excluded	0							Ex	clud	е																		
			Included	1							Inc	clude	e																		
d	RW	CH29									Inc	clude	or	excl	lud	e ch	ann	el 2	9												
			Excluded	0							Ex	clud	е																		
			Included	1							Inc	clude	9																		
е	RW	CH30									Inc	clude	or	excl	lud	e ch	ann	el 3	0												
			Excluded	0							Ex	clud	е																		
			Included	1							Inc	clude	9																		
f	RW	CH31									Inc	clude	or	excl	lud	e ch	ann	el 3	1												
			Excluded	0							Ex	clud	е																		
			Included	1							Inc	clude	9																		
е	RW	СН30	Excluded Included Excluded Included Excluded Excluded	1 0 1 0 1							Inco	clude clude clude clude clude clude clude	e or e or e e or e e e e or e e e e e e	excl	lude	e ch	ann	el 3	0												

21.2.46 CHG[2]

Address offset: 0x808 Channel group 2

Bit nu	umbe	r		31	30	29	28	27	26	25	24	- 23	3 22	2 2:	1 2	0 1	9 1	.8 1	7 1	.6 1	.5	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (
Id																																			B A
Rese	t 0x0	0000000																																	0 (
Id	RW	Field	Value Id	Va	lue							De	esc	ript	tioi	n																			
Α	RW	СН0										In	clu	de (or (exc	lud	e cl	nan	nel	0														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
В	RW	CH1										In	clu	de (or (exc	lud	e cl	nan	nel	1														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
С	RW	CH2										In	clu	de (or (exc	lud	e cl	nan	nel	2														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
D	RW	CH3										In	clu	de (or (exc	lud	e cl	nan	nel	3														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
Ε	RW	CH4										In	clu	de (or (exc	lud	e cl	nan	nel	4														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
F	RW	CH5										In	clu	de (or (exc	lud	e cl	nan	nel	5														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
G	RW	CH6										In	clu	de (or	exc	lud	e cl	nan	nel	6														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
Н	RW	CH7												de (or (exc	lud	e cl	nan	nel	7														
			Excluded	0								Ex	clu	ıde																					
			Included	1									clu																						
I	RW	CH8												de (or (exc	lud	e cl	nan	nel	8														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					



Bit r	numbe	er		31 30	29 2	8 27	7 26 2	25 24	23 22	2 21 2	20 19	18 1	17 1	5 15	14 :	13 12	2 11	10 !	9 8	7	6	5 4	4 3	2	1 (
Id									x w																
Res	et 0x0	0000000		0 0	0 (0 0	0	0 0	0 0	0	0 0	0	0 0	0	0	0 0	0	0	0 0	0	0	0 (0 0	0	0 (
Id	RW	Field	Value Id	Value					Descr	riptio	n														
J	RW	CH9							Includ	de or	exclud	de cl	hanr	iel 9											
			Excluded	0					Exclu	de															
			Included	1					Includ	de															
K	RW	CH10							Includ	de or	exclud	de cl	hanr	nel 10)										
			Excluded	0					Exclu	de															
			Included	1					Includ	de															
L	RW	CH11							Includ	de or	exclud	de cl	hanr	nel 11	l										
			Excluded	0					Exclu	de															
			Included	1					Includ	de															
М	RW	CH12							Includ	de or	exclud	de cl	hanr	el 12	2										
			Excluded	0					Exclu	de															
			Included	1					Includ	de															
N	RW	CH13							Includ	de or	exclud	de cl	hanr	el 13	3										
			Excluded	0					Exclu	de															
			Included	1					Includ																
0	RW	CH14							Includ	de or	exclud	de cl	hanr	el 14	1										
			Excluded	0					Exclu	de															
			Included	1					Includ																
Р	RW	CH15									exclud	de cl	hanr	el 15	5										
			Excluded	0					Exclu																
			Included	1					Includ																
Q	RW	CH16									exclud	de cl	hanr	iel 16	ō										
			Excluded	0					Exclu																
			Included	1					Includ																
R	RW	CH17									exclud	de cl	hanr	iel 17	7										
			Excluded	0					Exclu																
			Included	1					Includ																
S	RW	CH18		_							exclud	de cl	hanr	iel 18	3										
			Excluded	0					Exclu																
-	DIA	01140	Included	1					Includ				1	140											
Т	KW	CH19	Fundand	0							exclud	ie ci	nanr	iei 19	ð										
			Excluded	0					Exclu																
	DVA	CU20	Included	1					Includ					-1.20	,										
U	KVV	CH20	Final code of	0							exclud	ie ci	nanr	iei zu)										
			Excluded	0					Includ																
V	D\A/	CU21	Included	1							exclud	ام ما	h a m v	. al 31											
V	KVV	CH21	Evaluded	0					Exclu		exclud	ie ci	IIdIII	iei Z.	L										
			Excluded						Includ																
W	B/v/	CH22	Included	1							exclud	le c	hanr	ല 21	,										
٧V	11.44	0.144	Excluded	0					Exclu		CACIUC	ال ت	iaill	ıcı 22	-										
			Included	1					Includ																
Х	R\M	CH23	ciaucu	•							exclud	de cl	hanr	el 23	3										
^		5.125	Excluded	0					Exclu		CACIUL	ال ما	iuill	.c. Z3											
			Included	1					Includ																
Υ	RW	CH24		-							exclud	le cl	hanr	nel 24	1										
•			Excluded	0					Exclu		zciul			4*											
			Included	1					Includ																
Z	R\M	CH25		-							exclud	le cl	hanr	el 2º	5										
_		5.125	Excluded	0					Exclu		CACIUL	ال ما	iuill	.ci Z											
			Included	1					Includ																
a	R\M	CH26		•							exclud	le cl	hanr	el 26	5										
u	1.00	520	Excluded	0					Exclu		CACIUL			2 (•										
			Included	1					Includ																
b	RW	CH27		-							exclud	le cl	hanr	nel 27	7										
J		0.127							meiut	ال عد	CACIUL	ال ت	iarii	21											



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZY	'XWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Excluded	0	Exclude
	Included	1	Include
c RW CH28			Include or exclude channel 28
	Excluded	0	Exclude
	Included	1	Include
d RW CH29			Include or exclude channel 29
	Excluded	0	Exclude
	Included	1	Include
e RW CH30			Include or exclude channel 30
	Excluded	0	Exclude
	Included	1	Include
f RW CH31			Include or exclude channel 31
	Excluded	0	Exclude
	Included	1	Include

21.2.47 CHG[3]

Address offset: 0x80C

Channel group 3

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		fedcbaZYXWVUTSRQPONMLKJIHGFEDCB
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW CH0		Include or exclude channel 0
	Excluded	0 Exclude
	Included	1 Include
B RW CH1		Include or exclude channel 1
	Excluded	0 Exclude
	Included	1 Include
C RW CH2		Include or exclude channel 2
	Excluded	0 Exclude
	Included	1 Include
D RW CH3		Include or exclude channel 3
	Excluded	0 Exclude
	Included	1 Include
E RW CH4		Include or exclude channel 4
	Excluded	0 Exclude
	Included	1 Include
F RW CH5	moducu	Include or exclude channel 5
6.13	Excluded	0 Exclude
	Included	1 Include
G RW CH6	meladea	Include or exclude channel 6
d NW CHO	Excluded	0 Exclude
	Included	1 Include
H RW CH7	iliciadea	Include or exclude channel 7
II KW CII/	Excluded	0 Exclude
	Included	1 Include
I RW CH8	iliciadea	Include or exclude channel 8
I IVV CHO	Excluded	0 Exclude
I DW CHO	Included	1 Include
J RW CH9	5 1 1 1	Include or exclude channel 9
	Excluded	0 Exclude
	Included	1 Include
K RW CH10		Include or exclude channel 10



Bit r	numbe	er		31 30	29 28	27 2	6 25	24 :	23 22 21 20	19 18	17 1	16 15	14 13	12 1	11 10	9	8 7	6	5 4	1 3	2 1	0
Id				f e	d c	b a	a Z	Υ	x w v u	T S	R	Q P	O N	М	L K	J	ΙН	G	F I	E D	СВ	Α
Res	et OxO	0000000		0 0	0 0	0 (0 0	0	0 0 0 0	0 0	0	0 0	0 0	0	0 0	0	0 0	0	0 (0 0	0 0	0
Id	RW	Field	Value Id	Value					Description													
			Excluded	0					Exclude													
	5144		Included	1					Include													
L	RW	CH11	Evoluded	0					Include or ex	clude	chan	inel 1	1									
			Excluded Included	0					Exclude Include													
М	RW	CH12	iliciadea	1					include Include or ex	rclude	chan	nel 1	2									
		CHIZ	Excluded	0					Exclude	ciuuc	criari		_									
			Included	1					Include													
N	RW	CH13						- 1	Include or ex	clude	chan	nel 1	3									
			Excluded	0				-	Exclude													
			Included	1				ı	Include													
0	RW	CH14						- 1	Include or ex	clude	chan	nel 1	4									
			Excluded	0				ı	Exclude													
			Included	1				- 1	Include													
Р	RW	CH15						- 1	Include or ex	clude	chan	nel 1	5									
			Excluded	0					Exclude													
			Included	1					Include													
Q	RW	CH16							Include or ex	clude	chan	inel 1	6									
			Excluded	0					Exclude													
R	D\A/	CH17	Included	1					Include Include or ex	cludo	chan	nol 1	7									
N	NVV	CHI7	Excluded	0					Exclude of ex	ciuue	CHan	illei 1	,									
			Included	1					Include													
S	RW	CH18	o.uucu	-					Include or ex	clude	chan	nel 1	8									
			Excluded	0					Exclude													
			Included	1				ı	Include													
Т	RW	CH19						- 1	Include or ex	clude	chan	nel 1	9									
			Excluded	0					Exclude													
			Included	1				- 1	Include													
U	RW	CH20						ı	Include or ex	clude	chan	nel 20	0									
			Excluded	0				- 1	Exclude													
			Included	1					Include													
V	RW	CH21							Include or ex	clude	chan	inel 2	1									
			Excluded	0					Exclude													
۱۸/	D\A/	CH33	Included	1					Include Include or ex	cludo	chan	nol 2	,									
W	KVV	CH22	Excluded	0					include or ex Exclude	ciuue	Criari	mei z.	2									
			Included	1					Include													
Х	RW	CH23		_					Include or ex	clude	chan	nel 2	3									
			Excluded	0				1	Exclude													
			Included	1				ı	Include													
Υ	RW	CH24						ı	Include or ex	clude	chan	nel 2	4									
			Excluded	0				ı	Exclude													
			Included	1				ı	Include													
Z	RW	CH25						- 1	Include or ex	clude	chan	nel 2	5									
			Excluded	0					Exclude													
			Included	1					Include													
а	RW	CH26							Include or ex	clude	chan	inel 2	6									
			Excluded	0					Exclude													
h	D\47	CU27	Included	1					Include	rolphel -	che	nol 3	7									
b	KW	CH27	Evaludad	0					Include or ex	ciude	cnan	inel 2	/									
			Excluded Included	0					Exclude Include													
С	RW/	CH28	meluucu						include Include or ex	clude	chan	nel 2	B									
~			Excluded	0					Exclude of ex		J. 1011	21	-									
				-																		



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	Included	1 Include
d RW CH29		Include or exclude channel 29
	Excluded	0 Exclude
	Included	1 Include
e RW CH30		Include or exclude channel 30
	Excluded	0 Exclude
	Included	1 Include
f RW CH31		Include or exclude channel 31
	Excluded	0 Exclude
	Included	1 Include

21.2.48 CHG[4]

Address offset: 0x810 Channel group 4

011	uiii	iei group 4																										
Bit	numb	er		31 30	29 2	28 2	7 26	25 2	24 :	23 22 2:	L 20	19 1	L8 1	7 1	5 15	5 14	13	12 3	11 1	0 9	8	7	6	5	4 3	3 2	1	0
Id				f e	d	c k	о а	Z	Υ	x w v	U	Т	S	R C	Q P	0	Ν	М	L k	J	1	Н	G	F	E [) C	В	Α
Res	et 0x(0000000		0 0	0	0 (0	0	0	0 0 0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0
Id	RW	Field	Value Id	Value	•				ı	Descript	ion																	
Α	RW	CH0							-	Include	or ex	clud	e cl	nanr	el ()												
			Excluded	0					ı	Exclude																		
			Included	1					-	Include																		
В	RW	CH1							ı	Include	or ex	clud	e cl	nanr	el :	L												
			Excluded	0					- 1	Exclude																		
			Included	1					- 1	Include																		
С	RW	CH2							-	Include	or ex	clud	e cl	nanr	iel 2	2												
			Excluded	0					١	Exclude																		
			Included	1					-	Include																		
D	RW	CH3							- 1	Include	or ex	clud	e cl	nanr	iel 3	3												
			Excluded	0					- 1	Exclude																		
			Included	1					- 1	Include																		
E	RW	CH4								Include	or ex	clud	e cl	nanr	el 4	1												
			Excluded	0						Exclude																		
			Included	1						Include																		
F	RW	CH5								Include	or ex	clud	e cl	nanr	iel 5	5												
			Excluded	0						Exclude																		
	5111	0115	Included	1						Include																		
G	RW	CH6								Include	or ex	clud	e cl	nanr	iel 6	Ó												
			Excluded	0						Exclude																		
Н	DIA	CUZ	Included	1						Include Include		اد ، ، اد	1		-1-	,												
П	KVV	CH7	Excluded	0						Exclude	л ех	ciuu	e ci	Idili	iei .	′												
			Included	1						Include																		
1	R\M	CH8	Iliciadea	1						Include	or ev	clud	م دا	nanr	ا م	2												
•	11.00	CHO	Excluded	0						Exclude	JI CA	ciuu	C Ci	iaiii	ici	,												
			Included	1						Include																		
J	RW	CH9		-						Include	or exc	clud	e cl	nanr	el 9)												
			Excluded	0						Exclude																		
			Included	1						Include																		
K	RW	CH10								Include	or ex	clud	e cl	nanr	nel :	LO												
			Excluded	0					ı	Exclude																		
			Included	1					ı	Include																		
L	RW	CH11								Include	or exc	clud	e cl	nanr	el :	l1												
			Excluded	0					ı	Exclude																		



Bit n	umbe	er		31 30	29 2	28 27	26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id				f e	d	c b	a	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B
Rese	et OxO	0000000		0 0	0	0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			Included	1					Include
M	RW	CH12							Include or exclude channel 12
			Excluded	0					Exclude
			Included	1					Include
N	RW	CH13							Include or exclude channel 13
			Excluded	0					Exclude
_			Included	1					Include
0	RW	CH14							Include or exclude channel 14
			Excluded	0					Exclude
	DV4	CUAS	Included	1					Include
Р	KVV	CH15	Evaludad	0					Include or exclude channel 15
			Excluded Included	0					Exclude Include
Q	D\A/	CH16	mciuded	1					Include or exclude channel 16
Q	NVV	CHIO	Excluded	0					Exclude of exclude charmer 16
			Included	1					Include
R	D\A/	CH17	iliciadea	1					Include or exclude channel 17
N	NVV	CHIZ	Excluded	0					Exclude of exclude charmer 17
			Included	1					Include
S	RW/	CH18	meidaea	-					Include or exclude channel 18
,		CITIO	Excluded	0					Exclude
			Included	1					Include
Т	RW	CH19		_					Include or exclude channel 19
			Excluded	0					Exclude
			Included	1					Include
U	RW	CH20							Include or exclude channel 20
			Excluded	0					Exclude
			Included	1					Include
٧	RW	CH21							Include or exclude channel 21
			Excluded	0					Exclude
			Included	1					Include
W	RW	CH22							Include or exclude channel 22
			Excluded	0					Exclude
			Included	1					Include
Χ	RW	CH23							Include or exclude channel 23
			Excluded	0					Exclude
			Included	1					Include
Υ	RW	CH24							Include or exclude channel 24
			Excluded	0					Exclude
			Included	1					Include
Z	RW	CH25							Include or exclude channel 25
			Excluded	0					Exclude
			Included	1					Include
а	RW	CH26							Include or exclude channel 26
			Excluded	0					Exclude
			Included	1					Include
b	RW	CH27							Include or exclude channel 27
			Excluded	0					Exclude
			Included	1					Include
С	RW	CH28		_					Include or exclude channel 28
			Excluded	0					Exclude
		0.100	Included	1					Include
d	RW	CH29	5 1 1 1						Include or exclude channel 29
			Excluded	0					Exclude
			Included	1					Include



Bitı	numbe	er		31	30 2	9 :	28 2	27 :	26 2	5 2	24 2	3 22	2 21	20	19	18	17	16	15 1	.4 1	3 12	2 11	10	9	8	7	6	5	4	3	2	1 0
Id				f	е	d	С	b	a Z	7	Y X	W	/ V	U	Т	S	R	Q	Р (1 C	N N	1 L	K	J	1	Н	G	F	Ε	D	C I	ВА
Res	et 0x0	0000000		0	0	0	0	0	0 0)	0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						D	esci	ripti	on																		
е	RW	CH30									In	clu	de o	r ex	clu	de d	har	ine	I 30													
			Excluded	0							E	clu	de																			
			Included	1							In	clu	de																			
f	RW	CH31									In	clu	de o	r ex	clu	de d	har	ne	l 31													
			Excluded	0							E	clu	de																			
			Included	1							In	clu	de																			

21.2.49 CHG[5]

Address offset: 0x814 Channel group 5

F F F F F F F F F F	Reset	nannel grou	rb 2		
Series 100000000000000000000000000000000000	Reserve	number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
No.	Id RW CH0 Schuded Value Description A RW CH0 Excluded 0 Exclude Included 1 Include Include B RW CH1 Include Exclude Include 1 Include or exclude channel 1 Exclude Include 1 Include or exclude channel 2 Exclude Include 1 Include Include Include 1 Include Include Include 1 Include or exclude channel 3 Exclude Include 1 Include Include E RW CH4 Excluded 0 Exclude Include 1 Include or exclude channel 4 Exclude E RW CH5 Excluded 0 Exclude Included 1 Include or exclude channel 5 Exclude Excluded 0 Exclude Include or exclude channel 6 Excluded 0 <td></td> <td></td> <td>f e d c b a</td> <td>a ZYXWVUTSRQPONMLKJIHGFEDCBA</td>			f e d c b a	a ZYXWVUTSRQPONMLKJIHGFEDCBA
RW CH0	A RW brack CRU brackluded included i	set 0x00000000		0 0 0 0 0 0	
Excluded Included Included Included Include Included Include		RW Field	Value Id	Value	Description
	Note	RW CH0			Include or exclude channel 0
RW	B RW CH1 Excluded included 0 Exclude Exclude C RW Included 1 Include or exclude channel 2 C RW Included 0 Exclude Include or exclude channel 2 Exclude 0 Exclude Included 1 Include or exclude channel 3 Exclude Included 1 Include Include E RW Included 1 Include E RW Included 1 Include Included 1 Include Include or exclude channel 4 Exclude Include Include or exclude channel 4 Exclude Include Include or exclude channel 5 Exclude Include Include or exclude channel 5 Exclude Include Include or exclude channel 6 Exclude Include Include or exclude channel 7 Exclude Include Include or exclude channel 8 Exclude Include Include or exclude channel 9 Exclude Include <td< td=""><td></td><td>Excluded</td><td>0</td><td>Exclude</td></td<>		Excluded	0	Exclude
RW CH2 Excluded 0 Exclude 1 RW CH2 Excluded 0 Exclude 0 RW CH3 Excluded 0 Exclude 0 RW CH3 Excluded 0 Exclude 0 RW CH4 Included 1 Include 1 Included 1 Include 1 2 RW CH4 Included 1 Include 2 RW CH4 Excluded 0 Exclude 3 RW CH5 Included 1 Include 4 RW CH5 Excluded 0 Exclude 4 RW CH6 Excluded 0 Exclude 5 RW CH7 Excluded 0 Exclude 6 RW CH7 Excluded 0 Exclude 7 RW CH8 Excluded 0 Exclude			Included	1	Include
Include	Include	RW CH1			Include or exclude channel 1
RW	C RW CH2 Excluded 0 Exclude 1 mclude Exclude D RW CH3 Excluded 0 Exclude 1 mclude or exclude channel 3 E RW CH3 Excluded 0 Exclude 1 mclude or exclude channel 4 E RW CH4 Excluded 0 Exclude 6 1 mclude 1 mclude or exclude channel 4 1 mclude 6		Excluded	0	Exclude
Figure F			Included	1	Include
RW CH3	Note Control	RW CH2			Include or exclude channel 2
RW	D RW CH3 Excluded included 0 Exclude Exclude E RW CH4 Included 1 Include Include E RW CH4 Excluded 0 Exclude Exclude Included 1 Include or exclude channel 4 Include or exclude channel 5 F RW CH5 Excluded 0 Exclude Included 1 Include or exclude channel 5 Exclude Included 1 Include or exclude channel 5 Exclude Included 1 Include or exclude channel 6 Exclude Included 1 Include or exclude channel 6 Exclude Included 1 Include or exclude channel 7 Exclude Included 1 Include or exclude channel 8 Exclude Included 1 Include Exclude Include or exclude channel 9 Exclude Exclude Include Include or exclude channel 10 Exclude Include or exclude channel 10 Exclude Include or		Excluded	0	Exclude
RW CH4 Excluded 0 Exclude Include 1 Include Include or exclude channel 4 Include or exclude channel 4 Excluded 0 Exclude Include 1 Include Include or exclude channel 5 Excluded 0 Exclude Included 1 Include Include Include 1 Include Include Included 1 Include Include Include 2 Exclude Include Include 2 Exclude Include Include Include 4 Include Include Include	Excluded 0 Exclude Included 1 Include E RW CH4 Excluded 0 Exclude Include or exclude channel 4 Exclude 1 Include or exclude channel 4 Image: Free control or exclude channel o		Included	1	Include
RW CH4	RW	RW CH3			Include or exclude channel 3
RW	E RW CH4 Excluded included 0 Exclude Exclude Included 1 Include or exclude channel 5 F RW CH5 Excluded 0 Exclude Include or exclude channel 5 Exclude 0 Exclude Include or exclude channel 5 Exclude 0 Exclude Include or exclude channel 6 Exclude 0 Exclude Include or exclude channel 6 Exclude 0 Exclude Include or exclude channel 7 Exclude 0 Exclude Include or exclude channel 7 Exclude 0 Exclude Include or exclude channel 8 Exclude 0 Exclude Include or exclude channel 9 Exclude 0 Exclude Include or exclude channel 10 Exclude 0 Exclude Include or exclude channel 10 Exclude 0 Exclude Include or exclude channel 11 Exclude 0 Exclude Include or exclude channel 12 Exclude 0 Exclude <td></td> <td>Excluded</td> <td>0</td> <td>Exclude</td>		Excluded	0	Exclude
RW CH5 Excluded 0 Exclude nclude 6 RW CH5 Excluded 0 Exclude 6 RW CH6 Excluded 0 Exclude 6 RW CH6 Excluded 0 Exclude 6 RW CH7 Excluded 0 Exclude 6 RW CH7 Excluded 0 Exclude 6 RW CH8 Excluded 0 Exclude 6 RW CH8 Excluded 0 Exclude 6 RW CH9 Excluded 0 Exclude 6 RW CH9 Excluded 0 Exclude 7 RW CH10 Excluded 0 Exclude 8 RW CH9 Excluded 0 Exclude 8 RW CH10	F RW Included Excluded Included 1 Exclude Include F RW INTERPRETATION FOR THE PROPERTY OF THE		Included	1	Include
RW	F RW CH5 Excluded 0 Exclude Include or exclude channel 5 G RW CH6 Excluded 0 Exclude G RW CH6 Excluded 0 Exclude Include or exclude channel 6 Excluded 0 Exclude Include or exclude channel 7 Include or exclude channel 7 Include or exclude channel 7 RW CH7 Excluded 0 Exclude Include or exclude channel 8 Excluded 0 Exclude Include or exclude channel 9 Excluded 1 Include or exclude channel 9 Include or exclude channel 10 Excluded 1 Include or exclude channel 10 Include or exclude channel 10 Excluded 0 Exclude Include or exclude channel 11 Include Include Include or exclude channel 11 Include or exclude channel 11 Include or exclude channel 11 Include or exclude channel 11 Excluded or exclude channel 12 Include or exclude channel 12	RW CH4			Include or exclude channel 4
RW	F RW CH5 Excluded included 0 Exclude Exclude G RW CH6 Included 1 Include or exclude channel 6 G RW CH6 Excluded 0 Exclude Included 1 Include Include H RW CH7 Excluded 0 Exclude Included 1 Include or exclude channel 7 Include Include I RW CH8 Excluded 0 Exclude Included 1 Include or exclude channel 8 Exclude Include or exclude channel 9 Exclude Include or exclude channel 9 Exclude Include or exclude channel 10 Exclude Include Include Include or exclude channel 10 Exclude Include Include Include 1 Include or exclude channel 10 Exclude Include or exclude channel 11 Excluded Include or exclude channel 11 Include or exclude channel 11 Include or exclude channel 12 Exclude		Excluded	0	Exclude
Excluded D	Back Included Excluded 0 Exclude G RW Include 1 Include G RW Include 1 Include or exclude channel 6 Excluded 0 Exclude Include 1 Include Include or exclude channel 7 Exclude Excluded 0 Exclude Include 1 Include Include or exclude channel 7 Exclude Include or exclude channel 8 Exclude Exclude 0 Exclude Include or exclude channel 8 Exclude Include or exclude channel 9 Exclude Include 1 Include Include 1 Include Include or exclude channel 10 Exclude Include or exclude channel 11 Include or exclude channel 11 Include or exclude channel 11 Include or exclude channel 12 Include or exclude channel 12 Exclude or exclude channel 12		Included	1	Include
RW CH6	Included 1	RW CH5			Include or exclude channel 5
Include or exclude channel 6 Exclude Included Included Include Include or exclude channel 6 Exclude Include Include Include Include or exclude channel 7 Exclude Included Include	G RW CH6 Excluded Excluded Included 0 Exclude Include H RW Included 1 Include Include H RW Include or exclude channel 7 Excluded Include Include or exclude channel 7 I Include or exclude channel 8 Excluded Include Include or exclude channel 8 I Include or exclude channel 9 Excluded Included Include or exclude channel 9 I Include Or exclude channel 9 Excluded Included Include or exclude channel 10 I Include Or exclude channel 10 Exclude Include Include Or exclude channel 10 I Include Or exclude channel 10 Exclude Include Include Or exclude Channel 11 I Include Or exclude channel 11 Exclude Include Or exclude Channel 11 Include Or exclude Channel 11 I Include Or exclude Channel 11 Exclude Include Or exclude Channel 11 Include Or exclude Channel 12 I Include Or exclude Channel 12 Exclude Or exclude Channel 12 Include Or exclude Channel 12		Excluded	0	Exclude
RW	RW CH7 Excluded 0 Exclude I RW CH7 Excluded 0 Exclude I RW CH8 Excluded 0 Exclude I RW CH8 Excluded 0 Exclude I RW CH9 Excluded 0 Exclude I Excluded 0 Exclude I Include or exclude channel 9 Excluded 0 Exclude I Include or exclude channel 10 Excluded 0 Exclude I Include or exclude channel 10 Excluded 1 Include I Include or exclude channel 11 Excluded 0 Exclude I Include or exclude channel 11 Excluded 1 Include or exclude channel 12 Excluded 1 Include or exclude channel 12 Excluded 1 Include or exclude channel 12		Included	1	Include
Included 1 Include or exclude channel 7 Excluded 0 Exclude Included 1 Include or exclude channel 8 Excluded 0 Exclude channel 8 Excluded 0 Exclude channel 8 Excluded 0 Exclude channel 8 Excluded 1 Include or exclude channel 8 Excluded 1 Include Included 1 Include Include or exclude channel 9 Exclude included 0 Exclude channel 9 Excluded 0 Exclude channel 9 Excluded 1 Include or exclude channel 9 Excluded 1 Include or exclude channel 9 Exclude included 1 Include Exclude channel 10 Exclude or exclude channel 10 Excluded 1 Include or exclude channel 10	Include Incl	RW CH6			Include or exclude channel 6
Horse RW CH7 Excluded 0 Exclude Finclude Include Include 0 Exclude Channel 7 RW CH8 Excluded 0 Include O Exclude Channel 8 Excluded 0 Exclude Finclude Include Inc	H RW CH7 Excluded 0 Exclude Include or exclude channel 7 Excluded 1 Include Include or exclude channel 8 Excluded 0 Exclude Include or exclude channel 8 Excluded 0 Exclude Include or exclude channel 12 Exclude Include or exclude channel 12 Exclude		Excluded	0	Exclude
RW CH9 Excluded 0 Exclude RW CH9 Excluded 0 Exclude RW CH9 Excluded 1 Include or exclude channel 9 Excluded 0 Exclude Include or exclude channel 9 Exclude Include or exclude channel 9 Include Include 1 Include Include 1 Include	Excluded 0 Exclude Include I RW CH8 Excluded 0 Exclude Include or exclude channel 8 Excluded 0 Exclude Include I I RW CH9 Excluded 0 Exclude Include Included 1 Include Excluded 1 Include Excluded 1 Include Exclude Included 1 Include K RW CH10 Excluded 0 Exclude Include Included 1 Include Excluded 0 Exclude Include or exclude channel 10 Excluded 1 Include Excluded 0 Exclude Include 0 Exclude Include or exclude channel 11 Excluded 0 Exclude Include or exclude channel 11 Excluded 0 Exclude Include or exclude channel 11 Excluded 0 Include M CH12 Excluded 0 Exclude Include or exclude channel 11 Excluded 0 Exclude		Included	1	Include
RW CH8 Included 1 Include or exclude channel 8 Excluded 0 Exclude Included 1 Include RW CH9 Include or exclude channel 9 Excluded 0 Exclude Include 1 Include X RW CH10 Include or exclude channel 10 Excluded 0 Exclude Include or exclude channel 10 Exclude Included 1 Include	Included I RW CH8 Excluded 0 Exclude Include 0 Include Include or exclude channel 8 Excluded 1 Include Include Include 1 Include Include or exclude channel 9 Excluded 0 Exclude Include 0 Include K RW CH10 Excluded 0 Include 0 Include Excluded 0 Exclude Include or exclude channel 10 Excluded 0 Exclude Include 1 Include L RW CH11 Excluded 0 Exclude Include 0 Exclude Include 0 Include M RW CH12 Excluded 0 Exclude Include or exclude channel 11 Excluded 0 Exclude Include or exclude channel 12 Excluded 0 Exclude Include or exclude channel 12 Excluded 0 Exclude	RW CH7			Include or exclude channel 7
RW CH8 Excluded 0 Exclude Included 1 Include RW CH9 Excluded 0 Exclude Excluded 0 Exclude Include 1 Include X RW CH10 Included 1 Include or exclude channel 10 Excluded 0 Exclude Exclude Include Include	Include or exclude channel 8 Excluded Included Include Include		Excluded	0	Exclude
RW CH9 Excluded 0 Exclude Excluded 0 Include or exclude channel 9 Excluded 0 Exclude Included 1 Include X RW CH10 Included 1 Include or exclude channel 10 Excluded 0 Exclude Exclude Included 1 Include	Excluded 0 Exclude J RW CH9 Excluded 0 Exclude Include or exclude channel 9 Excluded 0 Exclude Include Include Include Include Include Include Include Include or exclude channel 10 Exclude or exclude channel 10 Excluded 0 Exclude Include or exclude channel 11 Excluded 0 Exclude Include Includ		Included	1	Include
RW CH9 Excluded 0 Exclude Include 1 Include Include 1 Include X RW CH10 Included 1 Include or exclude channel 10 Excluded 0 Exclude Include Include Include	Included J RW CH9 Excluded 0 Exclude Include 0 Include K RW CH10 Excluded 0 Include Included 1 Include or exclude channel 10 Excluded 0 Exclude Include or exclude channel 10 Excluded 1 Include L RW CH11 Excluded 0 Exclude Include or exclude channel 11 Excluded 0 Exclude Include or exclude channel 11 Excluded 0 Exclude Include or exclude channel 11 Excluded 1 Include M RW CH12 Excluded 0 Exclude Include or exclude channel 12 Excluded 0 Exclude Excluded 1 Excluded Include or exclude channel 12 Excluded 0 Exclude	RW CH8			Include or exclude channel 8
RW CH9 Include or exclude channel 9 Excluded 0 Exclude Included 1 Include X RW CH10 Include or exclude channel 10 Excluded 0 Exclude Include Include Include	Include or exclude channel 9 Excluded Included Included Include K RW CH10 Excluded Included Included Included Included Included Include Incl		Excluded	0	Exclude
Excluded 0 Exclude Included 1 Include RW CH10 Excluded 0 Exclude channel 10 Excluded 0 Exclude Included 1 Include	Excluded 0 Exclude Included 1 Include K RW CH10 Excluded 0 Exclude Include or exclude channel 10 Excluded 1 Include Include Include Include Include Include Include Include Include or exclude channel 11 Excluded 0 Exclude Include or exclude channel 11 Include Include Include Include Include Exclude Include Include Exclude Include Include Include Include Exclude Include Include Include Exclude Include or exclude channel 12 Exclude		Included	1	Include
Included 1 Include RW CH10 Include or exclude channel 10 Excluded 0 Exclude Included 1 Include	K RW CH10	RW CH9			Include or exclude channel 9
RW CH10 Include or exclude channel 10 Excluded 0 Exclude Included 1 Include	K RW CH10 Excluded 0 Exclude Include or exclude channel 10 Excluded 1 Include L RW CH11 Excluded 0 Exclude Include or exclude channel 11 Excluded 0 Exclude Include Include M RW CH12 Excluded 0 Exclude Include Include Exclude Excluded 0 Exclude Exclude Excluded 0 Exclude Exclude		Excluded	0	Exclude
Excluded 0 Exclude Included 1 Include	Excluded 0 Exclude Included 1 Include Include or exclude channel 11 Excluded 0 Exclude Include 1 Include M RW CH12 Excluded 0 Exclude Excluded 0 Exclude Include or exclude channel 12 Excluded 0 Exclude		Included	1	Include
Included 1 Include	L RW CH11 Included 1 Include or exclude channel 11 Excluded 0 Exclude Include 1 Include M RW CH12 Include Include or exclude channel 12 Excluded 0 Exclude	RW CH10			Include or exclude channel 10
	L RW CH11 Excluded 0 Exclude Included 1 Include M RW CH12 Include or exclude channel 12 Excluded 0 Exclude		Excluded	0	Exclude
	Excluded 0 Exclude Included 1 Include M RW CH12 Include or exclude channel 12 Excluded 0 Exclude		Included	1	Include
KW CH11 Include or exclude channel 11	M RW CH12 Included 1 Include Excluded 0 Exclude	RW CH11			Include or exclude channel 11
Excluded 0 Exclude	M RW CH12 Include or exclude channel 12 Excluded 0 Exclude		Excluded	0	Exclude
Included 1 Include	Excluded 0 Exclude		Included	1	Include
N RW CH12 Include or exclude channel 12		RW CH12			Include or exclude channel 12
Excluded 0 Exclude			Excluded	0	Exclude
	Included 1 Include		Included	1	Include



Bitı	numb	er		31 30	29 28	27 26	25 24	23 22 21 20	19 18	17 1	.6 15	14 13	12 11	. 10	9 8	7	6 5	4	3 2	1 0
Id				f e	d c	b a	ΖY	X W V U	T S	R	Q P	O N	M L	K	JI	Н	G F	Ε	D C	ВА
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0	0 0	0 (0 0	0 0	0 0	0	0 0	0	0 0	0	0 0	0 0
Id	RW	Field	Value Id	Value				Description												
N	RW	CH13						Include or ex	clude	chan	nel 13	3								
			Excluded	0				Exclude												
			Included	1				Include												
0	RW	CH14						Include or ex	clude	chan	nel 14	ı								
			Excluded	0				Exclude												
			Included	1				Include												
Р	RW	CH15						Include or ex	clude	chan	nel 15	;								
			Excluded	0				Exclude												
			Included	1				Include												
Q	RW	CH16						Include or ex	clude	chan	nel 16	j								
			Excluded	0				Exclude												
			Included	1				Include												
R	RW	CH17						Include or ex	clude	chan	nel 17	,								
			Excluded	0				Exclude												
			Included	1				Include												
S	RW	CH18						Include or ex	clude	chan	nel 18	3								
			Excluded	0				Exclude												
			Included	1				Include												
Т	RW	CH19		_				Include or ex	clude	chan	nel 19)								
			Excluded	0				Exclude												
			Included	1				Include												
U	RW	CH20	5 1 1 1					Include or ex	kclude	chan	nel 20)								
			Excluded	0				Exclude												
\ /	D\A/	CU24	Included	1				Include			121									
V	KW	CH21	Football d	0				Include or ex	ciuae	cnan	nei 21	-								
			Excluded	0				Exclude												
W	D\A/	CH22	Included	1				Include Include or ex	(cludo	chan	nol 22	,								
vv	NVV	CHZZ	Excluded	0				Exclude of ex	ciuue	CHAIL	1161 22	•								
			Included	1				Include												
Х	RW/	CH23	meidaea	_				Include or ex	clude	chan	nel 23	l l								
^		CITES	Excluded	0				Exclude	ciaac	criari	1101 23	,								
			Included	1				Include												
Υ	RW	CH24	moladed	-				Include or ex	clude	chan	nel 24									
-			Excluded	0				Exclude												
			Included	1				Include												
Z	RW	CH25						Include or ex	clude	chan	nel 25	;								
			Excluded	0				Exclude												
			Included	1				Include												
a	RW	CH26						Include or ex	clude	chan	nel 26	5								
			Excluded	0				Exclude												
			Included	1				Include												
b	RW	CH27						Include or ex	clude	chan	nel 27	,								
			Excluded	0				Exclude												
			Included	1				Include												
С	RW	CH28						Include or ex	clude	chan	nel 28	3								
			Excluded	0				Exclude												
			Included	1				Include												
d	RW	CH29						Include or ex	clude	chan	nel 29)								
			Excluded	0				Exclude												
			Included	1				Include												
e	RW	CH30						Include or ex	clude	chan	nel 30)								
			Excluded	0				Exclude												
			Included	1				Include												
f	RW	CH31						Include or ex	clude	chan	nel 31									



Bit number		31 30 29 28 27	6 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5	4 3 2 1 0
Id		fedcb	aZYXWVUTSRQ	PONMLKJIHGF	E D C B A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0
Id RW Field	Value Id	Value	Description		
	Excluded	0	Exclude		
	Included	1	Include		

21.2.50 FORK[0].TEP

Address offset: 0x910 Channel 0 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW TFP		Pointer to task register

21.2.51 FORK[1].TEP

Address offset: 0x914 Channel 1 task end-point

Bit n	مامسا	0.0		21	20	20	20	27	20	25	24	22	22	21	20	10	10	17	10	1 [11	12	12	11	10	0	0	7	_	г	1	2	.	1 0
DIL II	umb	er		31	30	29	28	21	20	25	24	23	22	21	20	19	10	1/	10	12	14	13	12	11	10	9	٥	/	О	Э	4	3	Ζ.	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	А А
Rese	t Ox(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	on																			
Α	RW	TEP										Pο	inte	r to	ta:	sk r	egis	ter																

21.2.52 FORK[2].TEP

Address offset: 0x918 Channel 2 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 1	l7 1	6 15	5 14	13	12	11	10	9 8	3 7	' 6	5	4	3	2	1 0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	A A	Α	Α	Α	Α	Α.	Δ ,	4 Α	Α	Α	Α	Α	Α	АА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																	
Α	RW	TEP		Pointer to task register																												

21.2.53 FORK[3].TEP

Address offset: 0x91C Channel 3 task end-point

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Id				A A A A A A A A A A A A A A A A A A A	Α
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
Id	RW	Field	Value Id	Value Description	
Α	RW	TEP		Pointer to task register	

21.2.54 FORK[4].TEP

Address offset: 0x920 Channel 4 task end-point



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0										
Id	A A A A A A A A A A A A A A A A A A A										
Reset 0x00000000	$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$										
Id RW Field Value Id	Value Description										
A RW TEP	Pointer to task register										

21.2.55 FORK[5].TEP

Address offset: 0x924 Channel 5 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0										
Id		A A A A A A A A A A A A A A A A A A A										
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0										
Id RW Field	Value Id	Value Description										
A RW TEP		Pointer to task register										

21.2.56 FORK[6].TEP

Address offset: 0x928 Channel 6 task end-point

Bit	numbe	r		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16 15	5 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id				A A A A A	A A A A A A A A A A A	. A A A A A	A A A A A A A A A
Res	et 0x0	0000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description		
Α	RW	TEP			Pointer to task register		

21.2.57 FORK[7].TEP

Address offset: 0x92C Channel 7 task end-point

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (j
Id	RW	Field	Value Id	Va	lue							De	scri	iptio	on																				ı
Α	RW	TEP		Value Description Pointer to task register																										7					

21.2.58 FORK[8].TEP

Address offset: 0x930 Channel 8 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

21.2.59 FORK[9].TEP

Address offset: 0x934 Channel 9 task end-point

Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2 :	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	A A	А А
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 (
ld RW Field	Value Id	0 0 0 0 0 0 0 Value								De	scri	ptic	on																			

A RW TEP Pointer to task register



21.2.60 FORK[10].TEP

Address offset: 0x938

Channel 10 task end-point

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ,	А А	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	
Id	RW	Field	Value Id	Va	lue							De	cri	ptic	n																				
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter																	

21.2.61 FORK[11].TEP

Address offset: 0x93C

Channel 11 task end-point

Bitı	num	bei	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	l
Res	et O	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	RV	٧	Field	Value Id	Va	lue							De	scri	ptic	on																				ı
Α	RV	٧	TEP		Pointer to task register																															

21.2.62 FORK[12].TEP

Address offset: 0x940

Channel 12 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 :	16 :	15 1	L4 1	13 1	.2 1	1 1	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A ,	Δ.	4 Α	A	Α	Α	Α	Α	Α	A	Δ Α	4 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	cri	otic	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	gis	ter															

21.2.63 FORK[13].TEP

Address offset: 0x944

Channel 13 task end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	! 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A		4 A
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	TEP		Pointer to task register																														

21.2.64 FORK[14].TEP

Address offset: 0x948

Channel 14 task end-point

Bit number		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2 1	1 0	
ld		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	4 A	
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	
ld RW Field	Value Id	Va	lue							De	scri	ptic	on																				
A RW TFP										Pο	inte	r to	ta	sk re	pis	ter																	

21.2.65 FORK[15].TEP

Address offset: 0x94C

Channel 15 task end-point



Bit r	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 1	16	15 :	14	13 1	12 1	11 1	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A	Α	Α	Α	Α	Α	Α	A A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	TEP														k re	gis	ter															

21.2.66 FORK[16].TEP

Address offset: 0x950

Channel 16 task end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13	12	11 1	0 9) ;	3 7	7 (5 5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A 4	۱ ۱	A /	۱ ۸	Δ Α	A	Α	Α	Α .	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0) (0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	TEP		Value Description Pointer to task register																7														

21.2.67 FORK[17].TEP

Address offset: 0x954

Channel 17 task end-point

Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22 :	21 2	20 :	19 1	18 :	17 1	16	15	14	13	12	11 :	.0	9 1	3 7	7 (5 5	5 4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A	Α	Α	Α	Α	Α	Α	Α,	Δ,	4 4	۱ ۸	A /	λ Α	A	Α	Α	Α
Rese	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0) (0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			
Α	RW	TEP											ntei	r to	tas	k re	gis	ter																_

21.2.68 FORK[18].TEP

Address offset: 0x958

Channel 18 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	ı
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	ı
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	on																				l
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter																	1

21.2.69 FORK[19].TEP

Address offset: 0x95C

Channel 19 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

21.2.70 FORK[20].TEP

Address offset: 0x960

Channel 20 task end-point

Bit number		31	30 2	29 2	28 2	27 2	26	25	24	23 :	22	21 2	20 1	19 1	.8 1	7 1	6 1	5 1	4 1	3 12	2 1:	10	9	8	7	6	5	4	3 2	2 1	0
Id		Α	Α	A .	Α	A	Α	Α	Α	Α	Α	Α	Α	Α ,	Δ ,	Δ Α	Δ Α	Δ Α	Δ Α	Δ Δ	A	Α.	Α	Α	Α	Α	Α	Α	A A	4 A	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 (0 (0	0	0	0	0	0	0	0	0	0	0 (0 0	0
Id RW Field	Value Id	Val	ue							Des	cri	otio	n																		

A RW TEP Pointer to task register



21.2.71 FORK[21].TEP

Address offset: 0x964

Channel 21 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW TFP		Pointer to task register

21.2.72 FORK[22].TEP

Address offset: 0x968

Channel 22 task end-point

Bitı	num	bei	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	l
Res	et O	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	RV	٧	Field	Value Id	Va	lue							De	scri	ptic	on																				ı
Α	RV	٧	TEP										Poi	nte	r to	tas	sk re	egis	ter																	

21.2.73 FORK[23].TEP

Address offset: 0x96C

Channel 23 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	17 1	16 1	L5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α.	A .	Δ ,	Δ Α	A A	Δ Δ	Α	Α	Α	Α	Α	Α	Α	Α.	АА
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	egist	ter															

21.2.74 FORK[24].TEP

Address offset: 0x970

Channel 24 task end-point

Bit n	umbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 :	16	15 1	14 :	13 1	.2 1	11 1	10 9	9	8	7	6	5 -	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ.	Α.	A A	Δ.	Α.	Α	Α	A .	Α	А А	. A	A
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	TEP										Poi	nte	r to	tas	sk re	gis	ter																

21.2.75 FORK[25].TEP

Address offset: 0x974

Channel 25 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

A RW TEP Pointer to task registe

21.2.76 FORK[26].TEP

Address offset: 0x978

Channel 26 task end-point



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW TEP	Pointer to task register

21.2.77 FORK[27].TEP

Address offset: 0x97C

Channel 27 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	TEP										Poi	inte	er to	ta	sk r	egis	ter																

21.2.78 FORK[28].TEP

Address offset: 0x980

Channel 28 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 :	21	20 :	19	18	17	16 :	15 :	14 1	13 :	L2 1	11 1	0 9	9 8	3 7	' 6	5 5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Α Α	Α /	A 4	A A	. Δ	A	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0) (0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	crip	otic	n																			
Α	RW	TEP										Poi	ntei	r to	tas	k re	egis	ter																

21.2.79 FORK[29].TEP

Address offset: 0x984

Channel 29 task end-point

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (j
Id	RW	Field	Value Id	Va	lue							De	scri	iptio	on																				ı
Α	RW	TEP										Ро	inte	er to	ta	sk r	egi	ster																	7

21.2.80 FORK[30].TEP

Address offset: 0x988

Channel 30 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

21.2.81 FORK[31].TEP

Address offset: 0x98C

Channel 31 task end-point

Bit number	31 30 29	29 28 27 26 25 24	23 22 21 20 19 1	18 17 16 15 14 13 12 11	10 9 8 7 6 5 4 3 2 1 0
Id	A A A	A A A A A A	A A A A A	A A A A A A A	A A A A A A A A A
Reset 0x00000000	0 0 0	0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value	ld Value		Description		

A RW TEP Pointer to task register





22 RADIO — 2.4 GHz Radio

The 2.4 GHz radio transceiver is compatible with multiple radio standards such as 1 Mbps, 2 Mbps and long range *Bluetooth*[®] low energy. IEEE 802.15.4 250 kbps mode is fully supported as well as Nordic's proprietary 1 Mbps and 2 Mbps modes of operation.

Listed here are main features for the RADIO:

- Multi-domain 2.4 GHz radio transceiver:
 - 1 Mbps, 2Mbps and long range (125kbps and 500kbps mode) Bluetooth® low energy modes
 - 250kbps IEEE 802.15.4 mode
 - 1Mbps and 2Mbps Nordic proprietary modes
- Best in class link budget and low power operation
- Efficient data interface with EasyDMA support
- Automatic address filtering and pattern matching

EasyDMA in combination with an automated packet assembler and packet disassembler, and an automated CRC generator and CRC checker, makes it very easy to configure and use the RADIO. See *Figure 30: RADIO block diagram* on page 249 for details.

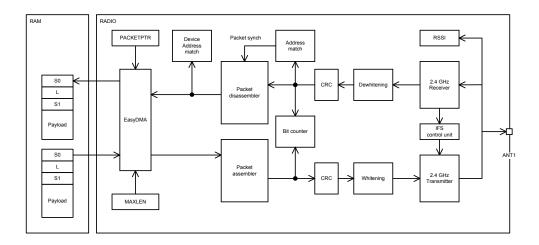


Figure 30: RADIO block diagram

The RADIO includes a Device Address match unit and an interframe spacing control unit that can be utilized to simplify address whitelisting and interframe spacing respectively in *Bluetooth* Smart and similar applications.

The RADIO also includes a Received Signal Strength Indicator (RSSI) and a bit counter. The bit counter generates events when a preconfigured number of bits have been sent or received by the RADIO.

22.1 Packet configuration

RADIO packet contains the following fields: PREAMBLE, ADDRESS, S0, LENGTH, S1, PAYLOAD and CRC.

The content of a RADIO packet is illustrated in *Figure 31: On-air packet layout* on page 250. The RADIO sends the different fields in the packet in the order they are illustrated below, from left to right:



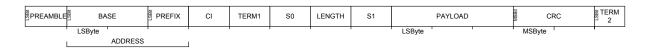


Figure 31: On-air packet layout

Not shown in the figure above is the static payload add-on (the length of which is defined in PCNF1.STATLEN, and which is 0 bytes long in a standard BLE packet). The static payload add-on is sent between the PAYLOAD and CRC fields.

PREAMBLE is sent with least significant bit first on-air. The size of the PREAMBLE depends on the mode selected in the MODE register:

- For all Nordic proprietary radio modes (Nrf_1Mbit, Nrf_2Mbit and Nrf_250Kbit) and for the Ble_1Mbit mode, the PREAMBLE is one byte long. The PLEN field in the PCNF0 register has to be set accordingly. If the first bit of the ADDRESS is 0, the PREAMBLE is set to 0xAA. Otherwise the PREAMBLE is set to 0x55.
- For the Ble_2Mbit mode, the PREAMBLE is 2 bytes long. The PLEN field in the PCNF0 register has to be set to 2 bytes accordingly. If the first bit of the ADDRESS is 0, the PREAMBLE is set to 0xAAAA. Otherwise the PREAMBLE is set to 0x55555.
- For the modes Ble_LR125Kbit and Ble_LR500Kbit, the PREAMBLE is 10 repetitions of 0x3C.
- For the leee802154 250Kbit mode, the PREAMBLE is 4 bytes long and set to all zeros.

Radio packets are stored in memory, inside instances of a radio packet data structure as illustrated in *Figure 32: In-RAM representation of radio packet - S0, LENGTH and S1 are optional* on page 250. The PREAMBLE, ADDRESS, CI, TERM1, TERM2 and CRC fields are omitted in this data structure.



Figure 32: In-RAM representation of radio packet - S0, LENGTH and S1 are optional

The byte ordering on the air is always:

- Least significant byte first for the fields ADDRESS and PAYLOAD. The ADDRESS fields are also always transmitted and received least significant bit first on-air.
- Most significant byte first for the CRC field. The CRC field is also always transmitted and received most significant bit first.

The bit endianness, i.e. the order in which the bits are sent and received, is configured in PCNF1.ENDIAN for the fields S0, LENGTH, S1 and PAYLOAD.

The sizes of the fields S0, LENGTH and S1 can be individually configured in the S0LEN, LFLEN and S1LEN fields of the PCNF0 register respectively. If any of these fields are configured to be less than 8 bit long, the least significant bits of the fields are used, as seen from the RAM representation.

If S0, LENGTH or S1 are specified with zero length, their fields will be omitted in memory. Otherwise each field will be represented as a separate byte, regardless of the number of bits in their on-air counterpart.

The combined length of S0, LENGTH, S1 and PAYLOAD cannot exceed 258 bytes, independent of the configuration in PCNF1.MAXLEN.

22.2 Address configuration

The on-air radio ADDRESS field is composed of two parts, the base address field and the address prefix field.

The size of the base address field is configurable via BALEN in PCNF1. The base address is truncated from LSByte if the BALEN is less than 4. See *Table 31: Definition of logical addresses* on page 251.



Table 31: Definition of logical addresses

Logical address	Base address	Prefix byte
0	BASE0	PREFIXO.APO
1	BASE1	PREFIXO.AP1
2	BASE1	PREFIXO.AP2
3	BASE1	PREFIXO.AP3
4	BASE1	PREFIX1.AP4
5	BASE1	PREFIX1.AP5
6	BASE1	PREFIX1.AP6
7	BASE1	PREFIX1.AP7

The on-air addresses are defined in the BASEn and PREFIXn registers, and it is only when writing these registers the user will have to relate to actual on-air addresses. For other radio address registers such as the TXADDRESS, RXADDRESSES and RXMATCH registers, logical radio addresses ranging from 0 to 7 are being used. The relationship between the on-air radio addresses and the logical addresses is described in *Table 31: Definition of logical addresses* on page 251.

22.3 Data whitening

The RADIO is able to do packet whitening and de-whitening.

See WHITEEN in PCNF1 register for how to enable whitening. When enabled, whitening and de-whitening will be handled by the RADIO automatically as packets are sent and received.

The whitening word is generated using polynomial $g(D) = D^7 + D^4 + 1$, which then is XORed with the data packet that is to be whitened, or de-whitened. See the figure below.

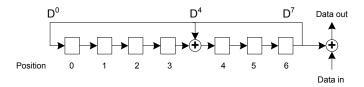


Figure 33: Data whitening and de-whitening

Whitening and de-whitening will be performed over the whole packet (except for the preamble and the address field).

The linear feedback shift register, illustrated in *Figure 33: Data whitening and de-whitening* on page 251 can be initialised via the DATAWHITEIV register.

22.4 CRC

The CRC generator in the RADIO calculates the CRC over the whole packet excluding the preamble. If desirable, the address field can be excluded from the CRC calculation as well

See CRCCNF register for more information.

The CRC polynomial is configurable as illustrated in *Figure 34: CRC generation of an n bit CRC* on page 252 where bit 0 in the CRCPOLY register corresponds to X⁰ and bit 1 corresponds to X¹ etc. See CRCPOLY for more information.



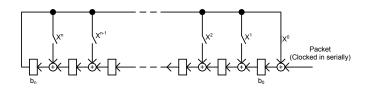


Figure 34: CRC generation of an n bit CRC

As illustrated in *Figure 34: CRC generation of an n bit CRC* on page 252, the CRC is calculated by feeding the packet serially through the CRC generator. Before the packet is clocked through the CRC generator, the CRC generator's latches b_0 through b_n will be initialized with a predefined value specified in the CRCINIT register. When the whole packet is clocked through the CRC generator, latches b_0 through b_n will hold the resulting CRC. This value will be used by the RADIO during both transmission and reception but it is not available to be read by the CPU at any time. A received CRC can however be read by the CPU via the RXCRC register independent of whether or not it has passed the CRC check.

The length (n) of the CRC is configurable, see CRCCNF for more information.

After the whole packet including the CRC has been received, the RADIO will generate a CRCOK event if no CRC errors were detected, or alternatively generate a CRCERROR event if CRC errors were detected.

The status of the CRC check can be read from the CRCSTATUS register after a packet has been received.

22.5 Radio states

Tasks and events are used to control the operating state of the RADIO.

The RADIO can enter the states described the table below.

Table 32: RADIO state diagram

State	Description
DISABLED	No operations are going on inside the radio and the power consumption is at a minimum
RXRU	The radio is ramping up and preparing for reception
RXIDLE	The radio is ready for reception to start
RX	Reception has been started and the addresses enabled in the RXADDRESSES register are being monitored
TXRU	The radio is ramping up and preparing for transmission
TXIDLE	The radio is ready for transmission to start
TX	The radio is transmitting a packet
RXDISABLE	The radio is disabling the receiver
TXDISARI F	The radio is disabling the transmitter

An overview state diagram for the RADIO is illustrated in Figure 35: Radio states on page 253.

Note: PHYEND is only generated in Ble_LR125Kbit, Ble_LR500Kbit and Ieee802154_250Kbit modes.

Note: The END to START shortcut should not be used with Ble_LR125Kbit, Ble_LR500Kbit and leee802154_250Kbit modes. Rather the PHYEND to START shortcut.



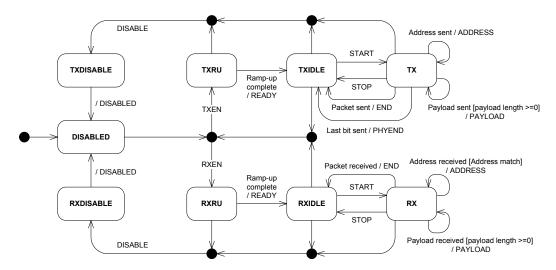


Figure 35: Radio states

This figure shows how the tasks and events relate to the RADIO's operation. The RADIO does not prevent a task from being triggered from the wrong state. If a task is triggered from the wrong state, for example if the RXEN task is triggered from the RXDISABLE state, this may lead to incorrect behaviour. As illustrated in *Figure 35: Radio states* on page 253, the PAYLOAD event is always generated even if the payload is zero.

22.6 Transmit sequence

Before the RADIO is able to transmit a packet, it must first ramp-up in TX mode.

See TXRU in *Figure 35: Radio states* on page 253 and *Figure 36: Transmit sequence* on page 253. A TXRU ramp-up sequence is initiated when the TXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet transmission can be initiate. A packet transmission is initiated by triggering the START task. As illustrated in *Figure 35: Radio states* on page 253 the START task can first be triggered after the RADIO has entered into the TXIDLE state.

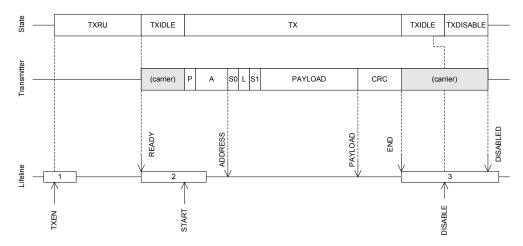


Figure 36: Transmit sequence

Figure 36: Transmit sequence on page 253 illustrates a single packet transmission where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay caused by CPU execution is expected between READY and START, and between END and DISABLE. As illustrated in Figure 36: Transmit sequence on page 253 the RADIO will by default transmit '1's between READY and START, and between END and DISABLED. What is transmitted can be programmed through the DTX field in the MODECNF0 register.

A slightly modified version of the transmit sequence from *Figure 36: Transmit sequence* on page 253 is illustrated in *Figure 37: Transmit sequence using shortcuts to avoid delays* on page 254 where the RADIO



is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.

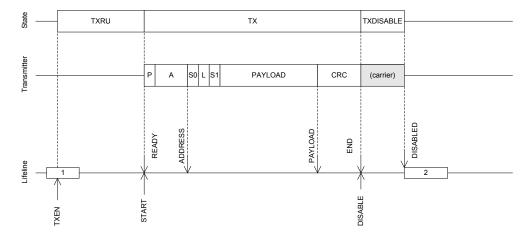


Figure 37: Transmit sequence using shortcuts to avoid delays

The RADIO is able to send multiple packets one after the other without having to disable and re-enable the RADIO between packets, this is illustrated in *Figure 38: Transmission of multiple packets* on page 254.

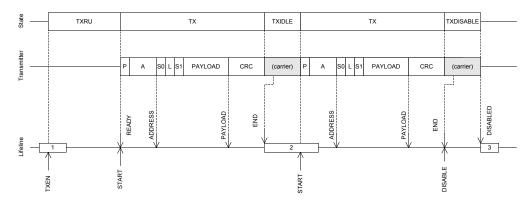


Figure 38: Transmission of multiple packets

22.7 Receive sequence

Before the RADIO is able to receive a packet, it must first ramp up in RX mode

See RXRU in Figure 35: Radio states on page 253 and Figure 39: Receive sequence on page 255.



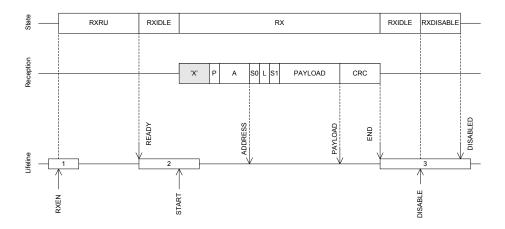


Figure 39: Receive sequence

An RXRU ramp-up sequence is initiated when the RXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet reception can be initiated. A packet reception is initiated by triggering the START task. As illustrated in *Figure 35: Radio states* on page 253 the START task can first be triggered after the RADIO has entered into the RXIDLE state.

Figure 39: Receive sequence on page 255 illustrates a single packet reception where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay, caused by CPU execution, is expected between READY and START, and between END and DISABLE. As illustrated Figure 39: Receive sequence on page 255 the RADIO will be listening and possibly receiving undefined data, represented with an 'X', from START and until a packet with valid preamble (P) is received.

A slightly modified version of the receive sequence from *Figure 39: Receive sequence* on page 255 is illustrated in *Figure 40: Receive sequence using shortcuts to avoid delays* on page 255 where the RADIO is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.

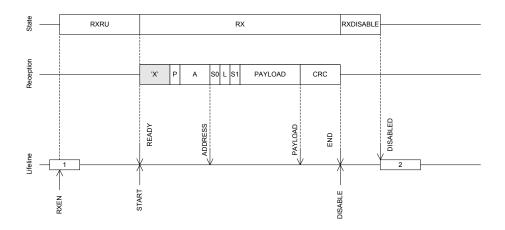


Figure 40: Receive sequence using shortcuts to avoid delays

The RADIO is able to receive multiple packets one after the other without having to disable and re-enable the RADIO between packets as illustrated in *Figure 41: Reception of multiple packets* on page 256.



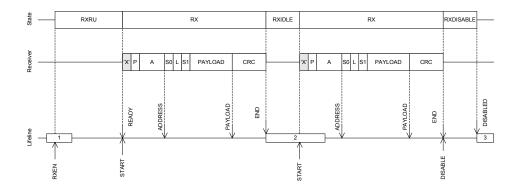


Figure 41: Reception of multiple packets

22.8 Received Signal Strength Indicator (RSSI)

The radio implements a mechanism for measuring the power in the received radio signal. This feature is called Received Signal Strength Indicator (RSSI).

Sampling of the received signal strength is started by using the RSSISTART task. The sample can be read from the RSSISAMPLE register.

The sample period of the RSSI is defined by *RSSI_{PERIOD}*. The RSSI sample will hold the average received signal strength during this sample period.

For the RSSI sample to be valid the radio has to be enabled in receive mode (RXEN task) and the reception has to be started (READY event followed by START task).

22.9 Interframe spacing

Interframe spacing is the time interval between two consecutive packets.

It is defined as the time, in micro seconds, from the end of the last bit of the previous packet received and to the start of the first bit of the subsequent packet that is transmitted. The RADIO is able to enforce this interval as specified in the TIFS register as long as TIFS is not specified to be shorter than the RADIO's turnaround time, i.e. the time needed to switch off the receiver, and switch back on the transmitter. The TIFS register can be written any time before the last bit on air is received.

This timing is illustrated in the *Figure 42: IFS Timing Detail* on page 257. As depicted the TIFS duration starts after the last bit on air, just before the END event, and elapses with first bit being transmitted on air (Just after READY event).



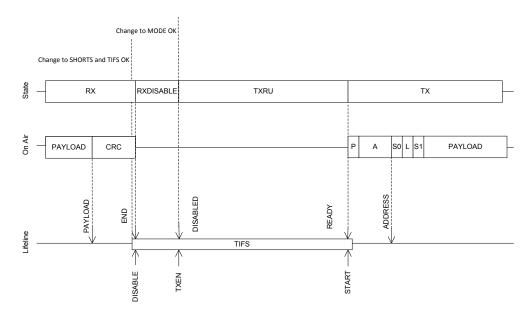


Figure 42: IFS Timing Detail

TIFS is only enforced if END_DISABLE and DISABLED_TXEN or END_DISABLE and DISABLED_RXEN shortcuts are enabled. TIFS is qualified for use in BLE_1MBIT, BLE_2MBIT, BLE_LR125KBIT, BLE_LR500KBIT and leee802154_250Kbit mode using default ramp-up mode. SHORTS and TIFS are not double buffered and can be updated at any point in time before the last bit on air is received. The MODE register is double buffered and sampled at the TXEN or RXEN task.

22.10 Device address match

The device address match feature is tailored for address white listing in a Bluetooth Smart and similar implementations.

This feature enables on-the-fly device address matching while receiving a packet on air. This feature only works in receive mode and as long as RADIO is configured for little endian, see PCNF1.ENDIAN.

The Device Address match unit assumes that the 48 first bits of the payload is the device address and that bit number 6 in S0 is the TxAdd bit. See the Bluetooth Core Specification for more information about device addresses, TxAdd and whitelisting.

The RADIO is able to listen for eight different device addresses at the same time. These addresses are specified in a DAB/DAP register pair, one pair per address, in addition to a TxAdd bit configured in the DACNF register. The DAB register specifies the 32 least significant bits of the device address, while the DAP register specifies the 16 most significant bits of the device address.

Each of the device addresses can be individually included or excluded from the matching mechanism. This is configured in the DACNF register.

22.11 Bit counter

The RADIO implements a simple counter that can be configured to generate an event after a specific number of bits have been transmitted or received.

By using shortcuts, this counter can be started from different events generated by the RADIO and hence count relative to these.

The bit counter is started by triggering the BCSTART task, and stopped by triggering the BCSTOP task. A BCMATCH event will be generated when the bit counter has counted the number of bits specified in the BCC register. The bit counter will continue to count bits until the DISABLED event is generated or until the BCSTOP task is triggered. The CPU can therefore, after a BCMATCH event, reconfigure the BCC value for new BCMATCH events within the same packet.



The bit counter can only be started after the RADIO has received the ADDRESS event.

The bit counter will stop and reset on BCSTOP, STOP, END and DISABLE tasks.

The figure below illustrates how the bit counter can be used to generate a BCMATCH event in the beginning of the packet payload, and again generate a second BCMATCH event after sending 2 bytes (16 bits) of the payload.

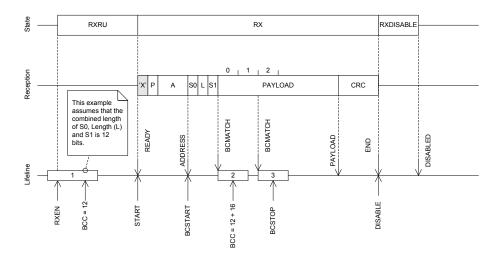


Figure 43: Bit counter example

22.12 IEEE 802.15.4 Operation

With the MODE=Ieee802154_250kbit the radio module will comply with the IEEE 802.15.4-2006 standard implementing its 250 kbps 2450MHz O-QPSK PHY.

The IEEE 802.15.4 standard differs from Nordic's proprietary and Bluetooth Smart modes. Obvious differences are modulation scheme and channel structure, but also packet structure, security and medium access control.

The main features of the IEEE 802.15.4 mode are:

- Ultra Low power 250 kbps 2450MHz IEEE 802.15.4-2006 compliant link
- · Clear Channel Assessment
- · Energy detection scan
- CRC Generation

22.12.1 Packet Structure

The IEEE 802.15.4 standard defines an on the air frame/packet that is different from what is used in BTLE mode.

Figure 44: IEEE 802.15.4 Frame Format - PHY-Layer Frame Structure (PPDU) on page 258 provides an overview of the physical frame structure and its timing.

■ 160usec ■ ■		 ◆32usec◆	<=4064usec-
	PHY Proto	col Data Un	it (PPDU)
Preamble Sequence	SFD	Length	PHY Payload
5 octets Synchronization Heade	er (SHR)	1 octet (PHR)	Maximum 127 octets (PSDU)
			MAC Protocol Data Unit (MPDU)

Figure 44: IEEE 802.15.4 Frame Format - PHY-Layer Frame Structure (PPDU)



The standard uses the term octet as storage unit for 8-bits within the PPDU. For timing the value symbol is used and it has the duration of 16usec.

The total usable payload (PSDU) is 127 octets - but when CRC is being used this is reduced to 125 octets of usable payload.

The preamble sequence consists of four octets that are all zero. These are used for the radio receiver to synchronize on. Following the four octets is a single octet named start of frame delimiter (SFD) with a fixed value of 0xA7. The user can program an alternative SFD through the SFD register. This feature is provided for an initial level of frame filtering for those who choose non standard compliance. It is a valuable feature when operating in a congested or private network. The preamble sequence and SFD is generated by the radio module and is not programmed by the user into the frame buffer.

The PHY header (PHR) is a single octet following the SHR. The least significant seven bits denote the frame length of the following PSDU. The most significant bit is reserved and shall be set to zero for frames that wishes to be standards compliant. The radio module will report all eight bits and it can potentially be used to carry some information. The PHR is the first byte that will be written to the frame Data Memory pointed to by PACKETPTR. Frames with zero length will be discarded and the FRAMESTART event will not be generated in this case.

The next N octets will carry the data of the PHY packet - where N equals the value of the PHR. For an implementation also using the IEEE 802.15.4 MAC layer, the PHY data will be a MAC frame of N-2 octets since two octets will occupy a CRC field.

An IEEE 802.15.4 MAC frame will always consist of a header (The frame control field (FCF), Sequence Number and Addressing Fields), a payload and the 16-bit Frame Control Sequence (FCS) as seen in *Figure 45: IEEE 802.15.4 Frame Format - MAC-Layer Frame Structure (MPDU)* on page 259.

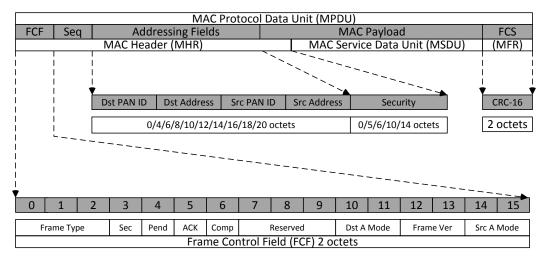


Figure 45: IEEE 802.15.4 Frame Format - MAC-Layer Frame Structure (MPDU)

The two FCF octets contains information about what type of frame this is, what addressing it uses and other control flags. This field is decoded when using the assisted operating modes offered by the radio.

The sequence number is a single octet in size and is unique for a frame. It will be used in the associated acknowledgement frame sent upon successful frame reception.

The addressing field can be zero (Acknowledgement Frame) or up to 20 octets in size. The field is used to direct packets to the correct recipient as well as denoting its origin. IEEE 802.15.4 bases it's addressing on networks being organized in PANs with 16-bit identifier and nodes having a 16 or 64-bit address. In the assisted receive mode these parameters are analyzed for address matching and acknowledgement.

The MAC payload carries the data of the next higher layer or in the case of a MAC command frame information used by the MAC layer itself.

The two last octets contain the 16-bit ITU-T CRC. The FCS is calculated over the MAC header (MHR) and MAC payload (MSDU) parts of the frame. This field is calculated automatically when sending a frame - or indicated in the CRCSTATUS register when a frame is received. This feature is taken care of autonomously by the CRC module if configured.



22.12.2 Operating Frequencies

The IEEE 802.15.4 standard defines 16 channels [11 - 26] in the 2450MHz frequency band of 5MHz each.

The FREQUENCY register of the radio module must be programmed according to *Table 33: IEEE 802.15.4 Center Frequency Definition* on page 260 for correct operation on the center frequency defined for each channel.

Table 33: IEEE 802.15.4 Center Frequency Definition

IEEE 802.15.4 Channel	Center Frequency (MHz)	FREQUENCY Setting
Channel 11	2405	5
Channel 12	2410	10
Channel 13	2415	15
Channel 14	2420	20
Channel 15	2425	25
Channel 16	2430	30
Channel 17	2435	35
Channel 18	2440	40
Channel 19	2445	45
Channel 20	2450	50
Channel 21	2455	55
Channel 22	2460	60
Channel 23	2465	65
Channel 24	2470	70
Channel 25	2475	75
Channel 26	2480	80

22.12.3 Energy Detection

The IEEE 802.15.4 standard requires that it is possible to sample the received signal power within the bandwidth of a channel for the purpose of determining presence of activity.

There should be no attempt made to decode the signals on the channel, and this is done by disabling the shortcut between READY event and START task before putting the radio in receive mode. The energy detection (ED) measurement time where RSSI samples are averaged over is 8 symbol periods (128 microseconds). The standard further specifies the measurement to be a number between 0 and 0xFF - where 0 shall indicate received power less than 10dB above the selected receiver sensitivity. The power range of the ED values must be at least 40dB with a linear mapping with accuracy of +-6dB. See section 6.9.7 Receiver ED in the standard for further details. An example of an ED scan is given below.

Below is a code snippet showing how to perform a single energy detection measurement.

It is the mlme-scan.req primitive of the MAC layer that is using the ED measurement to detect channels where there might be wireless activity. To assist this primitive a taylored mode of operation is available where the ED measurement runs for a defined number of iterations where it keeps track of the maximum ED level. This is enganged by writing the ED_CNT register to a value different from 0, it will then run the specified number of iterations reporting the maximum energy measurement in the EDSAMPLE register. The scan is started with EDSTART task and its end indicated with the EDEND event. This greatly reduces the interrupt frequency and hence power consumtion. *Figure 46: Energy Detection Measurement Examples* on page 261 shows how the ED measurement will operate depending on the ED_CNT register.



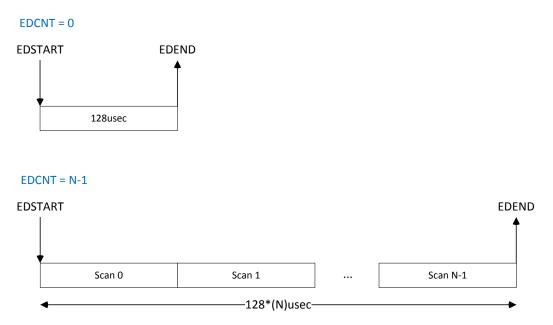


Figure 46: Energy Detection Measurement Examples

An ongoing scan can always be stopped by writing the EDSTOP task. It will be followed by the EDSTOPPED event when the module has terminated.

22.12.4 Clear Channel Assessment

IEEE 802.15.4 implements a listen-before-talk channel access method to avoid collisions when transmitting - namely Carrier Sense Multiple Access with Collision Avoidance (CSMA-CA). The key part of this is measuring if the wireless medium is busy or not.

At least three methods must be supported:

- Mode 1 (Energy above threshold): The medium is reported busy upon detecting any energy above the ED threshold
- Mode 2 (Carrier sense only): The medium is reported busy upon detection of a signal compliant with the IEEE 802.15.4 standard with the same modulation and spreading characteristics.
- Mode 3 (Carrier sense and threshold): The medium is reported busy by logically ANDing or ORing the results from Mode 1 and Mode 2.

It is furthermore specified that the clear channel assessment should survey a period equal to 8 symbols or 128usec.

The radio module has to be in receive mode and be able to recived correct packets when performing the CCA. The shortcut between READY and START must be disabled if baseband processing is not to be performed while the measurement is running.

Mode 1 is enabled by first configuring the CCA_MODE=EdMode and writing the CCA_EDTHRES to a chosen value. When the CCA_START task is written the radio module will perform a ED measurement for 8 symbols and compare the measured level with that found in the CCA_EDTHRES register. If the measured value is higher than or equal to this threshold the CCABUSY event is generated - the CCAIDLE event is generated if the measured level is less than the threshold.

Mode 2 is enabled by configuring the CCA_MODE=CarrierMode. In carrier mode the module will sample to see if a valid SFD is found during the 8 symbols. If a valid SFD is seen the CCABUSY event is generated and the node should not send any data. The CCABUSY event is also generated if the scan was performed during an ongoing frame reception. In the case where the measurement period completes with no SFD detection the CCAIDLE task is generated. With the CCA_CORR_COUNT unequal to zero the algorithm will look at the correlator output in addition to the SFD detection signal. If a SFD is reported during the scan period it will terminate immidiately indicating busy medium. Similarly, if the number of peaks above CCA_CORRTHRES crosses the CCA_CORR_COUNT the CCABUSY event is generated. If less than



CCA_CORR_COUNT crossings are found and no SFD is reported the CCAIDLE signal will be generated and it is ok for the node to commence sending data.

With the CCA_MODE=CarrierAndEdMode or CCA_MODE=CarrierOrEdMode a logical combination of the result from running both Mode 1 and Mode 2 is performed. The CCABUSY or CCAIDLE signal will be generated based on an ANDing or ORing of the internal signals from performing both the energy detection and carrier detection scans.

An ongoing CCA can always be stopped by issuing the CCASTOP task. This will trigger the associated CCASTOPPED event.

For CCA mode automation there are three shortcuts available. One is between CCAIDLE and TXEN. This short must always be used in conjunction with the short between CCAIDLE and STOP. This automation is provided so that the radio can automatically switch between RX (When performing the CCA) and to TX where the packet is sent. The last shortcut associated with the CCA mode is between CCABUSY and DISABLE. This will cause the radio to be disabled whenever the CCA reports a busy medium.

Another handy shortcut is between RXREADY and CCASTART. When the radio has ramped up into RX mode it can immidiately start a CCA.

22.12.5 Cyclic Redundancy Check

IEEE 802.15.4 uses a 16-bit ITU-T cyclic redundancy check (CRC) calculated over the MHR and MSDU.

The standard defines the following generator polynomial:

$$G(x) = x^{16} + x^{12} + x^5 + 1$$

In receive mode the radio will trigger the CRC module when the first octet after the frame length (PHR) is received. The CRC will then update on each consecutive octet received. When a complete frame is received the CRCSTATUS register will be updated accordingly and the EVENTS_CRCOK or EVENTS_CRCERROR generated. When the CRC module is enabled it will not write the two last octets (CRC) to the frame Data RAM. When transmitting the CRC will be computed on the fly, starting with the first octet after PHR, and inserted as the two last octets in the frame. The EasyDMA will fetch frame length - 2 octets from DataRAM and insert the CRC octets insitu.

Below is a code snippet for configuring the CRC module for correct operation when in IEEE 802.15.4 mode. The CRCCNF is written to 16-bit CRC and the CRCPOLY is written to 0x121. The start value used by IEEE 802.15.4 is zero and CRCINIT is configured to reflect this.

```
/* 16-bit CRC with ITU-T polynomial with 0 as start condition*/
write_reg(NRFRADIO_REG(CRCCNF), 0x202);
write_reg(NRFRADIO_REG(CRCPOLY), 0x11021);
write_reg(NRFRADIO_REG(CRCINIT), 0);
```

The ENDIANESS subregister must be set to LittleEndian since the FCS field is transmitted leftmost bit first.

22.12.6 Transmit Sequence

The transmission is started by first putting the radio in receive mode sending the RXEN task.



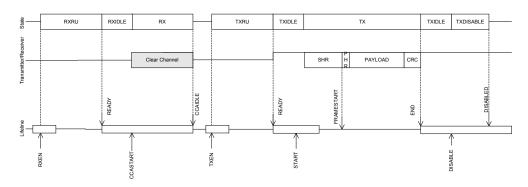


Figure 47: IEEE 802.15.4 Transmit Sequence

The receiver will ramp up and enter the RXIDLE state where the READY event is generated. Upon receiving the ready event the CCA is started by writing to the CCASTART task register. The chosen mode of assessment (CCA_MODE register) will be performed and signal the CCAIDLE or CCABUSY event 128usec later. If the CCABUSY is received the radio will have to retry the CCA after a specific back off period as outlined in the IEEE 802.15.4 standard (See Figure 69 in section 7.5.1.4 The CSMA-CA algorithm of the standard). An outline of the IEEE 802.15.4 transmission can be found in the figure below.

When the CCAIDLE event on the other hand is generated the user shall write to the TXEN task register to enter the TXRU state. The READY event will be generated when the radio is in TXIDLE state and ready to transmit. With the PACKETPTR pointing to the length (PHR) field of the frame the START task can be written. The radio will send the four octet preamble sequence followed by the start of frame delimiter (SFD register). The first byte read from the DataRAM is the length field (PHR) followed by the transmission of the number of bytes indicated as the frame length. If the CRC module is configured it will run for PHR-2 octets. The last two octets will be substituted with the results from running the CRC. The necessary CRC parameters are sampled on the START task. The FCS field of the frame is little endian.

In addition to the already available shortcuts, one is provided between READY event and CCASTART task so that a CCA can automatically start when the receiver is ready. And a second shortcut has been added between CCAIDLE event and the TXEN task so that upon detecting a clear channel the radio can immediately enter transmit mode.

22.12.7 Receive Sequence

The reception is started by first putting the radio in receive mode. Writing to the RXEN task the radio will start ramping up and enter the RXRU state.

When the READY event is generated the radio has entered the RXIDLE mode. For the baseband processing to be enabled the START task must be written. An outline of the IEEE 802.15.4 reception can be found in *Figure 48: IEEE 802.15.4 Receive Sequence* on page 263

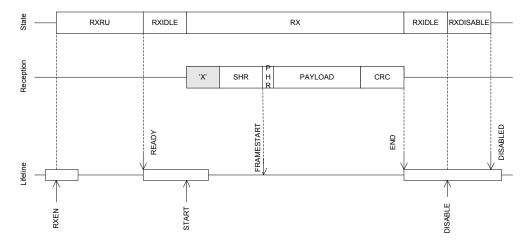


Figure 48: IEEE 802.15.4 Receive Sequence



When a valid SHR is received the radio will start storing future octets (Starting with PHR) to the DataMemory pointed to by PACKETPTR. After the SFD octet is received the FRAMESTART event is generated. If the CRC module is enabled it will start updating with the second byte received (First byte in payload) and run for the full frame length. The two last bytes in the frame is not written to DataRAM when CRC is configured. However, if the result of the CRC after running the full frame is zero the CRCOK event will be generated. The END event is generated when the last octet has been received and is available in DataRAM.

When a packet is received a link quality indicator (LQI) is also generated and appended immediately after the last received octet. When using IEEE 802.15.4 compliant frame this will be just after the MSDU since the FCS is not reported. In the case of a non-complient frame it will be appended after the full frame. The LQI is a number ranging from 0 (lowest link quality) to 255 (highest link quality). The LQI is only valid for frames equal to or longer than three octets. When receiving a frame the RSSI (Reported as negative dB) will be measured at three points during the reception. These three values will be sorted and the middle one selected (Median 3) for then to be remapped within the LQI range. See *Figure 49: IEEE 802.15.4 Frame In DataRAM* on page 264 for further detail on the LQI measurement and how the data is arranged in the DataRAM.

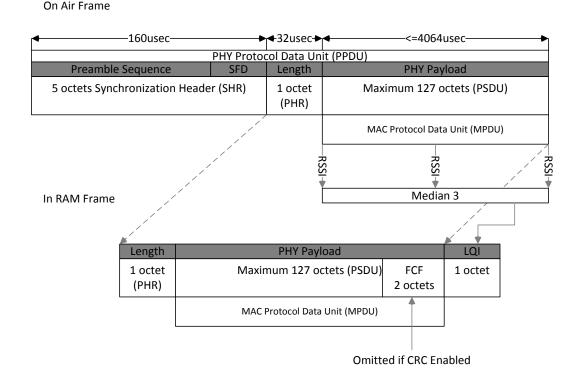


Figure 49: IEEE 802.15.4 Frame In DataRAM

A shortcut has been added between FRAMESTART event and the BCSTART task. This can be used to trig a BCMATCH event after N bits - such as when inspecting the MAC addressing fields.

22.12.8 Interframe Spacing

The IEEE 802.15.4 standard defines a specific time that is alotted for the MAC sublayer to process received data. Usage of this interframe spacing (IFS) comes into play to avoid that two frames are transmitted too close to eachother in time. If the a transmission is requesting an acknowledgement, the speration to the second frame shall be at least an IFS period.

The IFS is determined to be:

- IFS equals macMinSIFSPeriod (12 symbols) if the MPDU is less than or equal to aMaxSIFSFrameSize (18 octets) octets
- IFS equals macMinLIFSPeriod (40 symbols) if the MPDU is larger than aMaxSIFSFrameSize

The TIFS register must be manually updated by the user based upon the above mentioned length rules. *Figure 50: Interframe Spacing Examples* on page 265 provides further detail on what IFS period is valid in both acknowledged and unacknowledged transmissions.



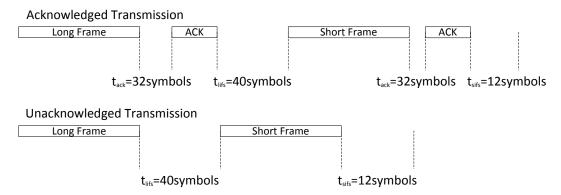


Figure 50: Interframe Spacing Examples

22.13 EasyDMA

The RADIO peripheral uses EasyDMA for reading of data packets from and writing to RAM, without CPU involvement.

As illustrated in *Figure 30: RADIO block diagram* on page 249, the RADIO's EasyDMA utilizes the same PACKETPTR for receiving and transmitting packets. This pointer should be reconfigured by the CPU each time before RADIO is started by the START task. Both the PACKETPTR and MAXLEN registers are double-buffered, meaning that they can be updated and prepared for the next transmission.

Important: If the PACKETPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The END event indicates that the last bit has been processed by the radio. The DISABLED event is issued to acknowledge that a DISABLE task is done.

The structure of a radio packet is described in detail in *Packet configuration* on page 249. The data that is stored in Data RAM and transported by EasyDMA consists of the following fields:

- S0
- LENGTH
- S1
- PAYLOAD

In addition, a static add-on is sent immediately after the payload.

The size of each of the above fields in the frame is configurable, and the space occupied in RAM depends on these settings. A size of zero is possible for any of the fields, it is up to the user to make sure that the resulting frame complies with the RF protocol chosen. All fields are extended in size to align with a byte boundary in RAM. For instance a 3 bit long field on air will occupy 1 byte in RAM while a 9 bit long field will be extended to 2 bytes.

The radio packet fields can be configured as follows:

- The fields CI, TERM1 and TERM2 are only present in Bluetooth Smart Long Range mode
- S0 is configured in the S0LEN field of the PCNF0 register
- LENGTH is configured in the LFLEN field of the PCNF0 register
- S1 is configured in the S1LEN field of the PCNF0 register
- The size of the payload is configured by the value in RAM corresponding to the LENGTH field
- The size of the static add-on to the payload is configured in the STATLEN field of the PCNF1 register

The MAXLEN field in the PCNF1 register configures the maximum packet payload plus add-on size in number of bytes that can be transmitted or received by the RADIO. This feature can be used to ensure that the RADIO does not overwrite, or read beyond, the RAM assigned to the packet payload. This means that if the packet payload length defined by the PCNF1.STATLEN and the LENGTH field in the packet specify a packet larger than MAXLEN, the payload will be truncated at MAXLEN. The packet's LENGTH field will not



be altered when the payload is truncated. The RADIO will calculate CRC as if the packet length is equal to MAXLEN.

Important: The MAXLEN includes the size of the payload and the add-on, but excludes the size occupied by the fields S0, LENGTH and S1. This has to be taken into account when allocating RAM.

22.14 Registers

Table 34: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40001000	RADIO	RADIO	2.4 GHz radio	

Table 35: Register Overview

Register	Offset	Description
TASKS_TXEN	0x000	Enable RADIO in TX mode
TASKS_RXEN	0x004	Enable RADIO in RX mode
TASKS_START	0x008	Start RADIO
TASKS_STOP	0x00C	Stop RADIO
TASKS_DISABLE	0x010	Disable RADIO
TASKS_RSSISTART	0x014	Start the RSSI and take one single sample of the receive signal strength.
TASKS_RSSISTOP	0x018	Stop the RSSI measurement
TASKS_BCSTART	0x01C	Start the bit counter
TASKS_BCSTOP	0x020	Stop the bit counter
TASKS_EDSTART	0x024	Start the Energy Detect measurement used in IEEE 802.15.4 mode
TASKS_EDSTOP	0x028	Stop the Energy Detect measurement
TASKS_CCASTART	0x02C	Start the Clear Channel Assessment used in IEEE 802.15.4 mode
TASKS_CCASTOP	0x030	Stop the Clear Channel Assessment
EVENTS_READY	0x100	RADIO has ramped up and is ready to be started
EVENTS_ADDRESS	0x104	Address sent or received
EVENTS_PAYLOAD	0x108	Packet payload sent or received
EVENTS_END	0x10C	Packet sent or received
EVENTS_DISABLED	0x110	RADIO has been disabled
EVENTS_DEVMATCH	0x114	A device address match occurred on the last received packet
EVENTS_DEVMISS	0x118	No device address match occurred on the last received packet
EVENTS_RSSIEND	0x11C	Sampling of receive signal strength complete.
EVENTS_BCMATCH	0x128	Bit counter reached bit count value.
EVENTS_CRCOK	0x130	Packet received with CRC ok
EVENTS_CRCERROR	0x134	Packet received with CRC error
EVENTS_FRAMESTART	0x138	IEEE 802.15.4 length field received
EVENTS_EDEND	0x13C	Sampling of Energy Detection complete. A new ED sample is ready for readout from the
_		RADIO.EDSAMPLE register
EVENTS_EDSTOPPED	0x140	The sampling of Energy Detection has stopped
EVENTS_CCAIDLE	0x144	Wireless medium in idle - clear to send
EVENTS_CCABUSY	0x148	Wireless medium busy - do not send
EVENTS_CCASTOPPED	0x14C	The CCA has stopped
EVENTS_RATEBOOST	0x150	Ble LR CI field received, receive mode is changed from Ble LR125Kbit to Ble LR500Kbit.
EVENTS TXREADY	0x154	RADIO has ramped up and is ready to be started TX path
EVENTS_RXREADY	0x158	RADIO has ramped up and is ready to be started RX path
EVENTS_MHRMATCH	0x15C	MAC Header match found.
EVENTS_PHYEND	0x16C	Generated in Ble_LR125Kbit, Ble_LR500Kbit and Bleleee802154_250Kbit modes when last bit is sent
		on air.
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CRCSTATUS	0x400	CRC status
RXMATCH	0x408	Received address
	5400	



Register	Offset	Description
RXCRC	0x40C	CRC field of previously received packet
DAI	0x410	Device address match index
PDUSTAT	0x414	Payload status
PACKETPTR	0x504	Packet pointer
FREQUENCY	0x508	Frequency
TXPOWER	0x50C	Output power
MODE	0x510	Data rate and modulation
PCNF0	0x514	Packet configuration register 0
PCNF1	0x518	Packet configuration register 1
BASE0	0x51C	Base address 0
BASE1	0x520	Base address 1
PREFIXO	0x524	Prefixes bytes for logical addresses 0-3
PREFIX1	0x528	Prefixes bytes for logical addresses 4-7
TXADDRESS	0x52C	Transmit address select
RXADDRESSES	0x530	Receive address select
CRCCNF	0x534	CRC configuration
CRCPOLY	0x538	CRC polynomial
CRCINIT	0x53C	CRC initial value
TIFS	0x544	Inter Frame Spacing in us
RSSISAMPLE	0x548	RSSI sample
STATE	0x550	Current radio state
DATAWHITEIV	0x554	Data whitening initial value
BCC	0x560	Bit counter compare
DAB[0]	0x600	Device address base segment 0
DAB[1]	0x604	Device address base segment 1
DAB[2]	0x608	Device address base segment 2
DAB[3]	0x60C	Device address base segment 3
DAB[4]	0x610	Device address base segment 4
DAB[5]	0x614	Device address base segment 5
DAB[6]	0x618	Device address base segment 6
DAB[7]	0x61C	Device address base segment 7
DAP[0]	0x620	Device address prefix 0
DAP[1]	0x624	Device address prefix 1
DAP[2]	0x628	Device address prefix 2
DAP[3]	0x62C	Device address prefix 3
DAP[4]	0x630	Device address prefix 4
DAP[5]	0x634	Device address prefix 5
DAP[6]	0x638	Device address prefix 6
DAP[7]	0x63C	Device address prefix 7
DACNF	0x640	Device address match configuration
MHRMATCHCONF	0x644	Search Pattern Configuration
MHRMATCHMAS	0x648	Pattern mask
MODECNF0	0x650	Radio mode configuration register 0
SFD	0x660	IEEE 802.15.4 Start of Frame Delimiter
EDCNT	0x664	IEEE 802.15.4 Energy Detect Loop Count
EDSAMPLE	0x668	IEEE 802.15.4 Energy Detect Level
CCACTRL	0x66C	IEEE 802.15.4 Clear Channel Assessment Control
POWER	0xFFC	Peripheral power control

22.14.1 SHORTS

Address offset: 0x200

Shortcut register



	iumbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	* 00	000000			UTSRQPONMLK H GFEDCBA
Id		0000000 Field	Value Id	Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
A		READY_START	value lu	value	Shortcut between READY event and START task
	-				
			Disabled	0	See EVENTS_READY and TASKS_START Disable shortcut
			Enabled	1	Enable shortcut
В	RW	END_DISABLE	Lilabica	1	Shortcut between END event and DISABLE task
			Disabled	0	See EVENTS_END and TASKS_DISABLE Disable shortcut
			Enabled	1	Enable shortcut
С	RW	DISABLED_TXEN	Eliablea	-	Shortcut between DISABLED event and TXEN task
			Disabled	0	See EVENTS_DISABLED and TASKS_TXEN Disable shortcut
			Disabled Enabled	1	Enable shortcut
D	RW	DISABLED_RXEN	Lilabica	1	Shortcut between DISABLED event and RXEN task
_		J.07.1022.0			
			Disabled	0	See EVENTS_DISABLED and TASKS_RXEN
			Disabled Enabled	0 1	Disable shortcut Enable shortcut
E	RW/	ADDRESS RSSISTART	Ellabled	1	Shortcut between ADDRESS event and RSSISTART task
-		7,001,000 THE			
			Disabled	0	See EVENTS_ADDRESS and TASKS_RSSISTART
			Disabled Enabled	0 1	Disable shortcut Enable shortcut
F	RW	END_START	Lilabled	1	Shortcut between END event and START task
•					
			Disabled	0	See EVENTS_END and TASKS_START
			Disabled Enabled	0 1	Disable shortcut Enable shortcut
G	RW	ADDRESS_BCSTART	Lilabled	1	Shortcut between ADDRESS event and BCSTART task
•		7.55.1.265_565.7			
			6: 11 1		See EVENTS_ADDRESS and TASKS_BCSTART
			Disabled Enabled	0 1	Disable shortcut Enable shortcut
Н	RW	DISABLED RSSISTOP	Lilabled	1	Shortcut between DISABLED event and RSSISTOP task
		013/10220_113313101			
			Disabled	0	See EVENTS_DISABLED and TASKS_RSSISTOP Disable shortsut
			Disabled Enabled	0 1	Disable shortcut Enable shortcut
K	RW	RXREADY_CCASTART	Lilabled	1	Shortcut between RXREADY event and CCASTART task
			Disabled	0	See EVENTS_RXREADY and TASKS_CCASTART Disable shortcut
			Enabled	1	Enable shortcut
L	RW	CCAIDLE_TXEN	Endoica	-	Shortcut between CCAIDLE event and TXEN task
			Disabled	0	See EVENTS_CCAIDLE and TASKS_TXEN Disable shortcut
			Enabled	1	Enable shortcut
М	RW	CCABUSY_DISABLE	Eliablea	-	Shortcut between CCABUSY event and DISABLE task
			Disabled	0	See EVENTS_CCABUSY and TASKS_DISABLE Disable shortcut
			Enabled	1	Enable shortcut
N	RW	FRAMESTART_BCSTART	z.idoled	•	Shortcut between FRAMESTART event and BCSTART task
	•				
			Disabled	0	See EVENTS_FRAMESTART and TASKS_BCSTART Disable chartcut
			Disabled Enabled	0 1	Disable shortcut Enable shortcut
0	RW/	READY_EDSTART	Lilabicu	1	Shortcut between READY event and EDSTART task
,					
					See EVENTS_READY and TASKS_EDSTART



Bitı	number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				UTSRQPONMLK H GFEDCBA
Res	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
Р	RW EDEND_DISABL	E		Shortcut between EDEND event and DISABLE task
				See EVENTS_EDEND and TASKS_DISABLE
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
Q	RW CCAIDLE_STOP			Shortcut between CCAIDLE event and STOP task
				See EVENTS_CCAIDLE and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
R	RW TXREADY_STAR	Т		Shortcut between TXREADY event and START task
				See EVENTS_TXREADY and TASKS_START
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
S	RW RXREADY_STAF		-	Shortcut between RXREADY event and START task
		8: 11 1	•	See EVENTS_RXREADY and TASKS_START
		Disabled	0	Disable shortcut Enable shortcut
Т	RW PHYEND DISAE	Enabled	1	Shortcut between PHYEND event and DISABLE task
ı	KW PHYEND_DISAE	ole.		SHOULD BETWEEN LUIEND SAELT AND DISABLE 1928
				See EVENTS_PHYEND and TASKS_DISABLE
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
U	RW PHYEND_STAR	Ī		Shortcut between PHYEND event and START task
				See EVENTS_PHYEND and TASKS_START
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut

22.14.2 INTENSET

Address offset: 0x304

Enable interrupt



Bit n	iumbe	er		31 30	29 28	27 2	16 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id						Z		VUTSRQPONMLK I HGFEDCBA
Rese	et 0x0	0000000		0 0	0 0	0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
								See EVENTS_END
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled
Ε	RW	DISABLED						Write '1' to Enable interrupt for DISABLED event
								See EVENTS_DISABLED
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled
F	RW	DEVMATCH						Write '1' to Enable interrupt for DEVMATCH event
								See EVENTS_DEVMATCH
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled
G	RW	DEVMISS						Write '1' to Enable interrupt for DEVMISS event
			6.1					See EVENTS_DEVMISS
			Set	1				Enable Part Dischlad
			Disabled	0				Read: Disabled
Н	D\A/	RSSIEND	Enabled	1				Read: Enabled Write '1' to Enable interrupt for RSSIEND event
П	NVV	KOSIEND						write 1 to Enable interrupt for NSSIEND event
								See EVENTS_RSSIEND
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled
I	RW	BCMATCH						Write '1' to Enable interrupt for BCMATCH event
								See EVENTS_BCMATCH
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled
K	RW	CRCOK						Write '1' to Enable interrupt for CRCOK event
								See EVENTS_CRCOK
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled
L	RW	CRCERROR						Write '1' to Enable interrupt for CRCERROR event
								See EVENTS_CRCERROR
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled
М	RW	FRAMESTART						Write '1' to Enable interrupt for FRAMESTART event
								See EVENTS_FRAMESTART
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled
N	RW	EDEND		_				Write '1' to Enable interrupt for EDEND event
	-							
			C-1	4				See EVENTS_EDEND
			Set	1				Enable Part Dischlad
			Disabled	0				Read: Disabled
0	DVA	EDSTORRED	Enabled	1				Read: Enabled Write '1' to Enable interrupt for EDSTORRED event
0	KW	EDSTOPPED						Write '1' to Enable interrupt for EDSTOPPED event
								See EVENTS_EDSTOPPED



Bit n	umber		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			Z	V U T S R Q P O N M L K I H G F E D C B A
Rese	t 0x00000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW Field	Value Id	Value	Description
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Р	RW CCAIDLE			Write '1' to Enable interrupt for CCAIDLE event
				See EVENTS_CCAIDLE
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Q	RW CCABUSY			Write '1' to Enable interrupt for CCABUSY event
				See EVENTS_CCABUSY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
R	RW CCASTOPPED			Write '1' to Enable interrupt for CCASTOPPED event
				See EVENTS_CCASTOPPED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
S	RW RATEBOOST		_	Write '1' to Enable interrupt for RATEBOOST event
				·
		Cat	1	See EVENTS_RATEBOOST Enable
		Set Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Т	RW TXREADY	Lilableu	1	Write '1' to Enable interrupt for TXREADY event
·	TAILERD !			
				See EVENTS_TXREADY
		Set	1	Enable
		Disabled	0	Read: Disabled
	DIAL DVDEADV	Enabled	1	Read: Enabled
U	RW RXREADY			Write '1' to Enable interrupt for RXREADY event
				See EVENTS_RXREADY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
V	RW MHRMATCH			Write '1' to Enable interrupt for MHRMATCH event
				See EVENTS_MHRMATCH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Z	RW PHYEND			Write '1' to Enable interrupt for PHYEND event
				See EVENTS_PHYEND
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

22.14.3 INTENCLR

Address offset: 0x308 Disable interrupt



Bit r	number	31 30 29 2	28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			Z	V U T S R Q P O N M L K I H G F E D C B A
Res	set 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field Value	d Value		Description
Α	RW READY			Write '1' to Disable interrupt for READY event
				See EVENTS_READY
	Clear	1		Disable
	Disable			Read: Disabled
_	Enable	d 1		Read: Enabled
В	RW ADDRESS			Write '1' to Disable interrupt for ADDRESS event
				See EVENTS_ADDRESS
	Clear	1		Disable
	Disable			Read: Disabled
_	Enable	d 1		Read: Enabled
С	RW PAYLOAD			Write '1' to Disable interrupt for PAYLOAD event
				See EVENTS_PAYLOAD
	Clear			Disable
	Disable			Read: Disabled
_	Enable	d 1		Read: Enabled
D	RW END			Write '1' to Disable interrupt for END event
				See EVENTS_END
	Clear			Disable
	Disable			Read: Disabled
E	RW DISABLED	d 1		Read: Enabled Write '1' to Disable interrupt for DISARIED event
_	NW DISABLED			Write '1' to Disable interrupt for DISABLED event
				See EVENTS_DISABLED
	Clear	1		Disable
	Disable			Read: Disabled
F	RW DEVMATCH	d 1		Read: Enabled Write '1' to Disable interrupt for DEVMATCH event
•	NW DEVINATEIT			
	_			See EVENTS_DEVMATCH
	Clear	1		Disable
	Disable Enable			Read: Disabled Read: Enabled
G	RW DEVMISS	, 1		Write '1' to Disable interrupt for DEVMISS event
Ü	NV DEVIVISS			
	Class	4		See EVENTS_DEVMISS
	Clear Disable	1 ed 0		Disable Read: Disabled
	Enable			Read: Enabled
Н	RW RSSIEND	- -		Write '1' to Disable interrupt for RSSIEND event
	Clear	1		See EVENTS_RSSIEND Disable
	Disable			Read: Disabled
	Enable			Read: Enabled
ı	RW BCMATCH			Write '1' to Disable interrupt for BCMATCH event
				See EVENTS_BCMATCH
	Clear	1		Disable
	Disable			Read: Disabled
	Enable			Read: Enabled
K	RW CRCOK			Write '1' to Disable interrupt for CRCOK event
				See EVENTS_CRCOK
	Clear	1		Disable
	Disable			Read: Disabled
	Enable			Read: Enabled
L	RW CRCERROR			Write '1' to Disable interrupt for CRCERROR event



Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		Z Z	V U T S R Q P O N M L K I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
			See EVENTS_CRCERROR
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
M RW FRAMESTART			Write '1' to Disable interrupt for FRAMESTART event
			See EVENTS_FRAMESTART
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
N RW EDEND			Write '1' to Disable interrupt for EDEND event
			See EVENTS_EDEND
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
O RW EDSTOPPED			Write '1' to Disable interrupt for EDSTOPPED event
			See EVENTS_EDSTOPPED
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
P RW CCAIDLE			Write '1' to Disable interrupt for CCAIDLE event
			See EVENTS_CCAIDLE
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
Q RW CCABUSY			Write '1' to Disable interrupt for CCABUSY event
			See EVENTS_CCABUSY
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
R RW CCASTOPPED			Write '1' to Disable interrupt for CCASTOPPED event
			See EVENTS_CCASTOPPED
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
S RW RATEBOOST			Write '1' to Disable interrupt for RATEBOOST event
			See EVENTS_RATEBOOST
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
T RW TXREADY			Write '1' to Disable interrupt for TXREADY event
			See EVENTS_TXREADY
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
U RW RXREADY			Write '1' to Disable interrupt for RXREADY event
	Clear	1	See EVENTS_RXREADY Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
V RW MHRMATCH			Write '1' to Disable interrupt for MHRMATCH event
			•

See EVENTS_MHRMATCH



Bit number		31	1 30	29 :	28 2	7 2	26 2	25 2	4 2	3 22	21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id					2	<u> </u>			١	/ U	Т	S	R	Q	Р	О	N	М	L	K	- 1			Н	G	F	Е	D C	В	Α
Reset 0x00000000		0	0	0	0 () (0 (0 (0 (0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0
Id RW Field	Value Id	Va	alue						D	escr	ipti	on																		
	Clear	1							D	isab	le																			
	Disabled	0							R	ead:	Dis	abl	ed																	
	Enabled	1							R	ead:	En	able	ed																	
Z RW PHYEND									٧	Vrite	'1'	to [Disa	ble	int	erru	ıpt	for	PHY	ENC	ev	ent								
									S	ee <i>E</i>	VEN	ITS_	_PH	IYEI	VD															
	Clear	1							D	isab	le																			
	Disabled	0							R	ead:	Dis	abl	ed																	
	Enabled	1							R	ead:	En	able	ed																	

22.14.4 CRCSTATUS

Address offset: 0x400

CRC status

Bit	numb	er		31	30 :	29 2	28 2	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	. 10	9	8	7	6	5	4	3	2 :	1 0
Id																																		Α
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Val	ue							De	scr	ipti	on																			
Α	R	CRCSTATUS										CR	C s	tatı	ıs o	f pa	cke	et re	ece	ive	d													
			CRCError	0								Pa	cke	t re	cei	ved	wi	h C	RC	er	or													
			CRCOk	1								Pa	cke	t re	cei	ved	wi	h C	RC	ok														

22.14.5 RXMATCH

Address offset: 0x408 Received address

Bitı	numbe	er		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A A A
Res	et 0x0	0000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value	Description
Α	R	RXMATCH			Received address

Logical address of which previous packet was received

22.14.6 RXCRC

Address offset: 0x40C

CRC field of previously received packet

Bit r	numbe	er		31	30 2	9 :	28 2	27 2	26 2	25 2	24 2	23 2	22 2	21 2	20 :	19 1	L8 1	17 1	16 1	15 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id												A .	Α	Α	Α	Α.	Α.	Α,	Α.	A A	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А	. A	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	R	RXCRC									(CRC	fie	ld c	of p	revi	ous	sly r	ece	ive	d pa	cket											

CRC field of previously received packet

22.14.7 DAI

Address offset: 0x410

Device address match index



Bit	numbe	r		3	1 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8 7	7 6	5 5	5 4	3	2	1	0
Id																																Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () () (0	0	0	0
Id	RW	Field	Value Id	٧	alue	9						De	scri	ptic	on																			
Α	R	DAI										De	vice	ad	dre	ss n	nate	ch i	nde	x														
													dex (dres	` ′			ce a	ddı	ress	s, se	ee C	DAB	[n]	and	d DA	νP[r	n], tl	nat	got	an				

22.14.8 PDUSTAT

Address offset: 0x414

Payload status

Bi	t numbe	er		31	30 2	9 2	28 2	7 2	26 2	5 2	24	23	22	21 2	0 1	19 1	8 1	l7 1	6 1	5 1	4 1	3 12	2 11	. 10	9	8	7	6	5	4	3 2	2 1	0
Id																															В	3 B	ВА
R	set 0x0	0000000		0	0 (0	0 0	0	0 (0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Val	ıe							Des	cri	ptio	n																		
Α	R	PDUSTAT									:	Sta	tus	on p	ay	load	l le	ngtl	ı vs	. PC	NF	1.M	ΑXΙ	.EN									
			LessThan	0								Pay	loa	d les	s t	han	PC	NF1	.M	AXL	ΕN												
			GreaterThan	1								Pay	loa	d gr	eat	er t	har	n PC	NF:	1.M	AXL	.EN											
В	R	CISTAT										Sta	tus	on v	vha	at ra	te	pac	ket	is re	ecei	ived	wi	th in	Lo	ng F	Ran	ge					
			LR125kbit	0								Fra	me	is re	cei	ived	at	125	kbį	os													
			LR500kbit	1								Fra	me	is re	cei	ived	at	500	kbį	os													
			GreaterThan LR125kbit	1							:	Pay Pay Stat	loa loa tus me	d les	ss t eat vha	han er t at ra	PC har te at	:NF1 n PC pacl	NF: ket kbj	AXL 1.M is re	EN AXL	.EN			ı Lo	ng F	Ran	ge					

22.14.9 PACKETPTR

Address offset: 0x504

Packet pointer

Bit	numbe	er		31	L 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17 :	16	15 3	14 :	13 1	2 1	1 10	9	8	7	6	5	4	3 2	2 2	1 0
Id				Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																		
Α	RW	PACKETPTR										Pad	cket	t po	int	er																	
												Pad	cket	t ad	dre	ess t	o b	e us	ed	for	the	ne	xt tı	ans	miss	sion	or						
												rec	ept	ion	. W	hen'	tra	ansr	nitt	ting	, th	е ра	icke	t pc	inte	d to	b by	/ thi	is				
												ado	dres	ss w	/ill l	be t	ran	smi	tte	d an	nd v	vhe	n re	ceiv	ing,	the	red	ceiv	ed				
												pac	cket	t wil	ll b	e wi	ritte	en t	o tl	nis a	dd	ress	. Th	is a	ddre	ess i	s a	byte	e				
												alig	gne	d ra	m	add	res	s.															

22.14.10 FREQUENCY

Address offset: 0x508

Frequency

Bit number		31	. 30	29	28	27	26 2	25 2	24 2	23 2	22	21	20	19	18	17	16	15	14	13	12	11	. 10	9	8	7	6	5	4	3	2	1	0
Id																									В		Α	Α	Α	Α	Α	Α	Α
Reset 0x00000002		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Id RW Field	Value Id	Va	lue							Des	cri	ptic	n																				
A RW FREQUENCY		[0.	10	0]					F	Rad	lio	cha	nne	el fr	eqı	uen	су																
									F	Fred	que	ency	/=:	240	00 +	FR	EQ	UE	NC	′ (N	1Hz).											
B RW MAP									(Cha	nn	el n	пар	se	lect	ion	١.																
	Default	0							(Cha	nn	el n	пар	be	twe	een	24	00	MF	IZ	25	00	МН	Z									
									F	Fred	que	ency	/=:	240	00 +	FR	EQ	UE	NC	′ (N	1Hz)											
	Low	1							(Cha	nn	el n	пар	be	twe	een	23	60	MF	IZ	24	60	МН	Z									
									F	Fred	que	ency	/=:	236	60 +	FR	EQ	UE	NC	′ (N	1Hz)											



22.14.11 TXPOWER

Address offset: 0x50C

Output power

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3	2 1 0
Id		АААА	A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0
Id RW Field	Value Id	Value Description	
A RW TXPOWER		RADIO output power.	
		Output power in number of dBm, i.e. if the value -20 is specified	
		the output power will be set to -20dBm.	
		• •	
	Pos8dBm	0x8 +8 dBm	
	Pos7dBm	0x7 +7 dBm	
	Pos6dBm	0x6 +6 dBm	
	Pos5dBm	0x5 +5 dBm	
	Pos4dBm	0x4 +4 dBm	
	Pos3dBm	0x3 +3 dBm	
	Pos2dBm	0x2 +2 dBm	
	0dBm	0x0 0 dBm	
	Neg4dBm	0xFC -4 dBm	
	Neg8dBm	0xF8 -8 dBm	
	Neg12dBm	0xF4 -12 dBm	
	Neg16dBm	0xF0 -16 dBm	
	Neg20dBm	0xEC -20 dBm	
	Neg30dBm	0xD8 -40 dBm De	eprecated
	Neg40dBm	0xD8 -40 dBm	

22.14.12 MODE

Address offset: 0x510

Data rate and modulation

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW MODE	Radio data rate and modulation setting. The radio supports
	Frequency-shift Keying (FSK) modulation.
Nrf_1Mbit	0 1 Mbit/s Nordic proprietary radio mode
Nrf_2Mbit	1 2 Mbit/s Nordic proprietary radio mode
Ble_1Mbit	3 1 Mbit/s Bluetooth Low Energy
Ble_2Mbit	4 2 Mbit/s Bluetooth Low Energy
Ble_LR125Kbit	5 Long range 125 kbit/s (TX Only - RX supports both)
Ble_LR500Kbit	6 Long range 500 kbit/s (TX Only - RX supports both)
leee802154_250Kl	it 15 IEEE 802.15.4-2006 250 kbit/s

22.14.13 PCNF0

Address offset: 0x514

Packet configuration register 0

Bit r	numbe	er		31	L 30	29	28	3 27	26	25	24	23	22 2	1 2	0 19	9 18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id					J	J			-1	Н	Н	G	G		E	Ε	Ε	Ε								С					Α	A ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							De	scrip	tio	1																		
Α	RW	LFLEN										Ler	igth	on a	air o	f LE	NG	TH 1	field	l in	nur	nbe	r o	f bit	s.								
С	RW	SOLEN										Ler	igth	on a	air o	f SC	fie	ld ir	า ทน	ımb	er o	of b	yte	s.									
Ε	RW	S1LEN										Ler	igth	on a	air o	f S1	fie	ld ir	า ทน	ımb	er	of b	its.										



Bit r	number			3	1 30	29	28 2	27 2	6 2	5 24	4 23	3 22	21	20 2	19 1	18 1	17 1	16 1	.5 1	4 1	3 12	11	10	9 8	3 7	6	5	4	3	2 1	0
Id					J	J			I F	1 Н	1 6	G		F	E I	E	Е	E						(2				A A	4 А	Α
Res	et 0x000000	0		0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0 (0	0	0	0	0 (0 0	0
Id	RW Field		Value Id	٧	alue						D	escr	iptic	on																	
F	RW S1INC	-									In	clud	e or	exc	lud	e S	1 fie	eld	in R	AM											
			Automatic	0							In	clud	e S1	l fie	ld ir	n RA	AΜ	onl	y if	S1LI	N >	0									
			Include	1							Α	lway	s in	clud	e S1	1 fie	eld i	n R	ΑM	ind	epei	nder	nt of	S1l	.EN						
G	RW CILEN										Le	engt	n of	Cod	le In	ndic	ato	r - I	on	g Ra	nge										
Н	RW PLEN										Le	engt	h of	pre	amb	ble	on a	air.	Dec	isio	n po	int:	TAS	KS_	STAF	RT ta	sk				
			8bit	0							8-	-bit p	rea	mbl	e																
			16bit	1							16	6-bit	pre	aml	ole																
			32bitZero	2							32	2-bit	zer	o pr	ean	nble	e - ι	ısed	d fo	rIEE	E 80	2.1	5.4								
			LongRange	3							Pı	rean	ıble	- us	ed f	for	BTL	E L	ong	Rar	ge										
T	RW CRCIN	С									In	dica	tes	if LE	NG	TH	field	d cc	nta	ins	CRC	or n	ot								
			Exclude	0							LE	NG	ΓH d	oes	not	t co	nta	in C	RC												
			Include	1							LE	NG	ΓH ir	nclu	des	CR	С														
J	RW TERM	.EN									Le	engt	h of	TER	M f	ielo	d in	Lor	ıg R	ang	е ор	erat	ion								

22.14.14 PCNF1

Address offset: 0x518

Packet configuration register 1

Bit	numbe	er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E 1	C C C B B B B B B B A A A A A A A
Res	et 0x0	0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	MAXLEN		[0255]	Maximum length of packet payload. If the packet payload is
					larger than MAXLEN, the radio will truncate the payload to
					MAXLEN.
В	RW	STATLEN		[0255]	Static length in number of bytes
					The static length parameter is added to the total length of the
					payload when sending and receiving packets, e.g. if the static
					length is set to N the radio will receive or send N bytes more
					than what is defined in the LENGTH field of the packet.
С	D\A/	BALEN		[24]	Base address length in number of bytes
C	11.00	DALLIN		[24]	base address length in number of bytes
					The address field is composed of the base address and the one
					byte long address prefix, e.g. set BALEN=2 to get a total address
					of 3 bytes.
D	RW	ENDIAN			On air endianness of packet, this applies to the SO, LENGTH, S1
					and the PAYLOAD fields.
			Little	0	Least Significant bit on air first
			Big	1	Most significant bit on air first
Е	RW	WHITEEN			Enable or disable packet whitening
			Disabled	0	Disable
			Enabled	1	Enable

22.14.15 BASE0

Address offset: 0x51C

Base address 0

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 :	L3 1	L2 1	111	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	. Α	Α	Α	Α	Α	Α	Α	Α	А А
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	BASE0										Bas	se a	ddr	ess	0																	

Radio base address 0.



22.14.16 BASE1

Address offset: 0x520

Base address 1

Bit r	numbe	er		31 30	29 2	8 2	7 26	25	24	23	22 2	1 2	0 19	18	17	16 1	L5 1	4 13	12	11	10	9	8	7	6	5 4	4 3	2	1	0
Id				A A	A	Α Α	A	Α	Α	Α	A A	۸ ۸	A A	Α	Α	A	A A	A	Α	Α	Α	Α	Α	Α	Α	A	Δ Δ	A	Α	Α
Res	et 0x0	0000000		0 0	0	0 0	0	0	0	0	0 () (0 0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Value						Des	crip	tior	1																	
Α	RW	BASE1								Bas	e ad	dre	ss 1																	

Radio base address 1.

22.14.17 PREFIX0

Address offset: 0x524

Prefixes bytes for logical addresses 0-3

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	В	В	В	В	В	В	В	В	Δ.	Α	Α	Α	A A	A 4	4 A
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	AP0		Value Description Address pr																														
В	RW	AP1										Ad	dre	ss p	ref	ix 1																		
С	RW	AP2										Ad	dre	ss p	ref	ix 2																		
D	RW	AP3										Ad	dre	ss p	ref	ix 3																		

22.14.18 PREFIX1

Address offset: 0x528

Prefixes bytes for logical addresses 4-7

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 :	20 1	19 :	18	17	16	15	14	13	12	11 :	10	9 8	3 7	' 6	5	4	3	2	1 (ĺ
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	В	В	В	В	В	В	В	3 /	Α Α	. A	. Α	Α	Α	A	ĺ
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0 (l
Id	RW	Field	Value Id	Va	alue	:						Des	scrip	otio	n																			l
Α	RW	AP4		Value Description Address prefix 4. Address prefix 4.																			1											
В	RW	AP5		·																														
С	RW	AP6										Add	dres	s p	refi	x 6.																		
D	RW	AP7										Add	dres	s p	refi	x 7.																		

22.14.19 TXADDRESS

Address offset: 0x52C
Transmit address select

Bit	numbe	er		31	30	29	28	3 27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	.0 9	9 ;	3 7	7 (5 5	5 4	1 3	2	1	0
Id																																Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 () (0) (0	0	0	0
Id	RW	Field	Value Id	Va	lue	•						De	scri	ptic	on																			
Α	RW	TXADDRESS										Tra	nsn	nit	add	Ires	s se	elec	:t															

 $\label{logical} \mbox{Logical address to be used when transmitting a packet}.$

22.14.20 RXADDRESSES

Address offset: 0x530 Receive address select



Bit r	numbe	er		31 3	0 29	9 28	27	26 2	25 2	4 23	3 22	2 21	20	19	18	17	16	15 1	L4 1	3 12	11	10	9	8 7	' (5 5	4	3	2	1 0
Id																								H	1 (6 F	Ε	D	C I	ВА
Res	et 0x0	0000000		0 (0 0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0 0) (0	0	0	0 (0 0
Id	RW	Field	Value Id	Valu	e					D	esc	ripti	on																	
Α	RW	ADDR0								Er	nab	le or	r di:	sab	le r	ecep	otio	n or	log	ical a	nddr	ess	0.							
			Disabled	0						Di	isab	ole																		
			Enabled	1						Er	nab	le																		
В	RW	ADDR1								Er	nab	le or	r di:	sab	le r	ecep	otio	n or	log	ical a	addı	ess	1.							
			Disabled	0						Di	isab	ole																		
			Enabled	1						Er	nab	le																		
С	RW	ADDR2								Er	nab	le or	r di	sab	le r	ecep	tio	n or	log	ical a	addı	ess	2.							
			Disabled	0						Di	isab	ole																		
			Enabled	1						Er	nab	le																		
D	RW	ADDR3								Er	nab	le or	r di	sab	le r	ecep	otio	n or	log	ical a	addı	ess	3.							
			Disabled	0						Di	isab	ole																		
			Enabled	1						Er	nab	le																		
Ε	RW	ADDR4								Er	nab	le or	r di	sab	le r	ecep	otio	n or	log	ical a	addı	ess	4.							
			Disabled	0						Di	isab	ole																		
			Enabled	1						Er	nab	le																		
F	RW	ADDR5								Er	nab	le or	r di	sab	le r	ecep	otio	n or	log	ical a	nddi	ess	5.							
			Disabled	0						Di	isab	ole																		
			Enabled	1						Er	nab	le																		
G	RW	ADDR6								Er	nab	le or	r di	sab	le r	ecep	otio	n or	log	ical a	addı	ess	6.							
			Disabled	0						Di	isab	ole																		
			Enabled	1						Er	nab	le																		
Н	RW	ADDR7								Er	nab	le or	r di	sab	le r	ecep	otio	n or	log	ical a	addı	ess	7.							
			Disabled	0						Di	isab	ole																		
			Enabled	1						Er	nab	le																		

22.14.21 CRCCNF

Address offset: 0x534 CRC configuration

Bitı	numbe	er		31	30 2	29 28	3 27	26	25 2	24 2	23 2	2 21	20	19	18	17 :	16 :	15 1	4 1	3 12	11	10	9	8 7	6	5	4	3	2 1	. 0
Id																							В	В					Δ	АА
Res	et 0x0	0000000		0	0	0 0	0	0	0 (0 (0 (0 0	0	0	0	0	0	0 (0	0	0	0	0	0 0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Va	lue					C	Desc	ripti	ion																	
Α	RW	LEN		[1.	.3]					C	CRC	leng	th i	n nu	ımb	er o	f by	ytes												
													N	Note	: F	or N	100	DE B	le_L	R12	5Kb	it an	d B	le_L	R50	0Kb	it,			
													0	only	LEN	set	to	3 is	sup	port	ed									
			Disabled	0						C	CRC	leng	th is	s zei	ro a	nd (CRC	cal	cula	tion	is d	isab	ed							
			One	1						C	CRC	leng	th is	s on	e b	/te a	and	CR	C ca	cula	tior	ı is e	nal	oled						
			Two	2						C	CRC	leng	th is	s tw	o b	ytes	an	d CF	C c	alcu	latic	n is	ena	bled	i					
			Three	3						C	CRC	leng	th is	s thr	ree	byte	es a	nd (CRC	calc	ulat	ion i	s ei	nable	ed					
В	RW	SKIPADDR								- b	nclu	ıde c	or ex	xclu	de p	ack	et a	addı	ess	field	d ou	t of	CRC	cal	cula	tion				
			Include	0						C	CRC	calcı	ulat	ion	incl	ude	s ac	ldre	ss f	eld										
			Skip	1						C	CRC	calcı	ulat	ion	doe	s no	ot ir	ıclu	de a	ddr	ess f	ield.	Th	e CR	С					
										С	alcu	ulatio	on v	will s	tar	at	the	firs	t by	te a	fter	the	add	ress						
			leee802154	2						C	CRC	calcı	ulat	ion	as p	er 8	302.	15.	4 sta	nda	ırd.	Star	ing	at f	irst	byte	9			
										a	fter	r len	gth	field	d.															

22.14.22 CRCPOLY

Address offset: 0x538 CRC polynomial



Bit	numb	er		31	. 30	29	28	27 :	26 2	25 2	4 23	3 22	21	20	19	18	17	16	15 1	L4 1	3 12	11	10	9	8	7	6	5	4	3 2	2	1 0
Id											Д	A	Α	Α	Α	Α	Α	Α	A .	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α /	А А
Res	et 0x0	0000000		0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																		
Α	RW	CRCPOLY									CI	RC p	olyr	non	nial																	
											re le ni Th	egist ast : umb	er w sign er C	vhich ifica of win	ch in ant the g ex	teri reg	x co m/b giste ple	rres it is er co	spor har	nds t nds t rd-w ent i n 8 b	o th ired s ign	ie te lint nore	erm erna d by	's ex ally y th	kpo to 1 e ha	nen L, ar ardv	t. T nd l war	oit e.				

22.14.23 CRCINIT

Address offset: 0x53C

CRC initial value

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۱,	А А
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	CRCINIT										CR	Cin	itia	l va	lue																		

Initial value for CRC calculation.

22.14.24 TIFS

Address offset: 0x544

Inter Frame Spacing in us

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Reset 0x00000000	Value Id	A A A A A A A A A A A A A A A A A A A
A RW TIFS	value iu	Inter Frame Spacing in us Inter frame space is the time interval between two consecutive packets. It is defined as the time, in micro seconds, from the end of the last bit of the previous packet to the start of the first bit of the subsequent packet.

22.14.25 RSSISAMPLE

Address offset: 0x548

RSSI sample

Bit	numb	er		31	. 30	29	28	27	26	25 :	24	23 2	22 2	21 2	20 1	19 1	L8 1	17 1	16	15	14 :	L3 1	2 1	1 10	9	8	7	6	5	4	3	2	1	0
Id																												Α	Α	Α	Α	Α	Α	Α
Re	set 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			
Α	R	RSSISAMPLE		[0	12	7]						RSS	l sa	mp	le																			
																							-	ster				•		ve				
												valu	ie w	vhil	e th	ie a	ctu	al r	ece	ive	d si	gna	l str	engt	h is	a n	ega	itive	9					
												valu	ıe. A	4ctı	ual	rece	eive	ed s	ign	al s	trei	ngth	is t	here	efor	e as	fol	low	/s:					
												rece	eive	d si	igna	al st	ren	igth	1 = -	A c	lBm													

22.14.26 STATE

Address offset: 0x550 Current radio state



Bit nun	nber			31	30 2	9 2	8 27	26	25 2	4 2	3 22	2 21 2	20 1	19 1	18 1	7 16	15	14	13 1	.2 11	. 10	9	8	7	6	5	4 3 <i>A</i>	3 2 A A		0 A
Reset (0x00	000000		0	0 (0	0	0	0 (0 (0 0	0	0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0
ld R	w	Field	Value Id	Va	lue					D	escr	riptio	n																	
A R	ł	STATE								С	urre	nt ra	dio	sta	te															
			Disabled	0						R	ADIO	o is ir	n th	e D	isab	led :	stat	е												
			RxRu	1						R	ADIO	o is ir	n th	e R	XRU	sta	:e													
			RxIdle	2						R	ADIO	o is ir	n th	e R	XIDL	E st	ate													
			Rx	3						R	ADIO	o is ir	n th	e R	X sta	ite														
			RxDisable	4						R	ADIO	o is ir	n th	e R	XDIS	ABL	ED:	state	9											
			TxRu	9						R	ADIO	o is ir	n th	e T	KRU	stat	e													
			TxIdle	10						R	ADIO	o is ir	n th	e T	KIDL	E st	ate													
			Tx	11						R	ADIO	O is ir	n th	e T	K sta	te														
			TxDisable	12						R	ADIO	o is ir	n th	e T	KDIS	ABL	ED :	state	9											

22.14.27 DATAWHITEIV

Address offset: 0x554

Data whitening initial value

Bit r	iumbe	r		31	. 30	29	28	3 27	' 26	25	24	23	3 22	2 2:	1 2	0 1	19	18	17	7 10	5 1	5 3	L4	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000040		0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	(0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	escr	ript	tio	n																					
Α	RW	DATAWHITEIV										Da	ata	wh	iite	nir	ng i	init	ial	val	ue	. В	it 6	is	har	d-v	vire	d t	o '1	', w	riti	ng '	0'				
												to	it h	has	no	ef	ffe	ct,	an	d it	wi	II a	lw	ays	be	re	ad I	oac	k ar	ıd u	isec	d by	/				
												th	e d	evi	ice	as	'1'																				
												Bit	t 0	cor	rres	spc	ond	ls t	o F	osi	itic	n 6	o of	th	e L	SFF	R, B	it 1	to I	os	itio	n 5,	,				
												et	c.																								

22.14.28 BCC

Address offset: 0x560 Bit counter compare

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 1	16 1	15 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A .	4 Α	A A	A A	A	Α	Α	Α	Α	Α	Α	А А	A	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
Α	RW	ВСС										Bit	cou	ınte	r co	omp	oare	e															

Bit counter compare register

22.14.29 DAB[0]

Address offset: 0x600

Device address base segment 0

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 1	LO	9	8	7	6	5	4	3 2	1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α	Α	Α	Α	Α	Α	A A	. 4	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	cri	ptic	on																			
Α	RW	DAB										Dev	/ice	ad	dre	ss b	ase	e se	gme	ent	0													

22.14.30 DAB[1]

Address offset: 0x604

Device address base segment 1



Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	DAB										De	vice	ad	dre	ss b	ase	se	gm	ent	1													

22.14.31 DAB[2]

Address offset: 0x608

Device address base segment 2

Bit n	iumbe	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20 :	19 1	8 1	L7 1	16 1	15 1	14 1	13 1	2 :	11 :	.0	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α,	Α,	Α.	Α.	Α	A	Α	Α	Δ,	Α	Α	Α	Α	Α	Α	A A	A 4	4 А
Rese	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																			
Α	RW	DAB										Dev	/ice	ado	dres	ss b	ase	seg	gme	ent	2													

22.14.32 DAB[3]

Address offset: 0x60C

Device address base segment 3

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19 :	18 1	L7 1	L6 1	L5 :	14	13 :	12	11 :	LO	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	n																				
Α	RW	DAB										Dev	vice	ad	dre	ss b	ase	seg	gme	ent	3														

22.14.33 DAB[4]

Address offset: 0x610

Device address base segment 4

Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13	12 :	11	10	9	8	7	6	5	4	3 2	1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	. Α	A A
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	DAB										De	vice	ad	dre	ss k	ase	e se	gm	ent	4													

22.14.34 DAB[5]

Address offset: 0x614

Device address base segment 5

Bit n	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ.	А А
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																			
Α	RW	DAB										De	vice	ad	dre	ess k	oase	e se	gm	ent	5													

22.14.35 DAB[6]

Address offset: 0x618

Device address base segment 6

Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2 1	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	A A
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 0
ld RW Field	Value Id	Va	lue							De	scri	ptic	on																			
										_									_													

A RW DAB Device address base segment 6



22.14.36 DAB[7]

Address offset: 0x61C

Device address base segment 7

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	.9 1	8 17	7 16	15	14	13	12	11	LO	9	8	7	6 !	5 4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A	Δ ,	A A	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ.	A A	4 Α	A	Α	A	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0 ()
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	DAB										Dev	ice	ado	ires	s ba	ise s	egr	nen	t 7													-

22.14.37 DAP[0]

Address offset: 0x620 Device address prefix 0

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 1	16 15 14 13 12 11	10 9 8 7 6	5 4 3 2 1 0
Id				AAAAA	AAAAA	A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0
Id RW Field	Value Id	Value	Description			
A RW DAP			Device address prefix 0	i		

22.14.38 DAP[1]

Address offset: 0x624

Device address prefix 1

Bit number		31 30 29 28 2	27 26 25 24 23 22 21 20 19 18	17 16 15 14 13 12 13	1 10 9 8 7 6	5 4 3 2 1 0
ld				A A A A A		AAAAAA
Reset 0x0000000	n	0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0		0 0 0 0 0
reset oxooooo	u	0 0 0 0	0 0 0 0 0 0 0 0 0	000000	, , , , , , , , , , , , , , , , , , , ,	0 0 0 0 0
ld RW Field	Value Id	Value	Description			
	74.40.14	74.40	2000			
A RW DAP			Device address pre	fix 1		

22.14.39 DAP[2]

Address offset: 0x628

Device address prefix 2

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	1 0
Id		A A A A A A A A A A A A A A A A A A A	А А
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
ld RW Field	Value Id	Value Description	
A RW DAP		Device address prefix 2	

22.14.40 DAP[3]

Address offset: 0x62C

Device address prefix 3

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A	A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0
Id RW Field	Value Id	Value Description	
A RW DAP		Device address prefix 3	

22.14.41 DAP[4]

Address offset: 0x630

Device address prefix 4



Bit	numbe	er		31	30 2	9 2	28 :	27 2	6 2	25 2	24 2	3 2	2 2	1 2	0 19	18	17	16	15	14	13	12 1	.1 1	9	8	7	6	5	4	3	2 1	. 0
Id																			Α	Α	Α	Α.	4 <i>A</i>	. A	Α	Α	Α	Α	Α	Α /	4 Δ	А
Res	et 0x0	0000000		0	0 ()	0	0 (0	0	0) (0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Val	ue						C	esc	ript	tion	ı																	
Α	RW	DAP									0	evi	ce a	ddı	ess	pre	fix 4	4														

22.14.42 DAP[5]

Address offset: 0x634

Device address prefix 5

Bit	numbe	er		31	30	29	28	27	26	25	24	23 :	22 2	1 2	0 1	9 1	8 17	7 16	15	14	13	12 :	11 1	.0 9	9 ;	8 7	7	6 5	4	3	2	1	0
Id																			Α	Α	Α	Α	Α.	Δ ,	۸ ,	A A	۱,	Α Α	A	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0 () (0 () (0 0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	DAP										Dev	ice	add	res	s pr	efix	5															7

22.14.43 DAP[6]

Address offset: 0x638

Device address prefix 6

Bitı	numbe	r		31	30	29	28	27	26 2	25 2	24 2	23 2	22 2	1 2	0 1	9 1	8 17	7 16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 Α	A A
Res	et 0x0(0000000		0	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	DAP									[Dev	ice a	add	res	pr	efix	6															

22.14.44 DAP[7]

Address offset: 0x63C

Device address prefix 7

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	! :	1 0
Id																				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A		А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	on																			
Α	RW	DAP										Dev	/ice	ad	dre	ss į	oret	fix 7	7															

22.14.45 DACNF

Address offset: 0x640

Device address match configuration

Bit n	umbe	r		31	30 2	29 2	28 2	27 2	26 25	5 2	4 2	3 22	2 21	. 20	19	18	17	16	15	14	13 :	12 :	11 1	0 9)	8 7	6	5	4	3	2	1 0
Id																			Р	0	N	M	L I	ζ.	J	I F	G	F	Ε	D	С	ВА
Rese	t 0x0	0000000		0	0	0	0 (0	0 0	0) (0 0	0	0	0	0	0	0	0	0	0	0	0 () ()	0 0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	ion																		
Α	RW	ENA0									Е	nab	le o	r dis	sabl	e d	evic	e a	ddr	ess	ma	tchi	ng ι	ısin	g d	evic	e a	ddre	ess			
											0																					
			Disabled	0							D	isab	led																			
			Enabled	1							Е	nab	led																			
В	RW	ENA1									Е	nab	le o	r dis	sabl	e d	evic	e a	ddr	ess	ma	tchi	ng ι	ısin	g d	evic	e a	ddre	ess			
											1																					
			Disabled	0							D	isab	led																			
			Enabled	1							Е	nab	led																			
С	RW	ENA2									Е	nab	le o	r dis	sabl	e d	evic	e a	ddr	ess	ma	tchi	ng ı	ısin	g d	evic	e a	ddre	ess			
											2																					
			Disabled	0							D	isab	led																			
			Enabled	1							Е	nab	led																			



Bit n	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					PONMLKJIHGFEDCBA
Rese	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
D	RW	ENA3			Enable or disable device address matching using device address
					3
			Disabled	0	Disabled
			Enabled	1	Enabled
Ε	RW	ENA4			Enable or disable device address matching using device address
					4
			Disabled	0	Disabled
			Enabled	1	Enabled
F	RW	ENA5			Enable or disable device address matching using device address
					5
			Disabled	0	Disabled
			Enabled	1	Enabled
G	RW	ENA6			Enable or disable device address matching using device address
					6
			Disabled	0	Disabled
			Enabled	1	Enabled
Н	RW	ENA7			Enable or disable device address matching using device address
					7
			Disabled	0	Disabled
			Enabled	1	Enabled
1		TXADD0			TxAdd for device address 0
J		TXADD1			TxAdd for device address 1
K		TXADD2			TxAdd for device address 2
L		TXADD3			TxAdd for device address 3
М		TXADD4			TxAdd for device address 4
N		TXADD5			TxAdd for device address 5
0		TXADD6			TxAdd for device address 6
Р	RW	TXADD7			TxAdd for device address 7

22.14.46 MHRMATCHCONF

Address offset: 0x644

Search Pattern Configuration

Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17	7 16 15 14 13 12	11 10 9 8 7 6	5 5 4 3 2 1 0
Id						
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0
Id RW Field	Value Id	Value	Description			

22.14.47 MHRMATCHMAS

Address offset: 0x648

Pattern mask

Bit number	31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 1	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id				
Reset 0x00000000	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description		

22.14.48 MODECNF0

Address offset: 0x650

Radio mode configuration register 0



C C Reset 0x00000200 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
and the second s	
Id RW Field Value Description	
A RW RU Radio ramp-up time	
Default 0 Default ramp-up time (tRXEN), compatible with firmware	
written for nRF51	
Fast 1 Fast ramp-up (tRXEN,FAST), see electrical specification for more	
information	
C RW DTX Default TX value	
Specifies what the RADIO will transmit when it is not started, i.e.	
between:	
RADIO.EVENTS_READY and RADIO.TASKS_START	
RADIO.EVENTS_END and RADIO.TASKS_START	
RADIO.EVENTS_END and RADIO.EVENTS_DISABLED	
B1 0 Transmit '1'	
BO 1 Transmit '0'	
Center 2 Transmit center frequency	
When tuning the crystal for centre frequency, the RADIO must	
be set in DTX = Center mode to be able to achieve the expected	
accuracy. This is only a valid setting for Nrf_1Mbit, Nrf_2Mbit,	
Ble_1Mbit and Ble_2Mbit.	

22.14.49 SFD

Address offset: 0x660

IEEE 802.15.4 Start of Frame Delimiter

Bit r	number		31 30 29 28 27	7 26 25 24	23 22	21 20	19 1	18 17	16 1	5 14	13	12 11	10	9	8	7 6	5	4	3	2	1 0
Id															,	4 <i>A</i>	A	Α	Α	A ,	А А
Res	et 0x000000	A7	0 0 0 0 0	0 0 0	0 0	0 0	0	0 0	0 (0	0	0 0	0	0	0	1 0	1	0	0	1 :	1 1
Id	RW Field	Value Id	Value		Descr	iption															
Α	RW SFD				IEEE 8	02.15.	.4 Sta	rt of	Fram	e De	limit	er. No	ote,	the	leas	t					
					signifi	cant 4	-bits	of th	e SFD	canr	not a	ll be :	zero	s.							

22.14.50 EDCNT

Address offset: 0x664

IEEE 802.15.4 Energy Detect Loop Count

Number of iterations to perform an ED scan. If set to 0 one scan is performed, otherwise the specified number + 1 of ED scans will be performed and the max ED value tracked in EDSAMPLE

Bit	numbe	er		3	1 3	30 2	9 2	8 2	7 2	6 2	25 2	24	23	22 :	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000000		0		0 0) (0 (0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	alι	ıe							Des	crip	otic	n																				
Α	RW	EDCNT											EEI	E 80	2.1	.5.4	l En	erg	y D	ete	ct I	.00	рC	our	nt											

22.14.51 EDSAMPLE

Address offset: 0x668

IEEE 802.15.4 Energy Detect Level



Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 1	8 17	' 16	15	14	13 :	L2 1	1 10	9	8	7	6	5	4	3	2 :	L 0
Id																										Α	Α	Α	Α	Α /	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0 (0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	EDLVL										IEE	80	2.1	5.4	Ene	rgy	Det	ect I	eve	el											

22.14.52 CCACTRL

Address offset: 0x66C

IEEE 802.15.4 Clear Channel Assessment Control

Bit	numbe	er		31 3	30 2	9 2	8 2.	7 26	25	24	23 :	22 21	1 20	19	18	17 :	16	15 1	.4 1	3 12	2 11	10	9	8	7 6	5	4	3 2	2 1	0
Id				D	D [) D) D	D	D	D	С	C C	C	С	С	С	С	В	ВЕ	3 B	В	В	В	В				A	A A	Α
Res	et 0x0	0000000		0	0 (0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0 (0	0
Id	RW	Field	Value Id	Valu	ıe						Des	cript	tion																	
Α	RW	CCAMODE									CCA	A Mo	de C	of O	per	atio	n													
			EdMode	0							Ene	rgy A	Abov	e Tł	hres	shol	d													
											Will	l repo	ort k	usy	wh	nene	ver	ene	ergy	is d	ete	ted	abo	ove						
											CCA	AEDT	HRE	S																
			CarrierMode	1							Car	rier S	Seen																	
											Will	l repo	ort k	usy	wh	nene	ver	con	npli	ant	IEEE	802	2.15	.4 si	igna	is				
											see	n																		
			CarrierAndEdMode	2							Ene	rgy A	Abov	e Tł	hres	shol	d A	ND (Carr	ier S	Seer	1								
			CarrierOrEdMode	3							Ene	rgy A	Abov	e Tł	hres	shol	d O	R Ca	arrie	er Se	en									
			EdModeTest1	4							Ene	rgy A	Abov	e Tł	hres	shol	d te	st n	nod	e th	at w	ill a	bort	wh	en f	irst	ED			
											mea	asure	eme	nt o	ver	thre	esh	old i	s se	en.	No a	ver	agir	ıg.						
В	RW	CCAEDTHRES									CCA	A Ene	rgy	Busy	y Th	resl	holo	d. Us	sed	in al	l th	e CC	A m	ode	es ex	сер	t			
											Car	rierN	/lode	€.																
С	RW	CCACORRTHRES									CCA	A Cor	rela	tor E	Bus	y Th	res	hold	l. Or	nly r	elev	ant	to 0	Carr	ierN	lode	,			
											Car	rierA	ndE	dMo	ode	and	l Ca	rrie	rOrl	EdM	ode	٠.								
D	RW	CCACORRCNT									Lim	it for	occ	ura	nce	s ab	ove	CC	ACC	RRT	HRI	ES. V	Vhe	n no	ot ed	qual	to			
											zero	o the	cor	rola	tor	base	ed s	igna	al de	etec	t is	enat	led							

22.14.53 POWER

Address offset: 0xFFC
Peripheral power control

Bit r	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	3 17	16	5 15	14	1 13	3 12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α
Res	et 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																				
Α	RW	POWER										Pe	ripl	hera	al p	ow	er o	cont	trol	. Tł	ne p	eri	phe	ral	and	its	reg	iste	rs v	will	be				
												res	set	to i	ts ii	nitia	al s	tate	e by	/ SW	itc	hin	g th	е р	erip	her	al o	ff a	nd	the	n				
												ba	ck (on a	agai	in.																			
			Disabled	0								Pe	ripl	hera	al is	s po	we	red	of	f															
			Enabled	1								Pe	ripl	hera	al is	s po	we	red	on																

22.15 Electrical specification

22.15.1 General Radio Characteristics

Symbol	Description	Min.	Тур.	Max.	Units
f _{OP}	Operating frequencies	2360		2500	MHz
f _{PLL,CH,SP}	PLL channel spacing		1		MHz
f _{DELTA,1M}	Frequency deviation @ 1 Mbps		±170		kHz
f _{DELTA,BLE,1M}	Frequency deviation @ BLE 1Mbps		±250		kHz



Symbol	Description	Min.	Тур.	Max.	Units
f _{DELTA,2M}	Frequency deviation @ 2 Mbps		±320		kHz
fsk _{BPS}	On-the-air data rate	125		2000	kbps
f _{chip, IEEE 802.15.4}	Chip rate in IEEE 802.15.4 mode		2000		kchip,
					•

22.15.2 Radio current consumption (Transmitter)

Symbol	Description	Min.	Тур.	Max.	Units
I _{TX,PLUS8dBM,DCDC}	TX only run current (DCDC, 3V) P _{RF} =+8 dBm		14.1		mA
I _{TX,PLUS8dBM}	TX only run current P _{RF} = +8 dBm		30.4		mA
I _{TX,PLUS4dBM,DCDC}	TX only run current (DCDC, 3V) P _{RF} =+4 dBm		9.3		mA
I _{TX,PLUS4dBM}	TX only run current P _{RF} = +4 dBm		18.9		mA
I _{TX,0dBM,DCDC,5V,REG0H}	TX only run current (DCDC, 5V, REG0 out = 3.3 V)P _{RF} = 0dBm		6.0		mA
I _{TX,OdBM,DCDC,5V,REGOL}	O TX only run current (DCDC, 5V, REGO out = 1.8 V)P _{RF} = 0dBm		5.2		mA
I _{TX,0dBM,DCDC}	TX only run current (DCDC, 3V)P _{RF} = 0dBm		4.9		mA
I _{TX,0dBM}	TX only run current P _{RF} = 0dBm		10.2		mA
I _{TX,MINUS4dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -4dBm		3.4		mA
I _{TX,MINUS4dBM}	TX only run current P _{RF} = -4 dBm		7.3		mA
I _{TX,MINUS8dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -8 dBm		3.0		mA
I _{TX,MINUS8dBM}	TX only run current P _{RF} = -8 dBm		6.4		mA
I _{TX,MINUS12dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -12 dBm		2.7		mA
I _{TX,MINUS12dBM}	TX only run current P _{RF} = -12 dBm		5.7		mA
I _{TX,MINUS16dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -16 dBm		2.5		mA
I _{TX,MINUS16dBM}	TX only run current P _{RF} = -16 dBm		5.3		mA
I _{TX,MINUS20dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -20 dBm		2.3		mA
I _{TX,MINUS20dBM}	TX only run current P _{RF} = -20 dBm		5.0		mA
I _{TX,MINUS40dBM,DCDC}	TX only run current DCDC, 3V P_{RF} = -40 dBm		2.0		mA
I _{TX,MINUS40dBM}	TX only run current P _{RF} = -40 dBm		4.0		mA
I _{START,TX,DCDC}	TX start-up current DCDC, 3V, P _{RF} = 4 dBm		5.2		mA
I _{START,TX}	TX start-up current, P _{RF} = 4 dBm		11.0		mA
I _{OdBm} (DCDC, 3V)	TX current (DCDC 3V) 1Mbps BLE measured from VBAT with P_{RF} =0dBm		6.4		mA
I _{2dBm} (DCDC, 3V)	TX current (DCDC 3V) 1Mbps BLE measured from VBAT with P_{RF} =2dBm		8.9		mA
I _{4dBm} (DCDC, 3V)	TX current (DCDC 3V) 1Mbps BLE measured from VBAT with P_{RF} =4dBm		10.6		mA
l _{9dBm} (DCDC, 3V)	TX current (DCDC 3V) 1Mbps BLE measured from VBAT with P _{RF} =9dBm		15.5		mA
I _{OdBm (3V)}	TX current (3V) 1Mbps BLE measured from VBAT with P _{RF} =0dBm		11.2		mA
I _{9dBm (3V)}	TX current (3V) 1Mbps BLE measured from VBAT with P _{RF} =9dBm		30.7		mA

22.15.3 Radio current consumption (Receiver)

Symbol	Description	Min.	Тур.	Max.	Units
I _{RX,1M,DCDC}	RX only run current (DCDC, 3V) 1Mbps / 1Mbps BLE		4.8		mA
I _{RX,1M}	RX only run current (LDO, 3V) 1Mbps / 1Mbps BLE		10.3		mA
I _{RX,2M,DCDC}	RX only run current (DCDC, 3V) 2Mbps / 2Mbps BLE		5.4		mA
I _{RX,2M}	RX only run current (LDO, 3V) 2Mbps / 2Mbps BLE		11.6		mA
I _{START,RX,1M,DCDC}	RX start-up current (DCDC 3V) 1Mbps / 1Mbps BLE		3.7		mA
I _{START,RX,1M}	RX start-up current 1Mbps / 1Mbps BLE		6.7		mA

22.15.4 Transmitter specification

Symbol	Description	Min.	Тур.	Max.	Units
P _{RF}	Maximum output power		8		dBm
P _{RFC}	RF power control range		28		dB
P _{RFCR}	RF power accuracy			±4	dB
P _{RF1.1}	1st Adjacent Channel Transmit Power 1 MHz (1 Mbps)		-23		dBc



Symbol	Description	Min.	Тур.	Max.	Units
P _{RF2,1}	2nd Adjacent Channel Transmit Power 2 MHz (1 Mbps)		-50		dBc
P _{RF1,2}	1st Adjacent Channel Transmit Power 2 MHz (2 Mbps)		-24		dBc
P _{RF2,2}	2nd Adjacent Channel Transmit Power 4 MHz (2 Mbps)		-50		dBc
E _{vm}	Error Vector Magnitude IEEE 802.15.4				%rms
P _{harm2nd} , IEEE 802.15.4	2nd Harmonics in IEEE 802.15.4 mode				dBm
P _{harm3rd, IEEE 802.15.4}	3rd Harmonics in IEEE 802.15.4				dBm

22.15.5 Receiver operation

Symbol	Description	Min.	Тур.	Max.	Units
P _{RX,MAX}	Maximum received signal strength at < 0.1% PER		0		dBm
P _{SENS,IT,1M}	Sensitivity, 1Mbps nRF mode ¹³		-93		dBm
P _{SENS,IT,SP,1M,BLE}	Sensitivity, 1Mbps BLE ideal transmitter, <=37 bytes BER=1E-3 ¹⁴		-95		dBm
P _{SENS,IT,LP,1M,BLE}	Sensitivity, 1Mbps BLE ideal transmitter >=128 bytes BER=1E-4 15		-95		dBm
P _{SENS,IT,2M}	Sensitivity, 2Mbps nRF mode ¹⁶		-89		dBm
P _{SENS,IT,SP,2M,BLE}	Sensitivity, 2Mbps BLE ideal transmitter, Packet length		-92		dBm
	<=37bytes				
P _{SENS,IT,BLE LE125k}	Sensitivity, 125kbps BLE mode		-103		dBm
P _{SENS,IT,BLE LE500k}	Sensitivity, 500kbps BLE mode		-99		dBm
P _{sense} , IEEE 802.15.4	Sensitivity in IEEE 802.15.4 mode		-100		dBm

22.15.6 RX selectivity

RX selectivity with equal modulation on interfering signal ¹⁷

Symbol	Description	Min.	Тур.	Max.	Units
C/I _{1M,co-channel}	1Mbps mode, Co-Channel interference		9		dB
C/I _{1M,-1MHz}	1 Mbps mode, Adjacent (-1 MHz) interference		-2		dB
C/I _{1M,+1MHz}	1 Mbps mode, Adjacent (+1 MHz) interference		-10		dB
C/I _{1M,-2MHz}	1 Mbps mode, Adjacent (-2 MHz) interference		-19		dB
C/I _{1M,+2MHz}	1 Mbps mode, Adjacent (+2 MHz) interference		-42		dB
C/I _{1M,-3MHz}	1 Mbps mode, Adjacent (-3 MHz) interference		-38		dB
C/I _{1M,+3MHz}	1 Mbps mode, Adjacent (+3 MHz) interference		-48		dB
C/I _{1M,±6MHz}	1 Mbps mode, Adjacent (≥6 MHz) interference		-50		dB
C/I _{1MBLE,co-channel}	1 Mbps BLE mode, Co-Channel interference		6		dB
C/I _{1MBLE,-1MHz}	1 Mbps BLE mode, Adjacent (-1 MHz) interference		-2		dB
C/I _{1MBLE,+1MHz}	1 Mbps BLE mode, Adjacent (+1 MHz) interference		-9		dB
C/I _{1MBLE,-2MHz}	1 Mbps BLE mode, Adjacent (-2 MHz) interference		-22		dB
C/I _{1MBLE,+2MHz}	1 Mbps BLE mode, Adjacent (+2 MHz) interference		-46		dB
C/I _{1MBLE,>3MHz}	1 Mbps BLE mode, Adjacent (≥3 MHz) interference		-50		dB
C/I _{1MBLE,image}	Image frequency Interference		-22		dB
C/I _{1MBLE,image,1MHz}	Adjacent (1 MHz) interference to in-band image frequency		-35		dB
C/I _{2M,co-channel}	2Mbps mode, Co-Channel interference		10		dB
C/I _{2M,-2MHz}	2 Mbps mode, Adjacent (-2 MHz) interference		6		dB
C/I _{2M,+2MHz}	2 Mbps mode, Adjacent (+2 MHz) interference		-19		dB
C/I _{2M,-4MHz}	2 Mbps mode, Adjacent (-4 MHz) interference		-20		dB
C/I _{2M,+4MHz}	2 Mbps mode, Adjacent (+4 MHz) interference		-44		dB
C/I _{2M,-6MHz}	2 Mbps mode, Adjacent (-6 MHz) interference		-42		dB

Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

As defined in the Bluetooth Core Specification v4.0 Volume 6: Core System Package (Low Energy Controller Volume)

¹⁵ Equivalent BER limit < 10E-04

¹⁶ Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

Wanted signal level at PIN = -67 dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented



Symbol	Description	Min.	Тур.	Max.	Units
C/I _{2M,+6MHz}	2 Mbps mode, Adjacent (+6 MHz) interference		-42		dB
C/I _{2M,≥12MHz}	2 Mbps mode, Adjacent (≥12 MHz) interference		-52		dB
C/I _{125k BLE LR,co-channel}	125 kbps BLE LR mode, Co-Channel interference				dB
C/I _{125k BLE LR,-1MHz}	125 kbps BLE LR mode, Adjacent (-1 MHz) interference				dB
C/I _{125k BLE LR,+1MHz}	125 kbps BLE LR mode, Adjacent (+1 MHz) interference				dB
C/I _{125k BLE LR,-2MHz}	125 kbps BLE LR mode, Adjacent (-2 MHz) interference				dB
C/I _{125k BLE LR,+2MHz}	125 kbps BLE LR mode, Adjacent (+2 MHz) interference				dB
C/I _{125k BLE LR,>3MHz}	125 kbps BLE LR mode, Adjacent (≥3 MHz) interference				dB
C/I _{125k BLE LR,image}	Image frequency Interference				dB
C/I _{500k BLE LR,co-channel}	500 kbps BLE LR mode, Co-Channel interference				dB
C/I _{500k BLE LR,-1MHz}	500 kbps BLE LR mode, Adjacent (-1 MHz) interference				dB
C/I _{500k BLE LR,+1MHz}	500 kbps BLE LR mode, Adjacent (+1 MHz) interference				dB
C/I _{500k BLE LR,-2MHz}	500 kbps BLE LR mode, Adjacent (-2 MHz) interference				dB
C/I _{500k BLE LR,+2MHz}	500 kbps BLE LR mode, Adjacent (+2 MHz) interference				dB
C/I _{500k BLE LR,>3MHz}	500 kbps BLE LR mode, Adjacent (≥3 MHz) interference				dB
C/I _{500k BLE LR,image}	Image frequency Interference				dB

22.15.7 RX intermodulation

RX intermodulation 18

Symbol	Description	Min.	Тур.	Max.	Units
P _{IMD,1M}	IMD performance, 1 Mbps, 3rd, 4th, and 5th offset channel		-29		dBm
P _{IMD,1M,BLE}	IMD performance, BLE 1 Mbps, 3rd, 4th, and 5th offset channel		-30		dBm
P _{IMD,2M}	IMD performance, 2 Mbps, 3rd, 4th, and 5th offset channel		-30		dBm

22.15.8 Radio timing

Symbol	Description	Min.	Тур.	Max.	Units
t _{TXEN}	Time between TXEN task and READY event after channel		140		us
	FREQUENCY configured				
t _{TXEN,FAST}	Time between TXEN task and READY event after channel		40		us
	FREQUENCY configured (Fast Mode)				
t _{TXDISABLE}	Time between DISABLE task and DISABLED event when the		6		us
	radio was in TX and mode is set to 1Mbps				
t _{TXDISABLE,2M}	Time between DISABLE task and DISABLED event when the				us
	radio was in TX and mode is set to 2Mbps				
t _{RXEN}	Time between the RXEN task and READY event after channel		140		us
	FREQUENCY configured in default mode				
t _{RXEN,FAST}	Time between the RXEN task and READY event after channel		40		us
	FREQUENCY configured in fast mode				
t _{RXDISABLE}	Time between DISABLE task and DISABLED event when the		0		us
	radio was in RX				
t _{TXCHAIN}	TX chain delay		0.6		us
t _{rxchain}	RX chain delay		9.4		us
t _{RXCHAIN,2M}	RX chain delay in 2Mbps mode		5		us
t _{RXCHAIN,LR 125k}	RX chain delay in BLE LR125kbps mode				us
t _{RXCHAIN,LR} 500k	RX chain delay in BLE LR500kbps mode				us
t _{RX-to-TX turnaround}	Maximum TX-to-RX or RX-to-TX turnaround time in IEEE				us
	802.15.4 mode				

22.15.9 Received Signal Strength Indicator (RSSI) specifications

Symbol	Description	Min.	Тур.	Max.	Units
RSSI _{ACC}	RSSI Accuracy Valid range -90 to -20 dBm		-2		dB

Wanted signal level at PIN = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is not modulated, the other interferer is modulated equal with the wanted signal. The input power of the interferers where the sensitivity equals BER = 0.1% is presented.



Symbol	Description	Min.	Тур.	Max.	Units
RSSI _{RESOLUTION}	RSSI resolution		1		dB
RSSI _{PERIOD}	Sample period		8		us
RSSI _{min, IEEE 802.15.4}	Minimum RSSI sensitivity in 802.15.4 mode				dBm

22.15.10 Jitter

Symbol	Description	Min.	Тур.	Max.	Units
t _{DISABLEDJITTER}	Jitter on DISABLED event relative to END event when shortcut		0.25		us
	between END and DISABLE is enabled.				
t _{READYJITTER}	Jitter on READY event relative to TXEN and RXEN task.		0.25		us

22.15.11 Delay when disabling the RADIO

Symbol	Description	Min.	Тур.	Max.	Units
t _{TXDISABLE,1M}	Disable delay from TX.		6		us
	Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit				
	and MODE = Ble_1Mbit				
t _{RXDISABLE,1M}	Disable delay from RX.		0		us
	Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit				
	and MODE = Ble_1Mbit				



23 TIMER — Timer/counter

The TIMER can operate in two modes: timer and counter.

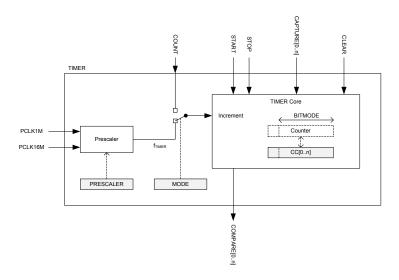


Figure 51: Block schematic for timer/counter

The timer/counter runs on the high-frequency clock source (HFCLK) and includes a four-bit (1/2X) prescaler that can divide the timer input clock from the HFCLK controller. Clock source selection between PCLK16M and PCLK1M is automatic according to TIMER base frequency set by the prescaler. The TIMER base frequency is always given as 16 MHz divided by the prescaler value.

The PPI system allows a TIMER event to trigger a task of any other system peripheral of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

The TIMER can operate in two modes, Timer mode and Counter mode. In both modes, the TIMER is started by triggering the START task, and stopped by triggering the STOP task. After the timer is stopped the timer can resume timing/counting by triggering the START task again. When timing/counting is resumed, the timer will continue from the value it had prior to being stopped.

The status (Started or Stopped) of each TIMER instance can be checked by reading its STATUS register.

In Timer mode, the TIMER's internal Counter register is incremented by one for every tick of the timer frequency f_{TIMER} as illustrated in *Figure 51: Block schematic for timer/counter* on page 292. The timer frequency is derived from PCLK16M as shown below, using the values specified in the PRESCALER register:

```
f_{TIMER} = 16 \text{ MHz} / (2^{PRESCALER})
```

When f_{TIMER} <= 1 MHz the TIMER will use PCLK1M instead of PCLK16M for reduced power consumption.

In counter mode, the TIMER's internal Counter register is incremented by one each time the COUNT task is triggered, that is, the timer frequency and the prescaler are not utilized in counter mode. Similarly, the COUNT task has no effect in Timer mode.

The TIMER's maximum value is configured by changing the bit-width of the timer in the *BITMODE* on page 297 register.



PRESCALER on page 298 and the *BITMODE* on page 297 must only be updated when the timer is stopped. If these registers are updated while the TIMER is started then this may result in unpredictable behavior.

When the timer is incremented beyond its maximum value the Counter register will overflow and the TIMER will automatically start over from zero.

The Counter register can be cleared, that is, its internal value set to zero explicitly, by triggering the CLEAR task.

The TIMER implements multiple capture/compare registers.

Independent of prescaler setting the accuracy of the TIMER is equivalent to one tick of the timer frequency f_{TIMER} as illustrated in *Figure 51: Block schematic for timer/counter* on page 292.

23.1 Capture

The TIMER implements one capture task for every available capture/compare register.

Every time the CAPTURE[n] task is triggered, the Counter value is copied to the CC[n] register.

23.2 Compare

The TIMER implements one COMPARE event for every available capture/compare register.

A COMPARE event is generated when the Counter is incremented and then becomes equal to the value specified in one of the capture compare registers. When the Counter value becomes equal to the value specified in a capture compare register CC[n], the corresponding compare event COMPARE[n] is generated.

BITMODE on page 297 specifies how many bits of the Counter register and the capture/compare register that are used when the comparison is performed. Other bits will be ignored.

23.3 Task delays

After the TIMER is started, the CLEAR task, COUNT task and the STOP task will guarantee to take effect within one clock cycle of the PCLK16M.

23.4 Task priority

If the START task and the STOP task are triggered at the same time, that is, within the same period of PCLK16M, the STOP task will be prioritized.

23.5 Registers

Table 36: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40008000	TIMER	TIMER0	Timer 0	This timer instance has 4 CC registers
				(CC[03])
0x40009000	TIMER	TIMER1	Timer 1	This timer instance has 4 CC registers
				(CC[03])
0x4000A000	TIMER	TIMER2	Timer 2	This timer instance has 4 CC registers
				(CC[03])
0x4001A000	TIMER	TIMER3	Timer 3	This timer instance has 6 CC registers
				(CC[05])
0x4001B000	TIMER	TIMER4	Timer 4	This timer instance has 6 CC registers
				(CC[05])



Table 37: Register Overview

Register	Offset	Description	
TASKS_START	0x000	Start Timer	
TASKS_STOP	0x004	Stop Timer	
TASKS_COUNT	0x008	Increment Timer (Counter mode only)	
TASKS_CLEAR	0x00C	Clear time	
TASKS_SHUTDOWN	0x010	Shut down timer	Deprecated
TASKS_CAPTURE[0]	0x040	Capture Timer value to CC[0] register	
TASKS_CAPTURE[1]	0x044	Capture Timer value to CC[1] register	
TASKS_CAPTURE[2]	0x048	Capture Timer value to CC[2] register	
TASKS_CAPTURE[3]	0x04C	Capture Timer value to CC[3] register	
TASKS_CAPTURE[4]	0x050	Capture Timer value to CC[4] register	
TASKS_CAPTURE[5]	0x054	Capture Timer value to CC[5] register	
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match	
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match	
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match	
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match	
EVENTS_COMPARE[4]	0x150	Compare event on CC[4] match	
EVENTS_COMPARE[5]	0x154	Compare event on CC[5] match	
SHORTS	0x200	Shortcut register	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
STATUS	0x400	Timer status	
MODE	0x504	Timer mode selection	
BITMODE	0x508	Configure the number of bits used by the TIMER	
PRESCALER	0x510	Timer prescaler register	
CC[0]	0x540	Capture/Compare register 0	
CC[1]	0x544	Capture/Compare register 1	
CC[2]	0x548	Capture/Compare register 2	
CC[3]	0x54C	Capture/Compare register 3	
CC[4]	0x550	Capture/Compare register 4	
CC[5]	0x554	Capture/Compare register 5	

23.5.1 SHORTS

Address offset: 0x200 Shortcut register

Bit r	numbe	r		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	COMPAREO_CLEAR			Shortcut between COMPARE[0] event and CLEAR task
					See EVENTS_COMPARE[0] and TASKS_CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
В	RW	COMPARE1_CLEAR			Shortcut between COMPARE[1] event and CLEAR task
					See EVENTS_COMPARE[1] and TASKS_CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
С	RW	COMPARE2_CLEAR			Shortcut between COMPARE[2] event and CLEAR task
					See EVENTS_COMPARE[2] and TASKS_CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
D	RW	COMPARE3_CLEAR			Shortcut between COMPARE[3] event and CLEAR task
					See EVENTS_COMPARE[3] and TASKS_CLEAR
			Disabled	0	Disable shortcut



Bit r	numbe	er		31 30	29	28 2	7 26	25	24 2	23 22 2	1 2	0 19	9 1	8 17	' 1	5 15	5 14	4 1	3 1	2 1	111	0 9	9 8	3 7	(5 5	4	3	2	1	0
Id																		L	_ k	<	J	l H	1 (ì		F	E	D	С	В	Α
Res	et 0x0	0000000		0 0	0	0 (0 0	0	0	0 0 0) (0 0	(0	0	0	0) ()	0 () (0	0	(0	0	0	0	0	0
Id	RW	Field	Value Id	Value						Descript	tio	n																			
			Enabled	1					Е	Enable s	sho	rtcu	t																		
Ε	RW	COMPARE4_CLEAR							S	Shortcu	t be	etwe	eer	СО	MF	ARE	[4]] ev	/en	t a	nd C	LEA	AR t	ask							
									S	See <i>EVE</i>	NT.	s_c	ΟN	1PAF	?E[4	4] aı	nd	TAS	sks_	_ <i>C</i>	LEAI	R									
			Disabled	0						Disable	shc	ortcu	ıt																		
			Enabled	1					Е	Enable s	sho	rtcu	t																		
F	RW	COMPARE5_CLEAR							S	Shortcu	t be	etwe	eer	СО	MF	ARE	[5]] ev	/en	t a	nd C	LEA	AR t	ask							
									S	See <i>EVE</i>	NT.	s_c	ΟN	IPAF	?E[.	5] aı	nd	TAS	sks_	_c	LEAI	R									
			Disabled	0					0	Disable	shc	ortcu	ıt																		
			Enabled	1					Е	Enable s	sho	rtcu	t																		
G	RW	COMPAREO_STOP							S	Shortcu	t be	etwe	eer	СО	MF	ARE	[0]] ev	/en	t a	nd S	то	P ta	sk							
									S	See <i>EVE</i>	NT.	s_c	ΟN	IPAF	? <i>E[</i> (<mark>0]</mark> aı	nd	TAS	SKS	_s	ГОР										
			Disabled	0						Disable	shc	ortcu	ıt																		
			Enabled	1					Е	Enable s	sho	rtcu	t																		
Н	RW	COMPARE1_STOP							S	Shortcu	t be	etwe	eer	СО	MF	ARE	[1]] ev	/en	t a	nd S	то	P ta	sk							
									S	See <i>EVE</i>	NT.	s_c	ΟN	1PAF	?E[.	1] aı	nd	TAS	sks __	_s	ГОР										
			Disabled	0						Disable	shc	ortcu	ıt																		
			Enabled	1					E	Enable s	sho	rtcu	t																		
I	RW	COMPARE2_STOP							S	Shortcu	t be	etwe	eer	СО	MF	ARE	[2]] ev	/en	t a	nd S	то	P ta	sk							
									S	See <i>EVE</i>	NT.	s_c	ΟN	1PAF	?E[.	2] aı	nd	TA:	SKS	_5	ГОР										
			Disabled	0						Disable	shc	ortcu	ıt																		
			Enabled	1					Е	Enable s	sho	rtcu	t																		
J	RW	COMPARE3_STOP							S	Shortcu	t be	etwe	eer	СО	MF	ARE	[3]] ev	/en	t a	nd S	то	P ta	sk							
									S	See <i>EVE</i>	NT.	S_C	ΟN	1PAF	?E[.	3] aı	nd	TA:	SKS	_5	ГОР										
			Disabled	0						Disable	shc	ortcı	ıt																		
			Enabled	1					E	Enable s	sho	rtcu	t																		
K	RW	COMPARE4_STOP							S	Shortcu	t be	etwe	eer	СО	MF	ARE	[4]] ev	/en	t a	nd S	то	P ta	sk							
									S	See <i>EVE</i>	NT.	s_c	ΟN	IPAF	RE[4	4] aı	nd	TAS	SKS <u>.</u>	_5	ГОР										
			Disabled	0						Disable	shc	ortcu	ıt																		
			Enabled	1					E	Enable s	sho	rtcu	t																		
L	RW	COMPARE5_STOP							S	Shortcu	t be	etwe	eer	СО	MF	ARE	[5]] ev	/en	t a	nd S	то	P ta	sk							
									S	See <i>EVE</i>	NT.	S_C	ON	1PAF	?E[.	5] aı	nd	TAS	SKS	S	ГОР										
			Disabled	0						Disable		_																			
			Enabled	1						Enable s																					

23.5.2 INTENSET

Address offset: 0x304

Enable interrupt

	iumbe	r		31	30 2	9 :	28 2	7 2	26 2	5 2	4 2	3 22							15 1	.4 1	3 12	2 11	10	9	8	7 (5 5	4	3	2	1	0
Id													F	Ε	D	С	В	A														
Res	et 0x0	0000000		0	0 ()	0 ()	0 () (0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0 () (0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	escri	ptio	n																		
Α	RW	COMPARE0									W	/rite '	'1' t	ο Ει	nab	le i	nte	rrup	ot fo	or C	ОМІ	PAR	E[0]	eve	nt							
											Se	ee <i>EV</i>	'ENT	TS_	coi	MР	4RE	[0]														
			Set	1							Er	nable	!																			
			Disabled	Value								ead: I	Disa	ble	d																	
			Enabled	1							R	ead: I	Enal	ble	d																	
В	RW	COMPARE1									W	/rite '	'1' t	o Eı	nab	le i	nte	rrup	ot fo	or C	ОМІ	PAR	E[1]	eve	nt							
											Se	ee <i>EV</i>	EN1	TS_	coi	MP	4RE	[1]														
			Set	1							Er	nable	•																			



Bit	numbe	er		31	30 2	29 28	8 27	26	25 2	24 23	3 22 2	21 20	0 19	18 :	17 1	6 1	5 14	13	12	11 1	0 9	8	7	6	5 4	4 3	2	1 0
Id												F E	D	С	ВА	4												
Res	et 0x0	0000000		0	0	0 0	0	0	0	0 0	0	0 0	0	0	0 (0	0	0	0	0 (0	0	0	0	0 (0 0	0	0 0
Id	RW	Field	Value Id	Va	ue					De	escrip	ption	1															
			Disabled	0						Re	ead: [Disab	oled															
			Enabled	1						Re	ead: E	Enab	led															
С	RW	COMPARE2								W	/rite '	'1' to	Enab	le i	nter	rupt	for	COI	MPA	RE[2	2] ev	ent						
										Se	ee <i>EV</i>	ENTS	s_coi	MPA	ARE[2]												
			Set	1						En	nable	:																
			Disabled	0						Re	ead: [Disab	oled															
			Enabled	1						Re	ead: E	Enab	led															
D	RW	COMPARE3								W	/rite '	'1' to	Enab	le ii	nter	rupt	for	COI	MPA	RE[3	8] ev	ent						
										Se	ee <i>EV</i>	ENTS	s_coi	MPA	ARE[3]												
			Set	1						En	nable	•																
			Disabled	0						Re	ead: [Disab	oled															
			Enabled	1						Re	ead: E	Enab	led															
E	RW	COMPARE4								W	/rite '	'1' to	Enab	le i	nter	rupt	for	COI	MPA	RE[4	l] ev	ent						
										Se	ee <i>EV</i>	ENTS	s coi	MPA	ARE[41												
			Set	1							nable																	
			Disabled	0						Re	ead: [Disab	oled															
			Enabled	1						Re	ead: E	Enab	led															
F	RW	COMPARE5								W	/rite '	'1' to	Enab	le i	nter	rupt	t for	COI	MPA	RE[5	5] ev	ent						
										Se	ee <i>EV</i>	'ENTS	s coi	MPA	4 <i>REI</i>	51												
			Set	1							nable				- 1	•												
			Disabled	0						Re	ead: [Disab	oled															
			Enabled	1						Re	ead: E	Enab	led															

23.5.3 INTENCLR

Address offset: 0x308

Disable interrupt

	number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0	
Id	RW Field	Value Id	Value	Description
Α	RW COMPAREO			Write '1' to Disable interrupt for COMPARE[0] event
				See EVENTS_COMPARE[0]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW COMPARE1			Write '1' to Disable interrupt for COMPARE[1] event
				See EVENTS_COMPARE[1]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW COMPARE2			Write '1' to Disable interrupt for COMPARE[2] event
				See EVENTS_COMPARE[2]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW COMPARE3			Write '1' to Disable interrupt for COMPARE[3] event
				See EVENTS_COMPARE[3]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
		Lilabica	1	nead. Endoica



Bit r	numbe	r		31	30 2	29 2	28 2	7 2	26 2	:5 2	24 2	23 22	2 21	1 20	19	9 1	8 1	7 1	16	15	14	13 1	.2 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id													F	Ε	D) (2 1	3 .	Α														
Res	et 0x0	0000000		0	0	0	0 (0	0 (0 (0	0 0	0	0	0) () ()	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Desci	ript	ion																			
E	RW	COMPARE4									١	Write	e '1'	to	Dis	abl	e i	nte	rru	pt 1	for	CON	ΛPΑ	RE[4] e	ver	nt						
											5	See E	VEI	NTS.		ОМ	1PA	RE	[4]														
			Clear	1								Disab	le																				
			Disabled	0							F	Read	: Dis	sab	led																		
			Enabled	1							F	Read	: En	abl	ed																		
F	RW	COMPARE5									١	Write	e '1'	to	Dis	abl	e i	nte	rru	pt 1	for	CON	ΛPΑ	RE[5] e	ver	nt						
											S	See E	VEI	NTS	_c	ОМ	IPA	RE	[5]														
			Clear	1							[Disab	le																				
			Disabled	0							F	Read	: Dis	sab	led																		
			Enabled	1							F	Read	: En	abl	ed																		

23.5.4 STATUS

Address offset: 0x400

Timer status

Bit r	numb	er		31 30	29	28	27	26	25	24	23	22 2	21 2	0 19	9 18	17	16	15	14 1	l3 1	2 11	10	9	8	7	6	5	4	3 2	2 1	0
Id				d 0																											Α
Res	et OxC	0000000		0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Value	•						Des	crip	tio	1																	
Α	R	STATUS									Tim	er s	tatı	IS																	
			Stopped	0							Tim	er i	s sto	рре	ed																
			Started	1							Tim	er i	s sta	rte	t																

23.5.5 MODE

Address offset: 0x504 Timer mode selection

Bit	numbe	r		31	30	29	28	27	26	25 2	24 :	23 2	2 2:	1 20	0 19	18	3 17	16	15	14	13	12 :	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																																А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	0 0 0 0 0 0 0 Value				ı	Desc	ript	ion	ı																				
Α	RW	MODE		0 0 0 0 0 0 0					-	Time	er m	ode	9																			
			Timer				:	Sele	ct Ti	me	r m	ode																				
			Counter	1	0 0 0 0 0 0 0			:	Sele	ct C	oun	ter	mo	de													Dep	rec	ated			
			LowPowerCounter	2							:	Sele	ct Lo	w	Pow	er (Cou	nte	r m	ode												

23.5.6 BITMODE

Address offset: 0x508

Configure the number of bits used by the TIMER

Bit r	numbe	er		31	30	29	28	27 :	26 2	25 :	24 :	23 2	22 :	21 :	20	19	18	17	16	15 :	L4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																																,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 Value 0 1 2							- 1	Des	crip	otio	n																		
Α	RW	BITMODE		Value 0 1							-	Γim	er l	bit v	wid	th																	
			16Bit	Value 0 1 2							:	16 k	oit t	time	er b	it v	/idt	h															
			08Bit	Value 0 1							3 bi	t tiı	mei	bit	t wi	dth																	
			24Bit	0 1 2						:	24 k	oit t	time	er b	it v	/idt	h																
			32Bit	Value 0 1 2							3	32 k	oit t	time	er b	it v	/idt	h															



23.5.7 PRESCALER

Address offset: 0x510
Timer prescaler register

Bit r	numbe	r		31	30 2	29 2	8 27	26	25	24 2	23 2	2 2	1 20) 19	18	17	16	15 1	.4 13	12	11	10 9) {	3 7	6	5 5	4	3	2	1 0
Id																												Α	Α	А А
Res	et 0x0	0000004		0 Val						0	0 (0 0	0	0	0	0	0	0	0 0	0	0	0 0) (0 0	C	0	0	0	1	0 0
Id	RW	Field	Value Id	Val	lue						Desc	cript	ion																	
Α	RW	PRESCALER		Value [09]						F	res	cale	r va	lue																

23.5.8 CC[0]

Address offset: 0x540

Capture/Compare register 0

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	9 18	3 17	7 16	15	14	13	12	11 1	10	9	8	7	6	5	4	3 2	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α.	A A	4 A	. A	Α	Α	Α	Α	Α	Α.	A	Α	Α .	Α.	Α.	Α	Α	A A	Α Α	A A				
Res	et Ox	0000000		0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0					
Id	RW	Field	Value Id			De	scri	ptio	n																								
Α	RW	CC										Cap	otur	e/C	omp	are	val	ue															
							On	ly th	ne n	uml	oer (of bi	its i	ndic	ate	d by	/ BI	TMC	DDE	Ew	ill be	e us	sed	by									
												the	TIN	ИER																			

23.5.9 CC[1]

Address offset: 0x544

Capture/Compare register 1

Bit	numbe	r		31	1 30	29	28	8 27	7 20	6 25	5 24	4 23	22	21 :	20 :	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	А	A	Α	A	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptio	n																				
Α	RW	CC										Ca	ptur	e/C	om	par	e v	alu	e																_
												Or	ıly th	ne n	ıum	ber	r of	bit	s ir	ndic	ate	d b	у В	ITIV	10D	Εw	rill k	oe ι	ıseo	d by	,				
												the	TIN	/ED	,																				

23.5.10 CC[2]

Address offset: 0x548

Capture/Compare register 2

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22 :	21 2	20 1	19 1	8 1	17 1	16 :	15 1	.4 1	13 1	.2	11 :	LO !	9	8	7	6	5	4	3	2 :	1 0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α,	Α,	Α	A	Α.	Α.	Д	Α	A ,	4	Α	Α	Α	Α	Α	A	Δ ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			
Α	RW	СС										Cap	tur	e/C	om	par	e va	alue	•															

Only the number of bits indicated by BITMODE will be used by the TIMER.

23.5.11 CC[3]

Address offset: 0x54C

Capture/Compare register 3



Bit	number		31	1 30	29	9 2	8 2	27 2	26	25	24	23 2	22 2	21 2	0 1	9 1	8 17	16	15	14	13	12	11 :	.0	9	8	7	6	5	4	3	2 1	L 0
Id			Α	Α	. 4	۱ ۸	Д	Α	Α	Α	Α	Α	A	Α ,	ДД		A	Α	Α	Α	Α	Α	Α	Δ.	Α	Α	Α	Α	Α	Α	Α /	A 4	A A
Res	et 0x00000000		0	0	0) (0	0	0	0	0	0	0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0
Id	RW Field	Value Id	V:	alue	_							Des	crip	tio	n																		
	NVV FIEIU	value lu	•		•								٠ ٦																				
Α	RW CC	value lu	•													are	valı	ue															

the TIMER.

23.5.12 CC[4]

Address offset: 0x550

Capture/Compare register 4

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	9 18	3 17	7 16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 A	. A	Α	Α	Α	Α	ДД	Α	Α	Α	Α	Α	Α	Α	Α /	4 Α	A
Res	et 0x(0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																	
Α	RW	CC										Cap	otur	e/C	omp	are	val	ue														
												On	ly th	ne n	umb	oer o	of b	its i	ndic	ate	d by	BITI	MOE	DE w	/ill k	oe u	ised	d by	,			
												the	TIN	ИER																		

23.5.13 CC[5]

Address offset: 0x554

Capture/Compare register 5

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 1	14 :	13 1	12 1	.1 1	0 9	9 8	3 7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	4 Α	۸ ۸	۸ ۸	4 Δ	A	A	Α	Α	Α	Α	Α
Res	et 0x(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	CC										Ca	ptu	re/C	Com	npai	re v	alu	9															
												_		L				le te.		J:			חוד			1	l ba							

Only the number of bits indicated by BITMODE will be used by the TIMER.

23.6 Electrical specification

23.6.1 Timers Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{TIMER_1M}	Run current with 1 MHz clock input (PCLK1M)	3	5	8	μΑ
I _{TIMER_16M}	Run current with 16 MHz clock input (PCLK16M)	50	70	120	μΑ
t _{TIMER,START}	Time from START task is given until timer starts counting		0.25		μs



24 RTC — Real-time counter

The Real-time counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK).

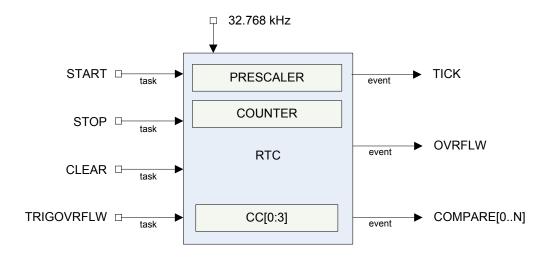


Figure 52: RTC block schematic

The RTC module features a 24-bit COUNTER, a 12-bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

24.1 Clock source

The RTC will run off the LFCLK.

The COUNTER resolution will therefore be $30.517 \,\mu s$. Depending on the source, the RTC is able to run while the HFCLK is OFF and PCLK16M is not available.

The software has to explicitely start LFCLK before using the RTC.

See CLOCK — Clock control on page 141 for more information about clock sources.

24.2 Resolution versus overflow and the PRESCALER

Counter increment frequency:

```
f_{RTC} [kHz] = 32.768 / (PRESCALER + 1 )
```

The PRESCALER register is read/write when the RTC is stopped. The PRESCALER register is read-only once the RTC is STARTed. Writing to the PRESCALER register when the RTC is started has no effect.

The PRESCALER is restarted on START, CLEAR and TRIGOVRFLW, that is, the prescaler value is latched to an internal register (<<PRESC>>) on these tasks.

Examples:

1. Desired COUNTER frequency 100 Hz (10 ms counter period)

 $f_{RTC} = 99.9 \text{ Hz}$



10009.576 µs counter period

2. Desired COUNTER frequency 8 Hz (125 ms counter period)

PRESCALER = round(32.768 kHz / 8 Hz) - 1 = 4095

 $f_{RTC} = 8 Hz$

125 ms counter period

Table 38: RTC resolution versus overflow

Prescaler	Counter resolution	Overflow
0	30.517 μs	512 seconds
28-1	7812.5 μs	131072 seconds
2 ¹² -1	125 ms	582.542 hours

24.3 COUNTER register

The COUNTER increments on LFCLK when the internal PRESCALER register (<<PRESC>>) is 0x00. <<PRESC>> is reloaded from the PRESCALER register. If enabled, the TICK event occurs on each increment of the COUNTER. The TICK event is disabled by default.

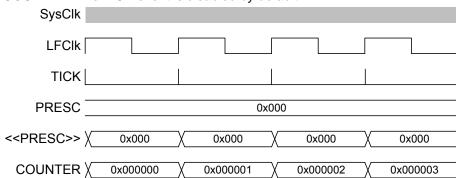


Figure 53: Timing diagram - COUNTER_PRESCALER_0

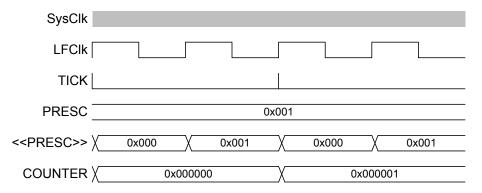


Figure 54: Timing diagram - COUNTER_PRESCALER_1

24.4 Overflow features

The TRIGOVRFLW task sets the COUNTER value to 0xFFFFF0 to allow SW test of the overflow condition.

OVRFLW occurs when COUNTER overflows from 0xFFFFFF to 0.

Important: The OVRFLW event is disabled by default.

24.5 TICK event

The TICK event enables low power "tick-less" RTOS implementation as it optionally provides a regular interrupt source for a RTOS without the need to use the ARM® SysTick feature.



Using the RTC TICK event rather than the SysTick allows the CPU to be powered down while still keeping RTOS scheduling active.

Important: The TICK event is disabled by default.

24.6 Event control feature

To optimize RTC power consumption, events in the RTC can be individually disabled to prevent PCLK16M and HFCLK being requested when those events are triggered. This is managed using the EVTEN register.

For example, if the TICK event is not required for an application, this event should be disabled as it is frequently occurring and may increase power consumption if HFCLK otherwise could be powered down for long durations.

This means that the RTC implements a slightly different task and event system compared to the standard system described in *Peripheral interface* on page 59. The RTC task and event system is illustrated in *Figure 55: Tasks, events and interrupts in the RTC* on page 302.

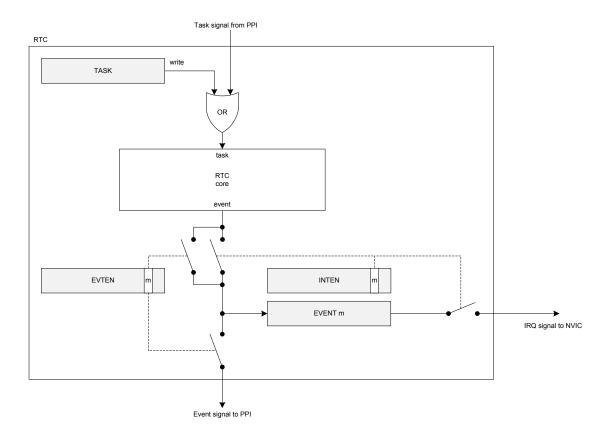


Figure 55: Tasks, events and interrupts in the RTC

24.7 Compare feature

There are a number of Compare registers.

For more information, see *Registers* on page 306.

When setting a compare register, the following behavior of the RTC compare event should be noted:

If a CC register value is 0 when a CLEAR task is set, this will not trigger a COMPARE event.



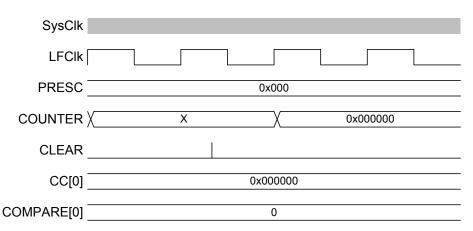


Figure 56: Timing diagram - COMPARE_CLEAR

• If a CC register is N and the COUNTER value is N when the START task is set, this will not trigger a COMPARE event.

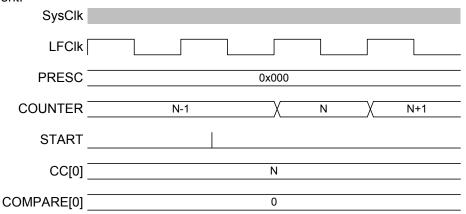


Figure 57: Timing diagram - COMPARE_START

• COMPARE occurs when a CC register is N and the COUNTER value transitions from N-1 to N.

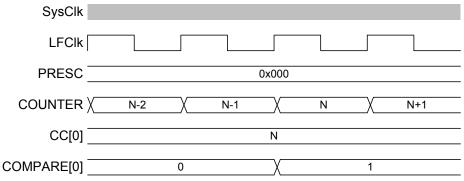


Figure 58: Timing diagram - COMPARE

• If the COUNTER is N, writing N+2 to a CC register is guaranteed to trigger a COMPARE event at N+2.



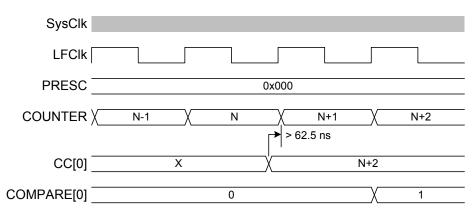


Figure 59: Timing diagram - COMPARE_N+2

• If the COUNTER is N, writing N or N+1 to a CC register may not trigger a COMPARE event.

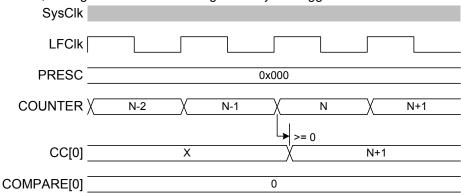


Figure 60: Timing diagram - COMPARE_N+1

• If the COUNTER is N and the current CC register value is N+1 or N+2 when a new CC value is written, a match may trigger on the previous CC value before the new value takes effect. If the current CC value greater than N+2 when the new value is written, there will be no event due to the old value.

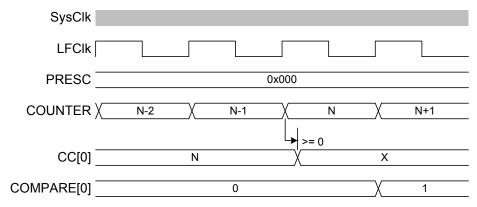


Figure 61: Timing diagram - COMPARE_N-1

24.8 TASK and EVENT jitter/delay

Jitter or delay in the RTC is due to the peripheral clock being a low frequency clock (LFCLK) which is not synchronous to the faster PCLK16M.

Registers in the peripheral interface, part of the PCLK16M domain, have a set of mirrored registers in the LFCLK domain. For example, the COUNTER value accessible from the CPU is in the PCLK16M domain and is latched on read from an internal register called COUNTER in the LFCLK domain. COUNTER is the register which is actually modified each time the RTC ticks. These registers must be synchronised between clock domains (PCLK16M and LFCLK).

The following is a summary of the jitter introduced on tasks and events. Figures illustrating jitter follow.



Table 39: RTC jitter magnitudes on tasks

 Task
 Delay

 CLEAR, STOP, START, TRIGOVRFLOW
 +15 to 46 μs

Table 40: RTC jitter magnitudes on events

Operation/Function	Jitter
START to COUNTER increment	+/- 15 μs
COMPARE to COMPARE 19	+/- 62.5 ns

1. CLEAR and STOP (and TRIGOVRFLW; not shown) will be delayed as long as it takes for the peripheral to clock a falling edge and rising of the LFCLK. This is between 15.2585 μ s and 45.7755 μ s – rounded to 15 μ s and 46 μ s for the remainder of the section.

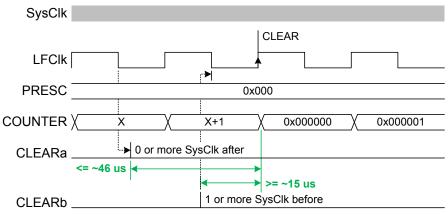


Figure 62: Timing diagram - DELAY_CLEAR

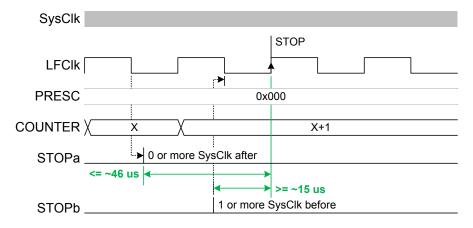


Figure 63: Timing diagram - DELAY_STOP

2. The START task will start the RTC. Assuming that the LFCLK was previously running and stable, the first increment of COUNTER (and instance of TICK event) will be typically after 30.5 μs +/-15 μs. In some cases, in particular if the RTC is STARTed before the LFCLK is running, that timing can be up to ~250 μs. The software should therefore wait for the first TICK if it has to make sure the RTC is running. Sending a TRIGOVRFLW task sets the COUNTER to a value close to overflow. However, since the update of COUNTER relies on a stable LFCLK, sending this task while LFCLK is not running will start LFCLK, but the update will then be delayed by the same amount of time of up to ~250 us. The figures show the smallest and largest delays to on the START task which appears as a +/-15 μs jitter on the first COUNTER increment.

Note: 32.768 kHz clock jitter is additional to the numbers provided above.

 $^{^{19}\,}$ Assumes RTC runs continuously between these events.



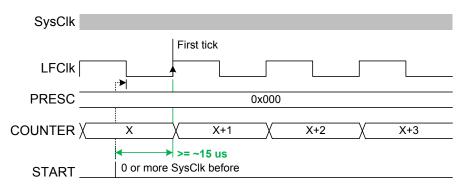


Figure 64: Timing diagram - JITTER_START-

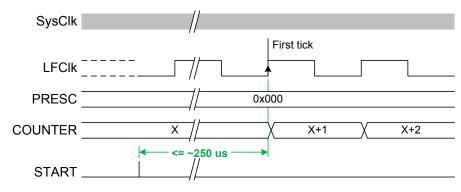


Figure 65: Timing diagram - JITTER_START+

24.9 Reading the COUNTER register

To read the COUNTER register, the internal <<COUNTER>> value is sampled.

To ensure that the <<COUNTER>> is safely sampled (considering an LFCLK transition may occur during a read), the CPU and core memory bus are halted for three cycles by lowering the core PREADY signal. The Read takes the CPU 2 cycles in addition resulting in the COUNTER register read taking a fixed five PCLK16M clock cycles.

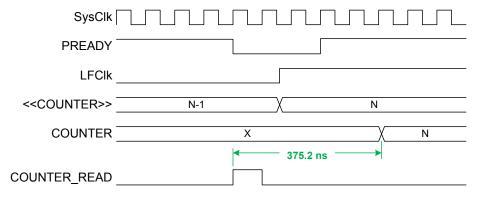


Figure 66: Timing diagram - COUNTER_READ

24.10 Registers

Table 41: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000B000	RTC	RTC0	Real-time counter 0	CC[02] implemented, CC[3] not
				implemented
0x40011000	RTC	RTC1	Real-time counter 1	CC[03] implemented



Base address	Peripheral	Instance	Description	Configuration
0x40024000	RTC	RTC2	Real-time counter 2	CC[03] implemented

Table 42: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start RTC COUNTER
TASKS_STOP	0x004	Stop RTC COUNTER
TASKS_CLEAR	0x008	Clear RTC COUNTER
TASKS_TRIGOVRFLW	0x00C	Set COUNTER to 0xFFFFF0
EVENTS_TICK	0x100	Event on COUNTER increment
EVENTS_OVRFLW	0x104	Event on COUNTER overflow
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
EVTEN	0x340	Enable or disable event routing
EVTENSET	0x344	Enable event routing
EVTENCLR	0x348	Disable event routing
COUNTER	0x504	Current COUNTER value
PRESCALER	0x508	12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)).Must be written when RTC is
		stopped
CC[0]	0x540	Compare register 0
CC[1]	0x544	Compare register 1
CC[2]	0x548	Compare register 2
CC[3]	0x54C	Compare register 3

24.10.1 INTENSET

Address offset: 0x304

Enable interrupt

		•			
Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
Α	RW	TICK			Write '1' to Enable interrupt for TICK event
					See EVENTS_TICK
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	OVRFLW			Write '1' to Enable interrupt for OVRFLW event
					See EVENTS_OVRFLW
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	COMPARE0			Write '1' to Enable interrupt for COMPARE[0] event
					See EVENTS_COMPARE[0]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	COMPARE1			Write '1' to Enable interrupt for COMPARE[1] event
					See EVENTS_COMPARE[1]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled



Bit r	numbe	er		31	30 2	9 2	8 27	26	25 2	4 2	23 22	21	. 20	19	18	17	16	15	14 1	3 12	11	10	9	8	7	6	5	4 3	3 2	1	0
Id														F	Ε	D	С													В	Α
Res	et 0x0	0000000		0	0 (0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue					D	Descr	ipti	ion																		
Ε	RW	COMPARE2								٧	Vrite	'1'	to E	Enal	ble	inte	erru	pt f	or C	OME	PAR	E[2]	eve	ent							
										S	iee <i>E</i>	VEN	NTS_	_co	МР	PAR	E[2]														
			Set	1						Е	nabl	e																			
			Disabled	0						R	Read	Dis	sabl	ed																	
			Enabled	1						R	Read	En	able	ed																	
F	RW	COMPARE3								٧	Vrite	'1'	to E	Enal	ble	inte	erru	pt f	or C	OME	PAR	E[3]	eve	ent							
										S	iee <i>E</i>	VEN	VTS_	_co	МР	PAR	E[3]	1													
			Set	1						Ε	nabl	e																			
			Disabled	0						R	Read	Dis	sabl	ed																	
			Enabled	1						R	Read	En	able	ed																	

24.10.2 INTENCLR

Address offset: 0x308

Disable interrupt			
Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			F E D C
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW TICK			Write '1' to Disable interrupt for TICK event
			See EVENTS_TICK
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW OVRFLW			Write '1' to Disable interrupt for OVRFLW event
			See EVENTS_OVRFLW
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW COMPAREO			Write '1' to Disable interrupt for COMPARE[0] event
			See EVENTS_COMPARE[0]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW COMPARE1			Write '1' to Disable interrupt for COMPARE[1] event
			See EVENTS_COMPARE[1]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW COMPARE2			Write '1' to Disable interrupt for COMPARE[2] event
			See EVENTS_COMPARE[2]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
F RW COMPARE3			Write '1' to Disable interrupt for COMPARE[3] event
			See EVENTS_COMPARE[3]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled



24.10.3 EVTEN

Address offset: 0x340

Enable or disable event routing

Bit	numbe	er		31 30	29	28.2	7 20	5 25	24	23	22 21	1 2	0 1	19 1	8 1	7 1	6 1	5 14	13	12	11	10	9	8 7	6	- 5	4	3	2	1 0
Id		•		01 00		202								F (- 10					,		J	·	J		ВА
	et 0x0	0000000		0 0	0	0 (0	0	0	0	0 0	0						0	0	0	0	0	0	0 0	0	0	0	0		0 0
Id	RW	Field	Value Id	Value						Des	script	ion	1																	
Α	RW	TICK									able o					nt i	rout	ing	for	TIC	K ev	ent								
			Disabled	0							able																			
			Enabled	1							able																			
В	RW	OVRFLW								Ena	able o	r d	lisa	ble	eve	nt i	rout	ing	for	OVI	RFLV	V ev	/ent							
																		Ĭ												
			Disabled	0							e <i>EVEI</i> able	N/2	s_c	JVK	FLVI	,														
			Enabled	1							able																			
С	D\A/	COMPARE0	Enabled	1							able o	r d	lica	hlo	01/0	nt i	rout	ina	for	COI	MDA	DEL	Λ1 c	von						
C	IVV	COMPARED																.iiig	101	COI	VIFA	INL	oj e	ven						
											e EVEI	NTS	S_C	CON	1PA	RE[0]													
			Disabled	0							able																			
			Enabled	1							able																			
D	RW	COMPARE1								Ena	able o	r d	lisa	ble	eve	nt i	rout	ing	for	COI	MPA	RE[1] e	ven	t					
										See	e EVEI	NTS	s_c	CON	1PA	RE[.	1]													
			Disabled	0						Dis	able																			
			Enabled	1						Ena	able																			
E	RW	COMPARE2								Ena	able o	r d	lisa	ble	eve	nt i	rout	ing	for	COI	MPA	RE[2] e	ven	t					
										See	e EVEI	NTS	s c	CON	1PA	RE[.	21													
			Disabled	0							able		-			•														
			Enabled	1						Ena	able																			
F	RW	COMPARE3								Ena	able o	r d	lisa	ble	eve	nt i	rout	ing	for	COI	MPA	RE[3] e	ven	t					
										Sec	e <i>EVEI</i>	NT	5 /	COM	1ΡΔ	RFſ	21													
			Disabled	0							able	412		JOIV	icAl	nL[.	<i>-</i>]													
			Enabled	1							able																			
			LITUDICU	1						LIIC	שוטוכ																			

24.10.4 EVTENSET

Address offset: 0x344 Enable event routing

Bit r	numbe	r		31	30 2	9 28	3 27	26 2	5 2	4 23 2	22 2	21 20	19	9 18	17	16	15	14	13 1	2 11	. 10	9	8	7	6 5	4	3	2	1 0
Id													F	Е	D	С													ВА
Rese	et 0x0	0000000		0	0 0	0	0	0 0	0	0 0	0 (0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue					Des	crip	tion																	
Α	RW	TICK								Writ	e '1	1' to	Ena	ble	eve	nt r	rout	ing	for '	TICK	eve	nt							
										See	EVE	ENTS	_TI	СК															
			Set	1						Enal	ble																		
			Disabled	0						Read	d: D	Disab	led																
			Enabled	1						Read	d: E	nabl	ed																
В	RW	OVRFLW								Writ	e '1	1' to	Ena	able	eve	nt i	rout	ing	for	OVR	FLW	eve	ent						
										See	EVE	ENTS	_0	VRF	LW														
			Set	1						Enal	ble																		
			Disabled	0						Read	d: D	Disab	led																
			Enabled	1						Read	d: E	nabl	ed																
С	RW	COMPARE0								Writ	e '1	1' to	Ena	ble	eve	nt i	rout	ing	for	COM	PAR	RE[O] eve	ent					
										See	EVE	ENTS	_cc	ЭМЕ	PAR	E[0]	1												
			Set	1						Enal	ble																		



Bit n	umber		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F E D C B A
Rese	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW COMPARE1			Write '1' to Enable event routing for COMPARE[1] event
				See EVENTS_COMPARE[1]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Е	RW COMPARE2			Write '1' to Enable event routing for COMPARE[2] event
				See EVENTS_COMPARE[2]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW COMPARE3			Write '1' to Enable event routing for COMPARE[3] event
				C FMENTS COMPARE[2]
		C-1	4	See EVENTS_COMPARE[3]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

24.10.5 EVTENCLR

Address offset: 0x348 Disable event routing

Bit r	numbe	er		31 30 29 28 27 26	25 24	23 2	22 21 2	20	19 1	18	17 1	16	15 :	14 1	13 :	l2 1	1 10	9	8	7	6	5	4 3	3 2	1	0
Id									F	Ε	D	С													В	Α
Res	et 0x0	0000000		0 0 0 0 0 0	0 0	0 (0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Value		Desc	criptio	n																		
Α	RW	TICK				Writ	te '1' t	o D	Disab	ole	evei	nt ı	rout	ting	for	TIC	K ev	ent								
						See	EVENT	TS_	TICK	K																
			Clear	1		Disa	ble																			
			Disabled	0		Read	d: Disa	able	ed																	
			Enabled	1		Read	d: Enal	ble	d																	
В	RW	OVRFLW				Writ	te '1' t	оΩ	Disab	ole (evei	nt ı	rout	ting	for	OVI	RFLV	V ev	ent							
						See	EVENT	TS_	OVE	RFL	w															
			Clear	1		Disa	ble																			
			Disabled	0		Read	d: Disa	able	ed																	
			Enabled	1		Read	d: Enal	ble	d																	
С	RW	COMPARE0				Writ	te '1' te	оΣ	Disab	ole	eve	nt ı	rout	ting	for	COI	MPA	RE[)] ev	/en	t					
						See	EVENT	TS_	CON	ИΡΑ	ARE _i	[0]														
			Clear	1		Disa	ble																			
			Disabled	0		Read	d: Disa	able	ed																	
			Enabled	1		Read	d: Enal	ble	d																	
D	RW	COMPARE1				Writ	te '1' t	o D	Disab	ole	eve	nt ı	rout	ting	for	COI	MPA	RE[1] ev	/en	t					
						See	EVENT	TS_	CON	ИΡΑ	ARE _i	[1]														
			Clear	1		Disa	ble																			
			Disabled	0		Read	d: Disa	ble	ed																	
			Enabled	1		Read	d: Enal	ble	d																	
Ε	RW	COMPARE2				Writ	te '1' t	o D	Disab	ole	eve	nt ı	rout	ting	for	COI	MPA	RE[2] ev	/en	t					
						See	EVENT	TS_	CON	ИΡΑ	ARE _i	[2]														
			Clear	1		Disa	ble																			
			Disabled	0		Read	d: Disa	ble	ed																	
			Enabled	1		Read	d: Enal	ble	d																	



Bitı	numbe	r		31	1 30	29	2	8 27	7 2	6 2	5 2	24 2	23 :	22	21	20	19	9 1	8 :	17	16	15	14	13	3 12	2 13	10	9	8	7	6	5	4	3	2	1	0
Id																	F	: E		D	С															В	Α
Res	et 0x0	0000000		0	0	0	C	0) (0 () (0	0	0	0	0	0) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•						ı	Des	cri	ipti	on																					
F	RW	COMPARE3										١	Vri	te	'1'	to I	Dis	abl	e e	eve	nt	roı	ıtin	g f	or (ON	ΛPΑ	RE	3] (eve	nt						
												9	See	E١	/EΝ	ITS	_C	OM	IP/	4RI	[3]	1															
			Clear	1								1	Disa	abl	e																						
			Disabled	0								F	Rea	d:	Dis	abl	led	ı																			
			Enabled	1								ı	Rea	d:	Ena	abl	ed																				

24.10.6 COUNTER

Address offset: 0x504

Current COUNTER value

Bit	numb	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A	A A A A A A A A A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description	
Α	R	COUNTER		Counter value	

24.10.7 PRESCALER

Address offset: 0x508

12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)). Must be written when RTC is stopped

Bit	numbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	.0 9	9	8	7	6	5	4	3	2 :	1 0
Id																								Α	Δ ,	4	A	Α	Α	Α	Α	A ,	Δ ,	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																			
Α	RW	PRESCALER										Pre	sca	ler	valı	ue																		

24.10.8 CC[0]

Address offset: 0x540 Compare register 0

Bit	nu	mbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	C
Id													Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ
Re	set	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D
Id	1	RW	Field	Value Id	Va	alue							De	scr	iptio	on																				
Α	-	RW	COMPARE										Co	mp	are	val	ue																			_

24.10.9 CC[1]

Address offset: 0x544 Compare register 1

Bitı	numbe	er		31	. 30	29	28	27	26 :	25 :	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue	:						Des	cri	ptic	on																			
Α	RW	COMPARE										Cor	np	are	val	ue																		

24.10.10 CC[2]

Address offset: 0x548 Compare register 2



Bit n	umbe	r		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ Α	A A
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																			
Α	RW	COMPARE										Coi	mpa	are	val	ue																		

24.10.11 CC[3]

Address offset: 0x54C Compare register 3

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	۱,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	on																			
Α	RW	COMPARE										Cor	npa	are	val	ue																		

24.11 Electrical specification

24.11.1 RTC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
Into	Run current Real Time Counter (LECLK source)		0.1		пΑ



25 RNG — Random number generator

The Random number generator (RNG) generates true non-deterministic random numbers based on internal thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

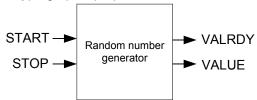


Figure 67: Random number generator

The RNG is started by triggering the START task and stopped by triggering the STOP task. When started, new random numbers are generated continuously and written to the VALUE register when ready. A VALRDY event is generated for every new random number that is written to the VALUE register. This means that after a VALRDY event is generated the CPU has the time until the next VALRDY event to read out the random number from the VALUE register before it is overwritten by a new random number.

25.1 Bias correction

A bias correction algorithm is employed on the internal bit stream to remove any bias toward '1' or '0'. The bits are then queued into an eight-bit register for parallel readout from the VALUE register.

It is possible to enable bias correction in the CONFIG register. This will result in slower value generation, but will ensure a statistically uniform distribution of the random values.

25.2 Speed

The time needed to generate one random byte of data is unpredictable, and may vary from one byte to the next. This is especially true when bias correction is enabled.

25.3 Registers

Table 43: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000D000	RNG	RNG	Random number generator	

Table 44: Register Overview

Register	Offset	Description
TASKS_START	0x000	Task starting the random number generator
TASKS_STOP	0x004	Task stopping the random number generator
EVENTS_VALRDY	0x100	Event being generated for every new random number written to the VALUE register
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CONFIG	0x504	Configuration register
VALUE	0x508	Output random number

25.3.1 SHORTS

Address offset: 0x200 Shortcut register



В	t nu	ımbe	r		31	1 30	29	28	3 27	7 26	25	24	23	22	21	20	19 1	18 :	17 1	6 1	.5 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																																		Α
R	eset	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 () (0	0	0	0	0	0	0	0	0	0 (0	0
Id	l	RW	Field	Value Id	Va	alue							De	scri	ptic	n																		
Α		RW	VALRDY_STOP										Sh	orto	ut b	etv	vee	n V	ALR	DY	eve	nt a	nd :	STO	P ta	sk								
													Se	e <i>EV</i>	/EN	TS_	VAL	RD	Y an	d 7.	ASK	:S_S	TOF	•										
				Disabled	0								Dis	abl	e sh	ort	cut																	
				Enabled	1								En	able	sho	orto	cut																	

25.3.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31	1 30	29	2	8 2	7 :	26	25	24	23	3 2:	2 2	1 2	0 :	19	18	17	16	1	5 1	4 1	13 :	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																						Α
Res	et 0x0	0000000		0	0	0	C) ()	0	0	0	0	0) () (0	0	0	0	0	0) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue)							D	esc	rip	tio	n																					
Α	RW	VALRDY											W	rite	e '1	' tc	Er	nab	le i	int	err	upt	t fo	r V	ΆL	RD۱	۷ e۱	ven	t									
													Se	e E	VE	NT	S_1	/AL	.RE	ΟY																		
			Set	1									Er	nab	le																							
			Disabled	0									Re	ead	l: D	isal	ble	d																				
			Enabled	1									Re	ead	l: E	nab	le	ł																				
			Enabled	1									Re	ead	l: Ei	nat	oleo	d																				

25.3.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	iumbe	r		31	. 30	29	28	8 27	7 26	5 25	5 24	23	22	21	20	19	18	17	16	15	14	13	12 1	111	0 9	8	7	6	5	4	3	2	1 0
Id																																	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																		
Α	RW	VALRDY										W	rite	'1'	to [Disa	ble	int	errı	ıpt	for	VAI	.RD	ev /	ent								
												Se	e <i>E</i>	VEN	ITS_	VA.	LRE	ŊΥ															
			Clear	1								Di	sab	le																			
			Disabled	0								Re	ad:	Dis	abl	ed																	
			Enabled	1								Re	ad:	Ena	able	ed																	

25.3.4 CONFIG

Address offset: 0x504 Configuration register

Bit	numbe	r		3:	1 30	29	28	3 27	7 26	5 25	5 24	23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	•						De	escr	ipti	on																			
Α	RW	DERCEN										Bia	as c	orre	ecti	on																		
			Disabled	0								Di	sab	led																				
			Enabled	1								En	abl	ed																				

25.3.5 VALUE

Address offset: 0x508

Output random number



Bit number		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A R VALUE		[0255]	Generated random number

25.4 Electrical specification

25.4.1 RNG Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{RNG}	Run current, CPU sleeping.		500		μΑ
t _{RNG,START}	Time from setting the START task to generation begins. This is		128		μs
	a one-time delay on START signal and does not apply between				
	samples.				
t _{RNG,RAW}	Run time per byte without bias correction. Uniform distribution		30		μs
	of 0 and 1 is not guaranteed.				
t _{RNG,BC}	Run time per byte with bias correction. Uniform distribution		120		μs
	of 0 and 1 is guaranteed. Time to generate a byte cannot be				
	guaranteed.				



26 TEMP — Temperature sensor

The temperature sensor measures die temperature over the temperature range of the device. Linearity compensation can be implemented if required by the application.

Listed here are the main features for TEMP:

- Temperature range is greater than or equal to operating temperature of the device
- Resolution is 0.25 degrees

TEMP is started by triggering the START task.

When the temperature measurement is completed, a DATARDY event will be generated and the result of the measurement can be read from the TEMP register.

To achieve the measurement accuracy stated in the electrical specification, the crystal oscillator must be selected as the HFCLK source, see *CLOCK* — *Clock control* on page 141 for more information.

When the temperature measurement is completed, TEMP analog electronics power down to save power.

TEMP only supports one-shot operation, meaning that every TEMP measurement has to be explicitly started using the START task.

26.1 Registers

Table 45: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000C000	TEMP	TEMP	Temperature sensor	

Table 46: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start temperature measurement
TASKS_STOP	0x004	Stop temperature measurement
EVENTS_DATARDY	0x100	Temperature measurement complete, data ready
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
TEMP	0x508	Temperature in °C (0.25° steps)
A0	0x520	Slope of 1st piece wise linear function
A1	0x524	Slope of 2nd piece wise linear function
A2	0x528	Slope of 3rd piece wise linear function
A3	0x52C	Slope of 4th piece wise linear function
A4	0x530	Slope of 5th piece wise linear function
A5	0x534	Slope of 6th piece wise linear function
B0	0x540	y-intercept of 1st piece wise linear function
B1	0x544	y-intercept of 2nd piece wise linear function
B2	0x548	y-intercept of 3rd piece wise linear function
В3	0x54C	y-intercept of 4th piece wise linear function
B4	0x550	y-intercept of 5th piece wise linear function
B5	0x554	y-intercept of 6th piece wise linear function
ТО	0x560	End point of 1st piece wise linear function
T1	0x564	End point of 2nd piece wise linear function
T2	0x568	End point of 3rd piece wise linear function
T3	0x56C	End point of 4th piece wise linear function
T4	0x570	End point of 5th piece wise linear function



26.1.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	numbe	er		31	1 30	29	2	8 2	7 2	6 2	5 2	4 2	23 2	22	21	20	19	18	3 1	7 1	6 1	15	14	13	12	11	10	9	8	3 7	7	6	5	4	3	2	1	0
Id																																						Α
Res	et 0x0	0000000		0	0	0	0	0) () () (0	0	0	0	0	0	0	() ()	0	0	0	0	0	0	0	() ()	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•							Des	cri	pti	on																						
Α	RW	DATARDY										١	Wri	te	'1'	to E	na	ble	in	ter	rup	t f	or I	DA ⁻	TAF	RD۱	ev ev	/en	t									
												5	See	ΕV	⁄EN	TS_	DA	ATA	RL	ÒΥ																		
			Set	1								E	Ena	ble	•																							
			Disabled	0								F	Rea	d:	Dis	abl	ed																					
			Enabled	1								F	Rea	d:	Ena	able	ed																					

26.1.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	2 2:	1 20	1	9 1	8 1	.7 1	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Val	lue							De	esci	ript	ion																				
Α	RW	DATARDY										W	rite	'1	' to	Dis	abl	e i	nte	rru	pt	for	DA	TAF	RDY	ev	ent								
												Se	e E	VE	NTS	_D	ΑT	4RI	DΥ																
			Clear	1								Di	sab	le																					
			Disabled	0								Re	ad	: Di	sab	led	ı																		
			Enabled	1								Re	ad	: Er	nabl	ed																			

26.1.3 TEMP

Address offset: 0x508

Temperature in °C (0.25° steps)

Bit	numbe	er		31	30	29	28	27	26	25 :	24	23 :	22 2	1 2	20 1	19 1	L8 1	.7 1	16 :	15 :	14 1	3 1:	2 11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ,	A	Α,	A ,	Α,	Α	Α	A	λ Δ	A	Α	Α	Α	Α	Α	Α	Α	A A	\ <i>A</i>	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 (0 (0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	R	TEMP														in °	C (C	.25	s° st	tep	s)												
				Value Description Temperature in °C (0.25° steps) Result of temperature measurement. Die temperature in °C, 2's complement format, 0.25 °C steps																													
												Dec	isio	n p	oint	t: D	AT/	ARD	Υ														

26.1.4 A0

Address offset: 0x520

Slope of 1st piece wise linear function

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 1	1 10 9 8 7 6 5 4 3 2 1 0
Id			,	
Reset 0x00000326		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 0 0 1 0 0 1 1 0
Id RW Field	Value Id	Value	Description	
A RW A0			Slope of 1st piece wise linear function	

26.1.5 A1

Address offset: 0x524



Slope of 2nd piece wise linear function

Bi	t num	oer					31	. 30 2	9 2	28 2	7 26	25	24	23 2	22 2	1 20	0 19	18	17	16	15	14 1	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id																								Α	Α	Α	Α	Α	Α	Α.	A A	4 Α	A	A
R	eset O	(0000	00348				0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	1	1	0	1	0	0 :	1 0	0	0
Id	RV	V Fi	eld		Value	ld	Va	lue						Des	crip	tion	,																	
Α	RV	/ A1	l	Value Id										Slor	e of	f 2n	d pi	ece	wis	e lin	ear	fun	ction	n										

26.1.6 A2

Address offset: 0x528

Slope of 3rd piece wise linear function

Bit	numbe	r		31 30 29 28 27	7 26 25 24 23 22 21 20 19 1	8 17 16 15 14 13 12	11 10 9 8	7 (6 5	4 3	2 1	0
Id							A A A A	(A)	А А	A A	A A	Α
Res	et 0x0	00003AA		0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 1 1	. 1 (0 1	0 1	0 1	0
Id	RW	Field	Value Id	Value	Description							
Α	RW	A2			Slope of 3rd piece	e wise linear function						

26.1.7 A3

Address offset: 0x52C

Slope of 4th piece wise linear function

Bitı	numb	er		31	30 2	9 2	28 27	7 26	25	24	23	22 2	21 2	20 1	9 1	8 1	7 10	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id																						Α	Α	Α	Α	Α	Α	Α	Α /	A A	Α	Α
Res	et 0x(000040E		0	0 0) (0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	1	0	0	0	0	0	0	l 1	1	0
Id	RW	Field	Value Id	Va	ue						Des	crip	tio	n																		
Α	RW	A3									Slot	oe o	f 4t	h p	iece	wi	se li	nea	r fu	ınct	ion											

26.1.8 A4

Address offset: 0x530

Slope of 5th piece wise linear function

																								_			_			_
Bit	numb	er			31 3	10 29	28 27	/ 26	25 2	24 2	3 22	21	20	19 1	8 17	16	15	14 1	.3 12	2 11	10	9	8	/	6 5	> 4	3	2	1	U
Id																				Α	Α	Α	A A	Α.	Α Α	4 A	Α.	Α	Α.	Α
Re	set 0x	000004	BD		0	0 0	0 0	0	0	0 (0	0	0	0 (0	0	0	0	0 0	0	1	0	0	1	0 :	l 1	1	1	0	1
Id	RW	Field		Value Id	Valu	ie				D	escr	iptio	on																	
Α	RW	v Field Value Id V A4								S	lope	of 5	th p	iece	wis	e lir	near	fun	ction											

26.1.9 A5

Address offset: 0x534

Slope of 6th piece wise linear function

D'I		24 20 20 20 27 26	25 24 22 22 24 20 40 40 47 46 45 44 42 42 44 4	00076540010
Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 1	098/6543210
Id			A A	A A A A A A A A A
Reset 0x000005A3		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1 0 1 1 0 1 0 0 0 1 1
Id RW Field	Value Id	Value	Description	
A RW A5			Slope of 6th piece wise linear function	

26.1.10 B0

Address offset: 0x540

y-intercept of 1st piece wise linear function



26.1.11 B1

Address offset: 0x544

y-intercept of 2nd piece wise linear function

Bit r	numbe	er		31	30 2	29 :	28 2	7 20	5 25	24	23	22	21	20	19	18	17	16	15	14 :	13 1	12 1	.1 1	0 9	8 (7	6	5	4	3	2	1 ()
Id																					A	Α.	4 Α	A A	. 4	A	. A	A	Α	Α	Α	Α ,	4
Res	et 0x0	0003FBE		0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1 1	۱ 1	. 1	. 1	0	1	1	1	1	1 ()
Id	RW	Field	Value Id	Va	lue						De	scr	ipti	on																			ı
Α	RW	B1	y-intercept of 2nd piece wise linear function												7																		

26.1.12 B2

Address offset: 0x548

y-intercept of 3rd piece wise linear function

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9 8 7 6	5 4 3 2 1 0
Id				A A A A A A A	AAAAAA
Reset 0x00003FBE		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1 1 1 0	1 1 1 1 1 0
ld RW Field	Value Id	Value	Description		
A RW B2			y-intercept of 3rd pie	ece wise linear function	

26.1.13 B3

Address offset: 0x54C

y-intercept of 4th piece wise linear function

Bit r	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	! 1	1 0
Id																						Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A		4 A
Res	et 0x0	0000012		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0 0) 1	1 0
Id	RW	Field	Value Id	Va	alue							Des	cri	otic	n																			
Α	RW	В3										y-ir	iter	сер	t o	f 4t	h p	iece	e w	ise l	ine	ar f	unc	tio	n									

26.1.14 B4

Address offset: 0x550

y-intercept of 5th piece wise linear function

Bit numb	er		31	30 2	9 28	27 2	26 2	5 2	4 23	3 22	21	20	19	18 1	17 1	6 1	5 14	1 13	12	11	10	9	8	7	6 !	5 4	3	2	1)
Id																		Α	Α	Α	Α	Α	Α	Α	A A	4 Α	A	Α	Α.	٨
Reset 0x0	00000124		0	0 0	0	0	0 (0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	1	0	0 :	1 (0	1	0	,
ld RW	Field	Value Id	Val	ue					D	escr	iptio	on																		ı
A RW	B4								у-	inte	rcep	ot o	f 5tl	ı pi	ece	wis	e lin	ear	fun	ctio	n									7

26.1.15 B5

Address offset: 0x554

y-intercept of 6th piece wise linear function

Bit	numb	er		31	30	29	28 2	7 2	6 25	5 2	4 2	3 2:	2 2	1 2	0 1	9 1	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id																					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Д Д	A	Α
Res	et 0x0	000027C		0	0	0	0 () (0) (0	0) (0) (0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1 1	. 0	0
Id	RW	Field	Value Id	Va	lue						D	esc	rip	tion	1																		
^	DIA	DE													- 4	CTL				11		c	_4:_	_									

RW B5 y-intercept of 6th piece wise linear function



26.1.16 TO

Address offset: 0x560

End point of 1st piece wise linear function

Bit nu	ımber		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9 8	7 6 5	4 3 2	1 0
Id						A A A	A A A .	А А
Reset	: 0x000000E2		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0000000000	1 1 1	0 0 0	1 0
Id	RW Field	Value Id	Value	Description				
Α	RW TO			End point of 1st piece	e wise linear function			

26.1.17 T1

Address offset: 0x564

End point of 2nd piece wise linear function

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	00000000
Id RW Field	Value Id	Value	Description		
A RW T1			End point of 2nd pie	ce wise linear function	

26.1.18 T2

Address offset: 0x568

End point of 3rd piece wise linear function

Bit	numbe	er		31	30 2	9 :	28	27	26	25	24	23	22	21	20 :	19 :	18	17 :	16	15 :	14 1	.3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 ()
Id																											Α	Α	Α	Α	Α .	Δ,	A A	4
Res	et 0x0	0000019		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	1	1	0 (0 1	Ĺ
Id	RW	Field	Value Id	Va	lue							Des	scrip	otic	n																			ı
Α	RW	T2										Enc	d po	int	of 3	Brd	pie	ce v	vise	e lin	ear	fur	ctic	n										٠

26.1.19 T3

Address offset: 0x56C

End point of 4th piece wise linear function

Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A
Reset 0x0000003C		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 0
ld RW Field	Value Id	Value	Description
A RW T3			End point of 4th piece wise linear function

26.1.20 T4

Address offset: 0x570

End point of 5th piece wise linear function

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000050		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	000000000	0 0 1 0 1 0 0 0 0
ld RW Field	Value Id	Value	Description		
A RW T4			End point of 5th piece	e wise linear function	

End point of 5th piece wise linear function



26.2 Electrical specification

26.2.1 Temperature Sensor Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{TEMP}	Time required for temperature measurement		36		μs
T _{TEMP,RANGE}	Temperature sensor range	-40		85	°C
T _{TEMP,ACC}	Temperature sensor accuracy	-5		5	°C
T _{TEMP,RES}	Temperature sensor resolution		0.25		°C
T _{TEMP,STB}	Sample to sample stability at constant device temperature	-0.25		0.25	°C
T _{TEMP,OFFST}	Sample offset at 25°C	-2.5		2.5	°C



27 ECB — AES electronic codebook mode encryption

The AES electronic codebook mode encryption (ECB) can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. The ECB encryption block supports 128 bit AES encryption (encryption only, not decryption).

AES ECB operates with EasyDMA access to system Data RAM for in-place operations on cleartext and ciphertext during encryption. ECB uses the same AES core as the CCM and AAR blocks and is an asynchronous operation which may not complete if the AES core is busy.

AES ECB features:

- 128 bit AES encryption
- · Supports standard AES ECB block encryption
- Memory pointer support
- DMA data transfer

AES ECB performs a 128 bit AES block encrypt. At the STARTECB task, data and key is loaded into the algorithm by EasyDMA. When output data has been written back to memory, the ENDECB event is triggered.

AES ECB can be stopped by triggering the STOPECB task.

27.1 Shared resources

The ECB, CCM, and AAR share the same AES module. The ECB will always have lowest priority and if there is a sharing conflict during encryption, the ECB operation will be aborted and an ERRORECB event will be generated.

27.2 EasyDMA

The ECB implements an EasyDMA mechanism for reading and writing to the Data RAM. This DMA cannot access the program memory or any other parts of the memory area except RAM.

If the ECBDATAPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The EasyDMA will have finished accessing the Data RAM when the ENDECB or ERRORECB is generated.

27.3 ECB data structure

Input to the block encrypt and output from the block encrypt are stored in the same data structure. ECBDATAPTR should point to this data structure before STARTECB is initiated.

Table 47: ECB data structure overview

Property	Address offset	Description
KEY	0	16 byte AES key
CLEARTEXT	16	16 byte AES cleartext input block
CIPHERTEXT	32	16 byte AES ciphertext output block



27.4 Registers

Table 48: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000E000	ECB	ECB	AES electronic code book (ECB) mode bloc	k
			encryption	

Table 49: Register Overview

Register	Offset	Description
TASKS_STARTECB	0x000	Start ECB block encrypt
TASKS_STOPECB	0x004	Abort a possible executing ECB operation
EVENTS_ENDECB	0x100	ECB block encrypt complete
EVENTS_ERRORECB	0x104	ECB block encrypt aborted because of a STOPECB task or due to an error
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ECBDATAPTR	0x504	ECB block encrypt memory pointers

27.4.1 INTENSET

Address offset: 0x304

Enable interrupt

	numbe	r		31	30	29 2	28 2	7 2	6 2	5 24	4 2	3 22	21	20	19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id																																В	Α
Res	et 0x0	0000000		0	0	0	0 (0 (0 0	0) (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0
Id	RW	Field	Value Id	Val	ue						D	escr	ipti	on																			
Α	RW	ENDECB									٧	Vrite	'1'	to E	Ena	ble	int	errı	ıpt	for	EN	DEC	Ве	ven	t								
											S	ee <i>E</i>	VEN	NTS_	_EN	IDE	СВ																
			Set	1							Ε	nabl	e																				
			Disabled	0							R	lead:	Dis	abl	ed																		
			Enabled	1							R	lead:	En	able	ed																		
В	RW	ERRORECB									٧	Vrite	'1'	to E	Ena	ble	int	errı	ıpt	for	ER	ROF	RECI	3 ev	ent								
											S	ee <i>E</i>	VEN	NTS_	_ER	RO	REC	В															
			Set	1							Ε	nabl	e																				
			Disabled	0							R	lead:	Dis	abl	ed																		
			Enabled	1							R	lead:	En	able	ed																		

27.4.2 INTENCLR

Address offset: 0x308 Disable interrupt

Bit r	numbe	r		31	. 30	29	28 2	27 :	26 2	25 2	24 2	23 22	2 21	20	19	18	17	16	15	14 1	13 :	12 :	11 1	.0 9	8	7	6	5	4	3	2	1 0
Id																																ВА
Rese	et 0x0	0000000		0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue						C	Desc	ripti	on																		
Α	RW	ENDECB									٧	Vrite	e '1'	to D	isal	ble	inte	erru	pt 1	for I	END	DEC	B ev	ent								
											S	ee E	VEN	NTS_	ENI	DEC	В															
			Clear	1								Disab	ole																			
			Disabled	0							R	Read	: Dis	sable	ed																	
			Enabled	1							R	Read	: En	able	d																	
В	RW	ERRORECB									٧	Vrite	e '1'	to E	isal	ble	inte	erru	pt i	for I	ERR	ROR	ECB	eve	nt							
											S	ee E	VEN	NTS_	ERF	ROR	RECI	3														
			Clear	1							C	Disab	le																			
			Disabled	0							R	Read	: Dis	sable	ed																	

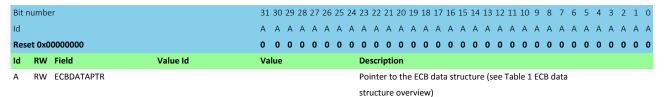


Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Id				ВА
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
ld RW Field	Value Id	Value	Description	
	Enabled	1	Read: Enabled	

27.4.3 ECBDATAPTR

Address offset: 0x504

ECB block encrypt memory pointers



27.5 Electrical specification

27.5.1 ECB Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{FCB}	Run time per 16 byte block in all modes			7.2	μs



28 CCM — AES CCM mode encryption

Cipher block chaining - message authentication code (CCM) mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer. CCM combines counter mode encryption and CBC-MAC authentication. The CCM terminology "Message authentication code (MAC)" is called the "Message integrity check (MIC)" in *Bluetooth* terminology and also in this document.

The CCM block generates an encrypted keystream that is applied to input data using the XOR operation and generates the 4 byte MIC field in one operation. The CCM and radio can be configured to work synchronously. The CCM will encrypt in time for transmission and decrypt after receiving bytes into memory from the radio. All operations can complete within the packet RX or TX time. CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF *RFC3610*, and depends on the AES-128 block cipher. A description of the CCM algorithm can also be found in *NIST Special Publication 800-38C*. The *Bluetooth* specification describes the configuration of counter mode blocks and encryption blocks to implement compliant encryption for BLE.

The CCM block uses EasyDMA to load key, counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

The AES CCM supports three operations: key-stream generation, packet encryption, and packet decryption. All these operations are done in compliance with the *Bluetooth* specification.²⁰

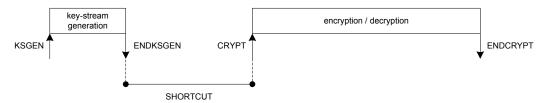


Figure 68: Key-stream generation followed by encryption or decryption. The shortcut is optional.

28.1 Shared resources

The CCM shares registers and other resources with other peripherals that have the same ID as the CCM. The user must therefore disable all peripherals that have the same ID as the CCM before the CCM can be configured and used.

Disabling a peripheral that have the same ID as the CCM will not reset any of the registers that are shared with the CCM. It is therefore important to configure all relevant CCM registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 23 for details on peripherals and their IDs.

28.2 Key-steam generation

A new key-stream needs to be generated before a new packet encryption or packet decryption operation can be started.

A key-stream is generated by triggering the KSGEN task and an ENDKSGEN event will be generated when the key-stream has been generated.

Key-stream generation, packet encryption, and packet decryption operations utilize the configuration specified in the data structure pointed to by *CNFPTR* on page 333. It is necessary to configure this pointer and its underlying data structure, and the *MODE* on page 332 register before the KSGEN task is triggered.

Bluetooth AES CCM 128 bit block encryption, see Bluetooth Core specification Version 4.0.



The key-stream will be stored in the AES CCM's temporary memory area, specified by the *SCRATCHPTR* on page 333, where it will be used in subsequent encryption and decryption operations.

For default length packets, that is when MODE.LENGTH is set to Default, the size of the generated key-stream is 27 bytes. When using extended length packets, that is when MODE.LENGTH is set to Extended, The *MAXPACKETSIZE* on page 333 register specifies the length of the key-stream to be generated. The length of the generated key-stream must be greater or equal to the length of the subsequent packet payload to be encrypted or decrypted. The maximum length of the key-stream in extended mode is 251 bytes, which means that the maximum packet payload size is 251.

If a shortcut is used between ENDKSGEN event and CRYPT task, the *INPTR* on page 333 pointer and the *OUTPTR* on page 333 pointers must also be configured before the KSGEN task is triggered.

28.3 Encryption

During packet encryption, the AES CCM will read the unencrypted packet located in RAM at the address specified in the INPTR pointer, encrypt the packet and append a four byte long Message Integrity Check (MIC) field to the packet.

Encryption is started by triggering the CRYPT task with the *MODE* on page 332 register set to ENCRYPTION. An ENDCRYPT event will be generated when packet encryption is completed

The AES CCM will also modify the length field of the packet to adjust for the appended MIC field, that is, add four bytes to the length, and store the resulting packet back into RAM at the address specified in the *OUTPTR* on page 333 pointer, see *Figure 69: Encryption* on page 326.

Empty packets (length field is set to 0) will not be encrypted but instead moved unmodified through the AES CCM.

The CCM supports different widths of the LENGTH field in the data structure for encrypted packets. This is configured in the MODE on page 332 register.

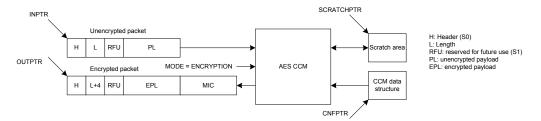


Figure 69: Encryption

28.4 Decryption

During packet decryption, the AES CCM will read the encrypted packet located in RAM at the address specified in the INPTR pointer, decrypt the packet, authenticate the packet's MIC field and generate the appropriate MIC status.

Decryption is started by triggering the CRYPT task with the *MODE* on page 332 register set to DECRYPTION. An ENDCRYPT event will be generated when packet decryption is completed

The AES CCM will also modify the length field of the packet to adjust for the MIC field, that is, subtract four bytes from the length, and then store the decrypted packet into RAM at the address pointed to by the OUTPTR pointer, see *Figure 70: Decryption* on page 327.

The CCM is only able to decrypt packet payloads that are at least 5 bytes long, that is, 1 byte or more encrypted payload (EPL) and 4 bytes of MIC. The CCM will therefore generate a MIC error for packets where the length field is set to 1, 2, 3 or 4.

Empty packets (length field is set to 0) will not be decrypted but instead moved unmodified through the AES CCM, these packets will always pass the MIC check.



The CCM supports different widths of the LENGTH field in the data structure for decrypted packets. This is configured in the MODE on page 332 register.

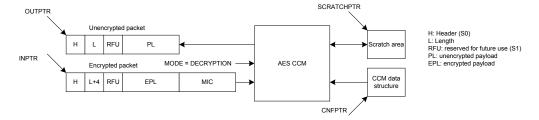


Figure 70: Decryption

28.5 AES CCM and RADIO concurrent operation

The CCM module is able to encrypt/decrypt data synchronously to data being transmitted or received on the radio.

In order for the CCM module to run synchronously with the radio, the data rate setting in the *MODE* on page 332 register needs to match the radio data rate. The settings in this register apply whenever either the KSGEN or CRYPT tasks are triggered.

The data rate setting of the *MODE* on page 332 register can also be overridden on-the-fly during an ongoing encrypt/decrypt operation by the contents of the *RATEOVERRIDE* on page 334 register. The data rate setting in this register applies whenever the RATEOVERRIDE task is triggered. This feature can be useful in cases where the radio data rate is changed during an ongoing packet transaction.

28.6 Encrypting packets on-the-fly in radio transmit mode

When the AES CCM is encrypting a packet on-the-fly at the same time as the radio is transmitting it, the radio must read the encrypted packet from the same memory location as the AES CCM is writing to.

The *OUTPTR* on page 333 pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the radio, see *Figure 71: Configuration of on-the-fly encryption* on page 327.

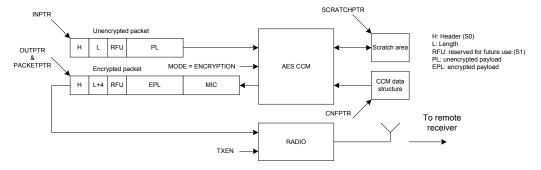


Figure 71: Configuration of on-the-fly encryption

In order to match the RADIO's timing, the KSGEN task must be triggered early enough to allow the keystream generation to complete before the encryption of the packet shall start.

For short packets, that is when MODE.LENGTH = Default, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered. In addition the shortcut between the ENDKSGEN event and the CRYPT task must be enabled. This use-case is illustrated in *Figure 72: On-the-fly encryption of short packets (MODE.LENGTH = Default) using a PPI connection* on page 328 using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM.

For long packets, that is when MODE.LENGTH = Extended, the key-stream generation will need to be started even earlier, for example at the time when the TXEN task in the RADIO is triggered.



Important: Refer to *Timing specification* on page 334 for information about the time needed for generating a key-stream.

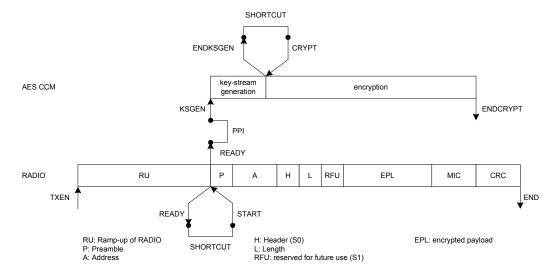


Figure 72: On-the-fly encryption of short packets (MODE.LENGTH = Default) using a PPI connection

28.7 Decrypting packets on-the-fly in radio receive mode

When the AES CCM is decrypting a packet on-the-fly at the same time as the RADIO is receiving it, the AES CCM must read the encrypted packet from the same memory location as the RADIO is writing to.

The *INPTR* on page 333 pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the RADIO, see *Figure 73: Configuration of on-the-fly decryption* on page 328.

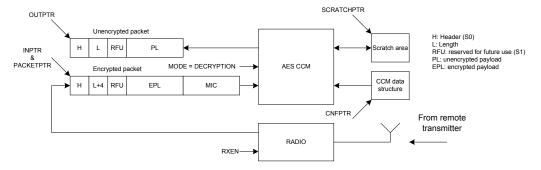


Figure 73: Configuration of on-the-fly decryption

In order to match the RADIO's timing, the KSGEN task must be triggered early enough to allow the keystream generation to complete before the decryption of the packet shall start.

For short packets, that is when MODE.LENGTH = Default, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered. In addition, the CRYPT task must be triggered no earlier than when the ADDRESS event is generated by the RADIO.

If the CRYPT task is triggered exactly at the same time as the ADDRESS event is generated by the RADIO, the AES CCM will guarantee that the decryption is completed no later than when the END event in the RADIO is generated.

This use-case is illustrated in *Figure 74: On-the-fly decryption of short packets (MODE.LENGTH = Default)* using a PPI connection on page 329 using a PPI connection between the ADDRESS event in the RADIO and the CRYPT task in the AES CCM. The KSGEN task is triggered from the READY event in the RADIO through a PPI connection.

For long packets, that is when MODE.LENGTH = Extended, the key-stream generation will need to be started even earlier, for example at the time when the RXEN task in the RADIO is triggered.



Important: Refer to *Timing specification* on page 334 for information about the time needed for generating a key-stream.

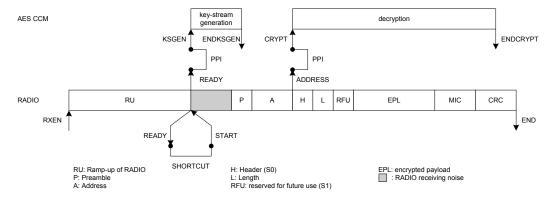


Figure 74: On-the-fly decryption of short packets (MODE.LENGTH = Default) using a PPI connection

28.8 CCM data structure

The CCM data structure is located in Data RAM at the memory location specified by the CNFPTR pointer register.

Table 50: CCM data structure overview

Property	Address offset	Description
KEY	0	16 byte AES key
PKTCTR	16	Octet0 (LSO) of packet counter
	17	Octet1 of packet counter
	18	Octet2 of packet counter
	19	Octet3 of packet counter
	20	Bit 6 – Bit 0: Octet4 (7 most significant bits of packet counter, with Bit 6 being the most significant
		bit) Bit7: Ignored
	21	Ignored
	22	Ignored
	23	Ignored
	24	Bit 0: Direction bit Bit 7 – Bit 1: Zero padded
IV	25	8 byte initialization vector (IV) Octet0 (LSO) of IV, Octet1 of IV,, Octet7 (MSO) of IV

The NONCE vector (as specified by the *Bluetooth* Core Specification) will be generated by hardware based on the information specified in the CCM data structure from *Table 50: CCM data structure overview* on page 329.

Table 51: Data structure for unencrypted packet

Property	Address offset	Description
HEADER	0	Packet Header
LENGTH	1	Number of bytes in unencrypted payload
RFU	2	Reserved Future Use
PAYLOAD	3	Unencrypted payload

Table 52: Data structure for encrypted packet

Property	Address offset	Description
HEADER	0	Packet Header
LENGTH	1.	Number of bytes in encrypted payload including length of MIC
		Important: LENGTH will be 0 for empty packets since the MIC is not added to empty
		packets
RFU	2	Reserved Future Use



Property	Address offset	Description
PAYLOAD	3	Encrypted payload
MIC	3 + payload length	ENCRYPT: 4 bytes encrypted MIC

Important: MIC is not added to empty packets

28.9 EasyDMA and ERROR event

The CCM implements an EasyDMA mechanism for reading and writing to the RAM.

In cases where the CPU and other EasyDMA enabled peripherals are accessing the same RAM block at the same time, a high level of bus collisions may cause too slow operation for correct on the fly encryption. In this case the ERROR event will be generated.

The EasyDMA will have finished accessing the RAM when the ENDKSGEN and ENDCRYPT events are generated.

If the CNFPTR, SCRATCHPTR, INPTR and the OUTPTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

28.10 Registers

Table 53: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000F000	ССМ	CCM	AES counter with CBC-MAC (CCM) mod	e
			block encryption	

Table 54: Register Overview

Register	Offset	Description	
TASKS_KSGEN	0x000	Start generation of key-stream. This operation will stop by itself when completed.	
TASKS_CRYPT	0x004	Start encryption/decryption. This operation will stop by itself when completed.	
TASKS_STOP	0x008	Stop encryption/decryption	
TASKS_RATEOVERRIDE	0x00C	Override DATARATE setting in MODE register with the contents of the RATEOVERRIDE register for	
		any ongoing encryption/decryption	
EVENTS_ENDKSGEN	0x100	Key-stream generation complete	
EVENTS_ENDCRYPT	0x104	Encrypt/decrypt complete	
EVENTS_ERROR	0x108	CCM error event	Deprecated
SHORTS	0x200	Shortcut register	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
MICSTATUS	0x400	MIC check result	
ENABLE	0x500	Enable	
MODE	0x504	Operation mode	
CNFPTR	0x508	Pointer to data structure holding AES key and NONCE vector	
INPTR	0x50C	Input pointer	
OUTPTR	0x510	Output pointer	
SCRATCHPTR	0x514	Pointer to data area used for temporary storage	
MAXPACKETSIZE	0x518	Length of key-stream generated when MODE.LENGTH = Extended.	
RATEOVERRIDE	0x51C	Data rate override setting.	

28.10.1 SHORTS

Address offset: 0x200 Shortcut register



В	it nu	ımbe	r		33	1 30	29	28	27	26	25	24	23	22	21 2	20 :	19 1	8 1	l7 1	6 1	5 14	4 13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
le	t																																	Α
R	ese	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 0
I	t	RW	Field	Value Id	V	alue							De	scrip	otio	n																		
Δ		RW	ENDKSGEN_CRYPT										Sho	ortci	ut b	etv	veei	n EN	NDK	SGE	N e	ven	t an	d CI	RYP	T ta	sk							
													See	e EV	ENT	rs_i	END	KSC	GEN	and	d T /	SKS	_CR	RYPT	•									
				Disabled	0								Dis	able	sh	orto	cut																	
				Enabled	1								Ena	able	sho	orto	ut																	

28.10.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					СВА
Res	et 0x0	0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	ENDKSGEN			Write '1' to Enable interrupt for ENDKSGEN event
					See EVENTS_ENDKSGEN
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	ENDCRYPT			Write '1' to Enable interrupt for ENDCRYPT event
					See EVENTS_ENDCRYPT
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	ERROR			Write '1' to Enable interrupt for ERROR event
					See EVENTS_ERROR
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

28.10.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bitı	numbe	er		31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					СВА
Res	et 0x0	0000000		0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
Α	RW	ENDKSGEN			Write '1' to Disable interrupt for ENDKSGEN event
					See EVENTS_ENDKSGEN
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	ENDCRYPT			Write '1' to Disable interrupt for ENDCRYPT event
					See EVENTS_ENDCRYPT
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	ERROR			Write '1' to Disable interrupt for ERROR event
					See EVENTS_ERROR
			Clear	1	Disable
			Disabled	0	Read: Disabled



	Enabled	1	Read: Enabled
Id RW Field	Value Id	Value	Description
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id			C B A
Bit number		31 30 29 28 27 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

28.10.4 MICSTATUS

Address offset: 0x400

MIC check result

А
0 0 0
0 0

28.10.5 ENABLE

Address offset: 0x500

Enable

Bit	numb	er		31 30	29	28 2	27 2	26 2	5 24	1 23	3 22	21	20	19 1	.8 1	7 1	5 15	14	13	12 1	1 10	9	8	7	6	5	4 3	3 2	1	0
Id																													Α	Α
Res	et 0x	00000000		0 0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Value						D	escri	iptio	on																	
Α	RW	ENABLE								Er	nable	e or	disa	ble	CCI	M														
			Disabled	0						Di	sabl	e																		
			Enabled	2						Er	nable	е																		

28.10.6 MODE

Address offset: 0x504

Operation mode

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			C B B A
Reset 0x00000001		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
A RW MODE			The mode of operation to be used. The settings in this register
			apply whenever either the KSGEN or CRYPT tasks are triggered.
	Encryption	0	AES CCM packet encryption mode
	Decryption	1	AES CCM packet decryption mode
B RW DATARATE			Radio data rate that the CCM shall run synchronous with
	1Mbit	0	1 Mbps
	2Mbit	1	2 Mbps
	125Kbps	2	125 Kbps
	500Kbps	3	500 Kbps
C RW LENGTH			Packet length configuration
	Default	0	Default length. Effective length of LENGTH field in encrypted/
			decrypted packet is 5 bits. A key-stream for packet payloads up
			to 27 bytes will be generated.
	Extended	1	Extended length. Effective length of LENGTH field in encrypted/
			decrypted packet is 8 bits. A key-stream for packet payloads up
			to MAXPACKETSIZE bytes will be generated.



28.10.7 CNFPTR

Address offset: 0x508

Pointer to data structure holding AES key and NONCE vector

Bitı	number		31	30	29	28	27	7 26	25	24	23	22 :	21	20 1	9 1	.8 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Α	A А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	Δ Α	4 А
Res	et 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
											_																					
Id	RW Field	Value Id	Va	lue							Des	scrip	otic	n																		
A	RW Field RW CNFPTR	Value Id	Va	iue											dat	a sti	ruct	ture	ho	ldin	g th	e A	ES I	key	an	d tl	he (CCN	Л			

28.10.8 INPTR

Address offset: 0x50C

Input pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0						
Id		A A A A A A A A A A A A A A A A A A A						
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0						
Id RW Field	Value Id	Value Description						
A RW INPTR	TR Input pointer							

28.10.9 OUTPTR

Address offset: 0x510

Output pointer

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	L7 1	6 1	5 14	4 13	3 12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	4 Α	, Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	Δ ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	OUTPTR										Ou	tpu	t pc	oint	er																	

28.10.10 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

Bit	numbe	er		31	1 30	29	28	27	26	25 2	24 2	23 2	22 2	1 2	0 19	18	17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3	2	1)
Id				Α	Α	Α	Α	Α	Α	Α	Α	A	A A	Δ Α	A A	Α	Α	Α	Α	Α	Α	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	4
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	Va	alue						ı	Desc	crip	tion	1																		
Α	RW	SCRATCHPTR									ı	Poin	iter	to a	scr	atcł	n da	ta a	rea	use	ed f	or te	mpo	orar	y st	ora	ige						
											(durii	ng k	ey-	stre	am	gen	era	tion	, M	IC g	gene	ratio	n a	nd e	enc	ryp	tior	n/				
											(decr	rypt	ion.																			
												The		.+.h				4 6-				ıry si			£ 4-	.+-	ما ، ، به						
												me	SCIC	atti	ı are	d IS	use	u ic) LE	amp	0018	iry Si	Oraş	ge o	ı ua	Ild	uui	IIIB					
											ŀ	key-	stre	am	gen	era	tion	an	d er	ncry	ptio	on.											
											١	Whe	en N	/OE	DE.LE	NG	TH:	= De	efau	ult,	a sp	ace	of 4	3 by	rtes	is r	requ	uire	ed				
											f	for t	his	tem	npor	ary	stor	age	. M	OD	E.LE	NG	H =	Ext	end	ed	(16	+					
											1	MAX	KPA	CKE	TSIZ	E) b	yte	s of	sto	rag	e is	requ	iired	١.									

28.10.11 MAXPACKETSIZE

Address offset: 0x518

Length of key-stream generated when MODE.LENGTH = Extended.



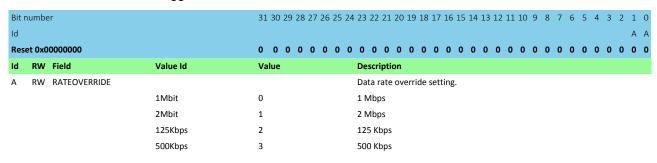
Bit	numbe	r		31 30	29 2	8 27	26	25 2	4 23	3 22	21	20 1	19 1	8 17	16	15	14 1	3 12	11	10	9 8	7	6	5	4	3 2	2 1	0
Id																						Α	Α	Α	Α	ΑА	A A	A
Res	et 0x0	00000FB		0 0	0 0	0 0	0	0 0	0	0	0	0	0 (0	0	0	0 (0 0	0	0	0 0	1	1	1	1	1 0) 1	1
Id	RW	Field	Value Id	Value					D	escr	iptio	on																
Α	RW	MAXPACKETSIZE		[0x001	LBOx	x00FE	3]		Le	engt	h of	key	-stre	am į	gene	erat	ed v	hen	МО	DE.I	ENC	HT						
									=	Exte	ende	d. T	his v	/alue	mu	st b	e gr	eate	ror	equa	al to	the						
									C I	ıhca	מווח	nt n	acke	t na	vloa	d to	h h a	oncr	vnta	۲/۲	ocrv	ntor	4					

28.10.12 RATEOVERRIDE

Address offset: 0x51C

Data rate override setting.

Override value to be used instead of the setting of MODE.DATARATE. This override value applies when the RATEOVERRIDE task is triggered.



28.11 Electrical specification

28.11.1 Timing specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{kgen}	Time needed for key-stream generation (given priority access to			50	μs
	destination RAM block).				



29 AAR — Accelerated address resolver

Accelerated address resolver is a cryptographic support function for implementing the "Resolvable Private Address Resolution Procedure" described in the *Bluetooth Core specification* v4.0. "Resolvable private address generation" should be achieved using ECB and is not supported by AAR.

The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address. The AAR block enables real-time address resolution on incoming packets when configured as described in this chapter. This allows real-time packet filtering (whitelisting) using a list of known shared keys (Identity Resolving Keys (IRK) in *Bluetooth*).

29.1 Shared resources

The AAR shares registers and other resources with the peripherals that have the same ID as the AAR. The user must therefore disable all peripherals that have the same ID as the AAR before the AAR can be configured and used.

Disabling a peripheral that have the same ID as the AAR will not reset any of the registers that are shared with the AAR. It is therefore important to configure all relevant AAR registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 23 for details on peripherals and their IDs.

29.2 EasyDMA

The AAR implements EasyDMA for reading and writing to the RAM. The EasyDMA will have finished accessing the RAM when the END, RESOLVED, and NOTRESOLVED events are generated.

If the IRKPTR, ADDRPTR and the SCRATCHPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

29.3 Resolving a resolvable address

As per Bluetooth specification, a private resolvable address is composed of six bytes.

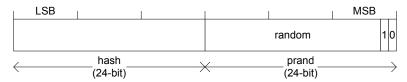


Figure 75: Resolvable address

To resolve an address the ADDRPTR register must point to the start of packet. The resolver is started by triggering the START task. A RESOLVED event is generated when the AAR manages to resolve the address using one of the Identity Resolving Keys (IRK) found in the IRK data structure. The AAR will use the IRK specified in the register IRK0 to IRK15 starting from IRK0. How many to be used is specified by the NIRK register. The AAR module will generate a NOTRESOLVED event if it is not able to resolve the address using the specified list of IRKs.

The AAR will go through the list of available IRKs in the IRK data structure and for each IRK try to resolve the address according to the Resolvable Private Address Resolution Procedure described in the *Bluetooth* Specification²¹. The time it takes to resolve an address may vary depending on where in the list the

²¹ Bluetooth Specification Version 4.0 [Vol 3] chapter 10.8.2.3.



resolvable address is located. The resolution time will also be affected by RAM accesses performed by other peripherals and the CPU. See the *Electrical specifications* for more information about resolution time.

The AAR will only do a comparison of the received address to those programmed in the module. And not check what type of address it actually is.

The AAR will stop as soon as it has managed to resolve the address, or after trying to resolve the address using NIRK number of IRKs from the IRK data structure. The AAR will generate an END event after it has stopped.

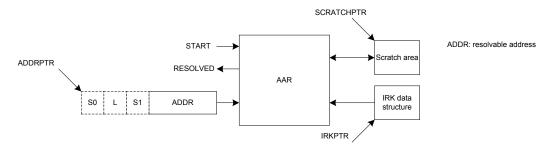


Figure 76: Address resolution with packet preloaded into RAM

29.4 Use case example for chaining RADIO packet reception with address resolution using AAR

The AAR may be started as soon as the 6 bytes required by the AAR have been received by the RADIO and stored in RAM. The ADDRPTR pointer must point to the start of packet.

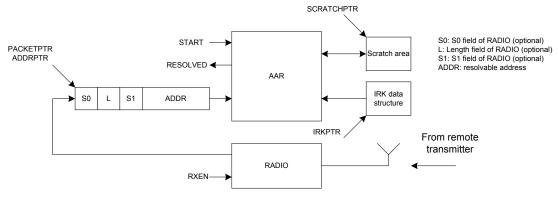


Figure 77: Address resolution with packet loaded into RAM by the RADIO

29.5 IRK data structure

The IRK data structure is located in RAM at the memory location specified by the CNFPTR pointer register.

Table 55: IRK data structure overview

Property	Address offset	Description
IRKO	0	IRK number 0 (16 - byte)
IRK1	16	IRK number 1 (16 - byte)
	**	
IRK15	240	IRK number 15 (16 - byte)



29.6 Registers

Table 56: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000F000	AAR	AAR	Accelerated address resolver	

Table 57: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start resolving addresses based on IRKs specified in the IRK data structure
TASKS_STOP	0x008	Stop resolving addresses
EVENTS_END	0x100	Address resolution procedure complete
EVENTS_RESOLVED	0x104	Address resolved
EVENTS_NOTRESOLVED	0x108	Address not resolved
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STATUS	0x400	Resolution status
ENABLE	0x500	Enable AAR
NIRK	0x504	Number of IRKs
IRKPTR	0x508	Pointer to IRK data structure
ADDRPTR	0x510	Pointer to the resolvable address
SCRATCHPTR	0x514	Pointer to data area used for temporary storage

29.6.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	numbe	er		31	30 2	29 2	8 2	7 2	6 25	24	23 2	2 21	20	19	18	17	16	15	14 :	13 1	.2 1	10	9	8	7	6	5 4	1 3	2	1 0
Id																													С	ВА
Res	et 0x0	0000000		0	0	0 (0 0) (0 0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0 0
Id	RW	Field	Value Id	Va	lue						Desc	ripti	ion																	
Α	RW	END									Write	e '1'	to E	nab	le i	nte	rru	pt f	or E	ND	eve	nt								
											See !	VEN	VTS_	ENL)															
			Set	1							Enab	le																		
			Disabled	0							Read	l: Dis	sable	ed																
			Enabled	1							Read	l: En	able	d																
В	RW	RESOLVED									Write	e '1'	to E	nab	le i	nte	rru	pt f	or F	RESC	LVE	D ev	ent							
											See !	EVEN	VTS_	RES	OL	VEC)													
			Set	1							Enab	le																		
			Disabled	0							Read	l: Dis	sable	ed																
			Enabled	1							Read	l: En	able	d																
С	RW	NOTRESOLVED									Write	e '1'	to E	nab	le i	nte	rru	pt f	or N	IOT	RESC	DLVE	D e	ven	t					
											See /	EVEN	VTS_	NO	TRE	SO	LVE	D												
			Set	1							Enab	le																		
			Disabled	0							Read	l: Dis	sable	ed																
			Enabled	1							Read	l: En	able	d																

29.6.2 INTENCLR

Address offset: 0x308 Disable interrupt



Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					СВА
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	END			Write '1' to Disable interrupt for END event
					See EVENTS_END
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	RESOLVED			Write '1' to Disable interrupt for RESOLVED event
					See EVENTS_RESOLVED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	NOTRESOLVED			Write '1' to Disable interrupt for NOTRESOLVED event
					See EVENTS_NOTRESOLVED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

29.6.3 STATUS

Address offset: 0x400

Resolution status

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ААА
Reset 0x00000000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
A R STATUS		[015]	The IRK that was used last time an address was resolved

29.6.4 ENABLE

Address offset: 0x500

Enable AAR

Bit	numbe	r		3:	1 30	29	28	8 27	7 2	6 2	25 2	24 2	23 2	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			А А
Res	et 0x0	0000000		0	0	0	0	0	0) (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	9						ı	Des	cri	otic	n																			
Α	RW	ENABLE										E	Ena	ble	or	disa	abl	e A	AR																
			Disabled	0								1	Disa	ble	è																				
			Enabled	3									Ena	ble																					

29.6.5 NIRK

Address offset: 0x504

Number of IRKs

Bit number	31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		АААА
Reset 0x00000001	0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value	Description
A RW NIRK	[116]	Number of Identity root keys available in the IRK data structure

29.6.6 IRKPTR

Address offset: 0x508



Pointer to IRK data structure

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 1	.2 1	.1 1	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ.	4 <i>A</i>	. A	. A	Α	Α	Α	Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scr	pti	on																		
Α	RW	IRKPTR										Ро	inte	er to	th	e IR	K d	ata	str	ucti	ure												

29.6.7 ADDRPTR

Address offset: 0x510

Pointer to the resolvable address

Bit r	numbe	er		31	30	29	28 2	27 2	26 2	25 2	24 2	3 2	2 2	1 20) 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				А	Α	Α	Α	Α	Α.	Α	A	4 /	4 Δ	. A	. Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						C	eso	cript	ion																			
Α	RW	ADDRPTR									Р	oin	ter	to t	he r	eso	lvab	le a	add	res	s (6	-by	tes)									

29.6.8 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

Bit r	numbe	er		31	1 30	29	28	3 27	26	25	24	23	22 2	1 20	19	18	17	16	15	14 1	l3 1	2 1:	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	Α	Α	Α	Α	Α	Α	A A	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue	•						Des	crip	tion																		
Α	RW	SCRATCHPTR										Poi	nter	to a	scr	atch	da	ta a	rea	use	d fo	r te	mpc	orar	y st	ora	ge					
												dur	ing r	esol	utic	n.A	spa	ace	of r	nini	mun	n 3 l	byte	s m	ust	be						
												rese	erve	d.																		

29.7 Electrical specification

29.7.1 AAR Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{AAR}	Address resolution time per IRK. Total time for several IRKs			6	μs
	is given as (1 μs + n * t_AAR), where n is the number of IRKs.				
	(Given priority to the actual destination RAM block).				
t _{AAR,8}	Time for address resolution of 8 IRKs. (Given priority to the			49	μs
	actual destination RAM block).				



30 SPIM — Serial peripheral interface master with EasyDMA

The SPI master can communicate with multiple SPI slaves using individual chip select signals for each slave.

Listed here are the main features for the SPIM

- EasyDMA direct transfer to/from RAM
- SPI mode 0-3
- · Individual selection of IO pin for each SPI signal
- Optional D/CX output line for distinguishing between command and data bytes

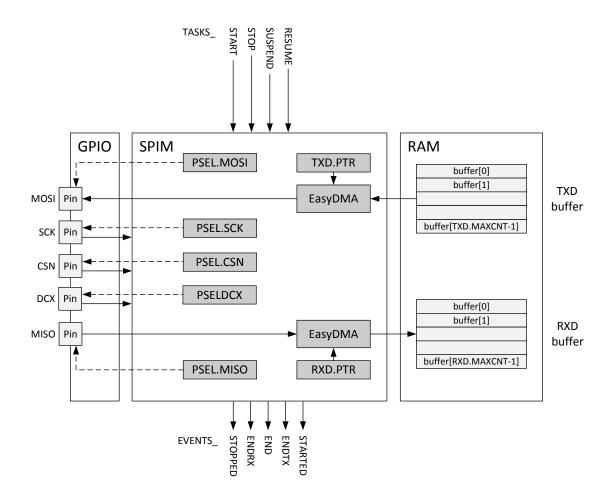


Figure 78: SPIM — SPI master with EasyDMA

30.1 SPI master transaction sequence

An SPI master transaction consists of a sequence started by the START task followed by a number of bytes being transmitted/received on MOSI/MISO.

An SPI master transaction is started by triggering the START task. When started, a number of bytes will be transmitted/received on MOSI/MISO. This is illustrated in *Figure 79: SPI master transaction* on page 341.

The ENDTX is generated when all bytes in the *TXD.PTR* on page 349 buffer as specified in the *TXD.MAXCNT* on page 349 register have been transmitted. The ENDRX event will be generated when



the *RXD.PTR* on page 349 buffer is full, that is after the number of bytes specified in the *RXD.MAXCNT* on page 349 register have been received. The transaction stops automatically after MAX(*TXD.MAXCNT* on page 349, *RXD.MAXCNT* on page 349) number of bytes have been transmitted/received. In the case when *RXD.MAXCNT* on page 349 > *TXD.MAXCNT* on page 349 the contents of the *ORC* on page 352 register will be transmitted after the last byte in the *TXD.PTR* on page 349 buffer has been transmitted.

The END event will be generated after both the ENDRX and ENDTX events have been generated.

The SPI master can be stopped in the middle of a transaction by triggering the STOP task. When triggering the STOP task the SPIM will wait for the transmission/reception of the current byte to complete before stopping. A STOPPED event is generated when the SPI master has stopped.

If the ENDTX event has not already been generated when the SPI master has come to a stop, the ENDTX event will be generated even though all bytes in the *TXD.PTR* on page 349 buffer have not been transmitted.

If the ENDRX event has not already been generated when the SPI master has come to a stop, the ENDRX event will be generated even though the *RXD.PTR* on page 349 buffer is not full.

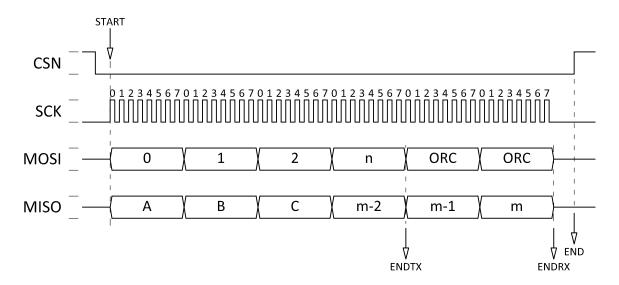


Figure 79: SPI master transaction

30.2 D/CX functionality

Some SPI slaves, as for example display drivers, require an additional signal from the SPI master to distinguish between command and data bytes. For displays drivers this line is often called D/CX.

The SPIM provides support for such a D/CX output line. The D/CX line is set low during transmission of command bytes and high during transmission of data bytes.

The D/CX pin number is selected using *PSELDCX* on page 351 and the number of command bytes preceding the data bytes is configured using *DCXCNT* on page 351.

It is not allowed to write to the *DCXCNT* on page 351 during an ongoing transmission.

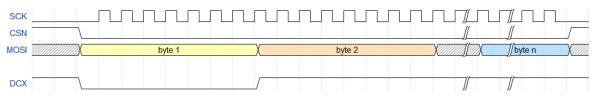


Figure 80: D/CX example. SPIM.DCXCNT = 1.



30.3 Pin configuration

The SCK, CSN, DCX, MOSI, and MISO signals associated with the SPIM are mapped to physical pins according to the configuration specified in the PSEL.n registers.

The contents of *PSEL.SCK* on page 347, *PSEL.CSN* on page 348, *PSELDCX* on page 351, *PSEL.MOSI* on page 347 and *PSEL.MISO* on page 348 registers are only used when the SPIM is enabled and retained only as long as the device is in System On mode. The PSEL.n registers can only be configured when the SPIM is disabled. Enabling/disabling is done using the *ENABLE* on page 347 register.

To ensure correct behavior the pins used by the SPIM must be configured in the GPIO peripheral as described in *Table 58: GPIO configuration* on page 342 before the SPIM is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 58: GPIO configuration

SPI master signal	SPI master pin	Direction	Output value	Comments
SCK	As specified in <i>PSEL.SCK</i> on page 347	Output	Same as CONFIG.CPOL	
CSN	As specified in <i>PSEL.CSN</i> on page 348	Output	Same as CONFIG.CPOL	
DCX	As specified in <i>PSELDCX</i> on page 351	Output	1	
MOSI	As specified in <i>PSEL.MOSI</i> on page 347	Output	0	
MISO	As specified in <i>PSEL.MISO</i> on page 348	Input	Not applicable	

Some SPIM instances do not have support for controlling CSN automatically. In these cases available GPIO pins needs to be used to control CSN directly. Refer to *Table 60: Instances* on page 344 for information about what features are supported in the various SPIM instances.

The SPIM supports SPI modes 0 through 3. The CONFIG on page 350 register allows setting CPOL and CPHA appropriately.

Table 59: SPI modes

Mode	Clock polarity CPOL	Clock phase CPHA	
SPI_MODE0	0 (Active High)	0 (Leading)	
SPI_MODE1	0 (Active High)	1 (Trailing)	
SPI_MODE2	1 (Active Low)	0 (Leading)	
SPI MODE3	1 (Active Low)	1 (Trailing)	

30.4 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.

Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 23 for details on peripherals and their IDs.

30.5 EasyDMA

The SPI master implements EasyDMA for reading and writing of data packets from and to the DATA RAM without CPU involvement.



The RXD.PTR and TXD.PTR point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively, see *Figure 78: SPIM* — *SPI master with EasyDMA* on page 340. RXD.MAXCNT and TXD.MAXCNT specify the maximum number of bytes allocated to the buffers.

The SPI master will automatically stop transmitting after TXD.MAXCNT bytes have been transmitted and RXD.MAXCNT bytes have been received. If TXD.MAXCNT is larger than RXD.MAXCNT, the superfluous received bytes will be ignored. If RXD.MAXCNT is larger than TXD.MAXCNT, the remaining transmitted bytes will contain the value defined in the ORC register.

If the RXD.PTR and the TXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next transmission immediately after having received the STARTED event.

The ENDRX/ENDTX event indicate that EasyDMA has finished accessing respectively the RX/TX buffer in RAM. The END event gets generated when both RX and TX are finished accessing the buffers in RAM.

In the case where several AHB bus masters try to access the same AHB slave at the same time, AHB bus congestion might occur. The SPIM is such an AHB master, and when congestion occurs the SPIM might have to wait for access to RAM to be granted. If the SPIM has to wait for bus access the transaction will be temporary stalled, but resume once the SPIM is granted access to the bus. See the AHB multilayer on page 25 for more information on this subject. Note that some SPIM instances do not support this stalling mechanism. Refer to Table 60: Instances on page 344 for information about what features are supported in the various instances.

30.5.1 EasyDMA list

EasyDMA supports one list type.

The supported list type is:

Array list

EasyDMA array list

The EasyDMA array list can be represented by the data structure ArrayList_type.

For illustration, see the code example below. This data structure includes only a buffer with size equal to Channel.MAXCNT. EasyDMA will use the Channel.MAXCNT register to determine when the buffer is full. Replace 'Channel' by the specific data channel you want to use, for instance 'NRF_SPIM->RXD', 'NRF_SPIM->TXD', 'NRF_TWIM->RXD', etc.

The Channel.MAXCNT register cannot be specified larger than the actual size of the buffer. If Channel.MAXCNT is specified larger than the size of the buffer, the EasyDMA channel may overflow the buffer.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

```
#define BUFFER_SIZE 4

typedef struct ArrayList
{
   uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type MyArrayList[3];

//replace 'Channel' below by the specific data channel you want to use,
// for instance 'NRF_SPIM->RXD', 'NRF_TWIM->RXD', etc.
Channel.MAXCNT = BUFFER_SIZE;
```



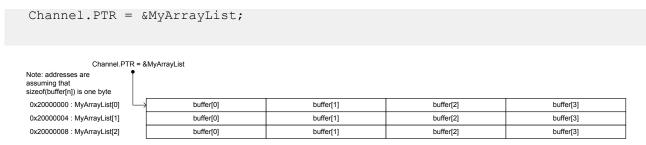


Figure 81: EasyDMA array list

30.6 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

30.7 Registers

Table 60: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	SPIM	SPIM0	SPI master 0	Not supported: > 8 Mbps data rate,
				CSNPOL register, DCX functionality,
				IFTIMING.x registers, hardware CSN control
				(PSEL.CSN), stalling mechanism during AHB
				bus contention. Limitations: TXD.MAXCNT/
				RXD.MAXCNT only 8 bits wide.
0x40004000	SPIM	SPIM1	SPI master 1	Not supported: > 8 Mbps data rate,
				CSNPOL register, DCX functionality,
				IFTIMING.x registers, hardware CSN control
				(PSEL.CSN), stalling mechanism during AHB
				bus contention. Limitations: TXD.MAXCNT/
				RXD.MAXCNT only 8 bits wide.
0x40023000	SPIM	SPIM2	SPI master 2	Not supported: > 8 Mbps data rate,
				CSNPOL register, DCX functionality,
				IFTIMING.x registers, hardware CSN control
				(PSEL.CSN), stalling mechanism during AHB
				bus contention. Limitations: TXD.MAXCNT/
				RXD.MAXCNT only 8 bits wide.
0x4002F000	SPIM	SPIM3	SPI master 3	

Table 61: Register Overview

Register	Offset	Description
TASKS_START	0x010	Start SPI transaction
TASKS_STOP	0x014	Stop SPI transaction
TASKS_SUSPEND	0x01C	Suspend SPI transaction
TASKS_RESUME	0x020	Resume SPI transaction
EVENTS_STOPPED	0x104	SPI transaction has stopped
EVENTS_ENDRX	0x110	End of RXD buffer reached
EVENTS_END	0x118	End of RXD buffer and TXD buffer reached
EVENTS_ENDTX	0x120	End of TXD buffer reached
EVENTS_STARTED	0x14C	Transaction started
SHORTS	0x200	Shortcut register



Register	Offset	Description
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STALLSTAT	0x400	Stall status for EasyDMA RAM accesses. The fields in this register is set to STALL by hardware
		whenever a stall occurres and can be cleared (set to NOSTALL) by the CPU.
ENABLE	0x500	Enable SPIM
PSEL.SCK	0x508	Pin select for SCK
PSEL.MOSI	0x50C	Pin select for MOSI signal
PSEL.MISO	0x510	Pin select for MISO signal
PSEL.CSN	0x514	Pin select for CSN
FREQUENCY	0x524	SPI frequency. Accuracy depends on the HFCLK source selected.
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
TXD.LIST	0x550	EasyDMA list type
CONFIG	0x554	Configuration register
IFTIMING.RXDELAY	0x560	Sample delay for input serial data on MISO
IFTIMING.CSNDUR	0x564	Minimum duration between edge of CSN and edge of SCK and minimum duration CSN must stay
		high between transactions
CSNPOL	0x568	Polarity of CSN output
PSELDCX	0x56C	Pin select for DCX signal
DCXCNT	0x570	DCX configuration
ORC	0x5C0	Byte transmitted after TXD.MAXCNT bytes have been transmitted in the case when RXD.MAXCNT is
		greater than TXD.MAXCNT

30.7.1 SHORTS

Address offset: 0x200 Shortcut register

Bit	numb	er		31	1 30	29	28	27	26	25	24	23	22 :	21 2	20	19 :	18	17	16	15	14	13	12	11 1	.0	9 8	3 7	6	5	4	3	2	1	0
Id																		Α																
Res	set 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•						Des	scrip	otio	n																			
Α	RW	END_START										Shc	ortcı	ut b	etv	vee	n E	ND	ev	ent	an	T2 b	AR	T tas	sk									
												See	EV	ENT	rs_	ENE) aı	nd	TAS	KS_	STA	ART												
			Disabled	0								Dis	able	sh	ort	cut																		
			Enabled	1								Ena	ble	sho	orto	ut																		

30.7.2 INTENSET

Address offset: 0x304 Enable interrupt

Bitı	numbe	er		31	L 30	29	28	27	26	25	2	4 2	3 2	2 2	21 2	0 1	L9 1	8 1	7 1	5 15	5 14	13	3 12	11	10	9	8	7	6	5 .	4 3	2	1	0
Id																	Ε										D		С		В		Α	
Res	et 0x0	0000000		0	0	0	0	0	0	0	C) () (0	0 (כ	0) (0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	alue							D	esc	crip	tio	ı																		
Α	RW	STOPPED										V	/rit	e ':	1' to	Er	nabl	e ir	teri	upt	for	ST	OPF	ED	evei	nt								
												S	ee i	EVI	ENT.	s_s	TO	PPE	D															
			Set	1								Е	nak	ole																				
			Disabled	0								R	eac	d: C	Disal	ole	d																	
			Enabled	1								R	eac	d: E	nab	lec	t																	
В	RW	ENDRX										W	/rit	e ':	1' to	Er	nabl	e ir	teri	upt	for	EN	IDR)	⟨ ev	ent									



Bit number	31 30 29 28 27 26 25	$24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0$
Id		E D C B A
Reset 0x00000000	0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field Value Id	d Value	Description
		See EVENTS_ENDRX
Set	1	Enable
Disabled	d 0	Read: Disabled
Enabled	1	Read: Enabled
C RW END		Write '1' to Enable interrupt for END event
		See EVENTS_END
Set	1	Enable
Disabled	d 0	Read: Disabled
Enabled	1	Read: Enabled
D RW ENDTX		Write '1' to Enable interrupt for ENDTX event
		See EVENTS_ENDTX
Set	1	Enable
Disabled	d 0	Read: Disabled
Enabled	1	Read: Enabled
E RW STARTED		Write '1' to Enable interrupt for STARTED event
		See EVENTS_STARTED
Set	1	Enable
Disabled	d 0	Read: Disabled
Enabled	1	Read: Enabled

30.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

		e interrupt																											
Bit	numbe	er		31 30 2	29 28 :	27 26	25	24 2	23 2	22 21	20	19 1	18	17 1	16	15 1	4 1	3 12	2 11	10	9	8	7	6	5	4 3	3 2	1	0
Id												Ε										D		С		В		Α	
Res	et 0x0	0000000		0 0	0 0	0 0	0	0 (0	0 0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Value				D	Des	cripti	on																		
Α	RW	STOPPED						۷	۷ri	ite '1'	to [Disab	ole i	inte	rru	pt f	or S	TOP	PED	eve	ent								
								S	ee	EVEN	ITS_	_STO	PPI	ED															
			Clear	1				D	Disa	able																			
			Disabled	0				R	Rea	d: Dis	abl	ed																	
			Enabled	1				R	Rea	d: Ena	able	ed																	
В	RW	ENDRX						٧	Vri	ite '1'	to [Disab	ole i	inte	rru	pt f	or E	NDF	XX e	ven	t								
								S	ee	EVEN	ITS_	END	ORX																
			Clear	1				D	Disa	able																			
			Disabled	0				R	Rea	d: Dis	abl	ed																	
			Enabled	1				R	Rea	d: Ena	able	ed																	
С	RW	END						٧	Vri	ite '1'	to [Disab	ole i	inte	rru	pt f	or E	ND	evei	nt									
								S	iee	EVEN	ITS_	END)																
			Clear	1				D	Disa	able																			
			Disabled	0				R	Rea	d: Dis	abl	ed																	
			Enabled	1				R	Rea	d: Ena	able	ed																	
D	RW	ENDTX						٧	۷ri	ite '1'	to [Disab	ole i	inte	rru	pt f	or E	NDI	X e	vent	t								
								S	ee	EVEN	ITS_	END	ЭΤΧ																
			Clear	1				D	Disa	able																			
			Disabled	0				R	Rea	d: Dis	abl	ed																	
			Enabled	1				R	Rea	d: Ena	able	ed																	
E	RW	STARTED						٧	Vri	ite '1'	to [Disab	ole i	inte	rru	pt f	or S	TAR	TED	eve	ent								
								S	iee	EVEN	ITS	STA.	RTI	D															
			Clear	1						able	_	_																	



Bit number		31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10	9 8 7	6 5	5 4 3	2 1 0)
Id			E		D	С	В	Α	
Reset 0x00000000		0 0 0 0 0	00000000000	0 0 0 0 0 0 0 0	0 0 0	0 0	0 0	0 0 0)
Id RW Field	Value Id	Value	Description						ı
	Disabled	0	Read: Disabled						_
	Enabled	1	Read: Enabled						

30.7.4 STALLSTAT

Address offset: 0x400

Stall status for EasyDMA RAM accesses. The fields in this register is set to STALL by hardware whenever a stall occurres and can be cleared (set to NOSTALL) by the CPU.

Bit r	numbe	er		31	30 2	9 2	28 2	7 2	26 2	5 24	4 2	3 22	2 2:	1 20	19	9 18	3 17	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id																																Е	3 A
Res	et 0x0	0000000		0	0 (0	0 0)	0 (0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	Val	ue						D	esc	ript	tion																			
Α	RW	TX		[1	0]						S	tall	stat	tus 1	for	Eas	yDľ	MΑ	RAI	M r	eads	6											
			NOSTALL	0							N	lo st	all																				
			STALL	1							Α	sta	ll ha	as o	ccu	ırre	d																
В	RW	RX		[1	0]						S	tall	stat	tus 1	for	Eas	yDľ	MΑ	RAI	Νv	rite	S											
			NOSTALL	0							N	lo st	all																				
			STALL	1							Α	sta	ll ha	as o	ccu	ırre	d																

30.7.5 ENABLE

Address offset: 0x500

Enable SPIM

Bitı	numbe	er		31	30	29	28 :	27 2	26 :	25 2	24 :	23 2	22 2	1 2	0 1	9 1	8 17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id																														Α	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 () () () (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	ue						- 1	Des	crip	tio	1																	
Α	RW	ENABLE									- 1	Ena	ble (or c	lisal	ble	SPIN	Л														
			Disabled	0							- 1	Disa	ble	SPI	M																	
			Enabled	7							ı	Ena	ble S	SPI	N																	

30.7.6 PSEL.SCK

Address offset: 0x508 Pin select for SCK

Bit r	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	вааа
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

30.7.7 PSEL.MOSI

Address offset: 0x50C Pin select for MOSI signal



Bit r	iumbe	er		31	30 2	29 2	28 2	7 2	6 2	5 2	4 2	23 2	2 2	1 2	0 19	9 18	3 17	16	15	14 :	13 1	12 1	.1 10	9	8	7	6	5	4	3	2 1	١ 0
Id				С																								В	Α	A	4 Α	A A
Res	et OxF	FFFFFF		1	1	1	1 :	1 :	L 1	1 1	1	1	1 :	1 1	l 1	. 1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1 1	. 1
Id	RW	Field	Value Id	Va	lue							Des	crip	tior	1																	
Α	RW	PIN		[0.	.31]						F	Pin r	nun	nbei	r																	
В	RW	PORT		[0.	.1]						F	ort	nu	mbe	er																	
С	RW	CONNECT									(Con	nec	tion	1																	
			Disconnected	1							[Disc	onn	ect																		
			Connected	0							(Con	nec	t																		

30.7.8 PSEL.MISO

Address offset: 0x510

Pin select for MISO signal

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	вааа
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	$1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

30.7.9 PSEL.CSN

Address offset: 0x514 Pin select for CSN

Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ваааа
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

30.7.10 FREQUENCY

Address offset: 0x524

SPI frequency. Accuracy depends on the HFCLK source selected.

D.1				24	20	20	20	27	26	25	24	22	22.24	- 20	. 40	40	47	1.0	4.5		2.4	2 4 4	40	_	_	7	_	_			1 0
Bit	numbe	er		31	. 30	29	28	27	26	25	24	23 .	22 21	L 2C) 19	18	1/	16	15	14 1	.3 1.	2 11	. 10	9	8	/	6	5	4 3	3 2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α	Α	Α	Α	Α	Α	Α /	4 Δ	A	Α	Α	Α	Α	Α	Α .	A A	A A	A A
Res	et 0x0	4000000		0	0	0	0	0	1	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cript	ion																	
Α	RW	FREQUENCY										SPI	mast	er c	lata	rat	e														
			K125	0x	020	000	000					125	kbps	5																	
			K250	0x	040	000	000					250	kbps	5																	
			K500	0x	080	000	000					500	kbps	5																	
			M1	0x	100	000	000					1 M	bps																		
			M2	0x	200	000	000					2 N	bps																		
			M4	0x	400	000	000					4 N	bps																		
			M8	0x	800	000	000					8 N	bps																		
			M16	0x	0A0	000	000					16 [Mbps																		
			M32	0x	140	000	000					32 [Mbps																		



30.7.11 RXD.PTR

Address offset: 0x534

Data pointer

Bit	nu	mbe	r		31	. 30	29	28	3 27	7 26	25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α	А	. A	Α	. A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Re	set	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id		RW	Field	Value Id	Va	lue							De	escr	ipti	on																			
Α		RW	PTR										Da	ata	noir	nter																			

30.7.12 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

	Bit n	umbe	er		31	30 2	9 2	28 27	7 26	25	24	23	22 :	21 2	20 1	.9 1	8 1	7 1	6 1	5 1	4 13	12	11	10	9	8	7	6	5	4	3	2 1	L 0
	ld																		A		A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	A A
1	Rese	t OxC	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0 () (0) (0	0	0	0	0	0	0	0	0	0	0	0 (0	0
ı	ld	RW	Field	Value Id	Va	lue						Des	cri	otio	n																		
	Α	RW	MAXCNT									Ma:	xim	um	nur	nbe	r o	f by	tes	in r	ece	ive	buff	er									

30.7.13 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit r	numbe	er		31 30 29 28 27	26 25 24 23 22 21 20 19 1	18 17 16 15 14 13 12 11	10 9 8 7 6 5 4 3 2	1 0
Id						$A \; A \; A \; A \; A \; A$	A A A A A A A A	АА
Res	et 0x0	0000000		0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0
Id	RW	Field	Value Id	Value	Description			
Α	R	AMOUNT			Number of bytes	transferred in the last tra	nsaction	

30.7.14 RXD.LIST

Address offset: 0x540 EasyDMA list type

Bit n	umbe	er		31	30	29	28	27	26	5 25	5 24	4 2	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (C
Id																																		A A	Д
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (D
Id	RW	Field	Value Id	Va	lue							D	esc	ripti	on																				
Α	RW	LIST										Li	st t	ype																					
			Disabled	0								D	isab	le E	asy	DΝ	1A I	ist																	
			ArrayList	1								U	se a	ırra	, lis	t																			

30.7.15 TXD.PTR

Address offset: 0x544

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value Description
A RW PTR		Data pointer

30.7.16 TXD.MAXCNT

Address offset: 0x548



Number of bytes in transmit buffer

Bi	t numb	er		31	30	9	28	27 :	26 :	25 :	24	23 :	22 2	21 2	0 1	9 1	8 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 C)
Id																			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	۱ ۸	A A	l.
R	eset Ox	00000000		0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0)
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																			ı
Α	RW	MAXCNT										Max	xim	ım	nun	nbe	r of	byt	es ii	n tr	ans	mit	buf	fer										7

30.7.17 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bitı	numbe	er		31	30	29	28	27 2	26 2	25 2	24 2	23 2	2 2:	1 20	2 19	18	3 17	16	15	14	13	12 :	11 1	0 9	8	7	6	5	4	3	2 :	1 0
Id																			Α	Α	Α	Α	A A	Δ Δ	Α	Α	Α	Α	Α	Α .	Δ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Desc	ript	ion																		
Α	R	AMOUNT									1	lum	ber	of	byte	es t	rans	fer	red	in t	he l	ast	trar	sact	ion							

30.7.18 TXD.LIST

Address offset: 0x550 EasyDMA list type

Bit r	numbe	r		31 30 29 28 27 20	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id					A
Res	et 0x0	0000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	LIST			List type
			Disabled	0	Disable EasyDMA list
			ArrayList	1	Use array list

30.7.19 CONFIG

Address offset: 0x554 Configuration register

Bit n	umbe	r		31	30	29	28 2	7 2	6 2	5 24	1 23	22	21 2	20 1	19 1	18 :	17 1	16 :	15 1	4 1	3 12	11	10	9	8	7	6	5 4	3	2	1 0
Id																														С	ВА
Rese	t 0x0	0000000		0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						De	escri	ptio	n																	
Α	RW	ORDER									Bit	tord	ler																		
			MsbFirst	0							M	ost s	igni	fica	nt l	bit :	shif	ted	out	tfirs	t										
			LsbFirst	1							Le	ast s	igni	fica	nt l	bit :	shif	ted	out	tfirs	t										
В	RW	СРНА									Se	rial	clock	c (S	CK)	ph	ase														
			Leading	0							Sa	mpl	e on	lea	din	ıg e	dge	of	clo	ck, s	hift	seri	ial d	lata	on 1	trai	ling				
											ed	lge																			
			Trailing	1							Sa	mpl	e on	tra	ilin	g e	dge	of	clo	k, s	hift	seri	al d	ata	on I	eac	ling				
											ed	lge																			
С	RW	CPOL									Se	rial	clock	k (S	CK)	ро	larit	ty													
			ActiveHigh	0							Ac	tive	high	1																	
			ActiveLow	1							Ac	tive	low																		

30.7.20 IFTIMING.RXDELAY

Address offset: 0x560

Sample delay for input serial data on MISO



Bit	numb	er		33	1 30	29	28	8 27	7 2	6 2	5 2	24 2	23	22	21	20	1	9 1	8 1	7 1	5 1	5 1	4 1	3 12	2 1:	1 10	9	8	7	6	5	4	3	2	1	0
Id																																		Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	(0) (0	0	0	0	0	0) () (0	(0) (0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	V	alue							ı	Des	scr	ipti	on																				
Α	RW	RXDELAY		[7	70]							9	San	np	le d	lela	y f	or i	np	ut s	eria	ıl da	ata	on l	MIS	0.1	he	valu	ıe s	pec	ifie	es				
												t	the	nι	umb	ber	of	64	MI	Hz c	loc	k cy	cle	s (1	5.62	25 n	s) d	ela	/ fr	om	the	9				
												t	the	sa	mp	ling	g e	dge	e of	SCI	((l	ead	ing	edg	ge f	or C	ONI	IG.	CPF	HA :	= 0,					
												t	trai	lin	g e	dge	fc	or C	O١	IFIG	.CP	НΑ	= 1) ur	til 1	the	inpu	ıt se	eria	l da	ita	is				
												9	sam	npl	led.	As	er	ı ex	an	ple	if	RXE	EL	ΔΥ =	0 a	and	100	NFIC	i.Cl	PHA	۱ = ۱	0,				
												t	the	in	put	se	ria	l da	ıta	is sa	ımı	oled	lor	the	e ris	sing	edg	e o	f SC	CK.						

30.7.21 IFTIMING.CSNDUR

Address offset: 0x564

Minimum duration between edge of CSN and edge of SCK and minimum duration CSN must stay high between transactions

Bit r	umbe	r		33	1 30	29	28	27	26 2	25 2	24 2	3 2	2 2:	1 20	0 19	18	3 17	' 16	15	14	13 3	12 1	1 10	9	8	7	6	5	4	3 2	2 1	1 0
Id																										Α	Α	Α	Α	A A	A A	A A
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 (0 (
Id	RW	Field	Value Id	V	alue						C	esc	ript	ion	ı																	
Α	RW	CSNDUR		[0	xFF.	.0]					Ν	/lini	mui	n d	ura	tior	n be	twe	een	edg	e of	CSI	N and	d ed	ge o	of S	CK	and				
											n	niniı	mur	n d	ura	tion	CS	N m	nust	sta	y hi	gh b	etw	een	trar	nsa	ctio	ns.				
											Т	he v	valu	e is	spe	ecifi	ied	in n	ium	ber	of 6	4 N	A A A A A A									
											n	s).												and edge of SCK and etween transactions.								

30.7.22 CSNPOL

Address offset: 0x568 Polarity of CSN output

Bit	num	ber			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16	15	14	13	12 :	11 :	10	9	8	7	6	5	4	3 2	2	1 0
Id																																			Α
Res	et 0	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0
Id	R۱	W	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	R۷	N	CSNPOL										Pol	larit	y o	f CS	Νo	utp	ut																
				LOW	0								Act	ive	lov	/ (ic	lle s	tat	e hi	gh)															
				HIGH	1								Act	ive	hig	h (i	dle	sta	te lo	w)															

30.7.23 PSELDCX

Address offset: 0x56C Pin select for DCX signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	B A A A A
Rese	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

30.7.24 DCXCNT

Address offset: 0x570 DCX configuration



Bit r	numbe	r		31	30 2	9 2	8 27	7 26	5 25	24	23	22	21	20	19	18	17	16	15	14	13 :	.2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																														Α	Α	А А
Res	et 0x0	0000000		0	0 0) (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Val	ue						De	scr	ipti	on																		
Α	RW	DCXCNT		0x0	0xF						Th	is r	egis	ster	spe	ecifi	ies	the	nun	nbe	r of	con	nma	nd l	yte	S						
											pr	ece	din	g th	ne d	ata	by	es.	The	PS	EL.C	CX	line	will	be l	low	dui	ring	3			
											tra	nsn	miss	sior	of	cor	nm	and	byt	es	and	higl	n du	ring	tra	nsn	nissi	on				
											of	dat	ta b	yte	s. V	alu	e 0:	κ F ir	ndic	ate	s th	it al	l by	es a	re d	com	ıma	nd				
											by	tes																				

30.7.25 ORC

Address offset: 0x5C0

Byte transmitted after TXD.MAXCNT bytes have been transmitted in the case when RXD.MAXCNT is greater than TXD.MAXCNT

Bit r	numbe	r		31 30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 1	3 17	7 16	15	14	13	12 1	.1 1) 9	8	7	6	5	4	3	2	1 0
Id																									Α	Α	Α	Α	Α	Α ,	4 А
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Value	•						Des	scrip	tio	n																	
Α	RW	ORC									Byt	e tra	ansr	nitt	ed a	fte	r TX	D.N	1AX	CNT	byt	es h	ave	be	en						
											trai	nsm	itte	d in	the	cas	e w	her	n RX	D.N	1AX(CNT	is g	eat	er t	han	1				
											TXE	D.M	٩XC	NT.																	

30.8 Electrical specification

30.8.1 Current consumption

Symbol	Description	Min.	Тур.	Max.	Units
I _{SPIM,2Mbps}	Run current for SPIM, 2 Mbps		50		μΑ
I _{SPIM,8Mbps}	Run current for SPIM, 8 Mbps		50		μΑ
I _{SPIM,16Mbps}	Run current for SPIM, 16 Mbps				μΑ
I _{SPIM,32Mbps}	Run current for SPIM, 32 Mbps				μΑ
I _{SPIM,IDLE}	Idle current for SPIM (STARTed, no CSN activity)		1		μΑ

30.8.2 Timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{SPIM}	Bit rates for SPIM ²²			8 ²³	Mbps
t _{SPIM,START}	Time from START task to transmission started		1		μs
t _{SPIM,CSCK}	SCK period	125			ns
t _{SPIM,RSCK,LD}	SCK rise time, standard drive ^a			t _{RF,25pF}	
t _{SPIM,RSCK,HD}	SCK rise time, high drive ^a			t _{HRF,25pF}	
t _{SPIM,FSCK,LD}	SCK fall time, standard drive ^a			t _{RF,25pF}	
t _{SPIM,FSCK,HD}	SCK fall time, high drive ^a			t _{HRF,25pF}	
t _{SPIM,WHSCK}	SCK high time ^a	(0.5*t _{CS}	ск		
		- t _{RSCK}			
t _{SPIM,WLSCK}	SCK low time ^a	(0.5*t _{CS}	ск		
		- t _{FSCK}			
t _{SPIM,SUMI}	MISO to CLK edge setup time	19			ns
t _{SPIM,HMI}	CLK edge to MISO hold time	18			ns
t _{SPIM,VMO}	CLK edge to MOSI valid			59	ns
t _{SPIM,HMO}	MOSI hold time after CLK edge	20			ns

²² High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.

^a At 25pF load, including GPIO pin capacitance, see GPIO spec.



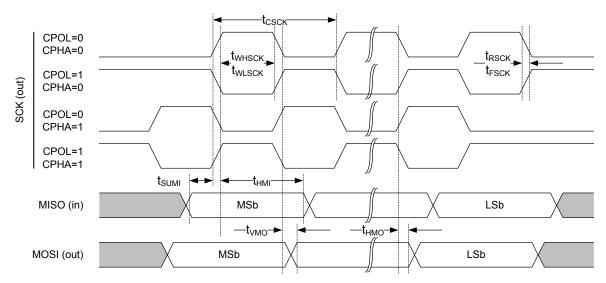


Figure 82: SPIM timing diagram



31 SPIS — Serial peripheral interface slave with EasyDMA

SPI slave (SPIS) is implemented with EasyDMA support for ultra low power serial communication from an external SPI master. EasyDMA in conjunction with hardware-based semaphore mechanisms removes all real-time requirements associated with controlling the SPI slave from a low priority CPU execution context.

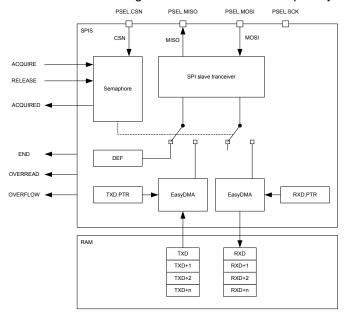


Figure 83: SPI slave

The SPIS supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

Table 62: SPI modes

Mode	Clock polarity	Clock phase
	CPOL	СРНА
SPI_MODE0	0 (Leading)	0 (Active High)
SPI_MODE1	0 (Leading)	1 (Active Low)
SPI_MODE2	1 (Trailing)	0 (Active High)
SPL MODE3	1 (Trailing)	1 (Active Low)

31.1 Shared resources

The SPI slave shares registers and other resources with other peripherals that have the same ID as the SPI slave. Therefore, you must disable all peripherals that have the same ID as the SPI slave before the SPI slave can be configured and used.

Disabling a peripheral that has the same ID as the SPI slave will not reset any of the registers that are shared with the SPI slave. It is important to configure all relevant SPI slave registers explicitly to secure that it operates correctly.

The Instantiation table in *Instantiation* on page 23 shows which peripherals have the same ID as the SPI slave.

31.2 EasyDMA

The SPI slave implements EasyDMA for reading and writing to and from the RAM. The END event indicates that EasyDMA has finished accessing the buffer in RAM.



If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

31.3 SPI slave operation

SPI slave uses two memory pointers, RXD.PTR and TXD.PTR, that point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively. Since these buffers are located in RAM, which can be accessed by both the SPI slave and the CPU, a hardware based semaphore mechanism is implemented to enable safe sharing.

See Figure 84: SPI transaction when shortcut between END and ACQUIRE is enabled on page 356.

Before the CPU can safely update the RXD.PTR and TXD.PTR pointers it must first acquire the SPI semaphore. The CPU can acquire the semaphore by triggering the ACQUIRE task and then receiving the ACQUIRED event. When the CPU has updated the RXD.PTR and TXD.PTR pointers the CPU must release the semaphore before the SPI slave will be able to acquire it. The CPU releases the semaphore by triggering the RELEASE task. This is illustrated in *Figure 84: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 356. Triggering the RELEASE task when the semaphore is not granted to the CPU will have no effect.

The semaphore mechanism does not, at any time, prevent the CPU from performing read or write access to the RXD.PTR register, the TXD.PTR registers, or the RAM that these pointers are pointing to. The semaphore is only telling when these can be updated by the CPU so that safe sharing is achieved.

The semaphore is by default assigned to the CPU after the SPI slave is enabled. No ACQUIRED event will be generated for this initial semaphore handover. An ACQUIRED event will be generated immediately if the ACQUIRE task is triggered while the semaphore is assigned to the CPU.

The SPI slave will try to acquire the semaphore when CSN goes low. If the SPI slave does not manage to acquire the semaphore at this point, the transaction will be ignored. This means that all incoming data on MOSI will be discarded, and the DEF (default) character will be clocked out on the MISO line throughout the whole transaction. This will also be the case even if the semaphore is released by the CPU during the transaction. In case of a race condition where the CPU and the SPI slave try to acquire the semaphore at the same time, as illustrated in lifeline item 2 in *Figure 84: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 356, the semaphore will be granted to the CPU.

If the SPI slave acquires the semaphore, the transaction will be granted. The incoming data on MOSI will be stored in the RXD buffer and the data in the TXD buffer will be clocked out on MISO.

When a granted transaction is completed and CSN goes high, the SPI slave will automatically release the semaphore and generate the END event.

As long as the semaphore is available the SPI slave can be granted multiple transactions one after the other. If the CPU is not able to reconfigure the TXD.PTR and RXD.PTR between granted transactions, the same TX data will be clocked out and the RX buffers will be overwritten. To prevent this from happening, the END_ACQUIRE shortcut can be used. With this shortcut enabled the semaphore will be handed over to the CPU automatically after the granted transaction has completed, giving the CPU the ability to update the TXPTR and RXPTR between every granted transaction.

If the CPU tries to acquire the semaphore while it is assigned to the SPI slave, an immediate handover will not be granted. However, the semaphore will be handed over to the CPU as soon as the SPI slave has released the semaphore after the granted transaction is completed. If the END_ACQUIRE shortcut is enabled and the CPU has triggered the ACQUIRE task during a granted transaction, only one ACQUIRE request will be served following the END event.

The MAXRX register specifies the maximum number of bytes the SPI slave can receive in one granted transaction. If the SPI slave receives more than MAXRX number of bytes, an OVERFLOW will be indicated in the STATUS register and the incoming bytes will be discarded.

The MAXTX parameter specifies the maximum number of bytes the SPI slave can transmit in one granted transaction. If the SPI slave is forced to transmit more than MAXTX number of bytes, an OVERREAD will be indicated in the STATUS register and the ORC character will be clocked out.



The RXD.AMOUNT and TXD.AMOUNT registers are updated when a granted transaction is completed. The TXD.AMOUNT register indicates how many bytes were read from the TX buffer in the last transaction, that is, ORC (over-read) characters are not included in this number. Similarly, the RXD.AMOUNT register indicates how many bytes were written into the RX buffer in the last transaction.

The ENDRX event is generated when the RX buffer has been filled.

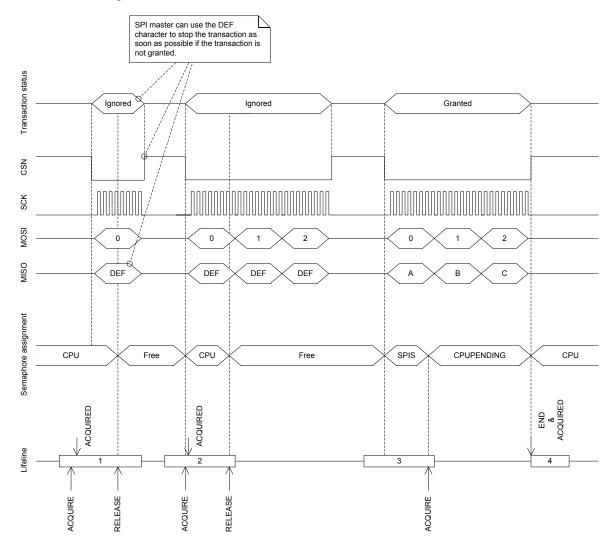


Figure 84: SPI transaction when shortcut between END and ACQUIRE is enabled

31.4 Pin configuration

The CSN, SCK, MOSI, and MISO signals associated with the SPI slave are mapped to physical pins according to the configuration specified in the PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If the CONNECT field of any of these registers is set to Disconnected, the associated SPI slave signal will not be connected to any physical pins.

The PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI slave is enabled, and retained only as long as the device is in System ON mode, see *POWER — Power supply* on page 66 chapter for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI slave is disabled.

To secure correct behavior in the SPI slave, the pins used by the SPI slave must be configured in the GPIO peripheral as described in *Table 63: GPIO configuration before enabling peripheral* on page 357 before enabling the SPI slave. This is to secure that the pins used by the SPI slave are driven correctly if the SPI



slave itself is temporarily disabled, or if the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the SPI slave is to be recognized by an external SPI master.

The MISO line is set in high impedance as long as the SPI slave is not selected with CSN.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 63: GPIO configuration before enabling peripheral

SPI signal	SPI pin	Direction	Output value	Comment
CSN	As specified in PSEL.CSN	Input	Not applicable	
SCK	As specified in PSEL.SCK	Input	Not applicable	
MOSI	As specified in PSEL.MOSI	Input	Not applicable	
MISO	As specified in PSEL.MISO	Input	Not applicable	Emulates that the SPI slave is not selected.

31.5 Registers

Table 64: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	SPIS	SPIS0	SPI slave 0		
0x40004000	SPIS	SPIS1	SPI slave 1		
0x40023000	SPIS	SPIS2	SPI slave 2		

Table 65: Register Overview

Register	Offset	Description	
TASKS_ACQUIRE	0x024	Acquire SPI semaphore	
TASKS_RELEASE	0x028	Release SPI semaphore, enabling the SPI slave to acquire it	
EVENTS_END	0x104	Granted transaction completed	
EVENTS_ENDRX	0x110	End of RXD buffer reached	
EVENTS_ACQUIRED	0x128	Semaphore acquired	
SHORTS	0x200	Shortcut register	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
SEMSTAT	0x400	Semaphore status register	
STATUS	0x440	Status from last transaction	
ENABLE	0x500	Enable SPI slave	
PSELSCK	0x508	Pin select for SCK	Deprecated
PSELMISO	0x50C	Pin select for MISO	Deprecated
PSELMOSI	0x510	Pin select for MOSI	Deprecated
PSELCSN	0x514	Pin select for CSN	Deprecated
PSEL.SCK	0x508	Pin select for SCK	
PSEL.MISO	0x50C	Pin select for MISO signal	
PSEL.MOSI	0x510	Pin select for MOSI signal	
PSEL.CSN	0x514	Pin select for CSN signal	
RXDPTR	0x534	RXD data pointer	Deprecated
MAXRX	0x538	Maximum number of bytes in receive buffer	Deprecated
AMOUNTRX	0x53C	Number of bytes received in last granted transaction	Deprecated
RXD.PTR	0x534	RXD data pointer	
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer	
RXD.AMOUNT	0x53C	Number of bytes received in last granted transaction	
TXDPTR	0x544	TXD data pointer	Deprecated
MAXTX	0x548	Maximum number of bytes in transmit buffer	Deprecated
AMOUNTTX	0x54C	Number of bytes transmitted in last granted transaction	Deprecated
TXD.PTR	0x544	TXD data pointer	
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer	
TXD.AMOUNT	0x54C	Number of bytes transmitted in last granted transaction	
CONFIG	0x554	Configuration register	



Register	Offset	Description
DEF	0x55C	Default character. Character clocked out in case of an ignored transaction.
ORC	0x5C0	Over-read character

31.5.1 SHORTS

Address offset: 0x200

Shortcut register

Bit	numbe	er		31	L 30	29	28	27	26	25	24	23	22	21	20	19 1	18 1	17 1	16 1	L5 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id																															A	١.	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0 (0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	n																		
Α	RW	END_ACQUIRE										Sho	ortc	ut k	etv	vee	n El	ND 6	eve	nt a	nd	ACC	UIR	E ta	sk								
												See	e <i>EV</i>	/EN	TS_	ENE	an	ıd T	ASK	(S_A	1CQ	UIR	E										
			Disabled	0								Dis	able	e sh	ort	cut																	
			Enabled	1								Ena	able	sh	orto	cut																	

31.5.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C B A
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW END			Write '1' to Enable interrupt for END event
				See EVENTS_END
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW ENDRX			Write '1' to Enable interrupt for ENDRX event
				See EVENTS_ENDRX
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW ACQUIRED			Write '1' to Enable interrupt for ACQUIRED event
				See EVENTS_ACQUIRED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

31.5.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	er		31	1 30	29	28	8 27	7 26	5 25	5 24	1 23	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																									С						В			Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							D	esc	ripti	on																			
Α	RW	END										W	rite	'1'	to [Disa	ble	int	err	upt	for	EN	Dе	ven	t									
												Se	ee E	VEN	ITS_	EN	D																	
			Clear	1								D	isak	le																				
			Disabled	0								Re	ead	: Dis	abl	ed																		
			Enabled	1								R	ead	: En	able	ed																		
В	RW	ENDRX										W	rite	'1'	to [Disa	ble	int	err	upt	for	EN	DR	K ev	ent	:								



Bit r	iumbe	er		31	30 2	29 2	28 2	7 2	6 25	5 24	23	22	21 2	20 1	19 1	8 1	7 1	5 15	5 14	13	12	11	10	9	8 7	' 6	5 5	4	3	2	1 0
Id																							С					В			Α
Rese	et OxO	0000000		0	0	0	0 0) (0 0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0 () (0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						De	scri	ptio	n																	
											See	e <i>EV</i>	/ENT	S_E	END	RX															
			Clear	1							Dis	able	e																		
			Disabled	0							Rea	ad:	Disa	ble	d																
			Enabled	1							Rea	ad:	Enab	oled	t																
С	RW	ACQUIRED									Wr	rite	'1' to) Di	isab	le ir	nter	rup	t fo	r AC	QU	REI) ev	ent							
											See	e <i>EV</i>	/ENT	S_/	4CQ	UIR	ED														
			Clear	1							Dis	able	e																		
			Disabled	0							Rea	ad:	Disa	ble	d																
			Enabled	1							Rea	ad:	Enab	oled	t																

31.5.4 SEMSTAT

Address offset: 0x400 Semaphore status register

Bitı	numbe	er		33	1 30	29	28	3 27	7 2	6 25	5 24	4 2	3 2:	2 2:	1 20	0 1	9 1	8 1	17 :	16	15	14	13	12	11	. 10	9	8	7	6	5	4	3	2	1	0
Id																																			Α	Α
Res	et 0x0	0000001		0	0	0	0	0	0	0	0) (0	0	0) () ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Id	RW	Field	Value Id	V	alue							D	esc	ript	tion	ı																				
Α	R	SEMSTAT										S	ema	aph	ore	sta	atu:	5																		
			Free	0								S	ema	aph	ore	is	free	è																		
			CPU	1								S	ema	aph	ore	is	ass	ign	ed	to	CPI	J														
			SPIS	2								S	ema	aph	ore	is	ass	ign	ed	to	SPI	sla	ve													
			CPUPending	3								S	ema	aph	ore	is	ass	ign	ed	to	SPI	bu	t a	har	ndo	ver	to	the	СР	U is						
												р	end	ling																						

31.5.5 STATUS

Address offset: 0x440

Status from last transaction

Individual bits are cleared by writing a '1' to the bits that shall be cleared

Bit nun	mbe	r		31	. 30	29	28 2	27 2	26 2	5 2	24 2	3 2	2 21	. 20	19	18	17	16	15 3	L4 1	.3 1	2 1	1 10	9	8	7	6	5	4 3	2	1	0
Id																															В	Α
Reset (0x00	0000000		0	0	0	0	0	0 (0	0	0 0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 (0	0	0
ld R	RW	Field	Value Id	Va	lue						0)esc	ripti	ion																		
A R	RW	OVERREAD									Т	Χbι	ıffe	rov	er-r	ead	det	ect	ed,	and	l pr	evei	nted									
			NotPresent	0							F	lead	: er	ror ı	not	pre	sen	:														
			Present	1							F	lead	: er	ror	pres	ent																
			Clear	1							٧	Vrite	e: cl	ear	erro	r o	n w	ritir	ıg '1	.'												
B R	RW	OVERFLOW									F	X b	uffe	r ov	erfl	ow	dete	ecte	d, a	and	pre	ven	ted									
			NotPresent	0							F	lead	: er	ror ı	not	pre	sen	:														
			Present	1							F	lead	: er	ror	pres	ent																
			Clear	1							٧	Vrite	e: cl	ear	erro	r o	n w	ritir	ıg '1	.'												

31.5.6 ENABLE

Address offset: 0x500 Enable SPI slave

Bit	number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			АААА
Res	set 0x00000000	0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW Field Value Id	Value	Description
Α	RW ENABLE		Enable or disable SPI slave



Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 17 16	5 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id					AAAA
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
	Disabled	0	Disable SPI slave		
	Enabled	2	Enable SPI slave		

31.5.7 PSELSCK (Deprecated)

Address offset: 0x508 Pin select for SCK

Bitı	numbe	er		31	1 30	29	28	27	26	25	24	23	22 :	21 :	20 1	19 1	l8 1	7 1	5 15	5 14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	A A	Α Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	alue							Des	crip	otio	n																		
Α	RW	PSELSCK		[0	31]						Pin	nur	nbe	er co	onfi	gur	atio	n fo	r SF	ı sc	K si	gna	ı									
			Disconnected	0х	(FFF	FFF	FF					Dis	con	nec	t:																		

31.5.8 PSELMISO (Deprecated)

Address offset: 0x50C Pin select for MISO

Bitı	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	PSELMISO		[031] Pin number configuration for SPI MISO signal
			Disconnected	0xFFFFFFF Disconnect

31.5.9 PSELMOSI (Deprecated)

Address offset: 0x510 Pin select for MOSI

Bit	numbe	er		31	1 30	29	28	8 27	7 26	5 25	5 24	23	22	21	20	19	18	17 1	16	15 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	. A	A	A	Α	. A	Α	Α	Α	Α	Α	Α	Α.	Α	Α.	Α,	A A		Α	Α	Α	Α	Α	Α	Α /	А А	Α	Α
Res	et OxF	FFFFFF		1	1	1	1	. 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	L 1	. 1	. 1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	alue	:						De	scri	ptic	on																		
Α	RW	PSELMOSI		[0)31	.]						Pir	n nu	mb	er c	onf	iguı	ratio	on t	for S	SPI I	MO:	SI si	gnal									
			Disconnected	0>	xFFF	FFF	FFF					Dis	cor	ne	ct																		

31.5.10 PSELCSN (Deprecated)

Address offset: 0x514 Pin select for CSN

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3	2 1 0
Id				A A A A A A A A A A A A A A A A A A A	A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1
Id	RW	Field	Value Id	Value Description	
Α	RW	PSELCSN		[031] Pin number configuration for SPI CSN signal	
			Disconnected	0xFFFFFFF Disconnect	

31.5.11 PSEL.SCK

Address offset: 0x508 Pin select for SCK



Bit r	iumbe	er		31	30 2	29 2	28 2	7 2	6 2	5 2	4 2	23 2	2 2	1 2	0 19	9 18	3 17	16	15	14 :	13 1	12 1	.1 10	9	8	7	6	5	4	3	2 1	١ 0
Id				С																								В	Α	A	4 Α	A A
Res	et OxF	FFFFFF		1	1	1	1 :	1 :	L 1	1 1	1	1	1 :	1 1	l 1	. 1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1 1	. 1
Id	RW	Field	Value Id	Va	lue							Des	crip	tior	1																	
Α	RW	PIN		[0.	.31]						F	Pin r	nun	nbei	r																	
В	RW	PORT		[0.	.1]						F	ort	nu	mbe	er																	
С	RW	CONNECT									(Con	nec	tion	1																	
			Disconnected	1							[Disc	onn	ect																		
			Connected	0							(Con	nec	t																		

31.5.12 PSEL.MISO

Address offset: 0x50C Pin select for MISO signal

Bit r	numbe	er		31 3	29	28	27 :	26 2	25 2	24 2	23 :	22	21	20	19	18	17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0	ı
Id				С																								В	Α	Α	Α	А А	l
Res	et OxF	FFFFFF		1 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	1	1	1	1	1	1	1	1 1	l
Id	RW	Field	Value Id	Valu	е					ı	Des	cri	ptic	on																			l
Α	RW	PIN		[03	1]					ı	Pin	nu	mb	er																			
В	RW	PORT		[01]						ı	Por	t nı	uml	ber																			
С	RW	CONNECT								(Con	nne	ctic	n																			
			Disconnected	1						1	Disc	con	neo	ct																			
			Connected	0						(Con	nne	ct																				

31.5.13 PSEL.MOSI

Address offset: 0x510

Pin select for MOSI signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ваааа
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

31.5.14 PSEL.CSN

Address offset: 0x514

Pin select for CSN signal

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	B A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

31.5.15 RXDPTR (Deprecated)

Address offset: 0x534 RXD data pointer



Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	RXDPTR										RX	D d	ata	poi	nte	r																	

31.5.16 MAXRX (Deprecated)

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit r	numbe	er		31	30 2	9 2	28 2	7 26	25	24	23	22 :	21 2	20 1	L9 1	8 1	7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id																										Α	Α	Α	Α.	A A	A	A
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0 () () (0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	otio	n																		
Α	RW	MAXRX									Ma	xim	um	nu	mbe	r o	f by	tes	in r	ece	ive l	ouff	er									

31.5.17 AMOUNTRX (Deprecated)

Address offset: 0x53C

Number of bytes received in last granted transaction

Bit number		31 30 29 28 27 26	6 25 24 23 22 21 20 19	9 18 17 16 15 14 13 12 1	1 10 9 8 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0000000	00000000	0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A R AMOUI	TRX		Number of byt	es received in the last grar	nted transaction

31.5.18 RXD.PTR

Address offset: 0x534 RXD data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW PTR		RXD data pointer

31.5.19 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A RW MAXCNT			Maximum number of b	bytes in receive buffer	

31.5.20 RXD.AMOUNT

Address offset: 0x53C

Number of bytes received in last granted transaction

Id	numbe	:1		31 30 29 28 27	26 25 24 23 22 21 20	19 18 17 16	15 14 15	12 11 10	9 6					1 0 A A
Res	et 0x0	0000000		0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0	0 0 0	0 0 0	0 0	0 (0	0	0 0	0 0
Id	RW	Field	Value Id	Value	Description									

A R AMOUNT Number of bytes received in the last granted transaction



31.5.21 TXDPTR (Deprecated)

Address offset: 0x544
TXD data pointer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW TXDPTR	TXD data pointer

31.5.22 MAXTX (Deprecated)

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number		31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9 8	3 7 6 5 4	3 2 1 0
Id					AAAA	A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0
Id RW Field	Value Id	Value	Description			
A RW MAXTX			Maximum number o	of bytes in transmit buffer		

31.5.23 AMOUNTTX (Deprecated)

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

Bit num	nber		31 30 29 28 27 26	5 24 23 22 21 20 19 18 17	7 16 15 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0
Id						A A A A A A A
Reset 0	0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	00000000
Id RV	W Field	Value Id	Value	Description		
A R	AMOUNTTX			Number of bytes trans	smitted in last granted transa	action

31.5.24 TXD.PTR

Address offset: 0x544

TXD data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW PTR		TXD data pointer

31.5.25 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
A RW MAXCNT			Maximum number of bytes in transmit buffer

31.5.26 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transmitted in last granted transaction



Bitı	numbe	er		31 30 29 28 2	27 26 2	5 24	23 2	2 21	20 1	.9 18	17	16 1	5 14	1 13	12 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																			Α	Α	Α	Α	A A	4 A	Α
Res	et 0x0	0000000		0 0 0 0	0 0 0	0	0 0	0	0	0 0	0	0 (0 0	0	0	0 0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Value			Desc	ripti	on																
Α	R	AMOUNT					Num	ber o	of by	tes ti	ransr	nitte	ed ir	last	grar	nted 1	tran	ısac	tior	า					

31.5.27 CONFIG

Address offset: 0x554 Configuration register

Bit r	umbe	r		31	30	29	28 :	27 :	26 2	5 2	4 2	3 22	21	20	19	18	17 :	16 1	L5 :	14 1	.3 1	2 11	. 10	9	8	7	6	5	4	3 2	1	0
Id																														С	В	Α
Res	t 0x0	0000000		0	0	0	0	0	0	0 0)	0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						0)escr	iptic	on																		
Α	RW	ORDER									Е	it or	der																			
			MsbFirst	0							Ν	Лost	sign	ific	ant	bit	shif	ted	ou	t fir	st											
			LsbFirst	1							L	.east	sign	ific	ant	bit	shif	ted	ou	t fir	st											
В	RW	СРНА									S	erial	clo	ck (5	SCK) ph	ase															
			Leading	0							S	amp	le o	n le	adiı	ng e	dge	of	clo	ck,	shift	ser	ial d	lata	on 1	trai	iling	5				
											e	dge																				
			Trailing	1							S	amp	le o	n tr	ailir	ng e	dge	of	clo	ck, s	hift	ser	al d	ata	on l	ead	ding	5				
											e	dge																				
С	RW	CPOL									S	erial	clo	ck (SCK) po	lari	ty														
			ActiveHigh	0							A	ctive	e hig	h																		
			ActiveLow	1							A	ctive	e lov	v																		

31.5.28 DEF

Address offset: 0x55C

Default character. Character clocked out in case of an ignored transaction.

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A
Reset 0x000000	00	0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
ld RW Field	Value Id	Value	Description
A RW DEF			Default character. Character clocked out in case of an ignored
			transaction.

31.5.29 ORC

Address offset: 0x5C0 Over-read character

Bit r	umber			31	L 30	29	28 2	27 26	5 2	5 24	1 23	3 22	2 21	. 20	19	18	17	16	15 3	L4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 2	1 0
Id																										Α	Α	A	Α.	A A	\ <i>A</i>	4 A
Res	et 0x00	000000		0	0	0	0	0 0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 () () 0
Id	RW I	Field	Value Id	Va	alue						De	esci	ripti	ion																		
Α	RW (ORC									Ο١	ver-	-rea	d c	hara	ecte	r. C	har	acte	r cl	ock	ed o	ut a	fter	an	ove	er-re	ead				
											of	the	e tra	ans	mit	buf	fer.															



31.6 Electrical specification

31.6.1 SPIS slave interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{SPIS}	Bit rates for SPIS ²⁴			8 ²⁵	Mbps
I _{SPIS,2Mbps}	Run current for SPIS, 2 Mbps		45		μΑ
I _{SPIS,8Mbps}	Run current for SPIS, 8 Mbps		45		μΑ
I _{SPIS,IDLE}	Idle current for SPIS (STARTed, no CSN activity)		1		μΑ
tspis start	Time from RELEASE task to receive/transmit (CSN active)		0.125		μs

31.6.2 Serial Peripheral Interface Slave (SPIS) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{SPIS,CSCKIN}	SCK input period	125			ns
t _{SPIS,RFSCKIN}	SCK input rise/fall time			30	ns
t _{SPIS,WHSCKIN}	SCK input high time	30			ns
t _{SPIS,WLSCKIN}	SCK input low time	30			ns
t _{SPIS,SUCSN}	CSN to CLK setup time	1000			ns
t _{SPIS,HCSN}	CLK to CSN hold time	2000			ns
t _{SPIS,ASA}	CSN to MISO driven	0			ns
t _{SPIS,ASO}	CSN to MISO valid ^a			1000	ns
t _{SPIS,DISSO}	CSN to MISO disabled ^a			68	ns
t _{SPIS,CWH}	CSN inactive time	300			ns
t _{SPIS,VSO}	CLK edge to MISO valid			19	ns
t _{SPIS,HSO}	MISO hold time after CLK edge	18 ²⁶			ns
t _{SPIS,SUSI}	MOSI to CLK edge setup time	59			ns
t _{SPIS,HSI}	CLK edge to MOSI hold time	20			ns

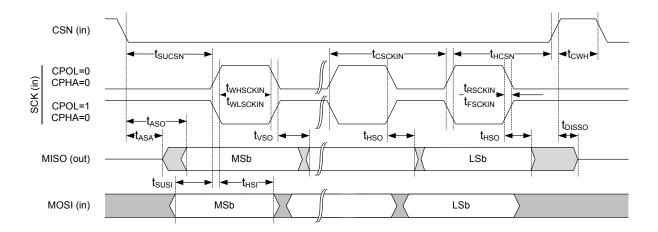
²⁴ High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

The actual maximum data rate depends on the master's CLK to MISO and MOSI setup and hold timings.

^a At 25pF load, including GPIO capacitance, see GPIO spec.

 $^{^{\}rm 26}$ This is to ensure compatibility to SPI masters sampling MISO on the same edge as MOSI is output





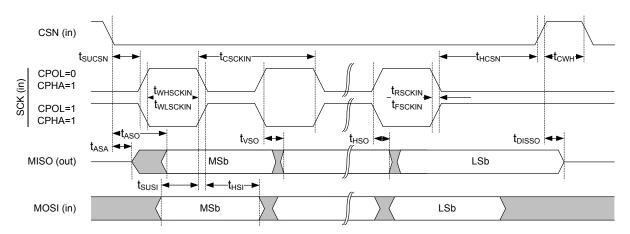


Figure 85: SPIS timing diagram

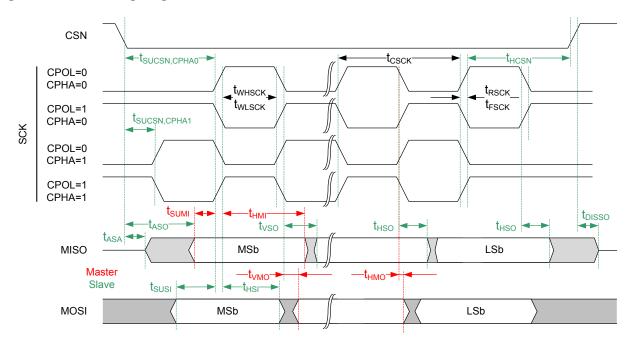


Figure 86: Common SPIM and SPIS timing diagram



32 TWIM — I²C compatible two-wire interface master with EasyDMA

TWI master with EasyDMA (TWIM) is a two-wire half-duplex master which can communicate with multiple slave devices connected to the same bus

Listed here are the main features for TWIM:

- I²C compatible
- 100 kbps, 250 kbps, or 400 kbps
- · Support for clock stretching
- EasyDMA

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. TWIM is not compatible with CBUS.

The GPIOs used for each two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

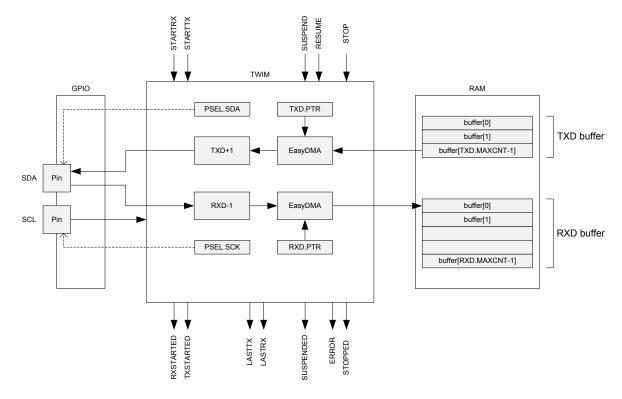


Figure 87: TWI master with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see *Figure 88: A typical TWI setup comprising one master and three slaves* on page 368. This TWIM is only able to operate as a single master on the TWI bus. Multi-master bus configuration is not supported.



Figure 88: A typical TWI setup comprising one master and three slaves

This TWI master supports clock stretching performed by the slaves. The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task. The TWI master will generate a STOPPED event when it has stopped following a STOP task.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

After the TWI master is started, the STARTTX task or the STARTRX task should not be triggered again before the TWI master has stopped, i.e. following a LASTRX, LASTTX or STOPPED event.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

32.1 Shared resources

The TWI master shares registers and other resources with other peripherals that have the same ID as the TWI master. Therefore, you must disable all peripherals that have the same ID as the TWI master before the TWI master can be configured and used.

Disabling a peripheral that has the same ID as the TWI master will not reset any of the registers that are shared with the TWI master. It is therefore important to configure all relevant registers explicitly to secure that the TWI master operates correctly.

The Instantiation table in *Instantiation* on page 23 shows which peripherals have the same ID as the TWI.

32.2 EasyDMA

The TWI master implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

32.3 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes found in the transmit buffer located in RAM at the address specified in the TXD.PTR register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave.

A typical TWI master write sequence is illustrated in *Figure 89: TWI master writing data to a slave* on page 369. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.



A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.

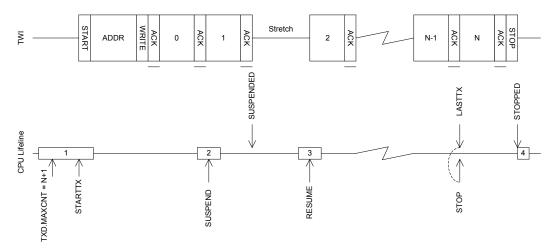


Figure 89: TWI master writing data to a slave

The TWI master will generate a LASTTX event when it starts to transmit the last byte, this is illustrated in *Figure 89: TWI master writing data to a slave* on page 369

The TWI master is stopped by triggering the STOP task, this task should be triggered during the transmission of the last byte to secure that the TWI will stop as fast as possible after sending the last byte. It is safe to use the shortcut between LASTTX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the whole RAM buffer has been sent, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

32.4 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1). The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

Data received will be stored in RAM at the address specified in the RXD.PTR register. The TWI master will generate an ACK after all but the last byte received from the slave. The TWI master will generate a NACK after the last byte received to indicate that the read sequence shall stop.

A typical TWI master read sequence is illustrated in *Figure 90: The TWI master reading data from a slave* on page 370. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.

The TWI master will generate a LASTRX event when it is ready to receive the last byte, this is illustrated in *Figure 90: The TWI master reading data from a slave* on page 370. If RXD.MAXCNT > 1 the LASTRX event is generated after sending the ACK of the previously received byte. If RXD.MAXCNT = 1 the LASTRX event is generated after receiving the ACK following the address and READ bit.



The TWI master is stopped by triggering the STOP task, this task must be triggered before the NACK bit is supposed to be transmitted. The STOP task can be triggered at any time during the reception of the last byte. It is safe to use the shortcut between LASTRX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the RAM buffer is full, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

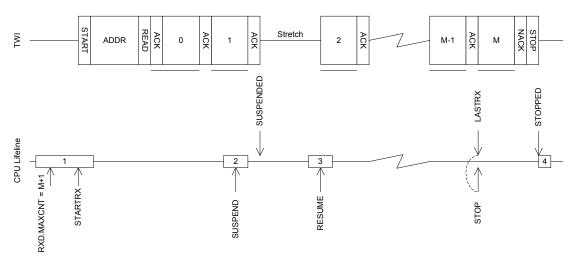


Figure 90: The TWI master reading data from a slave

32.5 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave. This example uses shortcuts to perform the simplest type of repeated start sequence, i.e. one write followed by one read. The same approach can be used to perform a repeated start sequence where the sequence is read followed by write.

The figure Figure 91: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave on page 370 illustrates this:

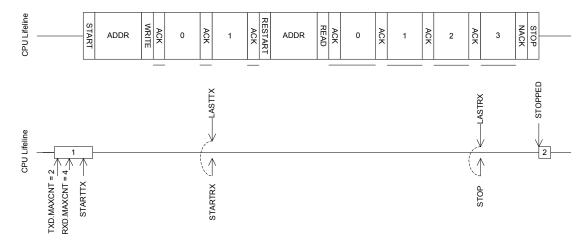


Figure 91: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave

If a more complex repeated start sequence is needed and the TWI firmware drive is serviced in a low priority interrupt it may be necessary to use the SUSPEND task and SUSPENDED event to guarantee that the



correct tasks are generated at the correct time. This is illustrated in *Figure 92: A double repeated start* sequence using the SUSPEND task to secure safe operation in low priority interrupts on page 371.

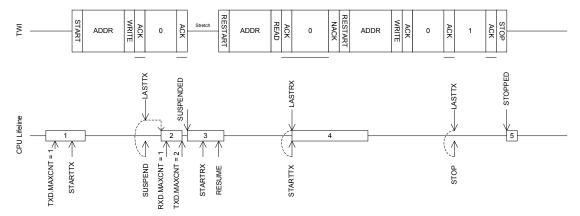


Figure 92: A double repeated start sequence using the SUSPEND task to secure safe operation in low priority interrupts

32.6 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

32.7 Master mode pin configuration

The SCL and SDA signals associated with the TWI master are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI master is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.SCL, PSEL.SDA must only be configured when the TWI master is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table 66: GPIO configuration before enabling peripheral* on page 371.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 66: GPIO configuration before enabling peripheral

TWI master signal	TWI master pin	Direction	Output value	Drive strength
SCL	As specified in PSEL.SCL	Input	Not applicable	S0D1
SDA	As specified in PSEL.SDA	Input	Not applicable	SOD1

32.8 Registers

Table 67: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	TWIM	TWIM0	Two-wire interface master 0	
0x40004000	TWIM	TWIM1	Two-wire interface master 1	



Table 68: Register Overview

TACKE STARTRY ON		
TASKS_STARTRX 0x	x000	Start TWI receive sequence
TASKS_STARTTX 0x	x008	Start TWI transmit sequence
TASKS_STOP 0x	x014	Stop TWI transaction. Must be issued while the TWI master is not suspended.
TASKS_SUSPEND 0x	x01C	Suspend TWI transaction
TASKS_RESUME 0x	x020	Resume TWI transaction
EVENTS_STOPPED 0x	x104	TWI stopped
EVENTS_ERROR 0x	x124	TWI error
EVENTS_SUSPENDED 0x	x148	Last byte has been sent out after the SUSPEND task has been issued, TWI traffic is now suspended.
EVENTS_RXSTARTED 0x	x14C	Receive sequence started
EVENTS_TXSTARTED 0x	x150	Transmit sequence started
EVENTS_LASTRX 0x	x15C	Byte boundary, starting to receive the last byte
EVENTS_LASTTX 0x	x160	Byte boundary, starting to transmit the last byte
SHORTS 0x	x200	Shortcut register
INTEN 0x	x300	Enable or disable interrupt
INTENSET 0x	x304	Enable interrupt
INTENCLR 0x	x308	Disable interrupt
ERRORSRC 0x	x4C4	Error source
ENABLE 0x	x500	Enable TWIM
PSEL.SCL 0x	x508	Pin select for SCL signal
PSEL.SDA 0x	x50C	Pin select for SDA signal
FREQUENCY 0x	x524	TWI frequency. Accuracy depends on the HFCLK source selected.
RXD.PTR 0x	x534	Data pointer
RXD.MAXCNT 0x	x538	Maximum number of bytes in receive buffer
RXD.AMOUNT 0x	x53C	Number of bytes transferred in the last transaction
RXD.LIST 0x	x540	EasyDMA list type
TXD.PTR 0x	x544	Data pointer
TXD.MAXCNT 0x	x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT 0x	x54C	Number of bytes transferred in the last transaction
TXD.LIST 0x	x550	EasyDMA list type
ADDRESS 0x	x588	Address used in the TWI transfer

32.8.1 SHORTS

Address offset: 0x200

Shortcut register

number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
			F D C B A
et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
RW Field	Value Id	Value	Description
RW LASTTX_STARTRX			Shortcut between LASTTX event and STARTRX task
			See EVENTS_LASTTX and TASKS_STARTRX
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut
RW LASTTX_SUSPEND			Shortcut between LASTTX event and SUSPEND task
			See EVENTS_LASTTX and TASKS_SUSPEND
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut
RW LASTTX_STOP			Shortcut between LASTTX event and STOP task
			See EVENTS_LASTTX and TASKS_STOP
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut
RW LASTRX_STARTTX			Shortcut between LASTRX event and STARTTX task
			See EVENTS_LASTRX and TASKS_STARTTX
	Disabled	0	Disable shortcut
	RW Field RW LASTTX_STARTRX RW LASTTX_SUSPEND RW LASTTX_STOP	RW Field Value Id RW LASTTX_STARTRX Disabled Enabled RW LASTTX_SUSPEND Disabled Enabled RW LASTTX_STOP Disabled Enabled RW LASTTX_STOP	RW Field Value Id Value I



Bit r	numbe	r		3	1 30	29	28	8 27	7 2	6 2	5 24	4 2	3 2	2 2	1 2	0 1	9 1	8 1	.7 1	6 :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																								F		D	С	В	Α							
Rese	et 0x0	0000000		0	0	0	0	0	C	0	0) (C	0	0) () ()	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	V	'alue							D	esc	ript	tion	1																				
			Enabled	1								Е	nab	le s	hoi	rtcı	ıt																			
F	RW	LASTRX_STOP										S	nor	tcut	t be	tw	eer	L/	STI	RX	eve	nt	and	TS b	ОР	tas	k									
												S	ee L	EVE	NTS	5_ <i>L</i> .	AS7	RX	an	d <i>T</i> .	ASI	(S_	STC)P												
			Disabled	0								D	isal	ble :	sho	rtc	ut																			
			Enabled	1								Е	nab	le s	hoi	rtcı	ıt																			

32.8.2 INTEN

Address offset: 0x300 Enable or disable interrupt

		or disable interre	<u>'</u>																							_	_	_		_	_	
	numbe	er		31	30 2	29 2	28 2.	/ 2	6 25			22 21				1/	16	15	14	13	12	11	10		8	/	6	5	4	3		
Id _														G										D								A
		0000000				0 (0 0) () (0		0 0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (
ld		Field	Value Id	Va	lue							scriptio																				
Α	RW	STOPPED									Ena	able or	dis	able	e in	terr	up	t fo	r S	IOP	PEI	e د	ven	t								
											See	EVEN	TS_	STC	PP	ED																
			Disabled	0							Disa	able																				
			Enabled	1							Ena	able																				
D	RW	ERROR									Ena	able or	dis	able	e in	terr	up	t fo	r E	RRC	Re	eve	nt									
											See	EVEN	TS	ERF	ROF	?																
			Disabled	0								able	Ī																			
			Enabled	1							Ena	able																				
F	RW	SUSPENDED									Ena	able or	dis	able	e in	terr	up	t fo	r S	JSP	ENI	DE	D ev	/en	t							
											۵۵۵	EVEN	ıTÇ	SLIS	DF	NDI	ח															
			Disabled	0								able	13_	.500	,, L	IVD	.0															
			Enabled	1							Ena																					
G	RW	RXSTARTED	2.100.00	-								able or	dis	able	in	terr	้นท	t fo	r R	XST.	٩R٦	ΓEΩ) ev	ent								
			5	_								EVEN	TS_	RXS	TA	RTE	D															
			Disabled	0								able																				
	DIA	TVCTADTED	Enabled	1							Ena								_	···												
Н	RW	TXSTARTED									Ena	able or	dis	able	e in	terr	up	t fo	r I.	XS I	ARI	IEL	ev ev	ent								
											See	EVEN	TS_	TXS	TA	RTE	D															
			Disabled	0							Disa	able																				
			Enabled	1							Ena	able																				
I	RW	LASTRX									Ena	able or	dis	able	e in	terr	up	t fo	r L	AST	RX (eve	ent									
											See	EVEN	TS_	LAS	TR.	X																
			Disabled	0							Disa	able																				
			Enabled	1							Ena	able																				
J	RW	LASTTX									Ena	ble or	dis	able	e in	terr	up	t fo	r L	AST	ГΧ є	eve	ent									
											See	EVEN	TS	LAS	TT	ĸ																
			Disabled	0								able	_																			
			Enabled	1							Ena																					
			2.100/04	-							Liid																					

32.8.3 INTENSET

Address offset: 0x304 Enable interrupt



Bit r	numb	er		31 30	29 2	28 2	7 26	25 2	24 :	2 21 20 19 18 17 16 15 14 13 12 13	10 9	8	7	5 5	4	3 2	2 1	0
Id									J	H G F	D						Α	
Res	et 0x0	00000000		0 0	0	0 0	0	0	0	0 0 0 0 0 0 0 0 0 0 0	0 0	0	0	0 0	0	0 0	0	0
Id	RW	Field	Value Id	Value					ı	cription								
Α	RW	STOPPED							١	e '1' to Enable interrupt for STOPPED	event							
									:	EVENTS_STOPPED								
			Set	1					ı	ole								
			Disabled	0					-	d: Disabled								
			Enabled	1					ı	d: Enabled								
D	RW	ERROR							١	e '1' to Enable interrupt for ERROR e	vent							
									:	EVENTS_ERROR								
			Set	1					ı	ole								
			Disabled	0					1	d: Disabled								
			Enabled	1					-	d: Enabled								
F	RW	SUSPENDED							١	e '1' to Enable interrupt for SUSPEND	ED ev	ent						
									:	EVENTS_SUSPENDED								
			Set	1					ı	ole								
			Disabled	0					-	d: Disabled								
			Enabled	1					ı	d: Enabled								
G	RW	RXSTARTED							١	e '1' to Enable interrupt for RXSTART	ED eve	nt						
									:	EVENTS_RXSTARTED								
			Set	1					1	ole								
			Disabled	0					ı	d: Disabled								
			Enabled	1					ı	d: Enabled								
Н	RW	TXSTARTED							١	e '1' to Enable interrupt for TXSTART	ED eve	nt						
									:	EVENTS_TXSTARTED								
			Set	1					ı	ole								
			Disabled	0					-	d: Disabled								
			Enabled	1					ı	d: Enabled								
1	RW	LASTRX							١	e '1' to Enable interrupt for LASTRX e	vent							
									:	EVENTS_LASTRX								
			Set	1					ı	ole								
			Disabled	0					-	d: Disabled								
			Enabled	1					ı	d: Enabled								
J	RW	LASTTX							١	e '1' to Enable interrupt for LASTTX e	vent							
									:	EVENTS_LASTTX								
			Set	1					1	ole								
			Disabled	0					ı	d: Disabled								
			Enabled	1					ı	d: Enabled								

32.8.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	r		31	30	29	28 2	27 2	6 2	5 24	1 23	3 22	21	20	19	18 1	7 1	6 15	5 14	1 13	12	11	10 9	9 8	7	6	5	4	3	2	1 0
Id										J	- 1			Н	G	F							[)						,	Α
Res	et 0x0	0000000		0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						D	escr	iptic	on																	
Α	RW	STOPPED									W	/rite	'1' t	o D	isat	le i	nter	rup	t fo	r ST	OPF	ED	ever	nt							
											Se	ee <i>E</i> '	VEN	TS_	STO	PPE	D														
			Clear	1							Di	isab	le																		
			Disabled	0							Re	ead:	Disa	able	ed																
			Enabled	1							Re	ead:	Ena	ble	d																
D	RW	ERROR									W	/rite	'1' t	o D	isak	le i	nter	rup	t fo	r ER	ROF	Rev	ent								
											Se	ee <i>E</i>	VEN	TS_	ERR	OR															



Reset 0x000000000	Bit r	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value Id Value Description Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled F RW SUSPENDED Write "1" to Disable interrupt for SUSPENDED event See EVENTS, SUSPENDED See EVENTS, SUSPENDED Clear 1 Disable Enabled 0 Read: Enabled G RW RXSTARTED Write "1" to Disable interrupt for RXSTARTED event Enabled 1 Disable Enabled 1 Read: Enabled H RW TXSTARTED Write "1" to Disable interrupt for TXSTARTED event Enabled 1 Read: Enabled Enabled 1 Read: Enabled I RW LASTRX Write "1" to Disable interrupt for LASTRX event Enabled 1 Read: Enabled I Read: Enabled Read: Disable Enabled 1 Read: Disable Enabled 1 Re	Id			J	I H G F D A
Clear	Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Disabled Enabled 1	Id	RW Field	Value Id	Value	Description
F RW SUSPENDED Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled F RW RXSTARTED Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled F RW TXSTARTED Clear 1 Disable Enabled 1 Read: Enabled F RW TXSTARTED Clear 1 Disable Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled F RW TXSTARTED Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled F Read: Disable Interrupt for LASTRX event F Read: Enabled F Read: Disable Interrupt for LASTRX event F Read: Enabled F Read: Disable Interrupt for LASTRX event F Read: Enabled F Read: Enabled F Read: Disable Interrupt for LASTRX event F Read: Enabled F Read: Disable Interrupt for LASTRX event F Read: Enabled F Read: Disable Interrupt for LASTRX event F Read: Enabled F Read: Disable Interrupt for LASTRX event F Read: Enabled F Read: Enabled F Read: Disabled			Clear	1	Disable
F RW SUSPENDED Clear			Disabled	0	Read: Disabled
Clear 1 Disable Read: Disabled 0 Read: Disabled Enabled 1 Read: Enabled GRAW RXSTARTED Clear 1 Disable Clear 1 Disable Clear 1 Disable Enabled 0 Read: Disabled Clear 1 Disable Enabled 0 Read: Disabled Enabled 1 Read: Enabled HRAW TXSTARTED Clear 1 Read: Enabled HRAW TXSTARTED Clear 1 Disable Clear 1 Disable Clear 1 Disabled Enabled 0 Read: Disabled Enabled 1 Read: Enabled Clear 1 Disabled Enabled 1 Read: Enabled Clear 1 Disabled Enabled 1 Read: Enabled IRAW LASTRX Clear 1 Disabled Enabled 1 Read: Enabled IRAW LASTRX Virite '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Virite '1' to Disable description interrupt for LASTRX event See EVENTS_LASTRX Virite '1' to Disabled Enabled 1 Read: Enabled IRAW LASTRX Clear 1 Disabled Enabled 1 Read: Enabled IRAW LASTRX Clear 1 Disabled Enabled 1 Read: Enabled IRAW LASTRX Virite '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Virite '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Disable Disabled 0 Read: Disabled			Enabled	1	Read: Enabled
Clear 1 Disable	F	RW SUSPENDED			Write '1' to Disable interrupt for SUSPENDED event
Clear 1 Disable					See EVENTS SUSPENDED
G RW RXSTARTED Clear 1 Disable H RW TXSTARTED Clear 1 Disable Enabled Disabled 0 Read: Disabled Enabled Enabled 1 Read: Enabled Read: Disabled Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for RXSTARTED Write '1' to Disable interrupt for TXSTARTED event See EVENTS_TXSTARTED Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled I Read: Enabl			Clear	1	_
G RW RXSTARTED Clear 1 Disable Brad: Enabled Clear 1 Read: Enabled H RW TXSTARTED Clear 1 Disable Enabled 1 Read: Enabled H RW TXSTARTED Clear 1 Disable Clear 1 Disable Enabled 0 Read: Disable interrupt for TXSTARTED event See EVENTS_TXSTARTED Clear 1 Disable Enabled 1 Read: Enabled I Read: Enable			Disabled	0	Read: Disabled
Clear 1 Disabled Brabled 1 Read: Disabled Enabled 1 Read: Disabled Interrupt for TXSTARTED Clear 1 Disable Clear 1 Disable From Polisabled 1 Read: Disable Interrupt for TXSTARTED Clear 1 Disable Enabled 1 Read: Enabled I Read: Disabled Enabled 1 Read: Enabled I Read: Disable Interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Disable Enabled 1 Read: Enabled I Read: Enabled I Read: Enabled I Read: Enabled Clear 1 Disable Enabled 1 Read: Enabled I Read: Enabled Read: Disable Interrupt for LASTTX event See EVENTS_LASTRX Clear 1 Disable Interrupt for LASTTX event See EVENTS_LASTRX Clear 1 Disable Read: Disable			Enabled	1	Read: Enabled
Clear 1 Disabled Disabled 0 Read: Disabled Enabled 1 Read: Enabled H RW TXSTARTED Clear 1 Disable Clear 1 Disable Disabled 0 Read: Disable interrupt for TXSTARTED event See EVENTS_TXSTARTED LASTRX Clear 1 Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Disable Enabled 1 Read: Enabled Unite '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Read: Enabled Disabled 0 Read: Disabled Read: Disabled Read: Disabled	G	RW RXSTARTED			Write '1' to Disable interrupt for RXSTARTED event
Clear 1 Disabled Disabled 0 Read: Disabled Enabled 1 Read: Enabled H RW TXSTARTED Clear 1 Disable Clear 1 Disable Disabled 0 Read: Disable interrupt for TXSTARTED event See EVENTS_TXSTARTED LASTRX Clear 1 Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Disable Enabled 1 Read: Enabled Unite '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Read: Enabled Disabled 0 Read: Disabled Read: Disabled Read: Disabled					Son EVENTS DYSTARTED
Disabled 0 Read: Disabled Enabled 1 Read: Enabled H RW TXSTARTED Clear 1 Disable Enabled 1 Read: Enabled Clear 1 Disable Enabled 1 Read: Disable Enabled 1 Read: Disable Enabled 1 Read: Disable Enabled 1 Read: Enabled I RW LASTRX Clear 1 Disable Enabled 0 Read: Disable interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Disable Enabled 1 Read: Enabled J Read: Disabled Enabled 1 Read: Disable Enabled 1 Read: Disable Enabled 1 Read: Disable Enabled 1 Read: Enabled J RW LASTTX Clear 1 Disable Enabled 1 Read: Enabled J Read: Disable interrupt for LASTRX event See EVENTS_LASTTX Original Provided Provid			Clear	1	
Enabled 1 Read: Enabled H RW TXSTARTED Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Read: Enabled Virite '1' to Disable interrupt for TXSTARTED Clear 1 Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Write '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Disabled Finabled 1 Read: Enabled Write '1' to Disable interrupt for LASTTX event See EVENTS_LASTTX Read: Disabled Read: Disabled Read: Disabled Read: Disabled					
H RW TXSTARTED Clear Disable Disabled Enabled Disabled Virite '1' to Disable interrupt for TXSTARTED Clear Disabled Read: Disabled Enabled Disabled Virite '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Clear Disabled					
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Read: Enabled Write '1' to Disable interrupt for LASTTX event See EVENTS_LASTTX Clear 1 Disable Disabled 0 Read: Disabled	Н	RW TXSTARTED	Enabled	-	
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled I RW LASTRX Clear 1 Disable Disabled 0 Read: Enabled I RW LASTRX Clear 1 Disable Enabled 1 Read: Disabled Enabled 1 Read: Disabled Enabled 1 Read: Enabled J RW LASTTX Clear 1 Disabled Enabled 1 Read: Enabled J Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for LASTTX event See EVENTS_LASTTX Clear 1 Disable Disable Disabled 0 Read: Disabled					
Disabled 0 Read: Disabled Enabled 1 Read: Enabled I RW LASTRX Clear 1 Disable Enabled 0 Read: Disabled Enabled 1 Read: Enabled Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled J RW LASTTX Clear 1 Disabled Enabled 1 Read: Enabled Disable interrupt for LASTTX event See EVENTS_LASTTX Write '1' to Disable interrupt for LASTTX event See EVENTS_LASTTX Clear 1 Disable Disable Read: Disabled					
Enabled 1 Read: Enabled I RW LASTRX Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled J RW LASTTX Vite '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Visabled Read: Disabled See EVENTS_LASTRX Vite '1' to Disable interrupt for LASTTX event See EVENTS_LASTTX Clear 1 Disable Disabled 0 Read: Disabled					
Write '1' to Disable interrupt for LASTRX event See EVENTS_LASTRX Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled J RW LASTTX Vite '1' to Disable interrupt for LASTRX event See EVENTS_LASTTX Clear 1 Disable Disabled 0 Read: Disabled					
See EVENTS_LASTRX Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled J RW LASTTX Clear 1 Disable interrupt for LASTTX event See EVENTS_LASTTX Clear 1 Disable Disabled 0 Read: Disabled			Enabled	1	
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled J RW LASTTX Write '1' to Disable interrupt for LASTTX event See EVENTS_LASTTX Clear 1 Disable Disabled 0 Read: Disabled	ı	RW LASTRX			Write '1' to Disable interrupt for LASTRX event
Disabled 0 Read: Disabled Enabled 1 Read: Enabled J RW LASTTX Write '1' to Disable interrupt for LASTTX event See EVENTS_LASTTX Clear 1 Disable Disabled 0 Read: Disabled					See EVENTS_LASTRX
Enabled 1 Read: Enabled J RW LASTTX Write '1' to Disable interrupt for LASTTX event See EVENTS_LASTTX Clear 1 Disable Disabled 0 Read: Disabled			Clear	1	Disable
J RW LASTTX Write '1' to Disable interrupt for LASTTX event See EVENTS_LASTTX Clear 1 Disable Disabled 0 Read: Disabled			Disabled	0	Read: Disabled
See EVENTS_LASTTX Clear 1 Disable Disabled 0 Read: Disabled			Enabled	1	Read: Enabled
Clear 1 Disable Disabled 0 Read: Disabled	J	RW LASTTX			Write '1' to Disable interrupt for LASTTX event
Disabled 0 Read: Disabled					See EVENTS_LASTTX
			Clear	1	Disable
Enabled 1 Read-Enabled			Disabled	0	Read: Disabled
בוומטוכט ב ווכמט. בוומטוכט			Enabled	1	Read: Enabled

32.8.5 ERRORSRC

Address offset: 0x4C4

Error source

Bit r	numbe	er		31 3	30 29	9 2	8 27	26	25	24	23 2	22 2	1 20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																													С	В	Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0 (0 0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Valu	ıe						Desc	crip	tion																		
Α	RW	OVERRUN									Ove	rrur	n err	or																	
											A ne	ew b	yte	was	re	ceiv	ed l	oefo	ore	orev	iou	s by	te g	ot t	ans	sfer	red				
											into	RXI	D bu	ffer	. (P	revi	ous	dat	a is	los	t)										
			NotReceived	0							Erro	r di	d no	t oc	cur																
			Received	1							Erro	r oc	curr	red																	
В	RW	ANACK									NAC	K re	eceiv	/ed	afte	er se	endi	ng 1	the	add	ress	(w	ite	'1' t	o cl	ear)					
			NotReceived	0							Erro	r di	d no	t oc	cur																
			Received	1							Erro	r oc	curr	red																	
С	RW	DNACK									NAC	K re	eceiv	/ed	afte	er se	endi	ng a	a da	ta b	yte	(wr	ite '	1' to	cle	ear)					
			NotReceived	0							Erro	r di	d no	t oc	cur																
			Received	1							Erro	r oc	curi	red																	

32.8.6 ENABLE

Address offset: 0x500



Enable TWIM

	Bit n	umbe	er		31 30	29	28 2	27 2	26 2	25 2	24	23	22	21 :	20 :	19 :	18	17	16	15	14	13	12	11 :	.0	9	8	7	6	5	4	3 :	2 1	L 0
	Id																															A A	A A	A A
	Rese	t 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0
	ld	RW	Field	Value Id	Value							Des	cri	otio	n																			
í	Α	RW	ENABLE									Ena	ble	or	disa	ble	TV	VIN	1															
				Disabled	0							Disa	able	TV	VIN	1																		
				Enabled	6							Ena	ble	ΤW	/IM																			

32.8.7 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

Bit n	iumbe	r		31	30 2	29 2	28 2	7 2	6 2	5 2	4 2	3 2	2 2	1 2	0 1	9 1	8 1	7 16	5 15	14	13	12	11 10	9	8	7	6	5	4	3	2	1 0
Id				С																								В	Α	Α.	Α,	А А
Rese	et OxF	FFFFFF		1	1	1	1 1	L 1	L 1	L 1	1	1 1	1 1	1 1	L 1	1 1	. 1	. 1	1	1	1	1	1 1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue						0	esc	rip	tior	1																	
Α	RW	PIN		[0.	.31]						P	in r	num	bei	r																	
В	RW	PORT		[0.	.1]						P	ort	nur	mbe	er																	
С	RW	CONNECT									C	oni	nect	tion	1																	
			Disconnected	1								Disc	onn	ect																		
			Connected	0							C	Conr	nect	t																		

32.8.8 PSEL.SDA

Address offset: 0x50C Pin select for SDA signal

Bit r	numbe	r		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ВАААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

32.8.9 FREQUENCY

Address offset: 0x524

TWI frequency. Accuracy depends on the HFCLK source selected.

Bit	numbe	r		31	30	29	28	27	26	25	24	23	22	21 :	20 :	19	18 1	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	A A	А А
Res	et 0x0	4000000		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	otio	n																			
Α	RW	FREQUENCY										ΤW	/I m	aste	er c	lock	c fre	qu	en	су														
			K100	0x	019	800	000					100) kb	ps																				
			K250	0x	040	000	000					250) kb	ps																				
			K400	0x	064	000	000					400) kb	ps																				

32.8.10 RXD.PTR

Address offset: 0x534

Data pointer



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Data pointer

32.8.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number		21 20 20 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
bit ilullibei		31 30 29 28 27 20 23	7 24 23 22 21 20 19 10 17 10 13 14 13 12 11 10 9 6 7 0 3 4 3 2 1 0
Id			A A A A A A A A
D+ 000000000			
Reset 0x00000000		0 0 0 0 0 0	
Id RW Field	Value Id	Value	Description
			•
A RW MAXCNT		[1255]	Maximum number of bytes in receive buffer

32.8.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit r	umbe	er		33	1 30	29	28	27 2	6 2	5 24	4 2	3 22	21	20 1	19 1	8 1	7 1	5 15	14	13	12	11 1	.0 9	9	8 7	' E	5	4	3	2	1)
Id																									A		A	Α	Α	Α	Α.	4
Res	t OxC	0000000		0	0	0	0	0 0) (0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 ()	0 0	0	0	0	0	0	0)
Id	RW	Field	Value Id	V	alue	•					D	escr	iptic	on																		ı
Α	R	AMOUNT									Ν	umb	er c	f by	tes	trar	ısfe	rred	in	the	last	trar	ısac	tio	n. Ir	ca	se o	f				_
											N	ACK	erro	or, ir	nclu	des	the	NA	CK'e	ed b	yte.											

32.8.13 RXD.LIST

Address offset: 0x540 EasyDMA list type

Bit	numbe	r		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16 1	.5 1	4 1	3 12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																A ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	alue	!						De	scri	ptic	on																		
Α	RW	LIST										Lis	t ty	pe																			
			Disabled	0								Dis	abl	e Ea	syE	M	۱ lis	t															
			ArrayList	1								Us	e ar	ray	list																		
				1											,																		

32.8.14 TXD.PTR

Address offset: 0x544

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW PTR		Data pointer

32.8.15 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer



ı	A RW MAXCNT		[1255]	Maximum number of bytes in transmit buffer
	ld RW Field	Value Id	Value	Description
	Reset 0x00000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
	Id			A A A A A A A A
	Bit number		31 30 29 28 27 26 25 24	$23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ \ 8\ \ 7\ \ 6\ \ 5\ \ 4\ \ 3\ \ 2\ \ 1\ \ 0$

32.8.16 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit	numbe	er		31	30 2	9 2	8 27	26	25	24	23 2	2 21	1 20) 19	18	17	16	15 1	4 1	3 12	11	10	9	8	7	6	5 -	4	3 2	1	0
Id																									Α	Α	A	Α /	4 A	Α	Α
Res	et 0x0	0000000		0	0	0 0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0
Id	RW	Field	Value Id	Va	lue						Desc	ript	ion																		
Α	R	AMOUNT									Num	ber	of I	byte	s tra	ansf	err	ed i	n the	e las	t tra	nsa	ctio	on.	ln c	ase	of				
											NIAC	K or	ror	incl	uda	c th	ωN	۸۲۱	ha'	hvt	2										

32.8.17 TXD.LIST

Address offset: 0x550 EasyDMA list type

Bit	numb	er		31	30 2	29 :	28 2	27 :	26	25	24	23	3 2:	2 2:	1 2	0 1	9 1	8 1	7 1	6 1	5 1	4 1	13 :	12 :	11 :	10	9	8	7	6	5	4	3	2	1 (
Id																																		Α	A A	
Res	et 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	(0) () ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	ı
Id	RW	Field	Value Id	Val	ue							De	esc	ript	ion																					ı
Α	RW	LIST										Lis	st t	ype																						
			Disabled	0								Di	sak	ole I	Eas	yDN	ЛΑ	list																		
			ArrayList	1								114		arra	1:	-+																				

32.8.18 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id				$A \; A \; A \; A \; A \; A \; A \; A$
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description	
A RW ADDRESS			Address used in the TWI transfer	

32.9 Electrical specification

32.9.1 TWIM interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIM,SCL}	Bit rates for TWIM ²⁷	100		400	kbps
I _{TWIM,100kbps}	Run current for TWIM, 100 kbps		50		μΑ
I _{TWIM,400kbps}	Run current for TWIM, 400 kbps		50		μΑ
t _{TWIM.START}	Time from STARTRX/STARTTX task to transmission started		1.5		μs

32.9.2 Two Wire Interface Master (TWIM) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{TWIM,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t _{TWIM,HD_DAT}	Data hold time after negative edge on SCL – all modes	500			ns

High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Symbol	Description	Min.	Тур.	Max.	Units
t _{TWIM,HD_STA,100kbps}	TWIM master hold time for START and repeated START	10000			ns
	condition, 100 kbps				
t _{TWIM,HD_STA,250kbps}	TWIM master hold time for START and repeated START	4000			ns
	condition, 250kbps				
$t_{TWIM,HD_STA,400kbps}$	TWIM master hold time for START and repeated START	2500			ns
	condition, 400 kbps				
$t_{TWIM,SU_STO,100kbps}$	TWIM master setup time from SCL high to STOP condition, 100	5000			ns
	kbps				
$t_{TWIM,SU_STO,250kbps}$	TWIM master setup time from SCL high to STOP condition, 250	2000			ns
	kbps				
$t_{TWIM,SU_STO,400kbps}$	TWIM master setup time from SCL high to STOP condition, 400	1250			ns
	kbps				
$t_{TWIM,BUF,100kbps}$	TWIM master bus free time between STOP and START	5800			ns
	conditions, 100 kbps				
t _{TWIM,BUF,250kbps}	TWIM master bus free time between STOP and START	2700			ns
	conditions, 250 kbps				
t _{TWIM,BUF,400kbps}	TWIM master bus free time between STOP and START	2100			ns
	conditions, 400 kbps				

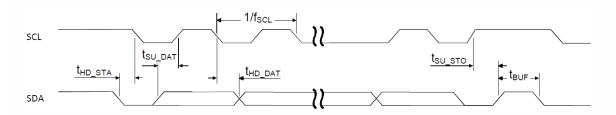


Figure 93: TWIM timing diagram, 1 byte transaction

32.10 Pullup resistor

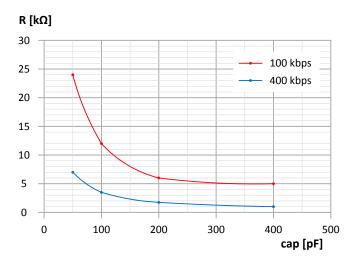


Figure 94: Recommended TWIM pullup value vs. line capacitance

- The I2C specification allows a line capacitance of 400 pF at most.
- The value of internal pullup resistor (R_{PU}) for nRF52840 can be found in the GPIO General purpose input/output on page 154 section.



33 TWIS — I²C compatible two-wire interface slave with EasyDMA

TWI slave with EasyDMA (TWIS) is compatible with I²C operating at 100 kHz and 400 kHz. The TWI transmitter and receiver implement EasyDMA.

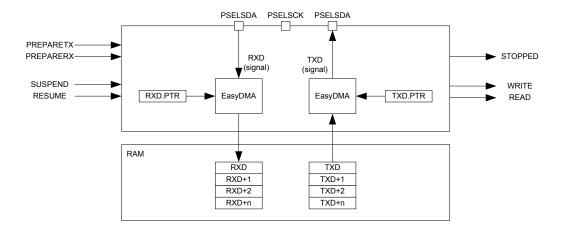


Figure 95: TWI slave with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see *Figure 96: A typical TWI setup comprising one master and three slaves* on page 380. TWIS is only able to operate with a single master on the TWI bus.

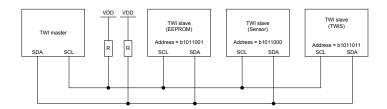


Figure 96: A typical TWI setup comprising one master and three slaves

The TWI slave state machine is illustrated in *Figure 97: TWI slave state machine* on page 381 and *Table 69: TWI slave state machine symbols* on page 381 is explaining the different symbols used in the state machine.



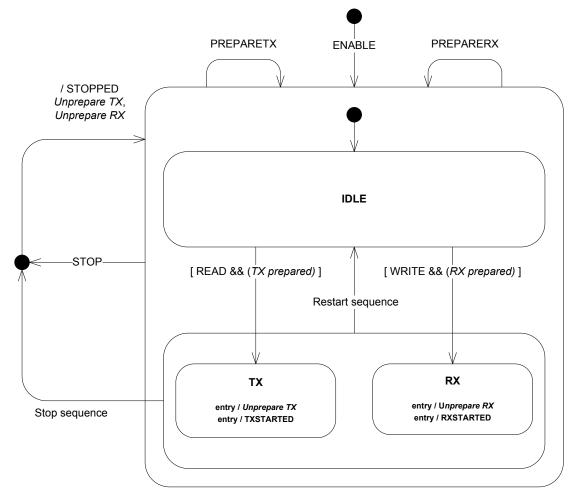


Figure 97: TWI slave state machine

Table 69: TWI slave state machine symbols

	_	
Symbol	Туре	Description
ENABLE	Register	The TWI slave has been enabled via the ENABLE register
PREPARETX	Task	The TASKS_PREPARETX task has been triggered
STOP	Task	The TASKS_STOP task has been triggered
PREPARERX	Task	The TASKS_PREPARERX task has been triggered
STOPPED	Event	The EVENTS_STOPPED event was generated
RXSTARTED	Event	The EVENTS_RXSTARTED event was generated
TXSTARTED	Event	The EVENTS_TXSTARTED event was generated
TX prepared	Internal	Internal flag indicating that a TASKS_PREPARETX task has been triggered. This flag is not visible to the user.
RX prepared	Internal	Internal flag indicating that a TASKS_PREPARERX task has been triggered. This flag is not visible to the user.
Unprepare TX	Internal	Clears the internal 'TX prepared' flag until next TASKS_PREPARETX task.
Unprepare RX	Internal	Clears the internal 'RX prepared' flag until next TASKS_PREPARERX task.
Stop sequence	TWI protocol	A TWI stop sequence was detected
Restart sequence	TWI protocol	A TWI restart sequence was detected

The TWI slave supports clock stretching performed by the master.

The TWI slave operates in a low power mode while waiting for a TWI master to initiate a transfer. As long as the TWI slave is not addressed, it will remain in this low power mode.

To secure correct behaviour of the TWI slave, PSEL.SCL, PSEL.SDA, CONFIG and the ADDRESS[n] registers, must be configured prior to enabling the TWI slave through the ENABLE register. Similarly, changing these settings must be performed while the TWI slave is disabled. Failing to do so may result in unpredictable behaviour.



33.1 Shared resources

The TWI slave shares registers and other resources with other peripherals that have the same ID as the TWI slave.

Therefore, you must disable all peripherals that have the same ID as the TWI slave before the TWI slave can be configured and used. Disabling a peripheral that has the same ID as the TWI slave will not reset any of the registers that are shared with the TWI slave. It is therefore important to configure all relevant registers explicitly to secure that the TWI slave operates correctly.

The Instantiation table in *Instantiation* on page 23 shows which peripherals have the same ID as the TWI slave.

33.2 EasyDMA

The TWI slave implements EasyDMA for reading and writing to and from the RAM.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

33.3 TWI slave responding to a read command

Before the TWI slave can respond to a read command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume $I_{\rm IDLE}$.

A read command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the TWI slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the read command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a READ event when it acknowledges the read command.

The TWI slave is only able to detect a read command from the IDLE state.

The TWI slave will set an internal 'TX prepared' flag when the PREPARETX task is triggered.

When the read command is received the TWI slave will enter the TX state if the internal 'TX prepared' flag is set.

If the internal 'TX prepared' flag is not set when the read command is received, the TWI slave will stretch the master's clock until the PREPARETX task is triggered and the internal 'TX prepared' flag is set.

The TWI slave will generate the TXSTARTED event and clear the 'TX prepared' flag ('unprepare TX') when it enters the TX state. In this state the TWI slave will send the data bytes found in the transmit buffer to the master using the master's clock. The TWI slave will consume I_{TX} in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the TX state

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the 'TX prepared' flag ('unprepare TX') and go back to the IDLE state when it has stopped.

The transmit buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to send TXD.MAXCNT bytes from the transmit buffer for each transaction. If the TWI master



forces the slave to send more than TXD.MAXCNT bytes, the slave will send the byte specified in the ORC register to the master instead. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see TXD.PTR etc., are latched when the TXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the 'TX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 385.

Each byte sent from the slave will be followed by an ACK/NACK bit sent from the master. The TWI master will generate a NACK following the last byte that it wants to receive to tell the slave to release the bus so that the TWI master can generate the stop condition. The TXD.AMOUNT register can be queried after a transaction to see how many bytes were sent.

A typical TWI slave read command response is illustrated in *Figure 98: The TWI slave responding to a read command* on page 383. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

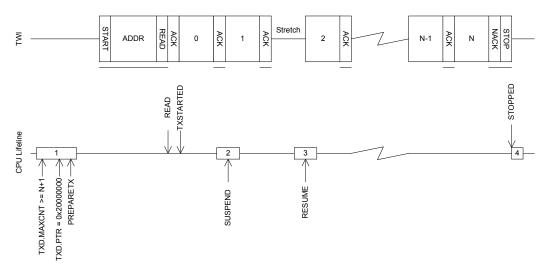


Figure 98: The TWI slave responding to a read command

33.4 TWI slave responding to a write command

Before the TWI slave can respond to a write command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume $I_{\rm IDLE}$.

A write command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the write command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a WRITE event if it acknowledges the write command.

The TWI slave is only able to detect a write command from the IDLE state.

The TWI slave will set an internal 'RX prepared' flag when the PREPARERX task is triggered.

When the write command is received the TWI slave will enter the RX state if the internal 'RX prepared' flag is set.

If the internal 'RX prepared' flag is not set when the write command is received, the TWI slave will stretch the master's clock until the PREPARERX task is triggered and the internal 'RX prepared' flag is set.



The TWI slave will generate the RXSTARTED event and clear the internal 'RX prepared' flag ('unprepare RX') when it enters the RX state. In this state the TWI slave will be able to receive the bytes sent by the TWI master. The TWI slave will consume I_{RX} in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the RX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the internal 'RX prepared' flag ('unprepare RX') and go back to the IDLE state when it has stopped.

The receive buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to receive as many bytes as specified in the RXD.MAXCNT register. If the TWI master tries to send more bytes to the slave than the slave is able to receive, these bytes will be discarded and the bytes will be NACKed by the slave. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see RXD.PTR etc., are latched when the RXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the internal 'RX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 385.

The TWI slave will generate an ACK after every byte received from the master. The RXD.AMOUNT register can be queried after a transaction to see how many bytes were received.

A typical TWI slave write command response is illustrated in *Figure 99: The TWI slave responding to a write command* on page 384. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

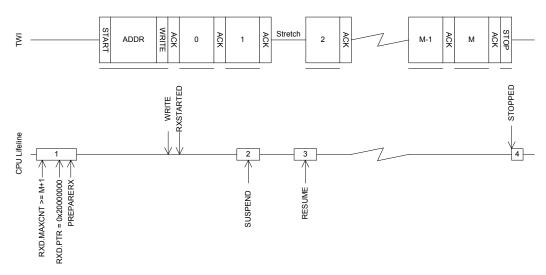


Figure 99: The TWI slave responding to a write command

33.5 Master repeated start sequence

An example of a repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave.

This is illustrated in Figure 100: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave on page 385.

It is here assumed that the receiver does not know in advance what the master wants to read, and that this information is provided in the first two bytes received in the write part of the repeated start sequence. To guarantee that the CPU is able to process the received data before the TWI slave starts to reply to the read command, the SUSPEND task is triggered via a shortcut from the READ event generated when the read command is received. When the CPU has processed the incoming data and prepared the correct data response, the CPU will resume the transaction by triggering the RESUME task.



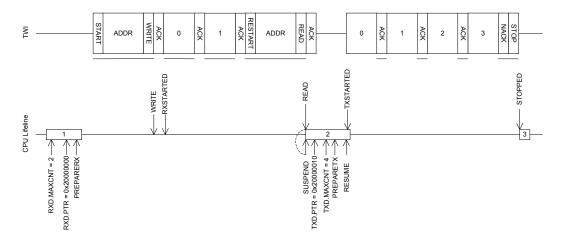


Figure 100: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave

33.6 Terminating an ongoing TWI transaction

In some situations, e.g. if the external TWI master is not responding correctly, it may be required to terminate an ongoing transaction.

This can be achieved by triggering the STOP task. In this situation a STOPPED event will be generated when the TWI has stopped independent of whether or not a STOP condition has been generated on the TWI bus. The TWI slave will release the bus when it has stopped and go back to its IDLE state.

33.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

33.8 Slave mode pin configuration

The SCL and SDA signals associated with the TWI slave are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI slave is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.SCL and PSEL.SDA must only be configured when the TWI slave is disabled.

To secure correct signal levels on the pins used by the TWI slave when the system is in OFF mode, and when the TWI slave is disabled, these pins must be configured in the GPIO peripheral as described in *Table 70: GPIO configuration before enabling peripheral* on page 385.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 70: GPIO configuration before enabling peripheral

TWI slave signal	TWI slave pin	Direction	Output value	Drive strength
SCL	As specified in PSEL.SCL	Input	Not applicable	SOD1
SDA	As specified in PSEL.SDA	Input	Not applicable	S0D1



33.9 Registers

Table 71: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
0x40004000	TWIS	TWIS1	Two-wire interface slave 1	

Table 72: Register Overview

Register	Offset	Description
TASKS_STOP	0x014	Stop TWI transaction
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
TASKS_PREPARERX	0x030	Prepare the TWI slave to respond to a write command
TASKS_PREPARETX	0x034	Prepare the TWI slave to respond to a read command
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_ERROR	0x124	TWI error
EVENTS_RXSTARTED	0x14C	Receive sequence started
EVENTS_TXSTARTED	0x150	Transmit sequence started
EVENTS_WRITE	0x164	Write command received
EVENTS_READ	0x168	Read command received
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4D0	Error source
MATCH	0x4D4	Status register indicating which address had a match
ENABLE	0x500	Enable TWIS
PSEL.SCL	0x508	Pin select for SCL signal
PSEL.SDA	0x50C	Pin select for SDA signal
RXD.PTR	0x534	RXD Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in RXD buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last RXD transaction
TXD.PTR	0x544	TXD Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in TXD buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last TXD transaction
ADDRESS[0]	0x588	TWI slave address 0
ADDRESS[1]	0x58C	TWI slave address 1
CONFIG	0x594	Configuration register for the address match mechanism
ORC	0x5C0	Over-read character. Character sent out in case of an over-read of the transmit buffer.

33.9.1 SHORTS

Address offset: 0x200

Shortcut register

Bit r	numbe	er		3	1 30	29	2	8 2	7 2	6 2	5 2	24 2	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																						В	Α													
Res	et 0x0	0000000		0	0	0	0	0) (0 0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ld	RW	Field	Value Id	٧	alue								Des	scr	iptio	on																				
Α	RW	WRITE_SUSPEND										9	Sho	orto	cut l	etv	we	en '	WR	ITE	eve	nt	and	l SU	SPE	ND	tas	k								
												9	See	e <i>E</i> '	VEN	TS_	W	RITI	ar	nd 7	ASI	(S_	SUS	PEI	VD											
			Disabled	0								[Disa	ab	le sh	ort	cu	t																		
			Enabled	1								E	Ena	abl	e sh	orto	cut	:																		
В	RW	READ_SUSPEND										9	Sho	orto	cut l	oetv	we	en l	REA	D e	eve	nt a	nd	SUS	PEI	ND t	ask									
												9	See	e <i>E</i> 1	VEN	TS_	RE	AD	and	d TA	4 <i>5K</i> .	s_s	USI	PEN	D											



Bit number		31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut

33.9.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit	numbe	r .		31 30) 20	9 2:	8 27	26	25	24	1 23	22	21	20	19	18	17	16	15	14	13	12	1	1 10) 9	8	7	6	5	4	3	2	1 (
Id	Turribe	, t		51 50	, 2.	J 21	0 27		G		. 23	22	21		E	10	1,	10	13	17	13	12	- 1	1 10	, Б		,	Ü	,	_	5		Α '
	et 0x0	0000000		0 0	0	0	0 (0	0	0			0	0	0	0	0	0	0	0	0			0	0	0	0	0		
Id	RW	Field	Value Id	Value									iptic																				
Α	RW	STOPPED									Ena	able	e or	dis	sabl	e in	iter	rup	t fo	or S	TOI	PPE	D	eve	nt								
											See	e <i>E</i> ۱	VEN	TS_	_ST(OPF	PED																
			Disabled	0							Dis	sabl	le																				
			Enabled	1							Ena	able	е																				
В	RW	ERROR									Ena	able	e or	dis	sabl	e in	iter	rup	t fo	or E	RR	OR	ev	ent									
				0							See	e <i>E</i> ۱	VEN	TS_	ER	ROF	?																
			Disabled	0							Dis	sabl	le																				
			Enabled	1							Ena	able	e																				
E	RW	RXSTARTED		1							Ena	able	e or	dis	sabl	e in	iter	rup	t fo	or R	XST	ΓAF	RTE	D e	ven	t							
				1							See	e <i>E</i> ۱	VEN	TS_	_RX.	STA	RTI	ED															
			Disabled	0							Dis	sabl	le																				
			Enabled	1							Ena	able	e																				
F	RW	TXSTARTED									Ena	able	e or	dis	sabl	e in	iter	rup	t fo	r T	XST	AR	RTE	D e	/en	t							
											See	e <i>E</i> ۱	VEN	TS_	_TX	STA	RT	D															
			Disabled	0							Dis	sabl	le																				
			Enabled	1							Ena	able	e																				
G	RW	WRITE									Ena	able	e or	dis	sabl	e in	iter	rup	t fo	or V	VRI	TE	eve	ent									
											See	e <i>E</i> \	VEN	TS_	_WF	RITE																	
			Disabled	0							Dis	sabl	le																				
			Enabled	1							Ena	able	e																				
Н	RW	READ									Ena	able	e or	dis	sabl	e in	iter	rup	t fo	or R	EAI	D e	vei	nt									
											See	e <i>E</i> ۱	VEN	TS_	_RE	AD																	
			Disabled	0							Dis	sabl	le																				
			Enabled	1							Ena	able	e																				

33.9.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	numbe	er		31 3	30 2	9 2	28 2	7 2	6 2	5 2	24 2	3 2	2 21	1 20	19	18	17	16	15	14	13 1	L2 1	.1 10	9	8	7	6	5	4	3	2	1 0
Id								ŀ	Н Э	ò				F	Ε									В								Α
Res	et 0x0	0000000		0	0 0) (0 0) (0 0) (0 () (0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe						D	esc	cript	ion																		
Α	RW	STOPPED									٧	√rit	e '1'	' to I	Ena	ble	inte	rru	pt f	or S	TO	PPE	D ev	ent								
											S	ee l	EVEI	NTS_	_ST	ОРІ	PED															
			Set	1							Ε	nab	ole																			
			Disabled	0							R	eac	d: Di	sabl	led																	
			Enabled	1							R	eac	d: En	nable	ed																	
В	RW	ERROR									٧	۷rit	e '1'	to l	Ena	ble	inte	rru	pt f	or E	RR	OR 6	even	t								



Bit number			31 3	25 24	4 23	3 22 21	. 20	19	18 1	7 1	5 15	14	13 :	12 1	1 10	9	8	7	6	5 4	3	2	1 0			
Id			H G 0 0 0 0 0 0 0 0 Value							F	Е								В							Α
Reset 0x000	000000		0	0 0	0 (0 0	0 0	0	0 0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id RW F	Field	Value Id	Valu	ıe				De	escripti	ion																
								Se	ee <i>EVEN</i>	VTS_	ERR	OR														
		Set	1					En	nable																	
		Disabled	0					Re	ead: Dis	sabl	ed															
		Enabled	1					Re	ead: En	able	ed															
E RW F	RXSTARTED							W	/rite '1'	to E	Enab	le in	terr	upt	for I	RXS	TART	ED 6	ever	nt						
								Se	ee <i>EVEN</i>	NTS_	RXS	TAR	TED	ı												
		Set	1						nable																	
		Disabled	0					Re	ead: Dis	sabl	ed															
		Enabled	1					Re	ead: En	able	ed															
F RW 1	TXSTARTED							W	/rite '1'	to E	Enab	le in	terr	upt	for 7	ΓXS٦	ΓART	ED 6	ever	nt						
								Se	ee <i>EVEN</i>	VTS	TXS	TAR	TED													
		Set	1						nable	_																
		Disabled	0					Re	ead: Dis	sabl	ed															
		Enabled	1					Re	ead: En	able	ed															
G RW V	WRITE							W	rite '1'	to E	Enab	le in	terr	upt	for \	WRI	TE e	vent								
								So	ee <i>EVEN</i>	UTC	IA/D	ITE														
		Set	1						nable	V13_	_ VV A.	IIE														
		Disabled	0						ead: Dis	ahl	ьd															
		Enabled	1						ead: En																	
H RW F	READ	Lindoled	-						/rite '1'			le in	terr	unt	for I	REA	D ev	ent								
									ee <i>EVEN</i>	VTS_	_REA	\D														
		Set	1						nable																	
		Disabled	0						ead: Dis																	
		Enabled	1					Re	ead: En	able	ed															

33.9.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	r		31 3	0 29	28 2	27 2	26 25	24	23	22	21 2	20 1	L9 18	8 17	7 16	15	14	13 1	2 1:	1 10	9	8	7	5 5	4	3	2	1 0
Id							1	H G					FI	E								В						,	Ą
Rese	et 0x0	0000000		0 (0 0	0	0	0 0	0	0	0	0 (0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0 (0 0
Id	RW	Field	Value Id	Valu	e					De	scri	iptio	n																
Α	RW	STOPPED								Wr	rite	'1' to	Di:	sabl	e in	terr	upt	for :	STOF	PEI) ev	ent							
										See	e <i>E</i> V	/ENT	'S_S	TOP	PEL)													
			Clear	1						Dis	sabl	e																	
			Disabled	0						Rea	ad:	Disal	bled	d															
			Enabled	1						Rea	ad:	Enab	oled	ł															
В	RW	ERROR								Wr	rite	'1' to	Di:	sabl	e in	terr	upt	for	ERRO	OR 6	even	t							
										See	e <i>E</i> V	/ENT	S_E	RRC)R														
			Clear	1						Dis	sabl	e																	
			Disabled	0						Rea	ad:	Disal	ble	d															
			Enabled	1						Rea	ad:	Enab	oled	ł															
E	RW	RXSTARTED								Wr	rite	'1' to	Di:	sabl	e in	terr	upt	for	RXST	AR	ΓED	eve	nt						
										See	e <i>E</i> V	/ENT	S_R	RXST	AR	ΓED													
			Clear	1						Dis	sabl	e																	
			Disabled	0						Rea	ad:	Disal	bled	d															
			Enabled	1						Rea	ad:	Enab	oled	ł															
F	RW	TXSTARTED								Wr	rite	'1' to	Di:	sabl	e in	terr	upt	for '	TXST	AR	ΓED	evei	nt						
										See	e <i>E</i> V	/ENT	S_7	TXST.	ART	ED													
			Clear	1							sabl																		



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		H G	F E B A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
G RW WRITE			Write '1' to Disable interrupt for WRITE event
			See EVENTS_WRITE
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
H RW READ			Write '1' to Disable interrupt for READ event
			See EVENTS_READ
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

33.9.5 ERRORSRC

Address offset: 0x4D0

Error source

Bit r	numbe	r		31	. 30	29	28 2	7 :	26 2	25 2	24 2	3 22	21	20	19	18	17 :	16	15	14 1	.3 1	.2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																														C E	3	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Va	alue)esci	iptio	on																		
Α	RW	OVERFLOW		0						F	RX bι	ffer	ove	erflo	w c	dete	ecte	ed,	and	pre	ver	ted										
			NotDetected	0 1					E	rror	did	not	occ	ur																		
			Detected							E	rror	occı	ırre	d																		
В	RW	DNACK									١	IACK	sen	t af	ter	rec	eivi	ng a	a da	ita b	yte	2										
			NotReceived	0							E	rror	did	not	occ	ur																
			Received	1							E	rror	occı	ırre	d																	
С	RW	OVERREAD									7	Χbι	ffer	ove	er-re	ad	det	ect	ed,	and	l pr	eve	nte	ł								
			NotDetected	0							E	rror	did	not	occ	ur																
			Detected	1							E	rror	occı	ırre	d																	

33.9.6 MATCH

Address offset: 0x4D4

Status register indicating which address had a match

Bit	numb	er		31 30 2	9 28	27 26	6 25	5 24	23	22 :	21 2	0 19	18	17	16	15 :	14 13	3 12	11 :	10 9	8	7	6	5	4 3	2	1)
Id																												4
Res	et 0x(0000000		0 0	0 0	0 0	0	0	0	0	0 (0	0	0	0	0	0 0	0	0	0 0	0	0	0	0	0 0	0	0)
Id	RW	Field	Value Id	Value					Des	crip	otior	,																
Α	R	MATCH		[01]					Wh	ich	of th	ne ad	ddre	sse	s in	(AD	DRE:	SS} n	natc	hed 1	he i	nco	min	g				
									add	lres	S																	

33.9.7 ENABLE

Address offset: 0x500

Enable TWIS

Bit	number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A
Res	et 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW ENABLE			Enable or disable TWIS
		Disabled	0	Disable TWIS



Bit number		31 30 29 28 27 20	6 25 24 23 22 21 20 19 18 17 16	5 15 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0
Id					АААА
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description		
	Enabled	9	Enable TWIS		

33.9.8 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

Bit r	numbe	r		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ВАААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1	$1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

33.9.9 PSEL.SDA

Address offset: 0x50C Pin select for SDA signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	вааа
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

33.9.10 RXD.PTR

Address offset: 0x534 RXD Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0										
Id		A A A A A A A A A A A A A A A A A A A										
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0										
Id RW Field	Value Id	Value Description										
A RW PTR		RXD Data pointer										

A RW PIR RXD Data pointe

33.9.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in RXD buffer

Bit r	umber			31	30	29	28 2	27 20	5 25	5 24	1 23	22	21	20	19	18	17 1	16	15 1	.4 1	3 12	11	10	9	8	7	6	5	4 3	2	1	0
Id																										Α	A	Α.	A A	A	Α	Α
Rese	et 0x000	00000		0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW Fi	eld	Value Id	Va	lue						De	scri	ptic	n																		
Α	RW M	IAXCNT		Maximum number of bytes in RXD buffer																												



33.9.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last RXD transaction

Bit	numb	er		31 30 2	29 28	3 27 20	5 25	24	23 2	2 21	. 20	19 3	18 1	7 10	5 15	14	13	12 :	11 10	9	8	7	6	5	4	3 :	2 1	0
Id																						Α	Α	Α	Α	A	4 A	Α
Reset 0x00000000 0 0 0 0 0						0 0	0	0	0 0	0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Value Description							ion																	
Α	R	AMOUNT		Number of bytes transferred in the last RXD transaction																								

33.9.13 TXD.PTR

Address offset: 0x544
TXD Data pointer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0												
Id	_ A A A A A A A A A A A A A A A A A A A												
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0												
Id RW Field Value Id	Value Description												
A RW PTR	TXD Data pointer												

33.9.14 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in TXD buffer

Bit r	numbe	er		31 30 29 28 27 2	26 25 24	23 22	21 2	0 19	18 17	7 16	15	14 1	3 12	11 10	9	8	7	6	5	4	3	2 1	. 0
Id																	Α	Α	Α	Α	Α .	A A	АА
Res	et 0x0	0000000		0 0 0 0 0	0 0 0	0 0	0 0	0 (0 0	0	0	0 (0 0	0 0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Value		Descr	iption	1															
Α	RW	MAXCNT		Maximum number of bytes in TXD buffer																			

33.9.15 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last TXD transaction

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A R AMOUNT		Number of bytes transferred in the last TXD transaction

33.9.16 ADDRESS[0]

Address offset: 0x588 TWI slave address 0

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0						
Id					A A A A A A						
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0						
Id RW Field	Value Id	Value	Description								
A RW ADDRESS		TWI slave address									

33.9.17 ADDRESS[1]

Address offset: 0x58C TWI slave address 1



Bit	numbe	er		31	30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 :	10	9	8	7	6	5	4	3 2	1	. 0
Id																													Α.	Α	Α /	Δ Δ	A	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue	:						De	scri	pti	on																			
Α	RW	ADDRESS		TWI slave address																														

33.9.18 CONFIG

Address offset: 0x594

Configuration register for the address match mechanism

Bit n	iumbe	r		31	L 30	29	28	3 27	26	25	24	23	22	21 :	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		ВА
Reset 0x00000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 1		
Id	RW	Field	Value Id	Va	alue							Des	cri	otio	n																			
A RW ADDRESSO											Ena	ble	or	dis	abl	e a	ddı	ess	ma	atch	ing	on	ΑD	DRI	ESS	[0]								
			Disabled	0								Dis	able	ed																				
			Enabled	1								Ena	ble	d																				
В	RW	ADDRESS1										Ena	ble	or	dis	abl	e a	ddı	ess	ma	atch	ing	on	ΑD	DRI	ESS	[1]							
			Disabled	0								Dis	able	ed																				
			Enabled	1								Ena	ble	d																				

33.9.19 ORC

Address offset: 0x5C0

Over-read character. Character sent out in case of an over-read of the transmit buffer.

Bit	numb	er		31 30	29 2	28 27	26	25 2	4 2	3 22	21	20 2	19 1	.8 17	16	15	14	13	12 1	1 10	9	8	7	6	5 -	4 3	2	1	0
Id																							Α	Α	A .	A A	Α	Α	Α
Re	set 0x0	0000000		0 0	0 (0 0	0	0 (0 (0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Value					D	escr	ipti	on																	
Α	RW	ORC		Over-read character. Character sent out in case of an over-read																									
									o	f the	tra	nsm	it b	uffer															

33.10 Electrical specification

33.10.1 TWIS slave interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIS,SCL}	Bit rates for TWIS ²⁸	100		400	kbps
I _{TWIS,100kbps}	Run current for TWIS (Average current to receive and transfer a		45		μΑ
	byte to RAM), 100 kbps				
I _{TWIS,400kbps}	Run current for TWIS (Average current to receive and transfer a		45		μΑ
	byte to RAM), 400 kbps				
I _{TWIS,IDLE}	Idle current for TWIS		1		μΑ
t _{TWIS,START}	Time from PREPARERX/PREPARETX task to ready to receive/		1.5		μs
	transmit				

33.10.2 TWIS slave timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{TWIS,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t _{TWIS,HD_DAT}	Data hold time after negative edge on SCL – all modes	500			ns
t _{TWIS,HD_STA,100kbps}	TWI slave hold time from for START condition (SDA low to SCL	5200			ns
	low), 100 kbps				

High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Symbol	Description	Min.	Тур.	Max.	Units
t _{TWIS,HD_STA,400kbps}	TWI slave hold time from for START condition (SDA low to SCL	1300			ns
	low), 400 kbps				
t _{TWIS,SU_STO,100kbps}	TWI slave setup time from SCL high to STOP condition, 100 kbps	5200			ns
t _{TWIS,SU_STO,400kbps}	TWI slave setup time from SCL high to STOP condition, 400 kbps	1300			ns
t _{TWIS,BUF,100kbps}	TWI slave bus free time between STOP and START conditions,		4700		ns
	100 kbps				
t _{TWIS,BUF,400kbps}	TWI slave bus free time between STOP and START conditions,		1300		ns
	400 kbps				

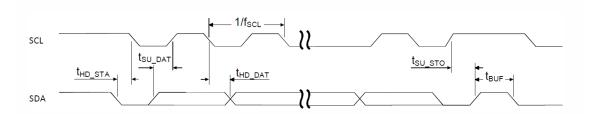


Figure 101: TWIS timing diagram, 1 byte transaction



34 UARTE — Universal asynchronous receiver/ transmitter with EasyDMA

The Universal asynchronous receiver/transmitter with EasyDMA (UARTE) offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware at a rate up to 1 Mbps, and EasyDMA data transfer from/to RAM.

Listed here are the main features for UARTE:

- Full-duplex operation
- · Automatic hardware flow control
- Optional even parity bit checking and generation
- EasyDMA
- Up to 1 Mbps baudrate
- · Return to IDLE between transactions supported (when using HW flow control)
- One or two stop bit
- Least significant bit (LSB) first

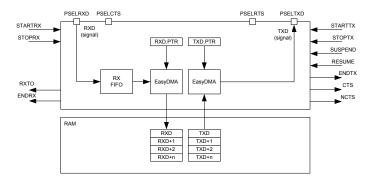


Figure 102: UARTE configuration

The GPIOs used for each UART interface can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

34.1 Shared resources

The UARTE shares registers and other resources with other peripherals that have the same ID as the UARTE.

Therefore, you must disable all peripherals that have the same ID as the UARTE before the UARTE can be configured and used. Disabling a peripheral that has the same ID as the UARTE will not reset any of the registers that are shared with the UARTE. It is therefore important to configure all relevant UARTE registers explicitly to ensure that it operates correctly.

See the Instantiation table in *Instantiation* on page 23 for details on peripherals and their IDs.

34.2 EasyDMA

The UARTE implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.



The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The ENDRX/ENDTX event indicates that EasyDMA has finished accessing respectively the RX/TX buffer in RAM.

34.3 Transmission

The first step of a DMA transmission is storing bytes in the transmit buffer and configuring EasyDMA. This is achieved by writing the initial address pointer to TXD.PTR, and the number of bytes in the RAM buffer to TXD.MAXCNT. The UARTE transmission is started by triggering the STARTTX task.

After each byte has been sent over the TXD line, a TXDRDY event will be generated.

When all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have been transmitted, the UARTE transmission will end automatically and an ENDTX event will be generated.

A UARTE transmission sequence is stopped by triggering the STOPTX task, a TXSTOPPED event will be generated when the UARTE transmitter has stopped.

If the ENDTX event has not already been generated when the UARTE transmitter has come to a stop, the UARTE will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

If flow control is enabled through the HWFC field in the CONFIG register, a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in *Figure 103: UARTE transmission* on page 395. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended.

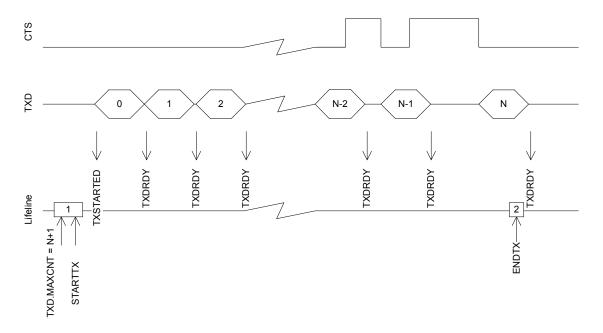


Figure 103: UARTE transmission

The UARTE transmitter will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTTX or after it has been stopped via STOPTX and the TXSTOPPED event has been generated. See *POWER* — *Power supply* on page 66 for more information about power modes.

34.4 Reception

The UARTE receiver is started by triggering the STARTRX task. The UARTE receiver is using EasyDMA to store incoming data in an RX buffer in RAM.



The RX buffer is located at the address specified in the RXD.PTR register. The RXD.PTR register is double-buffered and it can be updated and prepared for the next STARTRX task immediately after the RXSTARTED event is generated. The size of the RX buffer is specified in the RXD.MAXCNT register and the UARTE will generate an ENDRX event when it has filled up the RX buffer, see *Figure 104: UARTE reception* on page 396.

For each byte received over the RXD line, an RXDRDY event will be generated. This event is likely to occur before the corresponding data has been transferred to Data RAM.

The RXD.AMOUNT register can be queried following an ENDRX event to see how many new bytes have been transferred to the RX buffer in RAM since the previous ENDRX event.

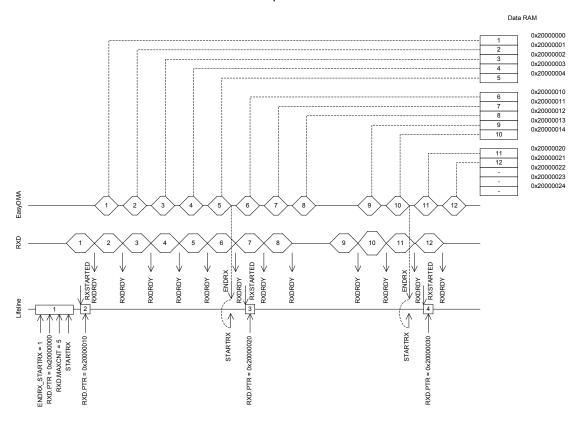


Figure 104: UARTE reception

The UARTE receiver is stopped by triggering the STOPRX task. An RXTO event is generated when the UARTE has stopped. The UARTE will make sure that an impending ENDRX event will be generated before the RXTO event is generated. This means that the UARTE will guarantee that no ENDRX event will be generated after RXTO, unless the UARTE is restarted or a FLUSHRX command is issued after the RXTO event is generated.

Important: If the ENDRX event has not already been generated when the UARTE receiver has come to a stop, which implies that all pending content in the RX FIFO has been moved to the RX buffer, the UARTE will generate the ENDRX event explicitly even though the RX buffer is not full. In this scenario the ENDRX event will be generated before the RXTO event is generated.

To be able to know how many bytes have actually been received into the RX buffer, the CPU can read the RXD.AMOUNT register following the ENDRX event or the RXTO event.

The UARTE is able to receive up to four bytes after the STOPRX task has been triggered as long as these are sent in succession immediately after the RTS signal is deactivated. This is possible because after the RTS is deactivated the UARTE is able to receive bytes for an extended period equal to the time it takes to send 4 bytes on the configured baud rate.

After the RXTO event is generated the internal RX FIFO may still contain data, and to move this data to RAM the FLUSHRX task must be triggered. To make sure that this data does not overwrite data in the RX buffer, the RX buffer should be emptied or the RXD.PTR should be updated before the FLUSHRX task is triggered.



To make sure that all data in the RX FIFO is moved to the RX buffer, the RXD.MAXCNT register must be set to RXD.MAXCNT > 4, see *Figure 105: UARTE reception with forced stop via STOPRX* on page 397. The UARTE will generate the ENDRX event after completing the FLUSHRX task even if the RX FIFO was empty or if the RX buffer does not get filled up. To be able to know how many bytes have actually been received into the RX buffer in this case, the CPU can read the RXD.AMOUNT register following the ENDRX event.

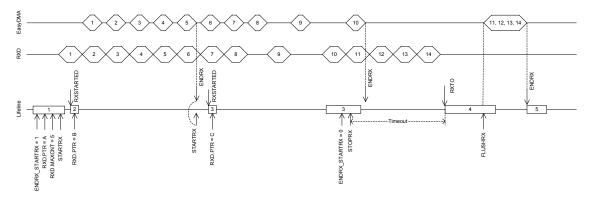


Figure 105: UARTE reception with forced stop via STOPRX

If HW flow control is enabled through the HWFC field in the CONFIG register, the RTS signal will be deactivated when the receiver is stopped via the STOPRX task or when the UARTE is only able to receive four more bytes in its internal RX FIFO.

With flow control disabled, the UARTE will function in the same way as when the flow control is enabled except that the RTS line will not be used. This means that no signal will be generated when the UARTE has reached the point where it is only able to receive four more bytes in its internal RX FIFO. Data received when the internal RX FIFO is filled up, will be lost.

The UARTE receiver will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTRX or after it has been stopped via STOPRX and the RXTO event has been generated. See *POWER* — *Power supply* on page 66 for more information about power modes.

34.5 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.

An ERROR event will not stop reception. If the error was a parity error, the received byte will still be transferred into Data RAM, and so will following incoming bytes. If there was a framing error (wrong stop bit), that specific byte will NOT be stored into Data RAM, but following incoming bytes will.

34.6 Using the UARTE without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

34.7 Parity and stop bit configuration

When parity is enabled through the PARITY field in the CONFIG register, the parity will be generated automatically from the even parity of TXD and RXD for transmission and reception respectively.

The amount of stop bits can be configured through the STOP field in the CONFIG register.



34.8 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOPTX and STOPRX tasks may not be always needed (the peripheral might already be stopped), but if STOPTX and/or STOPRX is sent, software shall wait until the TXSTOPPED and/or RXTO event is received in response, before disabling the peripheral through the ENABLE register.

34.9 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UARTE are mapped to physical pins according to the configuration specified in the PSEL.RXD, PSEL.RTS, and PSEL.TXD registers respectively.

The PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers and their configurations are only used as long as the UARTE is enabled, and retained only for the duration the device is in ON mode. PSEL.RXD, PSEL.RTS and PSEL.TXD must only be configured when the UARTE is disabled.

To secure correct signal levels on the pins by the UARTE when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Table 73: GPIO configuration before enabling peripheral* on page 398.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 73: GPIO configuration before enabling peripheral

UARTE signal	UARTE pin	Direction	Output value
RXD	As specified in PSEL.RXD	Input	Not applicable
CTS	As specified in PSEL.CTS	Input	Not applicable
RTS	As specified in PSEL.RTS	Output	1
TXD	As specified in PSEL.TXD	Output	1

34.10 Registers

Table 74: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40002000	UARTE	UARTE0	Universal asynchronous receiver/	
			transmitter with EasyDMA, unit 0	
0x40028000	UARTE	UARTE1	Universal asynchronous receiver/	
			transmitter with EasyDMA, unit 1	

Table 75: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS_STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_FLUSHRX	0x02C	Flush RX FIFO into RX buffer
EVENTS_CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_RXDRDY	0x108	Data received in RXD (but potentially not yet transferred to Data RAM)
EVENTS_ENDRX	0x110	Receive buffer is filled up
EVENTS_TXDRDY	0x11C	Data sent from TXD
EVENTS_ENDTX	0x120	Last TX byte transmitted
EVENTS_ERROR	0x124	Error detected
EVENTS RXTO	0x144	Receiver timeout



Register	Offset	Description	
EVENTS_RXSTARTED	0x14C	UART receiver has started	
EVENTS_TXSTARTED	0x150	UART transmitter has started	
EVENTS_TXSTOPPED	0x158	Transmitter stopped	
SHORTS	0x200	Shortcut register	
INTEN	0x300	Enable or disable interrupt	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
ERRORSRC	0x480	Error source	
		Note : this register is read / write one to clear.	
ENABLE	0x500	Enable UART	
PSEL.RTS	0x508	Pin select for RTS signal	
PSEL.TXD	0x50C	Pin select for TXD signal	
PSEL.CTS	0x510	Pin select for CTS signal	
PSEL.RXD	0x514	Pin select for RXD signal	
BAUDRATE	0x524	Baud rate. Accuracy depends on the HFCLK source selected.	
RXD.PTR	0x534	Data pointer	
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer	
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction	
TXD.PTR	0x544	Data pointer	
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer	
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction	
CONFIG	0x56C	Configuration of parity and hardware flow control	

34.10.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		D C
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
C RW ENDRX_STARTRX		Shortcut between ENDRX event and STARTRX task
		See EVENTS_ENDRX and TASKS_STARTRX
	Disabled	0 Disable shortcut
	Enabled	1 Enable shortcut
D RW ENDRX_STOPRX		Shortcut between ENDRX event and STOPRX task
		See EVENTS_ENDRX and TASKS_STOPRX
	Disabled	0 Disable shortcut
	Enabled	1 Enable shortcut

34.10.2 INTEN

Address offset: 0x300

Enable or disable interrupt

																																		i
Bit	numbe	er		33	1 30	29	2	8 27	7 26	5 25	5 24	4 23	22	2 21	20	19	18	17	16	15	14	13	12 :	11 1	0 9	8	7	6	5	4	3	2	1 0	ı
Id													L		J	1		Н							G	F	Ε			D		С	ВА	Ĺ
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	V	alue	:						De	esci	riptio	on																			l
Α	RW	CTS										En	abl	le or	dis	abl	e ir	ter	rup	t fo	r C	ΓS e	ven	t										
												Se	e E	VEN	TS_	СТ	5																	
			Disabled	0								Dis	sab	le																				
			Enabled	1								En	abl	le																				
В	RW	NCTS										En	abl	le or	dis	abl	e ir	ter	rup	t fo	r N	CTS	eve	ent										
												Se	e E	VEN	TS_	NC	TS																	



Bit r	numbe	er		31 30	29 28	27 26	5 25 24	23 22 21	20	19 3	18 1	.7 1	.6 15	14	13 3	L2 1	1 10	9	8	7	6 5	4	3	2 1	0
Id								L	J	1	F	Н						G	F	Е		D	(В	Α
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0	0	0	0 (0 (0 0	0	0	0 (0	0	0	0	0 0	0	0 (0	0
Id	RW	Field	Value Id	Value				Descript	ion																
			Disabled	0				Disable																	
			Enabled	1				Enable																	
С	RW	RXDRDY						Enable o	r dis	able	inte	erru	upt f	or R	XDR	DY e	vent	t							
								See EVEI	VTS_	RXD	RDY	Y													
			Disabled	0				Disable																	
			Enabled	1				Enable																	
D	RW	ENDRX						Enable o	r dis	able	inte	erru	upt f	or El	NDR	X ev	ent								
								See EVEI	VTS_	ENE	ORX														
			Disabled	0				Disable																	
			Enabled	1				Enable																	
Ε	RW	TXDRDY						Enable o	r dis	able	inte	erru	upt f	or T	XDR	DY e	vent	:							
								See EVEI	VTS	TXD	RDY	Y													
			Disabled	0				Disable																	
			Enabled	1				Enable																	
F	RW	ENDTX						Enable o	r dis	able	inte	erru	upt f	or El	NDT.	X ev	ent								
								See <i>EVEI</i>	VTS	END	OTX														
			Disabled	0				Disable																	
			Enabled	1				Enable																	
G	RW	ERROR						Enable o	r dis	able	inte	erru	upt f	or El	RRO	R ev	ent								
								See <i>EVEI</i>	VTS	ERR	OR														
			Disabled	0				Disable																	
			Enabled	1				Enable																	
Н	RW	RXTO						Enable o	r dis	able	inte	erru	upt f	or R	хто	eve	nt								
								See <i>EVEI</i>	VTS	RXT	0														
			Disabled	0				Disable	_	•	-														
			Enabled	1				Enable																	
ı	RW	RXSTARTED						Enable o	r dis	able	inte	erru	upt f	or R	XST/	ARTE	D ev	/ent							
								See <i>EVEI</i>	VTS	RXS	TAR	TF)												
			Disabled	0				Disable																	
			Enabled	1				Enable																	
J	RW	TXSTARTED						Enable o	r dis	able	inte	errı	upt f	or T	XST.	RTE	D ev	ent							
								See <i>EVEI</i>	VTS	TYC	TΔP	TFF)												
			Disabled	0				Disable	V13_	_175	IAN	ILL	,												
			Enabled	1				Enable																	
L	RW	TXSTOPPED		_				Enable o	r dis	able	inte	erru	upt f	or T	XSTC	PPE	D ev	/ent							
			Disabled	0				See EVEI	V15_	_IXS	ıUP	PEL	,												
			Disabled Enabled	1				Disable Enable																	
			LITADICU	1				LIIADIE																	

34.10.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	L J I I	H GFE D CBA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description	
A RW CTS	Write '1' to Enable in	nterrupt for CTS event
	See EVENTS_CTS	
Set	1 Enable	



Bit r	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 C
Id				L J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW NCTS			Write '1' to Enable interrupt for NCTS event
				See EVENTS_NCTS
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW RXDRDY			Write '1' to Enable interrupt for RXDRDY event
				See EVENTS_RXDRDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW ENDRX			Write '1' to Enable interrupt for ENDRX event
				See EVENTS_ENDRX
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E	RW TXDRDY			Write '1' to Enable interrupt for TXDRDY event
				See EVENTS_TXDRDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW ENDTX			Write '1' to Enable interrupt for ENDTX event
				See EVENTS_ENDTX
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW ERROR			Write '1' to Enable interrupt for ERROR event
				See EVENTS_ERROR
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW RXTO			Write '1' to Enable interrupt for RXTO event
				See EVENTS_RXTO
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
I	RW RXSTARTED			Write '1' to Enable interrupt for RXSTARTED event
				See EVENTS_RXSTARTED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
J	RW TXSTARTED			Write '1' to Enable interrupt for TXSTARTED event
				See EVENTS_TXSTARTED
		Set	1	 Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
L	RW TXSTOPPED			Write '1' to Enable interrupt for TXSTOPPED event
				See EVENTS_TXSTOPPED
		Set	1	Enable
		Disabled	0	Read: Disabled



Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			L JI H	G F E D C B
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
ld RW Field	Value Id	Value	Description	
	Enabled	1	Read: Enabled	

34.10.4 INTENCLR

Address offset: 0x308

Disable interrupt

Dis	abl	e interrupt			
Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					L J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
Α	RW	CTS			Write '1' to Disable interrupt for CTS event
					See EVENTS_CTS
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	NCTS			Write '1' to Disable interrupt for NCTS event
					See EVENTS_NCTS
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	RXDRDY			Write '1' to Disable interrupt for RXDRDY event
					See EVENTS_RXDRDY
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	ENDRX			Write '1' to Disable interrupt for ENDRX event
					See EVENTS_ENDRX
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW	TXDRDY			Write '1' to Disable interrupt for TXDRDY event
					See EVENTS_TXDRDY
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	ENDTX			Write '1' to Disable interrupt for ENDTX event
					See EVENTS_ENDTX
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	ERROR			Write '1' to Disable interrupt for ERROR event
					See EVENTS ERROR
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	RXTO			Write '1' to Disable interrupt for RXTO event
					·
			Clear	1	See EVENTS_RXTO Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
ı	RW	RXSTARTED			Write '1' to Disable interrupt for RXSTARTED event
					The state of the s



Bit number	31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		L JIH GFE D CBA
Reset 0x00000000	0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field Value I	d Value	Description
		See EVENTS_RXSTARTED
Clear	1	Disable
Disable	ed 0	Read: Disabled
Enable	d 1	Read: Enabled
J RW TXSTARTED		Write '1' to Disable interrupt for TXSTARTED event
		See EVENTS_TXSTARTED
Clear	1	Disable
Disable	ed 0	Read: Disabled
Enable	d 1	Read: Enabled
L RW TXSTOPPED		Write '1' to Disable interrupt for TXSTOPPED event
		See EVENTS_TXSTOPPED
Clear	1	Disable
Disable	ed 0	Read: Disabled
Enable	d 1	Read: Enabled

34.10.5 ERRORSRC

Address offset: 0x480

Error source

Note: this register is read / write one to clear.

Bit	numbe	er		31 30 29 28 27 26	5 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id						D C B A
Res	et 0x0	0000000		0 0 0 0 0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value		Description
Α	RW	OVERRUN				Overrun error
						A start bit is received while the previous data still lies in RXD.
						(Previous data is lost.)
			NotPresent	0		Read: error not present
			Present	1		Read: error present
В	RW	PARITY				Parity error
						A character with bad parity is received, if HW parity check is
						enabled.
			NotPresent	0		Read: error not present
			Present	1		Read: error present
С	RW	FRAMING				Framing error occurred
						A valid stop bit is not detected on the serial data input after all
						bits in a character have been received.
			NotPresent	0		Read: error not present
			Present	1		Read: error present
D	RW	BREAK				Break condition
						The serial data input is '0' for longer than the length of a data
						frame. (The data frame length is 10 bits without parity bit, and
						11 bits with parity bit.).
			NotPresent	0		Read: error not present
			Present	1		Read: error present
				-		nead end present

34.10.6 ENABLE

Address offset: 0x500

Enable UART



Bitı	numbe	er		31 30	29	28	27	26	25 2	24 2	23 2	22 2	21 2	0 19	9 18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																													4 Α	A	Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value	:						Des	crip	tior	1																	
Α	RW	ENABLE								E	Enal	ble	or d	lisat	le L	IAR	TE														
			Disabled	0						[Disa	ble	UA	RTE																	
			Enabled	8						E	Enal	ble	UAF	RTE																	

34.10.7 PSEL.RTS

Address offset: 0x508

Pin select for RTS signal

Bitı	numbe	er		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	вааа
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

34.10.8 PSEL.TXD

Address offset: 0x50C Pin select for TXD signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ВАААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

34.10.9 PSEL.CTS

Address offset: 0x510

Pin select for CTS signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	B A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

34.10.10 PSEL.RXD

Address offset: 0x514

Pin select for RXD signal



Bit r	numbe	er		31 3	30 29	28	3 27	26	25	24	23 :	22	21 2	20 1	9 1	8 17	7 16	15	14 1	.3 1	2 11	10	9	8	7 6	5	5 4	3	2	1 0
Id				С																						E	3 A	Α	Α	АА
Res	et OxF	FFFFFF		1	1 1	1	1	1	1	1	1	1	1	1	1 1	l 1	1	1	1	1 1	. 1	1	1	1	1 1	. 1	1	1	1	1 1
Id	RW	Field	Value Id	Valu	ıe						Des	cri	ptio	n																
Α	RW	PIN		[03	31]						Pin	nu	mbe	er																
В	RW	PORT		[0	L]						Por	t nı	umb	er																
С	RW	CONNECT									Con	nne	ctio	n																
			Disconnected	1							Disc	con	nec	t																
			Connected	0							Con	nne	ct																	

34.10.11 BAUDRATE

Address offset: 0x524

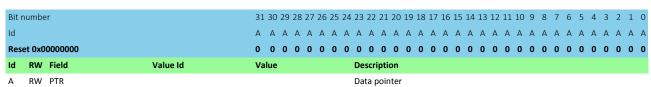
Baud rate. Accuracy depends on the HFCLK source selected.

Bit r	numbe	er		3	1 30	29	28	27	26 2	25 2	24 2	3 22	21	20	19	18	17	16	15 :	14 1	13 1	2 11	10	9	8	7	6	5	4 3	2	1	0
Id				Α	. A	Α	Α	Α	A	Α ,	Α Α	A A	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	Α	Α	Α	Α	Α	Α	A A	A	Α	Α
Res	et 0x0	400000		0	0	0	0	0	1	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	٧	alue	:					D	escr	iptic	on																		
Α	RW	BAUDRATE									В	aud	rate																			
			Baud1200	0	x000)4F(000				1	200	bau	d (a	ctua	al ra	ate:	12	05)													
			Baud2400	0	x000)9D(000				2	400	bau	d (a	ctua	al ra	ate:	23	96)													
			Baud4800	0	x001	13B(000				4	800	bau	d (a	ctua	al ra	ate:	48	08)													
			Baud9600	0	x002	2750	000				9	600	bau	d (a	ctua	al ra	ate:	95	98)													
			Baud14400	0	x003	3AF(000				1	440) baı	ud (actı	ual	rate	e: 1	440)1)												
			Baud19200	0	x004	1EA	000				1	9200) baı	ud (actı	ual	rate	e: 1	920	(8)												
			Baud28800	0	x007	75C	000				2	880) baı	ud (actı	ual	rate	e: 2	877	77)												
			Baud31250	0	300x	3000	000				3	1250) baı	Jud																		
			Baud38400	0	x009	9D0(000				3	8400) baı	Jd (actı	ual	rate	e: 3	836	9)												
			Baud56000	0	x00E	500	000				5	600) baı	Jd (actı	ual	rate	e: 5	594	14)												
			Baud57600	0	x00E	B00	000				5	760) baı	Jd (actı	ual	rate	e: 5	755	54)												
			Baud76800	0	x013	3A90	000				7	680) baı	Jd (actı	ual	rate	e: 7	692	23)												
			Baud115200	0	x01[060	000				1	1520	00 ba	aud	(ac	tua	l ra	te:	115	108	3)											
			Baud230400	0	x03E	3000	000				2	3040	00 ba	aud	(ac	tua	l ra	te:	231	.884	1)											
			Baud250000	0	x040	0000	000				2	5000	00 ba	aud																		
			Baud460800	0	x074	1000	000				4	608	00 ba	aud	(ac	tua	l ra	te:	457	143	3)											
			Baud921600	0	x0F0	0000	000				9	2160	00 ba	aud	(ac	tua	l ra	te:	941	176	5)											
			Baud1M	0	x100	0000	000				1	Meg	ga ba	ud																		

34.10.12 RXD.PTR

Address offset: 0x534

Data pointer



34.10.13 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer



Bit r	iumbe	er		31	30 :	9	28 2	27 2	6 2	5 2	24 2	23 2	2 2	1 2	0 1	9 1	8 1	7 10	5 15	5 14	1 13	3 12	11	10	9	8	7	6	5	4	3	2 :	L 0
Id																									Α	Α	Α	Α	Α	Α	Α.	A A	A A
Rese	et OxO	0000000		0	0	0	0	0 () (0	0	0 (0 () () () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Desc	crip	tior	1																		
Α	RW	MAXCNT									١	Иах	imu	ım ı	nun	ıbe	r of	by	es i	n r	ece	ive	buf	fer									

34.10.14 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit r	numbe	er		31	30 2	9 2	28 2	7 20	6 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13 :	L2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id																								Α	Α	Α	Α	Α	Α	Α .	Δ ,	4 А
Res	et 0x0	0000000		0	0)	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																		
Α	R	AMOUNT									N	umb	er (of b	yte	s tr	ans	feri	ed	in tl	ne la	ast 1	rans	act	ion							

34.10.15 TXD.PTR

Address offset: 0x544

Data pointer

Bit	numbe	r		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 17	17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				ААААА	. A A A A A A A A	A A A A A A A A A A A A A A A A
Res	et 0x0	0000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description	
Α	RW	PTR			Data pointer	

34.10.16 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit r	numbei			33	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (ı
Id																										Α	Α	Α	Α	Α	Α	A	Δ	A A	
Res	et 0x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (
Id	RW	Field	Value Id	V	alu	•						De	cri	otic	on																				l
Α	RW	MAXCNT										Ma	xim	um	า ทน	ımb	er	of b	yte	s in	tra	ansı	mit	buf	fer										

34.10.17 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit r	numbe	er		31 30	29	28 2	7 26	25	24	23	22 :	21 2	20 1	9 1	8 1	7 16	15	14	13	12	11 1	.0 9	8	7	6	5	4	3	2	1 0
Id																						Δ	. Α	. A	Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0 0	0	0 (0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value						Des	crip	otio	n																	
Α	R	AMOUNT								Nur	nbe	er of	f by	tes t	tran	sfe	red	in	the	last	trar	ısac	tion							

34.10.18 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

ı	Bit num	be	r		31	30	29	28 2	7 2	6 25	5 24	4 23	3 22	2 21	L 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
ı	ld																														С	В	В	В	Δ
ı	Reset 0	x0(000000		0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (o
	ld R\	w	Field	Value Id	Value		D	escr	ript	ion																									
	۸ ۵۱	۸,	LIMEC					- 11	d		o fl			tro l																					

A RW HWFC Hardware flow control



Bit numb	er		31	30 2	9 2	8 27	26	25	24 2	23 2	2 21	1 20	19	18	17 1	16 1	5 1	4 13	12	11 :	.0 9	8	7	6	5	4	3 2	1	0
Id																										С	в в	В	Α
Reset 0x	00000000		0	0	0 (0 0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0 0	0	0
ld RW	/ Field	Value Id	Val	lue					ı	Desc	ript	ion																	
		Disabled	0						ı	Disal	bled	l																	
		Enabled	1						1	Enab	oled																		
B RW	PARITY								ı	Parit	У																		
		Excluded	0x0)					1	Exclu	ıde	pari	ty b	it															
		Included	0x7	7					ı	nclu	ide e	ever	n pa	rity	bit														
C RW	STOP								9	Stop	bits	6																	
		One	0						(One	stop	bit c																	
		Two	1						1	Two	stop	p bit	:S																

34.11 Electrical specification

34.11.1 UARTE electrical specification

Symbol	Description	Min.	Тур.	Max.	Units
f _{UARTE}	Baud rate for UARTE ²⁹ .			1000	kbps
I _{UARTE1M}	Run current at max baud rate.		55		μΑ
I _{UARTE115k}	Run current at 115200 bps.		55		μΑ
I _{UARTE1k2}	Run current at 1200 bps.		55		μΑ
I _{UARTE,IDLE}	Idle current for UARTE (STARTed, no XXX activity)		1		μΑ
t _{UARTE,CTSH}	CTS high time	1			μs
t _{UARTE,START}	Time from STARTRX/STARTTX task to transmission started		1		μs

²⁹ High baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.



35 QDEC — Quadrature decoder

The Quadrature decoder (QDEC) provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors.

The sample period and accumulation are configurable to match application requirements. The QDEC provides the following:

- Decoding of digital waveform from off-chip quadrature encoder.
- · Sample accumulation eliminating hard real-time requirements to be enforced on application.
- Optional input de-bounce filters.
- Optional LED output signal for optical encoders.

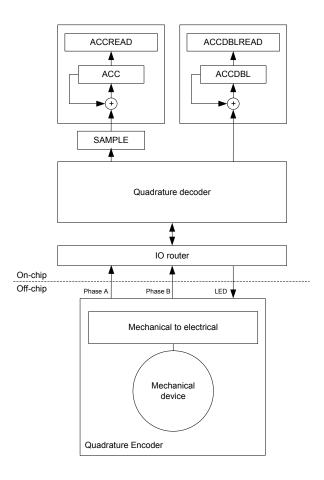


Figure 106: Quadrature decoder configuration

35.1 Sampling and decoding

The QDEC decodes the output from an incremental motion encoder by sampling the QDEC phase input pins (A and B).

The off-chip quadrature encoder is an incremental motion encoder outputting two waveforms, phase A and phase B. The two output waveforms are always 90 degrees out of phase, meaning that one always changes level before the other. The direction of movement is indicated by which of these two waveforms that changes level first. Invalid transitions may occur, that is when the two waveforms switch simultaneously. This may occur if the wheel rotates too fast relative to the sample rate set for the decoder.



The QDEC decodes the output from the off-chip encoder by sampling the QDEC phase input pins (A and B) at a fixed rate as specified in the SAMPLEPER register.

If the SAMPLEPER value needs to be changed, the QDEC shall be stopped using the STOP task. SAMPLEPER can be then changed upon receiving the STOPPED event, and QDEC can be restarted using the START task. Failing to do so may result in unpredictable behaviour.

It is good practice to change other registers (LEDPOL, REPORTPER, DBFEN and LEDPRE) only when the QDEC is stopped.

When started, the decoder continuously samples the two input waveforms and decodes these by comparing the current sample pair (n) with the previous sample pair (n-1).

The decoding of the sample pairs is described in the table below.

Table 76: Sampled value encoding

Previous sample - 1)	us e pair(n	Curre	nt les pair(n)	SAMPLE register	ACC operation	ACCDBL operation	Description
Α	В	Α	В				
0	0	0	0	0	No change	No change	No movement
0	0	0	1	1	Increment	No change	Movement in positive direction
0	0	1	0	-1	Decrement	No change	Movement in negative direction
0	0	1	1	2	No change	Increment	Error: Double transition
0	1	0	0	-1	Decrement	No change	Movement in negative direction
0	1	0	1	0	No change	No change	No movement
0	1	1	0	2	No change	Increment	Error: Double transition
0	1	1	1	1	Increment	No change	Movement in positive direction
1	0	0	0	1	Increment	No change	Movement in positive direction
1	0	0	1	2	No change	Increment	Error: Double transition
1	0	1	0	0	No change	No change	No movement
1	0	1	1	-1	Decrement	No change	Movement in negative direction
1	1	0	0	2	No change	Increment	Error: Double transition
1	1	0	1	-1	Decrement	No change	Movement in negative direction
1	1	1	0	1	Increment	No change	Movement in positive direction
1	1	1	1	0	No change	No change	No movement

35.2 LED output

The LED output follows the sample period, and the LED is switched on a given period before sampling and switched off immediately after the inputs are sampled. The period the LED is switched on before sampling is given in the LEDPRE register.

The LED output pin polarity is specified in the LEDPOL register.

For using off-chip mechanical encoders not requiring a LED, the LED output can be disabled by writing value 'Disconnected' to the CONNECT field of the PSEL.LED register. In this case the QDEC will not acquire access to a LED output pin and the pin can be used for other purposes by the CPU.

35.3 Debounce filters

Each of the two-phase inputs have digital debounce filters.

When enabled through the DBFEN register, the filter inputs are sampled at a fixed 1 MHz frequency during the entire sample period (which is specified in the SAMPLEPER register), and the filters require all of the samples within this sample period to equal before the input signal is accepted and transferred to the output of the filter.

As a result, only input signal with a steady state longer than twice the period specified in SAMPLEPER are guaranteed to pass through the filter, and any signal with a steady state shorter than SAMPLEPER will always be suppressed by the filter. (This is assumed that the frequency during the debounce period never exceeds 500 kHz (as required by the Nyquist theorem when using a 1 MHz sample frequency).

The LED will always be ON when the debounce filters are enabled, as the inputs in this case will be sampled continuously.



Note that when when the debounce filters are enabled, displacements reported by the QDEC peripheral are delayed by one SAMPLEPER period.

35.4 Accumulators

The quadrature decoder contains two accumulator registers, ACC and ACCDBL, that accumulate respectively valid motion sample values and the number of detected invalid samples (double transitions).

The ACC register will accumulate all valid values (1/-1) written to the SAMPLE register. This can be useful for preventing hard real-time requirements from being enforced on the application. When using the ACC register the application does not need to read every single sample from the SAMPLE register, but can instead fetch the ACC register whenever it fits the application. The ACC register will always hold the relative movement of the external mechanical device since the previous clearing of the ACC register. Sample values indicating a double transition (2) will not be accumulated in the ACC register.

An ACCOF event will be generated if the ACC receives a SAMPLE value that would cause the register to overflow or underflow. Any SAMPLE value that would cause an ACC overflow or underflow will be discarded, but any samples not causing the ACC to overflow or underflow will still be accepted.

The accumulator ACCDBL accumulates the number of detected double transitions since the previous clearing of the ACCDBL register.

The ACC and ACCDBL registers can be cleared by the READCLRACC and subsequently read using the ACCREAD and ACCDBLREAD registers.

The ACC register can be separately cleared by the RDCLRACC and subsequently read using the ACCREAD registers.

The ACCDBL register can be separately cleared by the RDCLRDBL and subsequently read using the ACCDBLREAD registers.

The REPORTPER register allows automating the capture of several samples before it can send out a REPORTRDY event in case a non-null displacement has been captured and accumulated, and a DBLRDY event in case one or more double-displacements have been captured and accumulated. The REPORTPER field in this register selects after how many samples the accumulators contents are evaluated to send (or not) REPORTRDY and DBLRDY events.

Using the RDCLRACC task (manually sent upon receiving the event, or using the DBLRDY_RDCLRACC shortcut), ACCREAD can then be read.

In case at least one double transition has been captured and accumulated, a DBLRDY event is sent. Using the RDCLRDBL task (manually sent upon receiving the event, or using the DBLRDY_RDCLRDBL shortcut), ACCDBLREAD can then be read.

35.5 Output/input pins

The QDEC uses a three-pin interface to the off-chip quadrature encoder.

These pins will be acquired when the QDEC is enabled in the ENABLE register. The pins acquired by the QDEC cannot be written by the CPU, but they can still be read by the CPU.

The pin numbers to be used for the QDEC are selected using the PSEL.n registers.

35.6 Pin configuration

The Phase A, Phase B, and LED signals are mapped to physical pins according to the configuration specified in the PSEL.A, PSEL.B, and PSEL.LED registers respectively.

If the CONNECT field value 'Disconnected' is specified in any of these registers, the associated signal will not be connected to any physical pin. The PSEL.A, PSEL.B, and PSEL.LED registers and their configurations are only used as long as the QDEC is enabled, and retained only as long as the device is in



ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register.

To secure correct behavior in the QDEC, the pins used by the QDEC must be configured in the GPIO peripheral as described in *Table 77: GPIO configuration before enabling peripheral* on page 411 before enabling the QDEC. This configuration must be retained in the GPIO for the selected IOs as long as the QDEC is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 77: GPIO configuration before enabling peripheral

QDEC signal	QDEC pin	Direction	Output value	Comment	
Phase A	As specified in PSEL.A	Input	Not applicable		
Phase B	As specified in PSEL.B	Input	Not applicable		
LED	As specified in PSEL.LED	Input	Not applicable		

35.7 Registers

Table 78: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40012000	QDEC	QDEC	Quadrature decoder	

Table 79: Register Overview

Register	Offset	Description
TASKS_START	0x000	Task starting the quadrature decoder
TASKS_STOP	0x004	Task stopping the quadrature decoder
TASKS_READCLRACC	0x008	Read and clear ACC and ACCDBL
TASKS_RDCLRACC	0x00C	Read and clear ACC
TASKS_RDCLRDBL	0x010	Read and clear ACCDBL
EVENTS_SAMPLERDY	0x100	Event being generated for every new sample value written to the SAMPLE register
EVENTS_REPORTRDY	0x104	Non-null report ready
EVENTS_ACCOF	0x108	ACC or ACCDBL register overflow
EVENTS_DBLRDY	0x10C	Double displacement(s) detected
EVENTS_STOPPED	0x110	QDEC has been stopped
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable the quadrature decoder
LEDPOL	0x504	LED output pin polarity
SAMPLEPER	0x508	Sample period
SAMPLE	0x50C	Motion sample value
REPORTPER	0x510	Number of samples to be taken before REPORTRDY and DBLRDY events can be generated
ACC	0x514	Register accumulating the valid transitions
ACCREAD	0x518	Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task
PSEL.LED	0x51C	Pin select for LED signal
PSEL.A	0x520	Pin select for A signal
PSEL.B	0x524	Pin select for B signal
DBFEN	0x528	Enable input debounce filters
LEDPRE	0x540	Time period the LED is switched ON prior to sampling
ACCDBL	0x544	Register accumulating the number of detected double transitions
ACCDBLREAD	0x548	Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

35.7.1 SHORTS

Address offset: 0x200 Shortcut register



Bit	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				G F E D C B A
Res	set 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW REPORTRDY_READCLRA	ACC		Shortcut between REPORTRDY event and READCLRACC task
				See EVENTS_REPORTRDY and TASKS_READCLRACC
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
В	RW SAMPLERDY_STOP			Shortcut between SAMPLERDY event and STOP task
				See EVENTS_SAMPLERDY and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
С	RW REPORTRDY_RDCLRACO			Shortcut between REPORTRDY event and RDCLRACC task
				See EVENTS_REPORTRDY and TASKS_RDCLRACC
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
D	RW REPORTRDY_STOP			Shortcut between REPORTRDY event and STOP task
				See EVENTS_REPORTRDY and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
E	RW DBLRDY_RDCLRDBL			Shortcut between DBLRDY event and RDCLRDBL task
				See EVENTS_DBLRDY and TASKS_RDCLRDBL
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
F	RW DBLRDY_STOP			Shortcut between DBLRDY event and STOP task
				See EVENTS_DBLRDY and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
G	RW SAMPLERDY_READCLRA	ACC		Shortcut between SAMPLERDY event and READCLRACC task
				See EVENTS_SAMPLERDY and TASKS_READCLRACC
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut

35.7.2 INTENSET

Address offset: 0x304 Enable interrupt

Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW SAMPLERDY			Write '1' to Enable interrupt for SAMPLERDY event
				See EVENTS_SAMPLERDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW REPORTRDY			Write '1' to Enable interrupt for REPORTRDY event
				See EVENTS_REPORTRDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW ACCOF			Write '1' to Enable interrupt for ACCOF event
				See EVENTS_ACCOF
		Set	1	Enable



Bit numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E D C B A
Reset 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW	Field	Value Id	Value	Description
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D RW	DBLRDY			Write '1' to Enable interrupt for DBLRDY event
				See EVENTS_DBLRDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E RW	STOPPED			Write '1' to Enable interrupt for STOPPED event
				See EVENTS_STOPPED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

35.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

	C B A
Id RW Field Value Id Value Description A RW SAMPLERDY Write '1' to Disable interrupt for SAMPLERDY event See EVENTS_SAMPLERDY Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled B RW REPORTRDY Write '1' to Disable interrupt for REPORTRDY event See EVENTS_REPORTRDY See EVENTS_REPORTRDY Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled	0 0 0
A RW SAMPLERDY Write '1' to Disable interrupt for SAMPLERDY See EVENTS_SAMPLERDY Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled B RW REPORTRDY Vite '1' to Disable interrupt for REPORTRDY event See EVENTS_REPORTRDY Clear 1 Disable Disabled 0 Read: Disabled Read: Enabled Read: Enabled Read: Enabled	
See EVENTS_SAMPLERDY Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled B RW REPORTRDY Clear 1 Disable interrupt for REPORTRDY event See EVENTS_REPORTRDY Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled	
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled B RW REPORTRDY Clear 1 Disable interrupt for REPORTRDY event See EVENTS_REPORTRDY Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled	
Disabled 0 Read: Disabled Enabled 1 Read: Enabled B RW REPORTRDY Clear 1 Disable Disabled 0 Read: Enabled Read: Enabled Read: Enabled Write '1' to Disable interrupt for REPORTRDY event See EVENTS_REPORTRDY Disable Read: Disabled Read: Disabled Read: Enabled	
Enabled 1 Read: Enabled B RW REPORTRDY Write '1' to Disable interrupt for REPORTRDY event See EVENTS_REPORTRDY Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled	
B RW REPORTRDY Write '1' to Disable interrupt for REPORTRDY event See EVENTS_REPORTRDY Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled	
See EVENTS_REPORTRDY Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled	
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled	
Disabled 0 Read: Disabled Enabled 1 Read: Enabled	
Enabled 1 Read: Enabled	
C RW ACCOF Write '1' to Disable interrupt for ACCOF event	
See EVENTS_ACCOF	
Clear 1 Disable	
Disabled 0 Read: Disabled	
Enabled 1 Read: Enabled	
D RW DBLRDY Write '1' to Disable interrupt for DBLRDY event	
See EVENTS_DBLRDY	
Clear 1 Disable	
Disabled 0 Read: Disabled	
Enabled 1 Read: Enabled	
E RW STOPPED Write '1' to Disable interrupt for STOPPED event	
See EVENTS_STOPPED	
Clear 1 Disable	
Disabled 0 Read: Disabled	
Enabled 1 Read: Enabled	

35.7.4 ENABLE

Address offset: 0x500

Enable the quadrature decoder



В	t nur		31	L 30	29	28	8 27	7 2	26 25	5 2	24 2	3 22	2 21	20	19	18	3 17	7 16	5 15	5 14	1 13	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1	0		
Id																																				Α
R	eset	0x0	0000000		0	0	0	0	0	(0 0) (0 0	0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0
Ic	l F	RW	Field	Value Id	Va	alue							D	esci	ripti	ion																				
Α	F	RW	ENABLE										Е	nabl	le o	r dis	sab	le t	he	qua	dra	atur	e d	lec	ode	r										
														/her	n en	nabl	ed	the	de	coc	ler	pin	s w	ill b	e a	ctiv	e. V	Vhe	n d	isal	oled	t				
													tł	ne q	uad	Iratı	ure	de	coc	ler	pins	ar	e n	ot a	acti	ve a	ınd	can	be	use	ed a	is				
														PIO																						
				Disabled	0								D	isab	le																					
				Enabled	1										le																					

35.7.5 LEDPOL

Address offset: 0x504 LED output pin polarity

Bit	num	nber			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			Α
Res	et 0)x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	R۱	W	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	R۱	W	LEDPOL										LEC) ou	ıtpı	ıt p	in p	ola	rity	,															
				ActiveLow	0								Lec	ac	tive	on	ou	tpu	t pi	n lo	ow														
				ActiveHigh	1								Lec	ac	tive	on	ou	tpu	t pi	n h	igh														

35.7.6 SAMPLEPER

Address offset: 0x508

Sample period

	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
		ААА
	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Value Id	Value	Description
		Sample period. The SAMPLE register will be updated for every
		new sample
128us	0	128 us
256us	1	256 us
512us	2	512 us
1024us	3	1024 us
2048us	4	2048 us
4096us	5	4096 us
8192us	6	8192 us
16384us	7	16384 us
32ms	8	32768 us
65ms	9	65536 us
131ms	10	131072 us
	128us 256us 512us 1024us 2048us 4096us 8192us 16384us 32ms 65ms	128us 0 256us 1 512us 2 1024us 3 2048us 4 4096us 5 8192us 6 16384us 7 32ms 8 65ms 9

35.7.7 SAMPLE

Address offset: 0x50C Motion sample value

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 :	13 1	.2 1	11 1	0 9	8 (7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ.	A A	\ A	. 4	A	Α	Α	Α	Α	Α	АА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	R	SAMPLE		[-1	2]							Las	t m	oti	on s	am	ple																



Id RW Field Value Id Value		Description			
Reset 0x00000000 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0
Id A A	A A A A A A	A A A A A A	A A A A A	A A A A A	A A A A A A
Bit number 31 30	30 29 28 27 26 25 24	23 22 21 20 19 18 1	7 16 15 14 13 12	11 10 9 8 7	6 5 4 3 2 1 0

The value is a 2's complement value, and the sign gives the direction of the motion. The value '2' indicates a double transition.

35.7.8 REPORTPER

Address offset: 0x510

Number of samples to be taken before REPORTRDY and DBLRDY events can be generated

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW REPORTPER			Specifies the number of samples to be accumulated in the ACC
			register before the REPORTRDY and DBLRDY events can be
			generated
			The report period in [us] is given as: RPUS = SP * RP Where
			RPUS is the report period in [us/report], SP is the sample period
			in [us/sample] specified in SAMPLEPER, and RP is the report
			period in [samples/report] specified in REPORTPER.
	10Smpl	0	10 samples / report
	40Smpl	1	40 samples / report
	80Smpl	2	80 samples / report
	120Smpl	3	120 samples / report
	160Smpl	4	160 samples / report
	200Smpl	5	200 samples / report
	240Smpl	6	240 samples / report
	280Smpl	7	280 samples / report
	1Smpl	8	1 sample / report

35.7.9 ACC

Address offset: 0x514

Register accumulating the valid transitions

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A R ACC		[-10241023] Register accumulating all valid samples (not double transition)
		read from the SAMPLE register
		Double transitions (SAMPLE = 2) will not be accumulated in
		bodole transitions (SAIVII EE - 2) will not be decumulated in
		this register. The value is a 32 bit 2's complement value. If a
		sample that would cause this register to overflow or underflow
		is received, the sample will be ignored and an overflow event
		(ACCOF) will be generated. The ACC register is cleared by

35.7.10 ACCREAD

Address offset: 0x518

Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task



Bit r	numbe	er		31	30	29	28	27 :	26	25	24	23	22	21 :	20	19 1	18 3	17 1	16 :	15 :	14 :	13 1	12 :	11 1	0 9	8	3 7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	A A	\ A	. 4	Δ Δ	. Δ	. A	Α	Α	Α	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (C	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptio	n																		
Α	R	ACCREAD		[-1	024	10	23]					Sna	psh	ot (of t	he A	٩CC	re	gist	er.													

The ACCREAD register is updated when the READCLRACC or RDCLRACC task is triggered

35.7.11 PSEL.LED

Address offset: 0x51C Pin select for LED signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	вааа
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

35.7.12 PSEL.A

Address offset: 0x520 Pin select for A signal

Bit n	iumbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	B A A A A
Rese	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

35.7.13 PSEL.B

Address offset: 0x524 Pin select for B signal

Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	вааа
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

35.7.14 DBFEN

Address offset: 0x528

Enable input debounce filters



Bit	numl	ber			31 3	0 29	28	3 27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																																Α
Res	et 0	x00	000000		0 0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RV	N	Field	Value Id	Valu	е						Des	crip	otio	n																	
Α	RV	N	DBFEN									Ena	ble	inp	ut d	ebo	ounc	e fi	lter	S												
				Disabled	0							Deb	ooui	nce	inp	ut fi	lter	s di	sabl	ed												
				Enabled	1							Deb	ooui	nce	inp	ut fi	lter	s en	abl	ed												

35.7.15 LEDPRE

Address offset: 0x540

Time period the LED is switched ON prior to sampling

Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A
Reset 0x00000010		0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
A RW LEDPRE		[1511]	Period in us the LED is switched on prior to sampling

35.7.16 ACCDBL

Address offset: 0x544

Register accumulating the number of detected double transitions

Bit r	numb	er		31	30 2	29	28 :	27 :	26 2	25 24	4 23	3 22	21	20	19 :	18	17 :	16 1	15 1	4 1	3 12	11	10	9	8	7	6	5 4		3 2 4 A	Ī	0 A
Res	Reset 0x00000000				0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						D	escri	ptic	n																		
Α	R	ACCDBL		[0.	15]						tra W ac ov illa re	ansi hen cum erfl egal	this nulat ow e	s. (reg tion eve nsiti	SAN giste of nt (ions fiel	APL er h dou AC are	E = nas i uble COF e de	2). read /il :) w	ched llega vill l	d its al tra be ge afte y tri	max ansit ener er th	kimu tion rate e m	um v s wi d if	/alu II st any mur	e tl op. do n va	ne An uble	e or	IS				

35.7.17 ACCDBLREAD

Address offset: 0x548

Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

Bit	numb	er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					АААА
Res	et 0x	0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
					Description
Α	R	ACCDBLREAD		[015]	Snapshot of the ACCDBL register. This field is updated when the

35.8 Electrical specification

35.8.1 QDEC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{QDEC}	Run current		5		μΑ
t _{SAMPLE}	Time between sampling signals from quadrature decoder	128		131072	μs
t _{LED}	Time from LED is turned on to signals are sampled	0		511	μs



36 SAADC — Successive approximation analog-todigital converter

The ADC is a differential successive approximation register (SAR) analog-to-digital converter.

Listed here are the main features of SAADC:

- 8/10/12-bit resolution, 14-bit resolution with oversampling
- Up to eight input channels
 - One channel per single-ended input and two channels per differential input
 - Scan mode can be configured with both single-ended channels and differential channels.
- Full scale input range (0 to VDD)
- Sampling triggered via a task from software or a PPI channel for full flexibility on sample frequency source from low power 32.768kHz RTC or more accurate 1/16MHz Timers
- One-shot conversion mode to sample a single channel
- Scan mode to sample a series of channels in sequence. Sample delay between channels is t_{ack} + t_{conv} which may vary between channels according to user configuration of t_{ack}.
- Support for direct sample transfer to RAM using EasyDMA
- · Interrupts on single sample and full buffer events
- Samples stored as 16-bit 2's complement values for differential and single-ended sampling
- · Continuous sampling without the need of an external timer
- Internal resistor string
- · Limit checking on the fly

36.1 Shared resources

The ADC can coexist with COMP, LPCOMP and other peripherals using one of AIN0-AIN7, provided these are assigned to different pins.

It is not recommended to select the same analog input pin for both modules.

36.2 Overview

The ADC supports up to eight external analog input channels, depending on package variant. It can be operated in a one-shot mode with sampling under software control, or a continuous conversion mode with a programmable sampling rate.

The analog inputs can be configured as eight single-ended inputs, four differential inputs or a combination of these. Each channel can be configured to select the AINO to AINO pins, the VDD pin, or the VDDH pin. Channels can be sampled individually in one-shot or continuous sampling modes, or, using scan mode, multiple channels can be sampled in sequence. Channels can also be oversampled to improve noise performance.



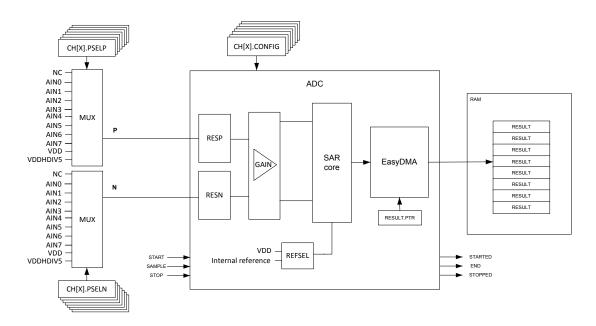


Figure 107: Simplified ADC block diagram

Internally, the ADC is always a differential analog-to-digital converter, but by default it is configured with single-ended input in the MODE field of the CH[n].CONFIG register. In single-ended mode, the negative input will be shorted to ground internally.

The assumption in single-ended mode is that the internal ground of the ADC is the same as the external ground that the measured voltage is referred to. The ADC is thus sensitive to ground bounce on the PCB in single-ended mode. If this is a concern we recommend using differential measurement.

36.3 Digital output

The output result of the ADC depends on the settings in the CH[n].CONFIG and RESOLUTION registers as follows:

```
RESULT = [V(P) - V(N)] * GAIN/REFERENCE * 2 (RESOLUTION - m)
```

where

V(P)

is the voltage at input P

V(N)

is the voltage at input N

GAIN

is the selected gain setting

REFERENCE

is the selected reference voltage

and m=0 if CONFIG.MODE=SE, or m=1 if CONFIG.MODE=Diff.

The result generated by the ADC will deviate from the expected due DC errors like offset, gain, differential non-linearity (DNL), and integral non-linearity (INL). See *Electrical specification* for details on these parameters. The result can also vary due to AC errors like non-linearities in the GAIN block, settling errors due to high source impedance and sampling jitter. For battery measurement the DC errors are most noticeable.



The ADC has a wide selection of gains controlled in the GAIN field of the CH[n].CONFIG register. If CH[n].CONFIG.REFSEL=0, the input range of the ADC core is nominally ±0.6 V differential and the input must be scaled accordingly.

The ADC has a temperature dependent offset. If the ADC is to operate over a large temperature range, we recommend running CALIBRATEOFFSET at regular intervals, a CALIBRATEDONE event will be fired when the calibration is complete. Since calibration involves acquiring a sample, a DONE and a RESULTDONE event will be fired as well.

36.4 Analog inputs and channels

Up to eight analog input channels, CH[n](n=0..7), can be configured.

See *Shared resources* on page 418 for shared input with comparators.

Any one of the available channels can be enabled for the ADC to operate in one-shot mode. If more than one CH[n] is configured, the ADC enters scan mode.

An analog input is selected as a positive converter input if CH[n].PSELP is set, setting CH[n].PSELP also enables the particular channel.

An analog input is selected as a negative converter input if CH[n].PSELN is set. The CH[n].PSELN register will have no effect unless differential mode is enabled, see MODE field in CH[n].CONFIG register.

If more than one of the CH[n].PSELP registers is set, the device enters scan mode. Input selections in scan mode are controlled by the CH[n].PSELP and CH[n].PSELN registers, where CH[n].PSELN is only used if the particular scan channel is specified as differential, see MODE field in CH[n].CONFIG register.

Important: Channels selected for either COMP or LPCOMP cannot be used at the same time for ADC sampling, though channels not selected for use by these blocks can be used by the ADC.

36.5 Operation modes

The ADC input configuration supports one-shot mode, continuous mode and scan mode.

Scan mode and oversampling cannot be combined.

36.5.1 One-shot mode

One-shot operation is configured by enabling only one of the available channels defined by CH[n].PSELP, CH[n].PSELN, and CH[n].CONFIG registers.

Upon a SAMPLE task, the ADC starts to sample the input voltage. The CH[n].CONFIG.TACQ controls the acquisition time.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA. For more information, see *EasyDMA* on page 422.

36.5.2 Continuous mode

Continuous sampling can be achieved by using the internal timer in the ADC, or triggering the SAMPLE task from one of the general purpose timers through the PPI.

Care shall be taken to ensure that the sample rate fulfils the following criteria, depending on how many channels are active:

$$f_{SAMPLE} < 1/[t_{ACQ} + t_{conv}]$$

The SAMPLERATE register can be used as a local timer instead of triggering individual SAMPLE tasks. When SAMPLERATE.MODE is set to Timers, it is sufficient to trigger SAMPLE task only once in order to start the SAADC and triggering the STOP task will stop sampling. The SAMPLERATE.CC field controls the sample rate.



The SAMPLERATE timer mode cannot be combined with SCAN mode, and only one channel can be enabled in this mode.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

36.5.3 Oversampling

An accumulator in the ADC can be used to average noise on the analog input. In general, oversampling improves the signal-to-noise ratio (SNR). Oversampling, however, does not improve the integral non-linearity (INL), or differential non-linearity (DNL).

Oversampling and scan should not be combined, since oversampling and scan will average over input channels.

The accumulator is controlled in the OVERSAMPLE register. The SAMPLE task must be set 2^{OVERSAMPLE} number of times before the result is written to RAM. This can be achieved by:

- Configuring a fixed sampling rate using the local timer or a general purpose timer and PPI to trigger a SAMPLE task
- Triggering SAMPLE 2^{OVERSAMPLE} times from software
- · Enabling BURST mode

CH[n].CONFIG.BURST can be enabled to avoid setting SAMPLE task $2^{\text{OVERSAMPLE}}$ times. With BURST = 1 the ADC will sample the input $2^{\text{OVERSAMPLE}}$ times as fast as it can (actual timing: $<(t_{\text{ACQ}}+t_{\text{CONV}})\times 2^{\text{OVERSAMPLE}})$. Thus, for the user it will just appear like the conversion took a bit longer time, but other than that, it is similar to one-shot mode. Scan mode can be combined with BURST=1, if burst is enabled on all channels.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals that enough conversions have taken place for an oversampled result to get transferred into RAM. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

36.5.4 Scan mode

A channel is considered enabled if CH[n].PSELP is set. If more than one channel, CH[n], is enabled, the ADC enters scan mode.

In scan mode, one SAMPLE task will trigger one conversion per enabled channel. The time it takes to sample all channels is:

```
Total time < Sum (CH[x].t<sub>ACQ</sub>+t<sub>CONV</sub>), x=0..enabled channels
```

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual values have been transferred into RAM by EasyDMA.

Figure 108: Example of RAM placement (even RESULT.MAXCNT), channels 1, 2 and 5 enabled on page 422 provides an example of results placement in Data RAM, with an even RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled.



	31 16	15 0
RESULT.PTR	CH[2] 1 st result	CH[1] 1 st result
RESULT.PTR + 4	CH[1] 2 nd result	CH[5] 1 st result
RESULT.PTR + 8	CH[5] 2 nd result	CH[2] 2 nd result
	(.)
RESULT.PTR + 2*(RESULT.MAXCNT – 2)	CH[5] last result	CH[2] last result

Figure 108: Example of RAM placement (even RESULT.MAXCNT), channels 1, 2 and 5 enabled

Figure 109: Example of RAM placement (odd RESULT.MAXCNT), channels 1, 2 and 5 enabled on page 422 provides an example of results placement in Data RAM, with an odd RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled. The last 32-bit word is populated only with one 16-bit result.

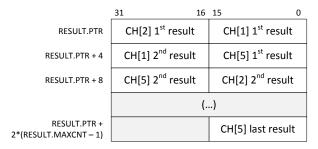


Figure 109: Example of RAM placement (odd RESULT.MAXCNT), channels 1, 2 and 5 enabled

36.6 EasyDMA

After configuring RESULT.PTR and RESULT.MAXCNT, the ADC resources are started by triggering the START task. The ADC is using EasyDMA to store results in a Result buffer in RAM.

The Result buffer is located at the address specified in the RESULT.PTR register. The RESULT.PTR register is double-buffered and it can be updated and prepared for the next START task immediately after the STARTED event is generated. The size of the Result buffer is specified in the RESULT.MAXCNT register and the ADC will generate an END event when it has filled up the Result buffer, see *Figure 110: ADC* on page 423. Results are stored in little-endian byte order in Data RAM. Every sample will be sign extended to 16 bit before stored in the Result buffer.

The ADC is stopped by triggering the STOP task. The STOP task will terminate an ongoing sampling. The ADC will generate a STOPPED event when it has stopped. If the ADC is already stopped when the STOP task is triggered, the STOPPED event will still be generated.



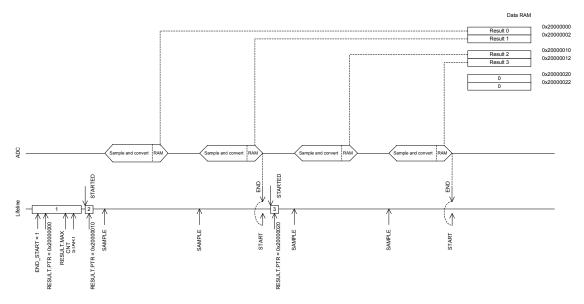


Figure 110: ADC

If the RESULT.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The EasyDMA will have finished accessing the RAM when the END or STOPPED event has been generated.

The RESULT.AMOUNT register can be read following an END event or a STOPPED event to see how many results have been transferred to the Result buffer in RAM since the START task was triggered.

In Scan mode, the size of the Result buffer must be large enough to have room for a minimum one result from each of the enabled channels. To secure this, RESULT.MAXCNT must be specified to RESULT.MAXCNT >= "number of channels enabled". See *Scan mode* on page 421 for more information about Scan mode.

36.7 Resistor ladder

The ADC has an internal resistor string for positive and negative input.

See Figure 111: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP) on page 424. The resistors are controlled in the CH[n].CONFIG.RESP and CH[n].CONFIG.RESN registers.



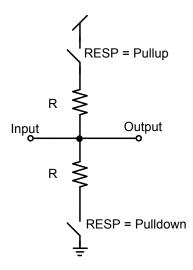


Figure 111: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP)

36.8 Reference

The ADC can use two different references, controlled in the REFSEL field of the CH[n].CONFIG register.

These are:

- · Internal reference
- VDD as reference

The internal reference results in an input range of ± 0.6 V on the ADC core. VDD as reference results in an input range of $\pm VDD/4$ on the ADC core. The gain block can be used to change the effective input range of the ADC.

```
Input range = (+- 0.6 \text{ V or } +-\text{VDD}/4)/\text{Gain}
```

For example, choosing VDD as reference, single ended input (grounded negative input), and a gain of 1/4 the input range will be:

```
Input range = (VDD/4)/(1/4) = VDD
```

With internal reference, single ended input (grounded negative input), and a gain of 1/6 the input range will be:

```
Input range = (0.6 \text{ V})/(1/6) = 3.6 \text{ V}
```

The AIN0-AIN7 inputs cannot exceed VDD, or be lower than VSS.

36.9 Acquisition time

To sample the input voltage, the ADC connects a capacitor to the input.

For illustration, see *Figure 112: Simplified ADC sample network* on page 425. The acquisition time indicates how long the capacitor is connected, see TACQ field in CH[n].CONFIG register. The required acquisition time depends on the source (R_{source}) resistance. For high source resistance the acquisition time should be increased, see *Table 80: Acquisition time* on page 425.

When using VDDHDIV5 as input, the acquisition time needs to be 10 µs or higher.



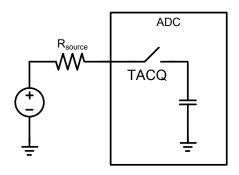


Figure 112: Simplified ADC sample network

Table 80: Acquisition time

TACQ [μs]	Maximum source resistance [kOhm]
3	10
5	40
10	100
15	200
20	400
40	800

36.10 Limits event monitoring

A channel can be event monitored by configuring limit register CH[n].LIMIT.

If the conversion result is higher than the defined high limit, or lower than the defined low limit, the appropriate event will get fired.

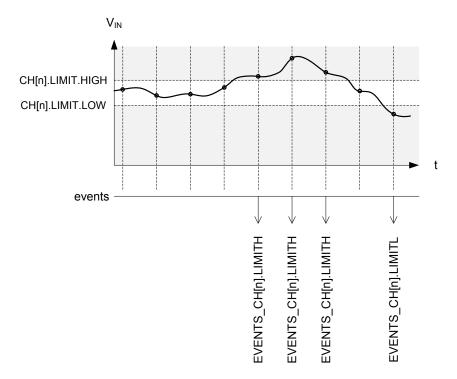


Figure 113: Example of limits monitoring on channel 'n'

Note that when setting the limits, CH[n].LIMIT.HIGH shall always be higher than or equal to CH[n].LIMIT.LOW . In other words, an event can be fired only when the input signal has been sampled



outside of the defined limits. It is not possible to fire an event when the input signal is inside a defined range by swapping high and low limits.

The comparison to limits always takes place, there is no need to enable it. If comparison is not required on a channel, the software shall simply ignore the related events. In that situation, the value of the limits registers is irrelevant, so it does not matter if CH[n].LIMIT.LOW is lower than CH[n].LIMIT.HIGH or not.

36.11 Registers

Table 81: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40007000	SAADC	SAADC	Analog to digital converter	

Table 82: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start the ADC and prepare the result buffer in RAM
TASKS_SAMPLE	0x004	Take one ADC sample, if scan is enabled all channels are sampled
TASKS_STOP	0x008	Stop the ADC and terminate any on-going conversion
TASKS_CALIBRATEOFFS	E 0x00C	Starts offset auto-calibration
EVENTS_STARTED	0x100	The ADC has started
EVENTS_END	0x104	The ADC has filled up the Result buffer
EVENTS_DONE	0x108	A conversion task has been completed. Depending on the mode, multiple conversions might be
		needed for a result to be transferred to RAM.
EVENTS_RESULTDONE	0x10C	A result is ready to get transferred to RAM.
EVENTS_CALIBRATEDO	N 0x110	Calibration is complete
EVENTS_STOPPED	0x114	The ADC has stopped
EVENTS_CH[0].LIMITH	0x118	Last results is equal or above CH[0].LIMIT.HIGH
EVENTS_CH[0].LIMITL	0x11C	Last results is equal or below CH[0].LIMIT.LOW
EVENTS_CH[1].LIMITH	0x120	Last results is equal or above CH[1].LIMIT.HIGH
EVENTS_CH[1].LIMITL	0x124	Last results is equal or below CH[1].LIMIT.LOW
EVENTS_CH[2].LIMITH	0x128	Last results is equal or above CH[2].LIMIT.HIGH
EVENTS_CH[2].LIMITL	0x12C	Last results is equal or below CH[2].LIMIT.LOW
EVENTS_CH[3].LIMITH	0x130	Last results is equal or above CH[3].LIMIT.HIGH
EVENTS_CH[3].LIMITL	0x134	Last results is equal or below CH[3].LIMIT.LOW
EVENTS_CH[4].LIMITH	0x138	Last results is equal or above CH[4].LIMIT.HIGH
EVENTS_CH[4].LIMITL	0x13C	Last results is equal or below CH[4].LIMIT.LOW
EVENTS_CH[5].LIMITH	0x140	Last results is equal or above CH[5].LIMIT.HIGH
EVENTS_CH[5].LIMITL	0x144	Last results is equal or below CH[5].LIMIT.LOW
EVENTS_CH[6].LIMITH	0x148	Last results is equal or above CH[6].LIMIT.HIGH
EVENTS_CH[6].LIMITL	0x14C	Last results is equal or below CH[6].LIMIT.LOW
EVENTS_CH[7].LIMITH	0x150	Last results is equal or above CH[7].LIMIT.HIGH
EVENTS_CH[7].LIMITL	0x154	Last results is equal or below CH[7].LIMIT.LOW
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STATUS	0x400	Status
ENABLE	0x500	Enable or disable ADC
CH[0].PSELP	0x510	Input positive pin selection for CH[0]
CH[0].PSELN	0x514	Input negative pin selection for CH[0]
CH[0].CONFIG	0x518	Input configuration for CH[0]
CH[0].LIMIT	0x51C	High/low limits for event monitoring a channel
CH[1].PSELP	0x520	Input positive pin selection for CH[1]
CH[1].PSELN	0x524	Input negative pin selection for CH[1]
CH[1].CONFIG	0x528	Input configuration for CH[1]
CH[1].LIMIT	0x52C	High/low limits for event monitoring a channel
CH[2].PSELP	0x530	Input positive pin selection for CH[2]



Register	Offset	Description
CH[2].PSELN	0x534	Input negative pin selection for CH[2]
CH[2].CONFIG	0x538	Input configuration for CH[2]
CH[2].LIMIT	0x53C	High/low limits for event monitoring a channel
CH[3].PSELP	0x540	Input positive pin selection for CH[3]
CH[3].PSELN	0x544	Input negative pin selection for CH[3]
CH[3].CONFIG	0x548	Input configuration for CH[3]
CH[3].LIMIT	0x54C	High/low limits for event monitoring a channel
CH[4].PSELP	0x550	Input positive pin selection for CH[4]
CH[4].PSELN	0x554	Input negative pin selection for CH[4]
CH[4].CONFIG	0x558	Input configuration for CH[4]
CH[4].LIMIT	0x55C	High/low limits for event monitoring a channel
CH[5].PSELP	0x560	Input positive pin selection for CH[5]
CH[5].PSELN	0x564	Input negative pin selection for CH[5]
CH[5].CONFIG	0x568	Input configuration for CH[5]
CH[5].LIMIT	0x56C	High/low limits for event monitoring a channel
CH[6].PSELP	0x570	Input positive pin selection for CH[6]
CH[6].PSELN	0x574	Input negative pin selection for CH[6]
CH[6].CONFIG	0x578	Input configuration for CH[6]
CH[6].LIMIT	0x57C	High/low limits for event monitoring a channel
CH[7].PSELP	0x580	Input positive pin selection for CH[7]
CH[7].PSELN	0x584	Input negative pin selection for CH[7]
CH[7].CONFIG	0x588	Input configuration for CH[7]
CH[7].LIMIT	0x58C	High/low limits for event monitoring a channel
RESOLUTION	0x5F0	Resolution configuration
OVERSAMPLE	0x5F4	Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is
		applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.
SAMPLERATE	0x5F8	Controls normal or continuous sample rate
RESULT.PTR	0x62C	Data pointer
RESULT.MAXCNT	0x630	Maximum number of buffer words to transfer
RESULT.AMOUNT	0x634	Number of buffer words transferred since last START

36.11.1 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0	$0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;$
Id RW Field	Value Id	Value	Description
A RW STARTED			Enable or disable interrupt for STARTED event
			See EVENTS_STARTED
	Disabled	0	Disable
	Enabled	1	Enable
B RW END			Enable or disable interrupt for END event
			See EVENTS_END
	Disabled	0	Disable
	Enabled	1	Enable
C RW DONE			Enable or disable interrupt for DONE event
			See EVENTS_DONE
	Disabled	0	Disable
	Enabled	1	Enable
D RW RESULTDONE			Enable or disable interrupt for RESULTDONE event
			See EVENTS_RESULTDONE
	Disabled	0	Disable
	Enabled	1	Enable



Bit n	umbe	er		31	30	29 :	28 2	7 26	25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld							_			V U T S R Q P O N M L K J I H G F E D C B A
		0000000				0	0 (0	0 (000000000000000000000000000000000000000
ld E		Field CALIBRATEDONE	Value Id	va	lue					Description Enable or disable interrupt for CALIBRATEDONE event
E .	NVV	CALIBRATEDONE								
			S. 11.1							See EVENTS_CALIBRATEDONE
			Disabled Enabled	0						Disable Enable
F	RW	STOPPED	Ellableu	_						Enable or disable interrupt for STOPPED event
		3.3.1.25								
			Disabled	0						See EVENTS_STOPPED Disable
			Enabled	1						Enable
G	RW	CHOLIMITH	Enabled	-						Enable or disable interrupt for CH[0].LIMITH event
			Disabled	0						See EVENTS_CH[0].LIMITH Disable
			Enabled	1						Enable
Н	RW	CHOLIMITL	Enabled	_						Enable or disable interrupt for CH[0].LIMITL event
			Disabled	0						See EVENTS_CH[0].LIMITL Disable
			Enabled	1						Enable
l	RW	CH1LIMITH	Lindoicu	-						Enable or disable interrupt for CH[1].LIMITH event
										See EVENTS CH[1].LIMITH
			Disabled	0						Disable
			Enabled	1						Enable
l	RW	CH1LIMITL								Enable or disable interrupt for CH[1].LIMITL event
										See EVENTS_CH[1].LIMITL
			Disabled	0						Disable
			Enabled	1						Enable
K	RW	CH2LIMITH								Enable or disable interrupt for CH[2].LIMITH event
										See EVENTS_CH[2].LIMITH
			Disabled	0						Disable
			Enabled	1						Enable
L	RW	CH2LIMITL								Enable or disable interrupt for CH[2].LIMITL event
										See EVENTS CH[2].LIMITL
			Disabled	0						Disable
			Enabled	1						Enable
М	RW	CH3LIMITH								Enable or disable interrupt for CH[3].LIMITH event
										See EVENTS_CH[3].LIMITH
			Disabled	0						Disable
			Enabled	1						Enable
N	RW	CH3LIMITL								Enable or disable interrupt for CH[3].LIMITL event
										See EVENTS_CH[3].LIMITL
			Disabled	0						Disable
			Enabled	1						Enable
0	RW	CH4LIMITH								Enable or disable interrupt for CH[4].LIMITH event
										See EVENTS_CH[4].LIMITH
			Disabled	0						Disable
			Enabled	1						Enable
Р	RW	CH4LIMITL								Enable or disable interrupt for CH[4].LIMITL event
										See EVENTS_CH[4].LIMITL
			Disabled	0						Disable
			Enabled	1						Enable
Q	RW	CH5LIMITH								Enable or disable interrupt for CH[5].LIMITH event
										See EVENTS_CH[5].LIMITH



Bitı	numbe	er		31	30 2	9 28	27	26 2	25 2	24 2	23	22 2	1 20	19	18	3 17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id												٧	/ L	Т	S	R	Q	Р	0	N	М	L K	J	-1	Н	G	F	Е	D (В	Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Val	ue					D	Des	script	tion																		
			Disabled	0						D	Disa	able																			
			Enabled	1						E	na	able																			
R	RW	CH5LIMITL CH5LIMITL								Е	na	able o	or d	isab	le i	ntei	rup	t fo	r Cl	1[5]].LIN	IITL	eve	nt							
										S	See	e EVE	NTS	C H	1[5]	.LIN	ΛΙΤΙ														
			Disabled	0						D	Disa	able		_																	
			Enabled	1						Ε	na	able																			
S	RW	CH6LIMITH								Ε	na	able o	or d	isab	le i	ntei	rrup	t fo	r Cl	1[6]].LIN	IITH	eve	ent							
										ς	ممة	e EVE	NITS	. CF	1[6]		літі	,													
			Disabled	0								able	1415		ı[U]	·LIII		•													
			Enabled	1								able																			
Т	RW	CH6LIMITL	2.102.00									able o	or d	isab	le i	ntei	rur	t fo	r Cl	1[6]	l.LIN	1ITL	eve	nt							
																	·				,										
												e EVE	NTS	_CF	1[6]	.LIN	ΛΙΤΙ														
			Disabled	0								able 																			
			Enabled	1								able																			
U	RW	CH7LIMITH								E	na	able o	or d	isab	le ii	ntei	rrup	t fo	r Cl	1[7]	J.LIIV	IITH	eve	ent							
										S	See	EVE	NTS	_CF	1[7]	.LIN	1ITI	1													
			Disabled	0						D	Disa	able																			
			Enabled	1						Е	na	able																			
٧	RW	CH7LIMITL								Ε	na	able o	or d	isab	le i	ntei	rup	t fo	r Cl	1[7]].LIN	IITL	eve	nt							
										S	See	e EVE	NTS	_CF	1[7]	.LIN	ΛΙΤΙ														
			Disabled	0						D	Disa	able																			
			Enabled	1						Е	na	able																			

36.11.2 INTENSET

Address offset: 0x304

Enable interrupt

	number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW Field V	/alue Id	Value	Description
Α	RW STARTED			Write '1' to Enable interrupt for STARTED event
				See EVENTS_STARTED
	Se	et	1	Enable
	D	Disabled	0	Read: Disabled
	E	nabled	1	Read: Enabled
В	RW END			Write '1' to Enable interrupt for END event
				See EVENTS_END
	Se	et	1	Enable
	D	Disabled	0	Read: Disabled
	E	nabled	1	Read: Enabled
С	RW DONE			Write '1' to Enable interrupt for DONE event
				See EVENTS_DONE
	Se	et	1	Enable
	D	Disabled	0	Read: Disabled
	E	nabled	1	Read: Enabled
D	RW RESULTDONE			Write '1' to Enable interrupt for RESULTDONE event
				See EVENTS_RESULTDONE
	Se	et	1	Enable
	D	Disabled	0	Read: Disabled
	E	nabled	1	Read: Enabled



Bit n	umber			31 30	29	28 2	27 2	6 25	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id -										V U T S R Q P O N M L K J I H G F E D C B A
	t 0x000					0	0 0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Fi		Value Id	Value	•					Description
E	KW C	ALIBRATEDONE								Write '1' to Enable interrupt for CALIBRATEDONE event
										See EVENTS_CALIBRATEDONE
			Set	1						Enable
			Disabled	0						Read: Disabled
_	D144 65	TODDED	Enabled	1						Read: Enabled
F	KW S	TOPPED								Write '1' to Enable interrupt for STOPPED event
										See EVENTS_STOPPED
			Set	1						Enable
			Disabled	0						Read: Disabled
_	D144 C		Enabled	1						Read: Enabled
G	RW C	HOLIMITH								Write '1' to Enable interrupt for CH[0].LIMITH event
										See EVENTS_CH[0].LIMITH
			Set	1						Enable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Н	RW C	H0LIMITL								Write '1' to Enable interrupt for CH[0].LIMITL event
										See EVENTS_CH[0].LIMITL
			Set	1						Enable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
I	RW C	H1LIMITH								Write '1' to Enable interrupt for CH[1].LIMITH event
										See EVENTS_CH[1].LIMITH
			Set	1						Enable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
J	RW C	H1LIMITL								Write '1' to Enable interrupt for CH[1].LIMITL event
										See EVENTS_CH[1].LIMITL
			Set	1						Enable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
K	RW C	H2LIMITH								Write '1' to Enable interrupt for CH[2].LIMITH event
										See EVENTS_CH[2].LIMITH
			Set	1						Enable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
L	RW C	H2LIMITL								Write '1' to Enable interrupt for CH[2].LIMITL event
										See EVENTS_CH[2].LIMITL
			Set	1						Enable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
М	RW C	нзымітн								Write '1' to Enable interrupt for CH[3].LIMITH event
										See EVENTS_CH[3].LIMITH
			Set	1						Enable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
N	RW C	H3LIMITL								Write '1' to Enable interrupt for CH[3].LIMITL event
										See EVENTS_CH[3].LIMITL
			Set	1						Enable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
0	RW C	H4LIMITH								Write '1' to Enable interrupt for CH[4].LIMITH event



Bit r	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
				See EVENTS_CH[4].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Р	RW CH4LIMITL			Write '1' to Enable interrupt for CH[4].LIMITL event
				See EVENTS_CH[4].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Q	RW CH5LIMITH			Write '1' to Enable interrupt for CH[5].LIMITH event
				See EVENTS_CH[5].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
R	RW CH5LIMITL			Write '1' to Enable interrupt for CH[5].LIMITL event
				See EVENTS_CH[5].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
S	RW CH6LIMITH			Write '1' to Enable interrupt for CH[6].LIMITH event
				See EVENTS_CH[6].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Т	RW CH6LIMITL			Write '1' to Enable interrupt for CH[6].LIMITL event
				See EVENTS_CH[6].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
U	RW CH7LIMITH			Write '1' to Enable interrupt for CH[7].LIMITH event
				See EVENTS_CH[7].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
V	RW CH7LIMITL			Write '1' to Enable interrupt for CH[7].LIMITL event
				See EVENTS CH[7].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
		2.7dbicd	-	

36.11.3 INTENCLR

Address offset: 0x308 Disable interrupt

Bit n	umbe	r		31	30	29	28	3 27	26	25	5 24	1 23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id														٧	U	Т	S	R	Q	Р	0	Ν	М	L	K	J	1	Н	G	F	Ε	D	С	B A	١.
Rese	et 0x00	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	RW	Field	Value Id	Va	lue							De	escr	ipti	on																				
Α	RW	STARTED										W	rite	'1'	to [Disa	ble	int	err	upt	fo	r ST	AR	ΓED	eve	ent									
															ITS_	_ST/	4R	TED																	
			Clear	1								Di	sab	e																					



Bit	numb	er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x(0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	END			Write '1' to Disable interrupt for END event
					See EVENTS_END
			Clear	1	Disable
			Disabled	0	Read: Disabled
6	DIA	DONE	Enabled	1	Read: Enabled
С	RW	DONE			Write '1' to Disable interrupt for DONE event
					See EVENTS_DONE
			Clear	1	Disable
			Disabled Enabled	0	Read: Disabled
D	B/W	RESULTDONE	Enabled	1	Read: Enabled Write '1' to Disable interrupt for RESULTDONE event
D	11.00	RESOLIDONE			Write 1 to bisable interrupt for RESOLIDONE event
			a.		See EVENTS_RESULTDONE
			Clear Disabled	1	Disable Read: Disabled
			Enabled	1	Read: Disabled Read: Enabled
E	RW	CALIBRATEDONE	Lilabica	1	Write '1' to Disable interrupt for CALIBRATEDONE event
_					
			Clear	1	See EVENTS_CALIBRATEDONE Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	STOPPED			Write '1' to Disable interrupt for STOPPED event
					See EVENTS_STOPPED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	CHOLIMITH			Write '1' to Disable interrupt for CH[0].LIMITH event
					See EVENTS_CH[0].LIMITH
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	CHOLIMITL			Write '1' to Disable interrupt for CH[0].LIMITL event
					See EVENTS_CH[0].LIMITL
			Clear	1	Disable
			Disabled	0	Read: Disabled
		CHALLA AITT	Enabled	1	Read: Enabled
ı	кW	CH1LIMITH			Write '1' to Disable interrupt for CH[1].LIMITH event
					See EVENTS_CH[1].LIMITH
			Clear	1	Disable
			Disabled	0	Read: Disabled
	B/V	CH1LIMITL	Enabled	1	Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITL event
J	11.00	CHILINATE			
			Class	1	See EVENTS_CH[1].LIMITL
			Clear Disabled	1	Disable Read: Disabled
			Enabled	1	Read: Enabled
K	RW	CH2LIMITH			Write '1' to Disable interrupt for CH[2].LIMITH event
			Clear	1	See EVENTS_CH[2].LIMITH Disable
			Disabled	0	Read: Disabled
				-	



No	Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
March Marc	Id					V U T S R Q P O N M L K J I H G F E D C B A
Frabled 1 Read: trainbed Write "1" to Disable interrupt for CN[2]_LIMITL event	Rese	et 0x0	0000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Clear	Id	RW	Field	Value Id	Value	Description
Clear				Enabled	1	Read: Enabled
Clear 1	L	RW	CH2LIMITL			Write '1' to Disable interrupt for CH[2].LIMITL event
Disabled Crabled 1 Read: chabled Read: chabled						See EVENTS_CH[2].LIMITL
Read				Clear	1	Disable
M				Disabled	0	Read: Disabled
Clear				Enabled	1	
Clear	M	RW	CH3LIMITH			Write '1' to Disable interrupt for CH[3].LIMITH event
N RW CHSUMITL						See EVENTS_CH[3].LIMITH
Read: Enabled Read: Enable				Clear	1	Disable
No. No. CH3LMTL						
See EVENTS, CHISLIMITE				Enabled	1	
Clear	N	RW	CH3LIMITL			Write '1' to Disable interrupt for CH[3].LIMITL event
Disabled Canabled						See EVENTS_CH[3].LIMITL
Part Char				Clear	1	Disable
O RW CH4LIMITH From the "1" to Disable interrupt for Ch[4], LIMITH event A Clear 1 Disable B Clear 1 Disable B Enabled 1 Read: Disabled B RW CH4LIMITL Write "1" to Disable interrupt for Ch[4], LIMITL event Clear 1 Disabled Clear 1 Read: Disabled B Part (F) To Disable interrupt for Ch[5], LIMITH event See EVENTS, Ch[5], LIMITH Clear 1 Disabled B Clear 1 Disabled B Clear 1 Disabled B Clear 1 Disabled B CH5LIMITH Write "1" to Disable interrupt for Ch[5], LIMITH event Clear 1 Disabled B Ch6umith 1 Read: Chabled B Enabled 1 Read: Disabled B Enabled 1 Read: Disabled B Clear 1 Disabled						
Clear		DIA	CUALINATE	Enabled	1	
Clear 1 Disable	U	KW	CH4LIIVII (H			write 1 to bisable interrupt for CH[4].LilviiTH event
RW CHALIMITL						
P RW CHALIMITL Write '1' to Disable interrupt for CH[4],LIMITL event Gear 1 Disable Disable 2 Read: Disabled Enabled 1 Disabled Read: Enabled Write '1' to Disable interrupt for CH[5],LIMITH event See EVENTS_CH[5],LIMITH See EVENTS_CH[5],LIMITH Clear 1 Disable Possible Write '1' to Disable interrupt for CH[5],LIMITL event See EVENTS_CH[5],LIMITL See EVENTS_CH[5],LIMITL Clear 1 Disable Disable 0 Read: Enabled See EVENTS_CH[5],LIMITL Write '1' to Disable interrupt for CH[6],LIMITH event See EVENTS_CH[6],LIMITH See EVENTS_CH[6],LIMITH See EVENTS_CH[6],LIMITH See EVENTS_CH[6],LIMITH To RW CHGLIMITL Write '1' to Disable interrupt for CH[6],LIMITL event See EVENTS_CH[6],LIMITL See EVENTS_CH[6],LIMITL Virte '1' to Disable interrupt for CH[6],LIMITL event See EVENTS_CH[6],LIMITL See EVENTS_CH[6],LIMITL See EVENTS_CH[6],LIMITL See EVENTS_CH[6],LIMITL See EVENTS_CH[6],LIMITL <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td></t<>						
Clear	D	D\A/	CHALIMITI	Enabled	1	
Clear	r	IVV	CHALIMITE			
Disabled Disabled Read: Disabled Read: Disabled Read: Enabled Read: Enabled Read: Enabled Read: Enabled Read: Enabled Read: Disable interrupt for CH[5], LIMITH event See EVENTS_CH[5], LIMITH Event						
Q RW CHSLIMITH Clear 1 Disable Disabled 0 Read: Disabled Read: Enabled CHSLIMITH Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Read: Disabled Enabled 1 Read: Enabled Read: Enabled Read: Disabled Enabled Read: Disabled Enabled Read: Disabled Enabled Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Read: Enabled See EVENTS_CH[S].LIMITL Clear 1 Disable Enabled 1 Read: Enabled See EVENTS_CH[S].LIMITH Clear 1 Disable Enabled 1 Read: Enabled T RW CHGLIMITH T RW CHGLIMITL Clear 1 Disable Enabled 1 Read: Enabled T RW CHGLIMITL Clear 1 Disable Enabled 0 Read: Disabled Enabled 1 Read: Enabled T Read: Enabled Read: Disabled Enabled 0 Read: Disabled Enabled 1 Read: Enabled Read: Disabled Enabled 0 Read: Disabled Enabled 1 Read: Enabled T Read: Enabled Read: Disabled Read: Disabled Read: Disabled Read: Disabled						
Q RW CHSLIMITH Clear						
Clear	Q	RW	CH5LIMITH	Endored	-	
Clear Clea						,
Disabled				Clear	1	
R RW CHSLIMITL Clear 1 Disable Enabled Clear 1 Clear Enabled Clear 1 Clear Enabled Clear 1 Clear Enabled Clear 1 Disable Enabled Clear 1 Disable Clear 1 Disable Enabled Clear 1 Disable Enabled Clear 1 Disable Enabled Clear 1 Disable Enabled Enabled Clear 1 Disable Clear 1 Disable Enabled Clear 1 Disable Enabled Clear 1 Disable Enabled Clear 1 Disable Enabled Enabled Clear 1 Disable Enabled Enabled Enabled Clear 1 Disable Enabled Enabled Enabled Clear 1 Disable Enabled Enabled Disable Enabled Enabled Disable Enabled OREAC: Disable Write '1' to Disable interrupt for CH[7].LIMITH Clear 1 Disable Write '1' to Disable interrupt for CH[7].LIMITH Clear 1 Disable Disable OREAC: ENABLE Write '1' to Disable OREAC: Disabled OREAC: Disabled OREAC: Disabled OREAC: Disabled						
See EVENTS_CH[5].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled S RW CH6LIMITH Clear 1 Disable Clear 1 Disable Clear 1 Disable Disable 0 Read: Enabled Clear 1 Disable Enabled 1 Read: Enabled T RW CH6LIMITL Clear 1 Read: Enabled T RW CH6LIMITL Clear 1 Disable Enabled 1 Read: Enabled Clear 1 Disable Read: Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Virite '1' to Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable Enabled 1 Read: Enabled Clear 1 Disable Enabled 0 Read: Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Clear 1 Disable Read: Disabled Clear 1 Disable Read: Disabled						
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled S RW CH6LIMITH Clear 1 Disable Disabled 0 Read: Disable interrupt for CH[6].LIMITH event See EVENTS_CH[6].LIMITH Clear 1 Disable Enabled 1 Read: Enabled T RW CH6LIMITL Clear 1 Disable Enabled 0 Read: Disable interrupt for CH[6].LIMITL Clear 1 Disable Disable 0 Read: Disable interrupt for CH[6].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[6].LIMITL Clear 1 Disable Write '1' to Disable interrupt for CH[7].LIMITH Clear 1 Read: Enabled Clear 1 Disable Clear 1 Read: Enabled Clear 1 Disable Read: Disabled Read: Disable interrupt for CH[7].LIMITH Clear 1 Disable Read: Disable Read: Disable	R	RW	CH5LIMITL			
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled S RW CH6LIMITH Clear 1 Disable Disabled 0 Read: Disable interrupt for CH[6].LIMITH event See EVENTS_CH[6].LIMITH Clear 1 Disable Enabled 1 Read: Enabled T RW CH6LIMITL Clear 1 Disable Enabled 0 Read: Disable interrupt for CH[6].LIMITL Clear 1 Disable Disable 0 Read: Disable interrupt for CH[6].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[6].LIMITL Clear 1 Disable Write '1' to Disable interrupt for CH[7].LIMITH Clear 1 Read: Enabled Clear 1 Disable Clear 1 Read: Enabled Clear 1 Disable Read: Disabled Read: Disable interrupt for CH[7].LIMITH Clear 1 Disable Read: Disable Read: Disable						See EVENTS CHISTUMITI
Disabled 0 Read: Disabled Enabled 1 Read: Enabled S RW CHGLIMITH Clear 1 Disable Enabled 1 Read: Enabled Clear 1 Disable Enabled 1 Read: Enabled T RW CHGLIMITL Clear 1 Disable Enabled 1 Read: Enabled T RW CHGLIMITL Clear 1 Disable Enabled 1 Read: Enabled T Disable Clear 1 Disable Clear 1 Disable Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled T Disable Clear 1 Disable Enabled 1 Read: Enabled T Read: Enabled Clear 1 Disable Enabled 1 Read: Enabled Clear 1 Read: E				Clear	1	
S RW CH6LIMITH Clear Disable Disabled Enabled Disabled Clear Disabled Enabled Disabled Disabled Enabled Disabled Disabled Enabled Disabled Disabled Enabled Disabled					0	
See EVENTS_CH[6].LIMITH Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled T RW CH6LIMITL Clear 1 Disable Clear 1 Disable Disabled 0 Read: Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable Enabled 1 Read: Enabled U CH7LIMITH Clear 1 Disable Disable 0 Read: Disable See EVENTS_CH[7].LIMITH Clear 1 Disable Disabled 0 Read: Disabled				Enabled	1	Read: Enabled
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled T RW CH6LIMITL Clear 1 Disable Disabled 0 Read: Enabled Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Clear 1 Disable Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Clear 1 Disable Disable Disabled 0 Read: Disabled	S	RW	CH6LIMITH			Write '1' to Disable interrupt for CH[6].LIMITH event
Disabled 0 Read: Disabled Enabled 1 Read: Enabled T RW CH6LIMITL Clear 1 Disable Enabled 0 Read: Disable interrupt for CH[6].LIMITL event Disabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable Enabled 1 Read: Enabled U CH7LIMITH Clear 1 Disable Disable (1' to Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Clear 1 Disable Disabled 0 Read: Disabled						See EVENTS_CH[6].LIMITH
T RW CH6LIMITL Clear Disabled Disabled 1 Read: Enabled Write '1' to Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Disable Read: Disabled Read: Disabled Read: Disabled Read: Disabled Write '1' to Disable interrupt for CH[7].LIMITH Write '1' to Disable interrupt for CH[7].LIMITH Clear Clear Disabled O Read: Disabled Read: Disabled				Clear	1	Disable
T RW CH6LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable Enabled 1 Read: Enabled Clear 1 Disable Disabled Read: Disable interrupt for CH[7].LIMITH Clear 1 Disable Read: Disable interrupt for CH[7].LIMITH Clear 1 Disable Disabled 0 Read: Disabled				Disabled	0	Read: Disabled
See EVENTS_CH[6].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable interrupt for CH[7].LIMITH Clear 1 Disable Disabled 0 Read: Disable				Enabled	1	Read: Enabled
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable Write '1' to Disable interrupt for CH[7].LIMITH See EVENTS_CH[7].LIMITH Clear 1 Disable Disabled 0 Read: Disabled	Т	RW	CH6LIMITL			Write '1' to Disable interrupt for CH[6].LIMITL event
Disabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable Disabled 0 Read: Enabled Prince 1' to Disable interrupt for CH[7].LIMITH Clear 1 Disable Read: Disabled						See EVENTS_CH[6].LIMITL
Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable Disabled 0 Read: Enabled Read: Enabled Write '1' to Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Disable Read: Disabled				Clear	1	Disable
U RW CH7LIMITH Write '1' to Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Clear 1 Disable Disabled 0 Read: Disabled				Disabled	0	Read: Disabled
See EVENTS_CH[7].LIMITH Clear 1 Disable Disabled 0 Read: Disabled				Enabled	1	
Clear 1 Disable Disabled 0 Read: Disabled	U	RW	CH7LIMITH			Write '1' to Disable interrupt for CH[7].LIMITH event
Disabled 0 Read: Disabled						See EVENTS_CH[7].LIMITH
Enabled 1 Read: Enabled						
				Enabled	1	Read: Enabled



Bit	numbe	r		31	1 30	29	2	8 2	7 :	26	25	24	23	22	2 21	L 20	19	18	17	16	15	14	13	3 12	11	10	9	8	7	6	5	4	3	2	1	0
Id															V	U	Т	S	R	Q	Р	0	N	M	L	K	J	1	Н	G	F	Ε	D	С	В	Α
Res	et 0x0	0000000		0	0	0	C	0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•							De	SCI	ripti	ion																				
V	RW	CH7LIMITL											W	rite	e '1'	to	Disa	able	in	terr	upt	fo	r Cl	1[7]	.LIN	ИΙΤ	L ev	ent								
													Se	e E	VEI	NTS.	_CF	1[7]	.LII	ИΙΤ	L															
			Clear	1									Dis	sab	le																					
			Disabled	0									Re	ad	: Dis	sab	led																			
			Enabled	1									Re	ad	: En	abl	ed																			

36.11.4 STATUS

Address offset: 0x400

Status

Bit	numbe	r		33	1 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue)						De	scri	iptio	on																			
Α	R	STATUS										Sta	atus	;																				
			Ready	0								ΑD	C is	rea	ady.	No	on	-go	ing	100	ıve	rsic	n.											
			Busy	1								ΑD	C is	bu	sy.	Con	ver	sioi	n in	pr	ogr	ess												

36.11.5 ENABLE

Address offset: 0x500 Enable or disable ADC

Bit	numbe	er		31 30	29	28 2	7 20	6 25	24	23	22	21	20	19	18	17	16	15	14	13 :	2 1	1 1	9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value						De	scri	ipti	ion																		
Α	RW	ENABLE								Ena	able	e o	r di	sab	le A	DC															
			Disabled	0						Dis	abl	le A	ADC	:																	
			Enabled	1						Ena	able	e A	DC																		
										Wh	nen	en	nabl	ed,	the	ΑĽ)C v	/ill a	ıcqu	iire	acce	ess 1	o th	e aı	nalc	g ir	npu	ıt			
										pin	s s	pec	cifie	d ir	th:	e C	H[n]	.PS	ELP	and	СН	[n].	PSEI	N r	egis	ters	s.				

36.11.6 CH[0].PSELP

Address offset: 0x510

Input positive pin selection for CH[0]

Rit	numl	ner .		21	30 29	רו	2 27	26	25	24	23	ר ר	1 20	10	10	17	16	15	1/	12	12 1	1 10	۱ ۵	8	7	6	5	4	3 2) 1	0
	Hulli	Jei		31	30 23	, 2	.0 21	20	23	24	23.	ZZ Z	.1 20	, 13	10	1/	10	13	14	13	12 1	.1 10	, 5	0	,	O	_	,			_
Id																												Α /	Α Α	A A	. A
Res	et 0x	00000000		0	0 0	(0 0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0
Id	RW	/ Field	Value Id	Va	lue						Des	crip	tion																		
Α	RW	PSELP									Ana	log	posit	tive	inp	ut d	har	nne	I												
			NC	0							Not	con	nect	ed																	
			AnalogInput0	1							AIN	0																			
			AnalogInput1	2							AIN	1																			
			AnalogInput2	3							AIN	2																			
			AnalogInput3	4							AIN	3																			
			AnalogInput4	5							AIN	4																			
			AnalogInput5	6							AIN	5																			
			AnalogInput6	7							AIN	6																			
			AnalogInput7	8							AIN	7																			
			VDD	9							VDI)																			
			VDDHDIV5	0x	0D						VDI)H/5	5																		



36.11.7 CH[0].PSELN

Address offset: 0x514

Input negative pin selection for CH[0]

Bit r	numbe	er		31	30 2	9 2	8 27	7 26	25 2	24 2	3 22	21 2	0 19	9 18	17 3	16	15 1	4 1	3 12	11	10	9	8	7	6 5	5 4	3	2	1 0
Id																										Α	Α	Α	А А
Res	et OxC	0000000		0	0 () (0 0	0	0	0 0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0 0
Id	RW	Field	Value Id	Va	lue					D	escri	ption	1																
Α	RW	PSELN								Α	nalo	g neg	ativ	e inp	out, e	ena	ble	dif	fere	ntia	l ch	ann	el						
			NC	0						N	ot co	nnec	ted																
			AnalogInput0	1						Α	IN0																		
			AnalogInput1	2						Α	IN1																		
			AnalogInput2	3						Α	IN2																		
			AnalogInput3	4						Α	IN3																		
			AnalogInput4	5						Α	IN4																		
			AnalogInput5	6						Α	IN5																		
			AnalogInput6	7						Α	IN6																		
			AnalogInput7	8						Α	IN7																		
			VDD	9						٧	DD																		
			VDDHDIV5	0x	0D					٧	DDH	/5																	

36.11.8 CH[0].CONFIG

Address offset: 0x518

Input configuration for CH[0]

	numb	er		3:	1 30	29	9 28	8 27	7 2	6 2			23	22 21						15	14	1 1	3 1:	2 1					6			3	2	1	0
Id												G			F		Ε	Ε	Ε				C)	(: C	. C			В	В			Α	A
Res	et 0x0	00020000		0	0	0	0	0) (0 (0	0	0	0 0	0	0	0	1	0	0	0	C	0) () (0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	alue	2						- 1	De	script	ion																				
Α	RW	RESP										١	Pos	sitive	cha	nne	el re	sist	or	cor	tro	ı													
			Bypass	0								١	Вур	pass r	esis	tor	lad	der																	
			Pulldown	1								١	Pul	II-dow	n t	o GI	ND																		
			Pullup	2								١	Pul	ll-up t	o V	DD																			
			VDD1_2	3								:	Set	t input	at	VD	D/2																		
В	RW	RESN										ı	Ne	gative	ch	ann	el r	esi	stoi	co	ntr	ol													
			Bypass	0								- 1	Вур	pass r	esis	tor	lad	der																	
			Pulldown	1								- 1	Pul	II-dow	n t	o GI	ND																		
			Pullup	2								- 1	Pul	ll-up t	o V	DD																			
			VDD1_2	3								:	Set	t input	at	VD	D/2																		
С	RW	GAIN										(Gai	in con	tro	I																			
			Gain1_6	0								:	1/6	6																					
			Gain1_5	1								:	1/5	5																					
			Gain1_4	2								:	1/4	4																					
			Gain1_3	3								:	1/3	3																					
			Gain1_2	4								:	1/2	2																					
			Gain1	5								:	1																						
			Gain2	6									2																						
			Gain4	7								4	4																						
D	RW	REFSEL										ı	Ref	ferenc	e c	ont	rol																		
			Internal	0								-	Int	ernal	ref	erer	nce	(0.6	5 V)																
			VDD1_4	1								١	VD	D/4 a	s re	fere	enc	е																	
Е	RW	TACQ										,	Aco	quisiti	on	tim	e, t	he 1	ime	e th	e A	\D(us	es 1	o s	am	ole	the	inp	ut					
												١	vol	ltage																					
			3us	0								3	3 u	ıs																					
			5us	1								!	5 u	ıs																					
			10us	2								:	10	us																					
			15us	3								:	15	us																					



Bit n	umb	er		31	L 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14 1	13	12 :	11 1	0 9	8	7	6	5	4	3	2 :	1 0	
Id											G				F		Е	Ε	Ε				D	(: c	С			В	В		A	А А	
Rese	t OxC	00020000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0	
ld	RW	Field	Value Id	Va	alue							Des	scri	ptic	on																			
			20us	4								20	us																					
			40us	5								40	us																					
F	RW	MODE										Ena	ble	dif	fere	enti	ial r	noc	de															
			SE	0								Sin	gle	enc	led,	PS	ELN	l w	II b	e ig	nor	ed,	ne	gativ	e in	put	to /	ADC	:					
												sho	rte	d to	GI	ND																		
			Diff	1								Diff	fere	enti	al																			
G	RW	BURST										Ena	ble	bu	rst	mo	de																	
			Disabled	0								Bur	st r	noc	de is	di	sab	led	(nc	rm	al o	per	atic	on)										
			Enabled	1								Bur	st r	noc	de is	s en	abl	led.	SA	ADO	C tal	kes	2^(OVE	RSA	MPI	E n	uml	ber	of				
												san	nple	es a	s fa	st a	s it	ca	n, a	nd:	sen	ds t	he	aver	age	to I	Data	a RA	M.					

36.11.9 CH[0].LIMIT

Address offset: 0x51C

High/low limits for event monitoring a channel

Bit	nu	mbe	er			31	30	29	28	27	26	25	24	23	22	21 2	20 1	19 1	8 1	7 16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id						В	В	В	В	В	В	В	В	В	В	В	В	В	3 B	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α Δ	. 4	AA
Res	set	0x7	FFF80	00		0	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	1	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	F	RW	Field	Va	lue							Des	scri	ptio	n																				
Α	F	RW	LOW			[-3	3276	8 t	0 +3	327	67]			Lov	v le	vel l	imi	t																	
В	F	RW	HIGH			[-3	3276	8 t	0 +3	327	67]			Hig	h le	vel	limi	it																	

36.11.10 CH[1].PSELP

Address offset: 0x520

Input positive pin selection for CH[1]

	numbe	er		31	30 2	9 2	28 2	7 2	26 25	5 24	4 23	22	21 20) 1:	9 18	17	16	15	14	13 :	12 1	1 10	9	8	7	6		4 3			0
Id	-+ 00	000000		_	0 (_		_				_	0	_	_	_	0 (_	_	_	_			A A		
Kes	ет ихи	0000000		0	0 (,	0 0	,	0 0	U	U	0	0 0	U	, 0	0	U	0	U	0	0 (0	0	U	U	U	U	0 (0	U	0
Id	RW	Field	Value Id	Va	lue						De	scri	ption																		
Α	RW	PSELP									Ana	alog	g posi	tive	e inp	ut (char	nne	I												
			NC	0							No	t co	nnec	ted	I																
			AnalogInput0	1							AIN	١0																			
			AnalogInput1	2							AIN	N 1																			
			AnalogInput2	3							AIN	٧2																			
			AnalogInput3	4							AIN	٧3																			
			AnalogInput4	5							AIN	۱4																			
			AnalogInput5	6							AIN	N 5																			
			AnalogInput6	7							AIN	۱6																			
			AnalogInput7	8							AIN	١7																			
			VDD	9							VD	D																			
			VDDHDIV5	0x0	OD						VD	DH/	/5																		

36.11.11 CH[1].PSELN

Address offset: 0x524

Input negative pin selection for CH[1]

Bit number		31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			АААА
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
Δ RW PSFIN			Analog negative input, enables differential channel



Bit number		31	30	29	28 2	27	26 2	25 2	24	23 2	2 2:	1 20	19	18	17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																											Α /	Δ Δ	A	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0	0
Id RW Field	Value Id	Va	lue							Desc	ript	tion																		
	NC	0								Not	con	nect	ted																	
	AnalogInput0	1								AINC)																			
	AnalogInput1	2								AIN1	l																			
	AnalogInput2	3								AIN2	2																			
	AnalogInput3	4								AIN3	3																			
	AnalogInput4	5								AIN4	ļ																			
	AnalogInput5	6								AIN5	;																			
	AnalogInput6	7								AING	6																			
	AnalogInput7	8								AIN7	7																			
	VDD	9							,	VDD																				
	VDDHDIV5	0x	0D						,	VDD	H/5																			

36.11.12 CH[1].CONFIG

Address offset: 0x528

Input configuration for CH[1]

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			G FEEE D C C C B B A A
Reset 0x00020000		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 &$
Id RW Field	Value Id	Value	Description
A RW RESP			Positive channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
B RW RESN			Negative channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
C RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
	Gain4	7	4
D RW REFSEL			Reference control
	Internal	0	Internal reference (0.6 V)
	VDD1_4	1	VDD/4 as reference
E RW TACQ			Acquisition time, the time the ADC uses to sample the input
			voltage
	3us	0	3 us
	5us	1	5 us
	10us	2	10 us
	15us	3	15 us
	20us	4	20 us
	40us	5	40 us
F RW MODE			Enable differential mode
	SE	0	Single ended, PSELN will be ignored, negative input to ADC
			shorted to GND
	Diff	1	Differential



Bit	nur	nbe	r		3:	1 30	29	9 28	8 27	7 26	25	24	1 23	3 22	21	20	19	18	17	16	15	14	13	12 1	11 1	LO	9	8	7	6	5	4	3	2	1 (0
Id												G				F		Ε	Ε	Ε				D		С	С	С			В	В		,	Δ ,	Α
Re	set (0x0	0020000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0
Id	R	RW	Field	Value Id	V	alue	:						D	escr	pti	on																				
G	R	RW	BURST										Er	nabl	e bu	ırst	mo	de																		7
				Disabled	0								Вι	urst	mo	de i	s di	sab	led	(no	orm	al o	per	atic	n)											
				Enabled	1								Вι	urst	mo	de i	s er	nab	led	. SA	AD	C ta	kes	2^(OVE	RSA	٩M	PLE	nu	mb	er	of				
													sa	ampl	es a	s fa	ast a	as it	ca	n, a	ınd	sen	ds t	he i	ave	rag	e to	o Da	ita	RAI	M.					

36.11.13 CH[1].LIMIT

Address offset: 0x52C

High/low limits for event monitoring a channel

Bit n	umbe	er		31	30	29	28	27	26	25 2	24 2	3 2	2 21	20	19	18 :	17 1	16 1	15 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id				В	В	В	В	В	В	В	ВЕ	3 B	В	В	В	В	В	В	A A	4 A	Α	Α	Α	A	Α	Α	Α	Α	Α	A A	. Α	A
Rese	t 0x7	FFF8000		0	1	1	1	1	1	1	1 :	l 1	1	1	1	1	1	1	1 (0 0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	on																		
Id A			Value Id				:0 +3	327	67]				ripti leve		nit																	

36.11.14 CH[2].PSELP

Address offset: 0x530

Input positive pin selection for CH[2]

Bit	numbe	r		31	30 2	9 2	28 2	7 2	26 25	5 2	4 23	3 22	21 2	0 1	19 18	8 17	7 16	5 15	14	13	12	11 1	0 9	8	3 7	6	5	4	3 2	1	0
Id																												Α	A A	A	Α
Res	et 0x0	0000000		0	0 ()	0 0)	0 0	C	0	0	0 0) (0 0	0	0	0	0	0	0	0 (0	C	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						De	escri	ption	1																	
Α	RW	PSELP									Ar	nalog	g posi	itiv	e in	put	cha	inne	el												
			NC	0							No	ot co	nnec	te	d																
			AnalogInput0	1							ΑI	N0																			
			AnalogInput1	2							ΑI	N1																			
			AnalogInput2	3							ΑI	N2																			
			AnalogInput3	4							ΑI	N3																			
			AnalogInput4	5							ΑI	N4																			
			AnalogInput5	6							ΑI	N5																			
			AnalogInput6	7							ΑI	N6																			
			AnalogInput7	8							ΑI	N7																			
			VDD	9							VE	DD																			
			VDDHDIV5	0x0	OD						VE	DDH,	/5																		

36.11.15 CH[2].PSELN

Address offset: 0x534

Input negative pin selection for CH[2]

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	АААА
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW PSELN	Analog negative input, enables differential channel
NC	0 Not connected
AnalogInput0	1 AINO
AnalogInput1	2 AIN1
AnalogInput2	3 AIN2
AnalogInput3	4 AIN3
AnalogInput4	5 AIN4



Bit number	31 30 29 28 27	26 25 24 23 22 21 20 19 18	17 16 15 14 13 12	2 11 10 9 8	7 6	5 4	3 2	1 0
Id						Α	A A	. A A
Reset 0x00000000	0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0	0 0	0 0	0 0	0 0
Id RW Field Value Id	Value	Description						
AnalogInput5	6	AIN5						
AnalogInput6	7	AIN6						
AnalogInput7	8	AIN7						
VDD	9	VDD						
VDDHDIV5	0x0D	VDDH/5						

36.11.16 CH[2].CONFIG

Address offset: 0x538

Input configuration for CH[2]

Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
d			G FEEE D CCC BB AA
Reset 0x00020000		0 0 0 0 0 0	000000001000000000000000000000
d RW Field	Value Id	Value	Description
A RW RESP			Positive channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
B RW RESN			Negative channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
C RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
	Gain4	7	4
D RW REFSEL			Reference control
	Internal	0	Internal reference (0.6 V)
	VDD1_4	1	VDD/4 as reference
E RW TACQ			Acquisition time, the time the ADC uses to sample the input
			voltage
	3us	0	3 us
	5us	1	5 us
	10us	2	10 us
	15us	3	15 us
	20us	4	20 us
	40us	5	40 us
F RW MODE			Enable differential mode
	SE	0	Single ended, PSELN will be ignored, negative input to ADC
			shorted to GND
	Diff	1	Differential
G RW BURST			Enable burst mode
	Disabled	0	Burst mode is disabled (normal operation)
	Enabled	1	Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
			samples as fast as it can, and sends the average to Data RAM.



36.11.17 CH[2].LIMIT

Address offset: 0x53C

High/low limits for event monitoring a channel

Bit r	numbe	er		31	1 30	29	28	27	7 26	5 25	5 2	4 2	3 2	2 2	1 2	0 1	9 1	8 17	7 16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	. 1	L 0
Id				В	В	В	В	В	В	В	S E	3 E	3 E	3 E	3 E	3 E	B E	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А		A A
Res	et 0x7	FFF8000		0	1	1	1	1	1	1	. 1	1 1	L 1	1 1	1 1	1	. 1	. 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0 0	(0 0
Id	RW	Field	Value Id	Va	alue	•						D	esc	rip	tio	1																		
Α	RW	LOW		[-3	327	68 1	to +	327	767]		L	ow	lev	el li	mit																		
В	RW	HIGH		[_3	327	68 t	to +	327	767	1		Н	iøh	lev	el l	imit																		

36.11.18 CH[3].PSELP

Address offset: 0x540

Input positive pin selection for CH[3]

Bit	numbe	er		31	30 2	9 :	28 2	27 :	26 2	5 2	4 2	3 22	21 2	20	19 1	L8 1	17 1	.6 1	15 2	14 1	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																													Α	A A	A	Α
Res	et 0x0	0000000		0	0	0	0	0	0 () (0 (0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						C	escr	iptio	n																		
Α	RW	PSELP									Δ	nalo	g po	siti	ve ir	npu	t ch	anı	nel													
			NC	0							Ν	lot c	onne	cte	d																	
			AnalogInput0	1							Δ	AIN0																				
			AnalogInput1	2							Δ	AIN1																				
			AnalogInput2	3							Δ	AIN2																				
			AnalogInput3	4							Δ	NIN3																				
			AnalogInput4	5							Δ	AIN4																				
			AnalogInput5	6							Δ	AIN5																				
			AnalogInput6	7							Δ	IN6																				
			AnalogInput7	8							Δ	AIN7																				
			VDD	9							٧	/DD																				
			VDDHDIV5	0x0	0D						٧	/DDH	1/5																			

36.11.19 CH[3].PSELN

Address offset: 0x544

Input negative pin selection for CH[3]

ld	A A A A A O O O
Reset 0x000000000 0 0 0 0 0 0 0 0 0 0 0 0 0	
Id RW Field Value Id Value Description	
A RW PSELN Analog negative input, enables differential channel	
NC 0 Not connected	
AnalogInput0 1 AIN0	
AnalogInput1 2 AIN1	
AnalogInput2 3 AIN2	
AnalogInput3 4 AIN3	
AnalogInput4 5 AIN4	
AnalogInput5 6 AIN5	
AnalogInput6 7 AIN6	
AnalogInput7 8 AIN7	
VDD 9 VDD	
VDDHDIV5 0x0D VDDH/5	

36.11.20 CH[3].CONFIG

Address offset: 0x548



Input configuration for CH[3]

Bit number	31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		G FEEE D C C C B B A A
Reset 0x00020000	0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value I	d Value	Description
A RW RESP		Positive channel resistor control
Bypass	0	Bypass resistor ladder
Pulldov	vn 1	Pull-down to GND
Pullup	2	Pull-up to VDD
VDD1_i	2 3	Set input at VDD/2
B RW RESN		Negative channel resistor control
Bypass	0	Bypass resistor ladder
Pulldov	vn 1	Pull-down to GND
Pullup	2	Pull-up to VDD
VDD1_2	2 3	Set input at VDD/2
C RW GAIN		Gain control
Gain1_	6 0	1/6
Gain1_	5 1	1/5
Gain1_	4 2	1/4
Gain1_	3 3	1/3
Gain1_	2 4	1/2
Gain1	5	1
Gain2	6	2
Gain4	7	4
D RW REFSEL		Reference control
Interna	0	Internal reference (0.6 V)
VDD1_4	1	VDD/4 as reference
E RW TACQ		Acquisition time, the time the ADC uses to sample the input
		voltage
3us	0	3 us
5us	1	5 us
10us	2	10 us
15us	3	15 us
20us	4	20 us
40us	5	40 us
F RW MODE		Enable differential mode
SE	0	Single ended, PSELN will be ignored, negative input to ADC
		shorted to GND
Diff	1	Differential
G RW BURST		Enable burst mode
Disable	d 0	Burst mode is disabled (normal operation)
Enabled	d 1	Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
		samples as fast as it can, and sends the average to Data RAM.

36.11.21 CH[3].LIMIT

Address offset: 0x54C

High/low limits for event monitoring a channel

Bit r	number		3	1 3	0 2	9 2	28 2	27 2	26 2	25 2	24 2	3 2	2 2	1 20	0 19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2 1	. 0
Id			В	E	3 E	3 I	В	В	В	В	В	В	3 B	В	В	В	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α Δ	А
Res	et 0x7FFF8000		0	1	L 1	1	1 :	1	1	1	1	1 :	1 1	1	. 1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
l al																																	
ıa	RW Field	Value Id	٧	alu	е							eso	ript	ion																			
A	RW Field RW LOW	Value Id			-	to	+32	276	57]				ript leve																				

36.11.22 CH[4].PSELP

Address offset: 0x550



Input positive pin selection for CH[4]

Bit number		31 30 2	9 28 27	7 26 2	5 24	23 22	21 20	0 19	18 1	7 16	15	14 13	12	11 10	9	8 7	' 6	5	4	3 2	1	0
Id																			Α .	А А	Α	Α
Reset 0x00000000		0 0 0	0 0	0 0	0 (0 0	0 0	0	0	0 0	0	0 0	0	0 0	0	0 (0	0	0	0 0	0	0
ld RW Field Va	alue Id	Value				Descri	iption	ı														
A RW PSELP						Analo	g posi	tive i	npu	t cha	nnel											
NC	C	0				Not co	onnec	ted														
An	nalogInput0	1				AIN0																
An	nalogInput1	2				AIN1																
An	nalogInput2	3				AIN2																
An	nalogInput3	4				AIN3																
An	nalogInput4	5				AIN4																
An	nalogInput5	6				AIN5																
An	nalogInput6	7				AIN6																
An	nalogInput7	8				AIN7																
VD	DD	9				VDD																
VD	DDHDIV5	0x0D				VDDH	/5															

36.11.23 CH[4].PSELN

Address offset: 0x554

Input negative pin selection for CH[4]

Bit number		31	30 29	28	3 27	26	25 2	24 2	3 22	21 2	20 1	L9 1	8 1	7 16	15	14	13 1	.2 13	10	9	8	7 6	5	4	3 2	2 1	0
Id																								Α	A A	A A	Α
Reset 0x00000000		0	0 0	0	0	0	0	0 (0 0	0	0	0 0	0	0	0	0	0	0 0	0	0	0 (0	0	0	0 0	0	0
ld RW Field	Value Id	Va	lue					D	escr	iptio	n																
A RW PSELN								Α	nalo	g ne	gati	ve ir	npu	t, er	abl	es d	iffer	enti	al ch	ann	el						
	NC	0						Ν	lot c	onne	cte	d															
	AnalogInput0	1						Α	NO.																		
	AnalogInput1	2						Α	IN1																		
	AnalogInput2	3						Α	IN2																		
	AnalogInput3	4						Α	NIN3																		
	AnalogInput4	5						Α	IN4																		
	AnalogInput5	6						Α	IN5																		
	AnalogInput6	7						Α	IN6																		
	AnalogInput7	8						А	IN7																		
	VDD	9						٧	'DD																		
	VDDHDIV5	0x	0D					٧	/DDH	/5																	

36.11.24 CH[4].CONFIG

Address offset: 0x558

Input configuration for CH[4]

Bit I	numbe	er		31	30 2	29	28 2	27 2	26 2		24 2 G	3 22	21	20 :			17 : E		15 :	14 1		2 11		9 C	8	7	Ŭ	5 · B	4 3 R	2	1 0 A A
	et 0x0	0020000		0	0	0	0	0	0	0		0 0	0	0	0	0	1	0	0	0	0 (0	0	0	0	0	0		0 0	0	0 0
Id	RW	Field	Value Id	Va	lue						C	escr	iptic	on																	
Α	RW	RESP									Р	ositi	ve cl	han	nel	res	isto	r c	ont	rol											
			Bypass	0							В	ypas	s re	sisto	or la	add	er														
			Pulldown	1							P	ull-d	own	to	GN	D															
			Pullup	2							P	ull-u	p to	VD	D																
			VDD1_2	3							S	et in	put	at V	DD,	/2															
В	RW	RESN									Ν	legat	ive	chai	nne	l re	sist	or	con	trol											
			Bypass	0							В	ypas	s re	sisto	or la	add	er														
			Pulldown	1							P	ull-d	own	to	GN	D															
			Pullup	2							Р	ull-u	p to	VD	D																
			VDD1_2	3							S	et in	put	at V	DD,	/2															
			Pulldown Pullup	1							P P	ull-d ull-u	own p to	to VD	GN D	D	Ci														



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		G	FEEE DCCC BB AA
Reset 0x00020000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
C RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
	Gain4	7	4
D RW REFSEL			Reference control
	Internal	0	Internal reference (0.6 V)
	VDD1_4	1	VDD/4 as reference
E RW TACQ			Acquisition time, the time the ADC uses to sample the input
			voltage
	3us	0	3 us
	5us	1	5 us
	10us	2	10 us
	15us	3	15 us
	20us	4	20 us
	40us	5	40 us
F RW MODE			Enable differential mode
	SE	0	Single ended, PSELN will be ignored, negative input to ADC
			shorted to GND
	Diff	1	Differential
G RW BURST			Enable burst mode
	Disabled	0	Burst mode is disabled (normal operation)
	Enabled	1	Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
			samples as fast as it can, and sends the average to Data RAM.

36.11.25 CH[4].LIMIT

Address offset: 0x55C

High/low limits for event monitoring a channel

Bit r	number		3	1 3	0 2	9 2	28 2	27 2	26 2	25 2	24 2	3 2	2 2	1 20	0 19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2 1	. 0
Id			В	E	3 E	3 I	В	В	В	В	В	В	3 B	В	В	В	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α Δ	А
Res	et 0x7FFF8000		0	1	L 1	1	1 :	1	1	1	1	1 :	1 1	1	. 1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
l al																																	
ıa	RW Field	Value Id	Value [-32768 to +32767]							eso	ript	ion																					
A	RW Field RW LOW	Value Id			-	to	+32	276	57]				ript leve																				

36.11.26 CH[5].PSELP

Address offset: 0x560

Input positive pin selection for CH[5]

Bit	numbe	er		31	L 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9 8	7	6	5	4	3	2	1 0
Id																														Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							De	escr	ipti	on																		
Α	RW	PSELP										Ar	nalo	g p	osit	ive	inp	ut	cha	nne	el												
			NC	0								No	ot c	onn	ect	ed																	
			AnalogInput0	1								ΑI	N0																				
			AnalogInput1	2								ΑI	N1																				
			AnalogInput2	3								ΑI	N2																				
Α	RW	PSELP	AnalogInput0 AnalogInput1	1								AI AI	ot c N0 N1	•			inp	ut	cha	nne	el												



Bit number		31 3	0 29	28	27	26 2	5 24	1 23	22	21 2	0 1	.9 18	3 17	16	15	14 1	L3 1	2 1:	1 10	9	8	7	6 5	4	3	2	1 0
Id																								Α	Α	Α	A A
Reset 0x00000000		0 (0 0	0	0	0 0	0	0	0	0 (0 (0 0	0	0	0	0	0 (0	0	0	0	0	0 0	0	0	0	0 0
Id RW Field	Value Id	Valu	e					De	scrip	ptio	n																
	AnalogInput3	4						All	N3																		
	AnalogInput4	5						All	N4																		
	AnalogInput5	6						All	N5																		
	AnalogInput6	7						All	N6																		
	AnalogInput7	8						All	N7																		
	VDD	9						VD	D																		
	VDDHDIV5	0x0E)					VD	DH/	′ 5																	

36.11.27 CH[5].PSELN

Address offset: 0x564

Input negative pin selection for CH[5]

Bit number		31 30	29	28 2	7 2	26 25	5 24	1 23 2	2 21	. 20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	_		3 2		0
Id																										Α /	4 A	. A	Α
Reset 0x00000000		0 0	0	0 (0	0 0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id RW Field	Value Id	Value						Desc	ripti	on																			
A RW PSELN								Anal	og n	ega	tive	inp	ut,	en	able	es d	iffe	ren	tial	cha	ınn	el							
	NC	0						Not o	conn	ect	ed																		
	AnalogInput0	1						AIN0	1																				
	AnalogInput1	2						AIN1																					
	AnalogInput2	3						AIN2																					
	AnalogInput3	4						AIN3																					
	AnalogInput4	5						AIN4																					
	AnalogInput5	6						AIN5																					
	AnalogInput6	7						AIN6	i																				
	AnalogInput7	8						AIN7																					
	VDD	9						VDD																					
	VDDHDIV5	0x0D						VDD	H/5																				

36.11.28 CH[5].CONFIG

Address offset: 0x568

Input configuration for CH[5]

E E E D C C C B B A A
$\begin{smallmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 &$
resistor control
adder
ID
0/2
el resistor control
adder
ID
0/2



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		G FEEE D C C C B B A .
Reset 0x00020000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	Gain1	5 1
	Gain2	6 2
	Gain4	7 4
D RW REFSEL		Reference control
	Internal	0 Internal reference (0.6 V)
	VDD1_4	1 VDD/4 as reference
E RW TACQ		Acquisition time, the time the ADC uses to sample the input
		voltage
	3us	0 3 us
	5us	1 5 us
	10us	2 10 us
	15us	3 15 us
	20us	4 20 us
	40us	5 40 us
F RW MODE		Enable differential mode
	SE	0 Single ended, PSELN will be ignored, negative input to ADC
		shorted to GND
	Diff	1 Differential
G RW BURST		Enable burst mode
	Disabled	0 Burst mode is disabled (normal operation)
	Enabled	1 Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
		samples as fast as it can, and sends the average to Data RAM.

36.11.29 CH[5].LIMIT

Address offset: 0x56C

High/low limits for event monitoring a channel

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	B B B B B B B B B B B B B	B
Reset 0x7FFF8000	0 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description	
A RW LOW	[-32768 to +32767] Low level limit	
B RW HIGH	[-32768 to +32767] High level limit	

36.11.30 CH[6].PSELP

Address offset: 0x570

Input positive pin selection for CH[6]

Bit r	iumbe	er		31	30 29	2	8 27	26	25	24	23 2	2 2	1 20	19	18	17	16	15	14	13	12	11 1	9	8	7	6	5	4	3	2 1	. 0
Id																												Α	A	А Д	A
Res	et 0x0	0000000		0	0 0	C	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	tion																		
Α	RW	PSELP									Ana	log _l	oosit	ive	inp	ut c	har	nne	I												
			NC	0							Not	con	nect	ed																	
			AnalogInput0	1							AIN)																			
			AnalogInput1	2							AIN	1																			
			AnalogInput2	3							AIN:	2																			
			AnalogInput3	4							AIN:	3																			
			AnalogInput4	5							AIN	4																			
			AnalogInput5	6							AIN:	5																			
			AnalogInput6	7							AIN	5																			
			AnalogInput7	8							AIN	7																			
			VDD	9							VDD)																			



Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 3	17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id					$A \; A \; A \; A \; A$
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
	VDDHDIV5	0x0D	VDDH/5		

36.11.31 CH[6].PSELN

Address offset: 0x574

Input negative pin selection for CH[6]

Bit	numb	er		31	30 2	9 2	28 2	7 2	26 25	5 24	23 2	2 21 2	20 :	19 1	8 17	16	15	14	13 1	2 11	10	9	8	7	6 5	4	3	2	1 0
Id																										Α	Α	Α .	А А
Res	et 0x0	0000000		0	0	0	0 (0	0 0	0	0 0	0	0	0 0	0	0	0	0	0 (0	0	0	0 (כ	0 0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						Desc	riptio	n																
Α	RW	PSELN									Anal	og neg	gati	ive ir	put	, en	able	s di	iffer	entia	l ch	ann	el						
			NC	0							Not o	onne	cte	d															
			AnalogInput0	1							AIN0																		
			AnalogInput1	2							AIN1																		
			AnalogInput2	3							AIN2																		
			AnalogInput3	4							AIN3																		
			AnalogInput4	5							AIN4																		
			AnalogInput5	6							AIN5																		
			AnalogInput6	7							AIN6																		
			AnalogInput7	8							AIN7																		
			VDD	9							VDD																		
			VDDHDIV5	0x	0D						VDDI	1 /5																	

36.11.32 CH[6].CONFIG

Address offset: 0x578

Input configuration for CH[6]

Bitı	numbe	er		31 30	29 28	27 2	26 25	24 2	23 2	2 21	20 1	L9 1	.8 17	16	15	14 13	3 12	11 1	.0 9	8	7	6	5 4	1 3	2	1 0
Id								G			F	ı	E E	Ε			D		СС	С			ВЕ	3		A A
Res	et 0x0	0020000		0 0	0 0	0	0 0	0	0 0	0 0	0	0 (0 1	0	0	0 0	0	0	0 0	0	0	0	0 (0	0	0 0
Id	RW	Field	Value Id	Value					Desc	cripti	on															
Α	RW	RESP						F	Posit	tive o	hanı	nel r	resist	tor c	ont	rol										
			Bypass	0				E	Вура	ass re	esisto	r la	dder													
			Pulldown	1				F	Pull-	dow	n to (GNE)													
			Pullup	2				F	Pull-	up to	VDI)														
			VDD1_2	3				5	Set ii	nput	at V	DD/	2													
В	RW	RESN						١	Nega	ative	char	nel	resi	stor	con	trol										
			Bypass	0				E	Вура	ass re	esisto	r la	dder													
			Pulldown	1				F	Pull-	dow	n to (GNE)													
			Pullup	2				F	Pull-	up to	VDI)														
			VDD1_2	3				5	Set ii	nput	at V	DD/	2													
С	RW	GAIN						(Gain	con	trol															
			Gain1_6	0				1	1/6																	
			Gain1_5	1				1	1/5																	
			Gain1_4	2				1	1/4																	
			Gain1_3	3				1	1/3																	
			Gain1_2	4				1	1/2																	
			Gain1	5				1	1																	
			Gain2	6				2	2																	
			Gain4	7				4	4																	
D	RW	REFSEL						F	Refe	renc	e cor	ntro	I													
			Internal	0				- 1	nter	rnal r	efer	ence	e (0.6	5 V)												
			VDD1_4	1				١	VDD,	/4 as	refe	ren	ce													



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		G FEEE D CCC BB A
Reset 0x00020000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
Id RW Field	Value Id	Value Description
E RW TACQ		Acquisition time, the time the ADC uses to sample the input
		voltage
	3us	0 3 us
	5us	1 5 us
	10us	2 10 us
	15us	3 15 us
	20us	4 20 us
	40us	5 40 us
F RW MODE		Enable differential mode
	SE	0 Single ended, PSELN will be ignored, negative input to ADC
		shorted to GND
	Diff	1 Differential
G RW BURST		Enable burst mode
	Disabled	0 Burst mode is disabled (normal operation)
	Enabled	1 Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
		samples as fast as it can, and sends the average to Data RAM.

36.11.33 CH[6].LIMIT

Address offset: 0x57C

High/low limits for event monitoring a channel

Bit	numb	er		31	L 30	29	28	27	7 26	25	24	23	22	21 :	20 :	19 :	18 1	17 1	.6 1	L5 1	14 :	13	12 :	11	10	9	8	7	6	5	4	3	2 1	L 0
Id				В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В.	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	A /	A A
Res	et 0x7	7FFF8000		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	alue							De	scri	ptio	n																			
Α	RW	LOW		[-3	3276	8 t	0 +	327	767]			Lov	v le	vel	limi	t																		,
									767]				th le																					

36.11.34 CH[7].PSELP

Address offset: 0x580

Input positive pin selection for CH[7]

•	•		Ċ																															
Bitı	numbe	er					31	30	29	28 2	27 2	26 2	5 24	1 23	22	21 2	0 1	9 18	8 17	16	15	14 1	13 1	2 11	10	9	8	7	6	5 4	4 3	3 2	1	0
Id																														,	A A	A A	Α	Α
Res	et 0x0	0000000					0	0	0	0	0	0 0	0	0	0	0 () (0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 (0	0	0
Id	RW	Field			Value Id		Va	lue						De	scri	ptior	1																	
Α	RW	PSELP												An	alog	pos	itiv	e in	put	cha	nne	I												
					NC		0							No	t co	nned	tec	ł																
					AnalogInp	ut0	1							ΑI	١0																			
					AnalogInp	ut1	2							ΑI	٧1																			
					AnalogInp	ut2	3							ΑI	٧2																			
					AnalogInp	ut3	4							ΑI	٧3																			
					AnalogInp	ut4	5							ΑI	٧4																			
					AnalogInp	ut5	6							ΑI	N 5																			
					AnalogInp	ut6	7							ΑI	۱6																			
					AnalogInp	ut7	8							ΑI	٧7																			
					VDD		9							VD	D																			
					VDDHDIV5	5	0x0	DC						VD	DH/	′ 5																		

36.11.35 CH[7].PSELN

Address offset: 0x584

Input negative pin selection for CH[7]



Bit r	numbe	r		31	30 2	9 2	8 27	7 26	25	24	23 22	2 21	20	19 1	18 1	17 1	6 1	5 14	13	12	11	10 9	8	3 7	6	5	4	3 2	2 1	0
Id																											Α .	Α /	A A	. A
Res	et 0x0	0000000		0	0 () (0 0	0	0	0	0 0	0	0	0	0	0 () (0	0	0	0	0 0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue						Desc	riptio	on																	
Α	RW	PSELN									Analo	og ne	egat	ive i	inpı	ut, e	nal	oles	diff	erer	itial	chan	ne	I						
			NC	0							Not c	onn	ecte	ed																
			AnalogInput0	1							AIN0																			
			AnalogInput1	2							AIN1																			
			AnalogInput2	3							AIN2																			
			AnalogInput3	4							AIN3																			
			AnalogInput4	5							AIN4																			
			AnalogInput5	6							AIN5																			
			AnalogInput6	7							AIN6																			
			AnalogInput7	8							AIN7																			
			VDD	9							VDD																			
			VDDHDIV5	0x	0D						VDDI	1/5																		

36.11.36 CH[7].CONFIG

Address offset: 0x588

Input configuration for CH[7]

Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
d			G F E E E D C C C B B A A
Reset 0x00020000			0000000001000000000000000000000
ld RW Field	Value Id	Value	Description
A RW RESP			Positive channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
B RW RESN			Negative channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
C RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
D DW DEECE	Gain4	7	4
D RW REFSEL	laternal	0	Reference control
	Internal	0	Internal reference (0.6 V)
F DW TACO	VDD1_4	1	VDD/4 as reference
E RW TACQ			Acquisition time, the time the ADC uses to sample the input voltage
	3us	0	3 us
	5us	1	5 us
	10us	2	10 us
	15us	3	15 us
	20us	4	20 us
	40us	5	40 us
F RW MODE			Enable differential mode
	SE	0	Single ended, PSELN will be ignored, negative input to ADC
	32	ŭ	shorted to GND



Bit	numbe	er		31	1 30	29	28	3 27	26	25	24	23	22	21	20 :	19	18	17	16	15	14 1	13 :	L2 1	1 10	9	8	7	6	5	4	3	2	1	0
Id											G				F		Ε	Ε	Ε				D	С	С	С			В	В			Α	Α
Res	et 0x0	00020000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																			
			Diff	1								Dif	fere	nti	al																			
G	RW	BURST										Ena	able	bu	rst	mo	de																	
			Disabled	0								Bui	rst r	noc	de is	dis	ab	led	(nc	rm	al o	oer	atio	n)										
			Enabled	1								Bui	rst r	noc	de is	s en	abl	ed.	SA	ADO	C tal	ces	2^C	VEF	SAN	ИPL	Εn	uml	ber	of				
												sar	nple	es a	s fa	st a	s it	cai	n, a	nd:	sen	ds t	he a	ver	age	to D	ata	RA	M.					

36.11.37 CH[7].LIMIT

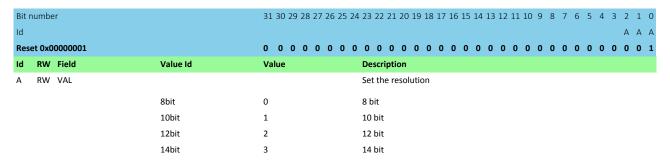
Address offset: 0x58C

High/low limits for event monitoring a channel

Bit r	umber		3:	1 30	29	28	27	26	25	24 :	23 :	22 2	1 2	0 19	18	17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5	4	3	2 1	1 0
Id			В	В	В	В	В	В	В	В	В	ВЕ	3 E	3 B	В	В	В	Α	Α	Α.	A 4	A	Α	Α	Α	Α	Α	Α	Α /	A A	A A
Rese	et 0x7FFF800		0	1	1	1	1	1	1	1	1	1 1	L 1	l 1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	DVA/ Et-1-1	Value Id	W	alue							D	crip	tion																		
	RW Field	value lu	•	aiuc							Des	crip	LIUI	•																	
A	RW LOW	value lu		327		to +3	327	767]				lev																			

36.11.38 RESOLUTION

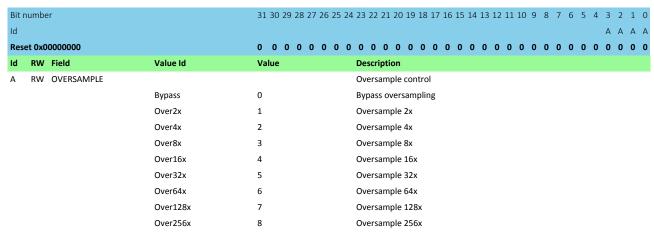
Address offset: 0x5F0
Resolution configuration



36.11.39 OVERSAMPLE

Address offset: 0x5F4

Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.





36.11.40 SAMPLERATE

Address offset: 0x5F8

Controls normal or continuous sample rate

Bitı	numbe	er		31 3	30 2	9 28	3 27	26	25	24	23 2	22 2	21 2	0 1	9 18	3 17	7 16	15	14 :	13 1	2 11	10	9	8	7	6	5 4	4 3	2	1	0
Id																				E		Α	Α	Α	Α	Α.	A A	4 Α	A	Α	Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Valu	ıe						Des	crip	tio	1																	
Α	RW	CC		[80.	.204	7]					Cap	ture	e an	d co	mp	are	valı	ue. S	Sam	ple i	ate	s 16	М	Hz/	CC						
В	RW	MODE									Sele	ct r	nod	e fo	r sa	mp	le ra	ate o	cont	rol											
			Task	0							Rate	e is	con	trol	led '	fror	n SA	MP	LE t	ask											
			Timers	1							Rate	e is	con	trol	led	fror	n lo	cal t	ime	r (us	e CC	to	con	trol	the	rat	te)				

36.11.41 RESULT.PTR

Address offset: 0x62C

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW PTR		Data pointer

36.11.42 RESULT.MAXCNT

Address offset: 0x630

Maximum number of buffer words to transfer

Bit	numb	er		31	30 2	9 2	8 2	7 26	25	24	23	22 :	21 :	20 :	19 1	8 1	7 1	6 15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id																			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Res	et 0x0	0000000		0	0 () (0 0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 1 A A A O O O O O O O O O O O O O O O O																												
Α	RW	MAXCNT									Ma	xim	um	nu	mbe	er o	f bu	ffer	wo	rds	to t	ran	sfer									

36.11.43 RESULT.AMOUNT

Address offset: 0x634

Number of buffer words transferred since last START

Bit r	numbe	r		31	30	29	28	27	26 :	25 2	24 2	23 2	2 2	1 2	0 1	9 1	8 1	7 1	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 A	Α	Α															
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 (0 () (0 () (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	tio	n																		
Α	R	AMOUNT									ı	lun	nbe	r of	bu	ffer	wc	rds	trai	nsfe	rre	d sir	ice	last	ST	ART	. т	his					

register can be read after an END or STOPPED event.

36.12 Electrical specification

36.12.1 SAADC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
DNL	Differential non-linearity, 10-bit resolution	-0.95	<1		LSB
INL	Integral non-linearity, 10-bit resolution		1		LSB
V _{OS}	Differential offset error (calibrated), 10-bit resolution ^a		+-2		LSB
E _{VDDHDIV5}	Error on VDDHDIV5 input		+-1		%

^a Digital output code at zero volt differential input.



Symbol	Description	Min.	Тур.	Max.	Units
C _{EG}	Gain error temperature coefficient		0.02		%/°C
f _{SAMPLE}	Maximum sampling rate			200	kHz
t _{ACQ,10k}	Acquisition time (configurable), source Resistance <= 10kOhm		3		μs
t _{ACQ,40k}	Acquisition time (configurable), source Resistance <= 40kOhm		5		μs
t _{ACQ,100k}	Acquisition time (configurable), source Resistance <= 100kOhm		10		μs
t _{ACQ,200k}	Acquisition time (configurable), source Resistance <= 200kOhm		15		μs
t _{ACQ,400k}	Acquisition time (configurable), source Resistance <= 400kOhm		20		μs
t _{ACQ,800k}	Acquisition time (configurable), source Resistance <= 800kOhm		40		μs
t _{CONV}	Conversion time		<2		μs
I _{ADC,CONV}	ADC current during ACQuisition and CONVersion		700		μΑ
I _{ADC,IDLE}	Idle current, when not sampling, excluding clock sources and regulator base currents ³⁰		<5		μΑ
E _{G1/6}	Error ^b for Gain = 1/6	-3		3	%
E _{G1/4}	Error ^b for Gain = 1/4	-3		3	%
E _{G1/2}	Error ^b for Gain = 1/2	-3		4	%
E _{G1}	Error ^b for Gain = 1	-3		4	%
C _{SAMPLE}	Sample and hold capacitance at maximum gain ³¹		2.5		pF
R _{INPUT}	Input resistance		>1		ΜΩ
E _{NOB}	Effective number of bits, differential mode, 12-bit resolution,		9		Bit
	1/1 gain, 3 μs acquisition time, crystal HFCLK, 200 ksps				
S _{NDR}	Peak signal to noise and distortion ratio, differential mode, 12-		56		dB
	bit resolution, 1/1 gain, 3 μs acquisition time, crystal HFCLK, 200				
	ksps				
S _{FDR}	Spurious free dynamic range, differential mode, 12-bit		70		dBc
	resolution, 1/1 gain, 3 μs acquisition time, crystal HFCLK, 200				
	ksps				
R _{LADDER}	Ladder resistance		160		kΩ

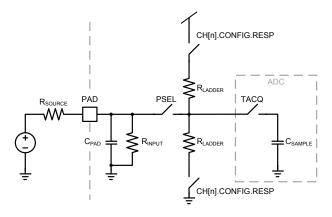


Figure 114: Model of SAADC input (one channel)

Note: SAADC average current calculation for a given application is based on the sample period, conversion and acquisition time (t_{conv} and t_{ACQ}) and conversion and idle current ($t_{ADC,CONV}$). For example, sampling at 4kHz gives a sample period of 250µs. The average current consumption would then be:

$$I_{AVERAGE} = \left(\frac{\left(t_{CONV} + t_{ACQ}\right)}{250}\right) \left(I_{ADC,CONV}\right) + \left(\frac{250 - \left(t_{CONV} + t_{ACQ}\right)}{250}\right) \left(I_{ADC,IDLE}\right)$$

When t_{ACQ} is 10us or longer, and if DC/DC is active, it will be allowed to work in refresh mode if no other resource is requiring a high quality power supply from 1V3. If t_{ACQ} is smaller than 10us and DC/DC is active, refresh mode will not be allowed, and it will remain in normal mode from the START task to the STOPPED event. So depending on t_{ACQ} and other resources' needs, the appropriate base current needs to be taken into account.

^b Does not include temperature drift

³¹ Maximum gain corresponds to highest capacitance.



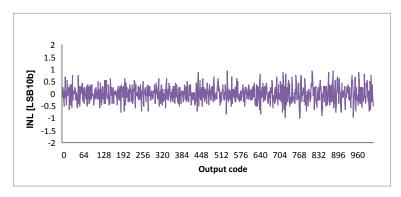


Figure 115: ADC INL vs Output Code

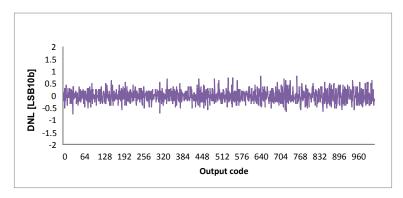


Figure 116: ADC DNL vs Output Code

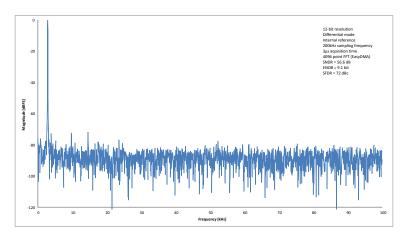


Figure 117: FFT of a 2.8 kHz sine at 200 ksps ()

36.13 Performance factors

Clock jitter, affecting sample timing accuracy, and circuit noise can affect ADC performance.

Jitter can be between START tasks or from START task to acquisition. START timer accuracy and startup times of regulators and references will contribute to variability. Sources of circuit noise may include CPU activity and the DC/DC regulator. Best ADC performance is achieved using START timing based on the TIMER module, HFXO clock source, and Constant Latency mode.



37 COMP — Comparator

The comparator (COMP) compares an input voltage (VIN+) against a second input voltage (VIN-). VIN+ can be derived from an analog input pin (AIN0-AIN7). VIN- can be derived from multiple sources depending on the operation mode of the comparator.

Main features of the comparator are:

- Input range from 0 V to VDD
- Single-ended mode
 - · Fully flexible hysteresis using a 64-level reference ladder
- Differential mode
 - Configurable 50 mV hysteresis
- Reference inputs (VREF):
 - VDD
 - External reference from AIN0 to AIN7 (between 0 V and VDD)
 - Internal references 1.2 V, 1.8 V and 2.4 V
- Three speed/power consumption modes: low-power, normal and high-speed
- Single-pin capacitive sensor support
- · Event generation on output changes
 - UP event on VIN- > VIN+
 - DOWN event on VIN- < VIN+
 - · CROSS event on VIN+ and VIN- crossing
 - · READY event on core and internal reference (if used) ready

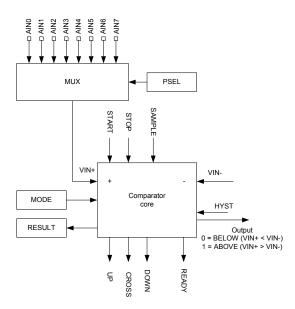


Figure 118: Comparator overview

Once enabled (using the *ENABLE* register), the comparator is started by triggering the START task and stopped by triggering the STOP task. After a start-up time of $t_{COMP,START}$, the comparator will generate a READY event to indicate that it is ready for use and that its output is correct. When the COMP module is started, events will be generated every time VIN+ crosses VIN-.



37 Operation modes

The comparator can be configured to operate in two main operation modes, differential mode and single-ended mode. See the *MODE* register for more information. In both operation modes, the comparator can operate in different speed and power consumption modes (low-power, normal and high-speed). High-speed mode will consume more power compared to low-power mode, and low-power mode will result in slower response time compared to high-speed mode.

Use the *PSEL* register to select any of the AIN0-AIN7 pins as VIN+ input, irregardless of the operation mode selected for the comparator. The source of VIN- depends on which operation mode is used:

- Differential mode: Derived directly from AIN0 to AIN7
- Single-ended mode: Derived from VREF. VREF can be derived from VDD, AIN0-AIN7 or internal 1.2 V, 1.8 V and 2.4 V references.

The selected analog pins will be acquired by the comparator once it is enabled.

An optional hysteresis on VIN+ and VIN- can be enabled when the module is used in differential mode through the *HYST* register. In single-ended mode, VUP and VDOWN thresholds can be set to implement a hysteresis using the reference ladder (see *Figure 121: Comparator in single-ended mode* on page 456). This hysteresis is in the order of magnitude of 50 mV, and shall prevent noise on the signal to create unwanted events. See *Figure 122: Hysteresis example where VIN+ starts below VUP* on page 456 for illustration of the effect of an active hysteresis on a noisy input signal.

An upward crossing will generate an UP event and a downward crossing will generate a DOWN event. The CROSS event will be generated every time there is a crossing, independent of direction.

The immediate value of the comparator can be sampled to *RESULT* register by triggering the SAMPLE task.

37.1 Differential mode

In differential mode, the reference input VIN- is derived directly from one of the AINx pins.

Before enabling the comparator via the *ENABLE* register, the following registers must be configured for the differential mode:

- PSEL
- MODE
- EXTREFSEL

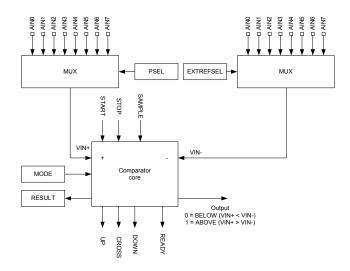


Figure 119: Comparator in differential mode



Restriction: Depending on the device, not all the analog inputs may be available for each MUX. See definitions for *PSEL* and *EXTREFSEL* for more information about which analog pins are available on a particular device.

When *HYST* register is turned on while in this mode, the output of the comparator (and associated events) will change from ABOVE to BELOW whenever VIN+ becomes lower than VIN- - (V_{DIFFHYST} / 2). It will also change from BELOW to ABOVE whenever VIN+ becomes higher than VIN- + (V_{DIFFHYST} / 2). This behavior is illustrated in *Figure 120: Hysteresis enabled in differential mode* on page 455.

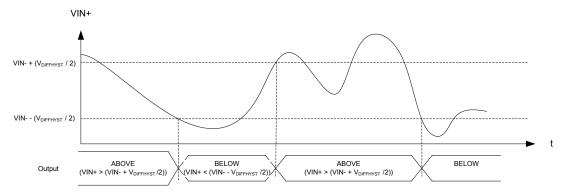


Figure 120: Hysteresis enabled in differential mode

37.2 Single-ended mode

In single-ended mode, VIN- is derived from the reference ladder.

Before enabling the comparator via the *ENABLE* register, the following registers must be configured for the single-ended mode:

- PSEL
- MODE
- REFSEL
- EXTREFSEL
- TH

The reference ladder uses the reference voltage (VREF) to derive two new voltage references, VUP and VDOWN. VUP and VDOWN are configured using THUP and THDOWN respectively in the *TH* register. VREF can be derived from any of the available reference sources, configured using the *EXTREFSEL* and *REFSEL* registers as illustrated in *Figure 121: Comparator in single-ended mode* on page 456. When AREF is selected in the *REFSEL* register, the *EXTREFSEL* register is used to select one of the AIN0-AIN7 analog input pins as reference input. The selected analog pins will be acquired by the comparator once it is enabled.



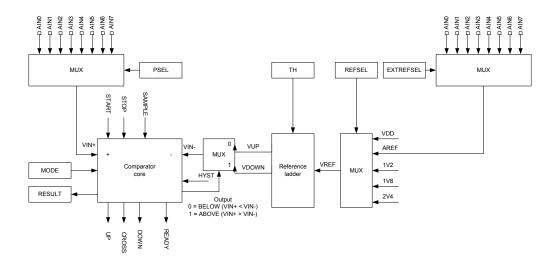


Figure 121: Comparator in single-ended mode

Restriction: Depending on the device, not all the analog inputs may be available for each MUX. See definitions for *PSEL* and *EXTREFSEL* for more information about which analog pins are available on a particular device.

When the comparator core detects that VIN+ > VIN-, i.e. ABOVE as per the *RESULT* register, VIN- will switch to VDOWN. When VIN+ falls below VIN- again, VIN- will be switched back to VUP. By specifying VUP larger than VDOWN, a hysteresis can be generated as illustrated in *Figure 122: Hysteresis example where VIN+ starts below VUP* on page 456 and *Figure 123: Hysteresis example where VIN+ starts above VUP* on page 457.

Writing to HYST has no effect in single-ended mode, and the content of this register is ignored.

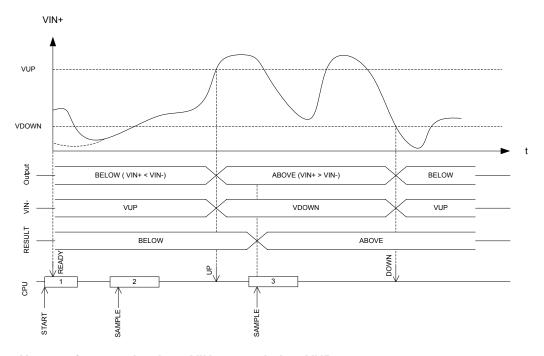


Figure 122: Hysteresis example where VIN+ starts below VUP



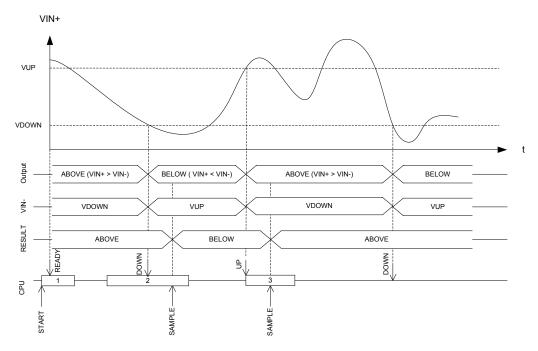


Figure 123: Hysteresis example where VIN+ starts above VUP

37.3 Registers

Table 83: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40013000	COMP	COMP	General purpose comparator		

Table 84: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start comparator
TASKS_STOP	0x004	Stop comparator
TASKS_SAMPLE	0x008	Sample comparator value
EVENTS_READY	0x100	COMP is ready and output is valid
EVENTS_DOWN	0x104	Downward crossing
EVENTS_UP	0x108	Upward crossing
EVENTS_CROSS	0x10C	Downward or upward crossing
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RESULT	0x400	Compare result
ENABLE	0x500	COMP enable
PSEL	0x504	Pin select
REFSEL	0x508	Reference source select for single-ended mode
EXTREFSEL	0x50C	External reference select
TH	0x530	Threshold configuration for hysteresis unit
MODE	0x534	Mode configuration
HYST	0x538	Comparator hysteresis enable

37.3.1 SHORTS

Address offset: 0x200



Shortcut register

Bit	numbe	er		31 3	0 29	9 28	27	26	25 2	24 23	3 2	2 21	1 20	19	18	17	16	15 1	L4 1	13 1	2 1	1 10	9	8	7	6	5 .	4 3	2	1	0
Id																												E C	С	В	Α
Res	et 0x0	0000000		0 (0	0	0	0	0	0 0	0 (0 0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Valu	e					D	esc	cript	ion																		
Α	RW	READY_SAMPLE								Sł	hor	tcut	be	twe	en l	REA) YC	ever	nt a	nd S	ΑN	IPLE	tas	k							
										Se	ee l	EVEI	NTS	RE	AD	Y an	d <i>T</i> ,	4 <i>5K</i> .	s_s.	AM.	PLE										
			Disabled	0						D	isal	ble s	shor	rtcu	t																
			Enabled	1						Er	nab	ole s	hor	tcut	t																
В	RW	READY_STOP								Sł	hor	tcut	be	twe	en l	REA) YC	ever	nt a	nd S	то	P ta	sk								
										Se	ee l	EVEI	NTS	_RE	AD	Y an	d T ,	4 <i>5K</i> .	s_s	TOF											
			Disabled	0						D	isal	ble s	shor	tcu	t																
			Enabled	1						Er	nab	ole s	hor	tcut	t																
С	RW	DOWN_STOP								Sł	hor	tcut	be	twe	en l	DOV	/N	eve	nt a	nd :	то	P ta	sk								
										Se	ee l	EVEI	NTS	DO	วพเ	V an	d <i>T</i> .	ASK	s_s	TOF	,										
			Disabled	0						D	isal	ble s	shor	rtcu	t																
			Enabled	1						Er	nab	ole s	hor	tcut	t																
D	RW	UP_STOP								Sł	hor	tcut	be	twe	en I	UP e	ver	nt ar	nd S	тоі	ta:	sk									
										Se	ee l	EVEI	NTS	UF	an	d TA	SK.	s_ <i>s</i> 1	ΌΡ												
			Disabled	0						D	isal	ble s	shor	rtcu	t																
			Enabled	1						Er	nab	ole s	hor	tcut	t																
Ε	RW	CROSS_STOP								Sł	hor	tcut	be	twe	en (CRO:	SS 6	ever	ıt a	nd S	то	P ta	sk								
										Se	ee l	EVEI	NTS	_CR	205	s and	d T /	4 <i>5K</i> 5	5_5	ТОР											
			Disabled	0								ble s							_												
			Enabled	1						Er	nab	ole s	hor	tcut	t																

37.3.2 INTEN

Address offset: 0x300

Enable or disable interrupt

numb	er		31	. 30	29	28	27 :	26 2	5 2	4 2	3 22	2 21	20	19	18	17	16	15	14 1	13 1	2 11	. 10	9	8	7 (5 5	4	3	2	1 0
																												D	С	ВА
et 0x0	0000000		0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0 (0	0	0	0	0 0
RW	Field	Value Id	Va	lue						D	esci	ripti	on																	
RW	READY									Er	nabl	le oi	dis	abl	e in	terr	up	t fo	RE	ADY	eve	nt								
										ç,	00 F	VEN	ITC	DE	ΛDV	,														
			_										113_		וטר															
		Disabled	0																											
		Enabled	1							Eı	nab	le																		
RW	DOWN									Er	nabl	le oi	dis	abl	e in	terr	up	t fo	DC.	NW	eve	nt								
										Se	ee <i>E</i>	VEN	ITS_	DO	W٨	ı														
		Disabled	0							D	isab	le																		
		Enabled	1							Er	nabl	le																		
RW	UP									Er	nabl	le oi	dis	abl	e in	terr	up	t fo	· UF	eve	nt									
										Se	ee E	VEN	ITS_	UP																
		Disabled	0							D	isab	le																		
		Enabled	1							Er	nabl	le																		
RW	CROSS									Er	nabl	le oi	dis	abl	e in	terr	up	t fo	CR	oss	eve	nt								
										Se	op F	VFN	ITS	CRI	oss															
		Disabled	0																											
		Enabled	1							Eı	nabl	le																		
	RW RW	RW Field RW READY RW UP	et 0x000000000 RW Field Value Id RW READY Disabled Enabled RW DOWN Disabled Enabled RW UP Disabled Enabled	Page Page	Page Page	RW Field Value Id Value RW Field Value Id Value	RW Field Value Id Value RW Field Value Id Value RW READY	RW Field Value Id Value Valu	RW Field Value Id Value RW Field Value Id Value RW READY Disabled Disab	Pet Ox000000000	RW Field Value Id Value RW READY Disabled 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	### Provided No. 0	### Pield Value Id Value Description	### Pield Value Id Value Description	RW Field Value Id Value Value Pescription	RW READY Disabled Disable Enabled RW UP Disabled Disabled	RW Field Value Id Value Enable or disable internations of the Company of the Comp	et 0x000000000 RW Field Value Id Value Description RW READY Disabled Enabled Disable Enable Enable Enable Disable Enable Enable	et 0x000000000 RW Field Value Id Value Description RW READY Disabled 0 Disable Enable or disable interrupt for See EVENTS_READY Disabled 0 Disable Enable or disable interrupt for See EVENTS_DOWN Disabled 0 Disable Enable Enable Disable Enable O Disable Enable Disable Enable O Disable Enable O Disable Enable Disable	et 0x000000000 RW Field Value Id Value Description RW READY Disabled 0 Disable Enable or disable interrupt for RE See EVENTS_READY Disabled 0 Disable Enable or disable interrupt for DO See EVENTS_DOWN Disabled 0 Disable Enable or disable interrupt for DO See EVENTS_DOWN Disabled 1 Enable RW UP Enable or disable interrupt for UP See EVENTS_UP Disabled 0 Disable Enable or disable interrupt for UP See EVENTS_UP Disabled 1 Enable Enable or disable interrupt for UP See EVENTS_UP Disabled 1 Enable Enable or disable interrupt for UP See EVENTS_UP Disabled 0 Disable Enable or disable interrupt for CR See EVENTS_CROSS Disabled 0 Disable	Part Part	et 0x000000000 RW Field Value Id Value Enable or disable interrupt for READY even See EVENTS_READY Disabled Enabled Disabled Enabled Disabled Enabled Disable Enable Enable	RW Field Value Id Val	RW Field Value Id Val	RW Field Value Id Value Pascription	RW Field Value Id Val	RW Field Value Id Description Id Id Id Id Id Id Id I	RW Field Value Id Value Valu	RW READY	RW Field Value Value

37.3.3 INTENSET

Address offset: 0x304



Enable interrupt

Bitı	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	READY			Write '1' to Enable interrupt for READY event
					See EVENTS_READY
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	DOWN			Write '1' to Enable interrupt for DOWN event
					See EVENTS_DOWN
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	UP			Write '1' to Enable interrupt for UP event
					See EVENTS_UP
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	CROSS			Write '1' to Enable interrupt for CROSS event
					See EVENTS_CROSS
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

37.3.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bitı	number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Res	set 0x00000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW Field Va	alue Id	Value	Description
Α	RW READY			Write '1' to Disable interrupt for READY event
				See EVENTS_READY
	Cl	lear	1	Disable
	Di	isabled	0	Read: Disabled
	Er	nabled	1	Read: Enabled
В	RW DOWN			Write '1' to Disable interrupt for DOWN event
				See EVENTS_DOWN
	Cl	lear	1	Disable
	Di	isabled	0	Read: Disabled
	Er	nabled	1	Read: Enabled
С	RW UP			Write '1' to Disable interrupt for UP event
				See EVENTS_UP
	Cl	lear	1	Disable
	Di	isabled	0	Read: Disabled
	Er	nabled	1	Read: Enabled
D	RW CROSS			Write '1' to Disable interrupt for CROSS event
				See EVENTS_CROSS
	Cl	lear	1	Disable
	Di	isabled	0	Read: Disabled
	Er	nabled	1	Read: Enabled



37.3.5 RESULT

Address offset: 0x400

Compare result

Bitı	numbe	er		33	1 30	29	28	3 27	7 26	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12 :	11 1	.0 9	8	7	6	5	4	3	2	1 0
Id				0 0 0 Value 0 1																													Α
Res	et OxC	0000000		0 0 0 0 0 0 0 Value							0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id									De	escr	ipti	on																		
Α	R	RESULT										Re	esult	t of	las	t co	mpa	are.	De	cisi	on	poir	nt S	ΑМІ	PLE	task	ί.						
			Below	Value 0								In	put	vol	tage	e is	bel	ow 1	the	thr	esh	old	(VI	N+ <	IIV >	N-)							
			Above	0 1								In	put	vol	tage	e is	abo	ve	the	thr	esh	old	(VII	V+ >	NV <	۱-)							

37.3.6 ENABLE

Address offset: 0x500

COMP enable

Bit	num	ber			3	31 3	30 2	29 2	28	27	26	5 25	5 24	4 2	3 2	2 2	21	20	19	18	17	10	5 1	.5 :	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																						Α	Α
Re	et 0	x00	000000		(0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	(0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RV	W	Field	Value Id	١	Valu	ıe							C)es	crip	otic	on																					
Α	RV	N	ENABLE											Е	nal	ole	or	dis	ab	e (O	ЛP																	
				Disabled	(0								D	Disa	ble	:																						
				Enabled	2	2								Е	nal	ole																							

37.3.7 PSEL

Address offset: 0x504

Pin select

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW PSEL	Analog pin select
AnalogInput0	0 AINO selected as analog input
AnalogInput1	1 AIN1 selected as analog input
AnalogInput2	2 AIN2 selected as analog input
AnalogInput3	3 AIN3 selected as analog input
AnalogInput4	4 AIN4 selected as analog input
AnalogInput5	5 AIN5 selected as analog input
AnalogInput6	6 AIN6 selected as analog input
AnalogInput7	7 AIN7 selected as analog input

37.3.8 REFSEL

Address offset: 0x508

Reference source select for single-ended mode

Bit	numbe	er		31	30 2	9 2	28 2	7 2	26 2	5 24	4 23	3 22	21	20	19	18	17	16	15	14	13	12 1	.1 1	0 9	8	7	6	5	4	3	2	1 0
Id																															Α	А А
Res	et 0x0	0000004		0	0 (0	0 0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	1	0 0
Id	RW	Field	Value Id	Val	ue						D	escr	iptio	on																		
Α	RW	REFSEL									Re	efer	ence	se	lect																	
			Int1V2	0							VI	REF	= int	err	nal 1	1.2	V re	efer	end	e (VDE) >=	1.7	V)								
			Int1V8	1							VI	REF	= int	err	nal 1	1.8	V re	efer	end	e (VDE) >=	VRI	F +	0.2	V)						
			Int2V4	2							VI	REF	= int	err	nal 2	2.4	V re	efer	end	e (VDE) >=	VRI	F +	0.2	V)						
			VDD	4							VI	REF	= V[D																		
			ARef	5							VI	REF	= AF	REF	(VD	D >	>= V	RE	F >=	AF	REF	ΛIN)									



37.3.9 EXTREFSEL

Address offset: 0x50C External reference select

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW EXTREFSEL		External analog reference select
	AnalogReference0	0 Use AINO as external analog reference
	AnalogReference1	1 Use AIN1 as external analog reference
	AnalogReference2	2 Use AIN2 as external analog reference
	AnalogReference3	3 Use AIN3 as external analog reference
	AnalogReference4	4 Use AIN4 as external analog reference
	AnalogReference5	5 Use AIN5 as external analog reference
	AnalogReference6	6 Use AIN6 as external analog reference
	AnalogReference7	7 Use AIN7 as external analog reference

37.3.10 TH

Address offset: 0x530

Threshold configuration for hysteresis unit

Bit number		31 30	29 28 27 26	25 24	23 22	21 20	19 1	.8 17	16 1	l5 14	1 13	12 1	1 10	9	8	7 (5 5	4	3	2 :	1 0
Id											В	В	3 B	В	В		Α	Α	Α .	A A	А А
Reset 0x00	000000	0 0	0 0 0 0	0 0	0 0	0 0	0	0 0	0	0 0	0	0	0	0	0	0 (0	0	0	0 (0 0
ld RW	Field Va	lue Id Value			Descri	ption															
A RW	THDOWN	[63:0]	l		VDOW	N = (T	HDO	WN+	1)/6	4*VF	REF										
B RW	THUP	[63:0]			VUP =	(THUP	+1)/	64*V	REF												

37.3.11 MODE

Address offset: 0x534 Mode configuration

Bit number		31	30 2	29 2	28 2	7 2	6 25	24	23	22	21 2	0 1	9 1	8 1	7 10	5 1	5 14	13	12 3	11 1	0 9	8	7	6	5	4 3	2	1	0
Id																						В						Α	Α
Reset 0x00000000		0	0	0	0 (0	0	0	0	0	0	0	0 () (0 0	C	0	0	0	0 (0	0	0	0	0	0 0	0	0	0
Id RW Field	Value Id	Val	ue						De	scri	ptio	n																	
A RW SP									Spe	eed	and	po	wer	mo	odes	;													
L	Low	0							Lov	v-p	owe	r m	ode																
1	Normal	1							No	rma	al mo	ode																	
H	High	2							Hig	gh-s	pee	m b	ode																
B RW MAIN									Ma	in c	per	atic	n m	od	es														
S	SE	0							Sin	gle-	end	ed	mod	de															
	Diff	1							Dif	fere	entia	l m	ode																

37.3.12 HYST

Address offset: 0x538

Comparator hysteresis enable

Bitı	numb	er		31	. 30	29	28	27	26	25	24	23	22 :	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α
Res	et 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	/ Field	Value Id	Va	lue							Des	crip	otic	on																			
Α	RW	HYST										Cor	npa	ırat	or l	ıys	tere	esis																
			NoHyst	0								Cor	npa	ırat	or l	nys	tere	esis	dis	able	ed													
			Hyst50mV	1								Cor	npa	ırat	or l	nys	tere	sis	ena	ble	d													
			Hyst50mV	1								Cor	npa	ırat	or l	ıys	tere	esis	ena	ıble	d													



37.4 Electrical specification

37.4.1 COMP Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{COMP,LP}	Core run current in low power mode		2		μΑ
I _{COMP,N}	Core run current in normal mode		5		μΑ
I _{COMP,HS}	Core run current in high-speed mode		10		μΑ
t _{PROPDLY,LP}	Propagation delay, low-power mode ^a		0.6		μS
t _{PROPDLY,N}	Propagation delay, normal mode ^a		0.2		μS
t _{PROPDLY,HS}	Propagation delay, high-speed mode ^a		0.1		μS
V _{DIFFHYST}	Optional hysteresis applied to differential input		30		mV
V _{VDD-VREF}	Required difference between VDD and a selected VREF, VDD >	0.3			V
	VREF				
I _{INT_REF}	Current used by the internal bandgap reference when selected		13		μΑ
	as source for VREF				
t _{INT_REF,START}	Startup time for the internal bandgap reference		50	80	μS
E _{INT_REF}	Internal bandgap reference error	-3		3	%
R _{LADDER}	Reference ladder resistance, I _{LADDER} = VREF / R _{LADDER}		550		kΩ
V _{INPUTOFFSET}	Input offset	-10		10	mV
D _{NLLADDER}	Differential non-linearity of reference ladder				LSB
t _{COMP,START}	Startup time for the comparator core		3		μS

Total comparator run current must be calculated from the I_{COMP} , I_{INT_REF} , and I_{LADDER} values for a given reference voltage.

^a Propagation delay is with 10 mV overdrive.



38 LPCOMP — Low power comparator

LPCOMP compares an input voltage against a reference voltage.

Listed here are the main features of LPCOMP:

- 0 VDD input range
- Ultra low power
- Eight input options (AINO to AIN7)
- Reference voltage options:
 - · Two external analog reference inputs, or
 - 15-level internal reference ladder (VDD/16)
- Optional hysteresis enable on input
- Wakeup source from OFF mode

In System ON, the LPCOMP can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the selected reference. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

Restriction: LPCOMP cannot be used (STARTed) at the same time as COMP. Only one comparator can be used at a time.

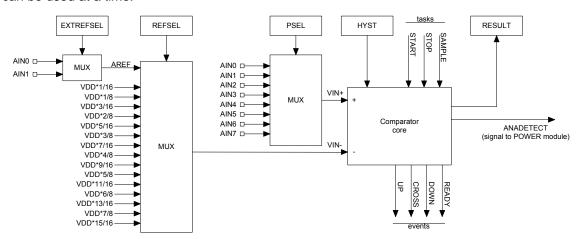


Figure 124: Low power comparator

The wakeup comparator (LPCOMP) compares an input voltage (VIN+), which comes from an analog input pin selected via the PSEL register against a reference voltage (VIN-) selected via the *REFSEL* on page 468 and *EXTREFSEL* registers.

The *PSEL*, *REFSEL*, and *EXTREFSEL* registers must be configured before the LPCOMP is enabled through the *ENABLE* register.

The *HYST* register allows enabling an optional hysteresis in the comparator core. This hysteresis shall prevent noise on the signal to create unwanted events. See *Figure 125: Effect of hysteresis on a noisy input signal* on page 464 for illustration of the effect of an active hysteresis on a noisy input signal. It is disabled by default, and shall be configured before enabling LPCOMP as well.

The LPCOMP is started by triggering the START task. After a start-up time of $t_{LPCOMP,STARTUP}$ the LPCOMP will generate a READY event to indicate that the comparator is ready to use and the output of the LPCOMP is correct. The LPCOMP will generate events every time VIN+ crosses VIN-. More specifically, every time VIN+ rises above VIN- (upward crossing) an UP event is generated along with a CROSS event. Every time VIN+ falls below VIN- (downward crossing), a DOWN event is generated along with a CROSS event. When hysteresis is enabled, the upward crossing level becomes (VIN- + VHYST/2), and the downward crossing level becomes (VIN- - VHYST/2).



The LPCOMP is stopped by triggering the STOP task.

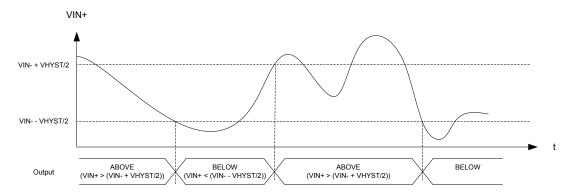


Figure 125: Effect of hysteresis on a noisy input signal

LPCOMP will be operational in both System ON and System OFF mode when it is enabled through the ENABLE register. See *POWER* — *Power supply* on page 66 for more information about power modes. Note that it is not allowed to go to System OFF when a READY event is pending to be generated.

All LPCOMP registers, including *ENABLE*, are classified as retained registers when the LPCOMP is enabled. However, when the device wakes up from System OFF, all LPCOMP registers will be reset.

The LPCOMP can wake up the system from System OFF by asserting the ANADETECT signal. The ANADETECT signal can be derived from any of the event sources that generate the UP, DOWN and CROSS events. In case of wakeup from System OFF, no events will be generated, only the ANADETECT signal. See the ANADETECT register (*ANADETECT* on page 468) for more information on how to configure the ANADETECT signal.

The immediate value of the LPCOMP can be sampled to *RESULT* on page 467 by triggering the SAMPLE task.

See *RESETREAS* on page 77 for more information on how to detect a wakeup from LPCOMP.

38.1 Shared resources

The LPCOMP shares resources with other peripherals.

The LPCOMP shares analog resources with SAADC and COMP. While it is possible to use SAADC at the same time as COMP or LPCOMP, COMP and LPCOMP are mutually exclusive: enabling one will automatically disable the other. In addition, when using SAADC and COMP or LPCOMP simultaneously, it is not possible to select the same analog input pin for both modules.

The LPCOMP peripheral shall not be disabled (by writing to the ENABLE register) before the peripheral has been stopped. Failing to do so may result in unpredictable behaviour.

38.2 Pin configuration

You can use the LPCOMP.PSEL register to select one of the analog input pins, AINO through AINO, as the analog input pin for the LPCOMP.

See *GPIO* — *General purpose input/output* on page 154 for more information about the pins. Similarly, you can use *EXTREFSEL* on page 468 to select one of the analog reference input pins, AINO and AINI, as input for AREF in case AREF is selected in *EXTREFSEL* on page 468. The selected analog pins will be acquired by the LPCOMP when it is enabled through *ENABLE* on page 467.



38.3 Registers

Table 85: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40013000	LPCOMP	LPCOMP	Low power comparator	

Table 86: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start comparator
TASKS_STOP	0x004	Stop comparator
TASKS_SAMPLE	0x008	Sample comparator value
EVENTS_READY	0x100	LPCOMP is ready and output is valid
EVENTS_DOWN	0x104	Downward crossing
EVENTS_UP	0x108	Upward crossing
EVENTS_CROSS	0x10C	Downward or upward crossing
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RESULT	0x400	Compare result
ENABLE	0x500	Enable LPCOMP
PSEL	0x504	Input pin select
REFSEL	0x508	Reference select
EXTREFSEL	0x50C	External reference select
ANADETECT	0x520	Analog detect configuration
HYST	0x538	Comparator hysteresis enable

38.3.1 SHORTS

Address offset: 0x200

Shortcut register

	ortour rogiotor			
Bit	number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E D C B A
Res	et 0x00000000		0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW Field	Value Id	Value	Description
Α	RW READY_SAMPLE			Shortcut between READY event and SAMPLE task
				See EVENTS_READY and TASKS_SAMPLE
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
В	RW READY_STOP			Shortcut between READY event and STOP task
				See EVENTS_READY and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
С	RW DOWN_STOP			Shortcut between DOWN event and STOP task
				See EVENTS_DOWN and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
D	RW UP_STOP			Shortcut between UP event and STOP task
				See EVENTS_UP and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
E	RW CROSS_STOP			Shortcut between CROSS event and STOP task
				See EVENTS_CROSS and TASKS_STOP
		Disabled	0	Disable shortcut



Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10	0 9 8 7 6 5 4 3 2 1 0
Id					E D C B A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
	Enabled	1	Enable shortcut		

38.3.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numb	er		31 3	0 29	28 2	27 2	26 25	5 24	23	22 2	21 2	20 19	9 18	3 17	16	15 1	L4 1	3 12	11	10	9	8 7	7 6	5 5	4	3	2	1 0
Id																											D	C I	ВА
Res	et 0x	0000000		0 0	0	0	0	0 0	0	0	0 (0	0 0	0	0	0	0	0 (0	0	0	0	0 () (0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	е					De	escrip	tio	n																
Α	RW	READY								W	rite '1	1' to	o Ena	able	inte	rru	pt fo	or R	EAD	ev ev	ent								
										Se	e <i>EVE</i>	ENT	S_RI	EAD	Y														
			Set	1						En	able																		
			Disabled	0						Re	ad: D	Disa	bled																
			Enabled	1						Re	ad: E	nal	oled																
В	RW	DOWN								W	rite '1	1' to	o Ena	able	inte	rru	pt fo	or D	1WO	l ev	ent								
										Se	e <i>EVE</i>	ENT	S_D	ow	N														
			Set	1						En	able																		
			Disabled	0						Re	ad: D	Disa	bled																
			Enabled	1						Re	ad: E	nal	oled																
С	RW	UP								W	rite '1	1' to	o Ena	able	inte	rru	pt fo	or U	P ev	ent									
										Se	e <i>EVE</i>	ENT	S_U	P															
			Set	1						En	able																		
			Disabled	0						Re	ad: D	Disa	bled																
			Enabled	1						Re	ad: E	nal	oled																
D	RW	CROSS								W	rite '1	1' to	o Ena	able	inte	rru	pt fo	or C	ROSS	ev	ent								
										Se	e <i>EVE</i>	ENT	S_CI	ROS	S														
			Set	1						En	able																		
			Disabled	0						Re	ad: D	Disa	bled																
			Enabled	1						Re	ad: E	nal	oled																

38.3.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	er		31	30 :	29 2	28 2	27 2	26 2	5 2	24 2	23 2:	2 2	1 20	0 1	9 18	8 17	7 16	5 15	14	13	12	11	10	9	8 7	,	s 5	4	3	2	1 0
Id																														D	С	ВА
Rese	et 0x0	0000000		0	0	0	0	0	0 (0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Desc	ript	tion	1																	
Α	RW	READY									١	Vrite	e '1	' to	Dis	abl	e in	teri	upt	t fo	r RE	AD۱	ev(ent								
											5	See E	EVE	NTS	S_R	EAL	ΟY															
			Clear	1								Disab	ble																			
			Disabled	0							F	Read	l: Di	isab	oled																	
			Enabled	1							F	Read	l: Er	nab	led																	
В	RW	DOWN									١	Vrite	e '1	' to	Dis	abl	e in	teri	upt	t fo	r DC	١W	l ev	ent								
											S	See E	EVE	NTS	S_D	oи	/N															
			Clear	1							[Disak	ble																			
			Disabled	0							F	Read	l: Di	isab	oled	l																
			Enabled	1							F	Read	l: Er	nab	led																	
С	RW	UP									١	Vrite	e '1	' to	Dis	abl	e in	teri	upt	fo	r UP	eve	ent									
											5	See E	EVE	NTS	s_ <i>U</i>	P																



Bit number		31 30 29 28 2	27 26 2	25 2	4 23	3 22	21	20	19	18 1	17 1	16 1	15 1	4 13	12	11	10	9	8	7	6	5 4	, ,	2 C	1 B	0
Reset 0x00000000		0 0 0 0	0 0	0 0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0	0	0	
Id RW Field	Value Id	Value			De	escri	iptic	on																		
	Clear	1			Di	isabl	le																			
	Disabled	0			Re	ead:	Disa	able	ed																	
	Enabled	1			Re	ead:	Ena	ble	d																	
D RW CROSS					W	/rite	'1' t	o D	isal	ole i	nte	rru	pt fo	or CF	ROSS	s ev	ent									
					Se	ee <i>E</i> \	VEN	TS_	CRC	oss																
	Clear	1			Di	isabl	le																			
	Disabled	0			Re	ead:	Disa	able	ed																	
	Enabled	1			Re	ead:	Ena	ble	d																	

38.3.4 RESULT

Address offset: 0x400

Compare result

Bit	numbe	er		31 3	0 29	28	3 27	26	25	24	23	22	21 :	20 1	9 1	8 1	7 1	6 1	5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																																Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0	0	0 () () () () () () () (0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Valu	ie						De	scri	ptio	n																		
Α	R	RESULT									Res	ult	of I	ast (com	par	e. I	Dec	isio	n p	oin	t SA	MP	LE t	ask							
			Below									ut v	olta	age	is b	elov	v th	ne r	efe	ren	ce 1	thre	eshc	ld (VIN	+ <	VIN	-).				
			Above	1							Inp	ut v	olta	age	is al	oov	e th	ne r	efe	ren	ce 1	thre	shc	ld (VIN	+>	VIN	-).				

38.3.5 ENABLE

Address offset: 0x500 Enable LPCOMP

Bitı	numb	er		31 30	29	28 2	27 2	6 25	5 24	23	22	21	20	19	18 1	L7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5 4	1 3	2	1 0
Id																														A A
Res	et 0x	00000000		0 0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0 (0 0	0	0 0
Id	RW	Field	Value Id	Value						De	scri	ptic	on																	
Α	RW	ENABLE								En	able	e or	disa	able	LP	CON	ЛP													
			Disabled	0						Dis	abl	e																		
			Enabled	1						En	able	9																		

38.3.6 PSEL

Address offset: 0x504

Input pin select

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PSEL		Analog pin select
	AnalogInput0	0 AINO selected as analog input
	AnalogInput1	1 AIN1 selected as analog input
	AnalogInput2	2 AIN2 selected as analog input
	AnalogInput3	3 AIN3 selected as analog input
	AnalogInput4	4 AIN4 selected as analog input
	AnalogInput5	5 AIN5 selected as analog input
	AnalogInput6	6 AIN6 selected as analog input
	AnalogInput7	7 AIN7 selected as analog input



38.3.7 REFSEL

Address offset: 0x508 Reference select

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
АААА
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
/alue Description
Reference select
VDD * 1/8 selected as reference
VDD * 2/8 selected as reference
2 VDD * 3/8 selected as reference
3 VDD * 4/8 selected as reference
VDD * 5/8 selected as reference
VDD * 6/8 selected as reference
VDD * 7/8 selected as reference
External analog reference selected
3 VDD * 1/16 selected as reference
VDD * 3/16 selected as reference
VDD * 5/16 selected as reference
VDD * 7/16 selected as reference
VDD * 9/16 selected as reference
VDD * 11/16 selected as reference
VDD * 13/16 selected as reference
0 1 2 3 1 1 1 1 1

38.3.8 EXTREFSEL

Ref15_16Vdd

Address offset: 0x50C External reference select

Bitı	numbe	er		3	1 30	29	28	3 27	7 26	5 25	5 24	1 23	3 22	2 21	. 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	'alue	е						De	esci	ripti	ion																				
Α	RW	EXTREFSEL										Ex	ter	nal	ana	log	ret	ere	nce	sel	ect														
			AnalogReference0	0								Us	se A	AINC	as)	ext	err	al a	nal	og r	efe	ren	ce												
			AnalogReference1	1						Us	se A	AIN1	Las	ext	err	al a	nal	og r	efe	ren	ce														

VDD * 15/16 selected as reference

38.3.9 ANADETECT

Address offset: 0x520

Analog detect configuration

Bit r	numbe	er		31	1 30	29	28	27 :	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							Des	scri	ptic	on																				
Α	RW	ANADETECT										Ana	alog	g de	tec	t cc	onfi	gur	atio	on															
			Cross	0								Ger	nera	ate	ΑN	ADI	ETE	СТ	on	cro	ssir	ıg, l	botl	n up	wa	rd o	ros	sin	g a	nd					
												dov	vnv	war	d cr	oss	ing																		
			Up	1								Ger	nera	ate	ΑN	ADI	ETE	СТ	on	upv	var	d cı	ross	ing	onl	У									
			Down	2								Ger	nera	ate	ΑN	ADI	ETE	СТ	on	dov	vnv	var	d cr	ossi	ng	onl	У								

38.3.10 HYST

Address offset: 0x538

Comparator hysteresis enable



Bit r	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A
Res	et OxO	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value Description
Α	RW	HYST		Comparator hysteresis enable
			Disabled	0 Comparator hysteresis disabled
			Enabled	1 Comparator hysteresis enabled

38.4 Electrical specification

38.4.1 LPCOMP Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{LPC}	Run current for low power comparator		0.5		μΑ
t _{LPCANADET}	Time from VIN crossing (>=50mV above threshold) to		5		μs
	ANADETECT signal generated.				
V _{INPOFFSET}	Input offset including reference ladder error	-40		40	mV
V _{HYST}	Optional hysteresis		35		mV
t _{STARTUP}	Startup time for LPCOMP		140		μs



39 WDT — Watchdog timer

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up.

The watchdog timer is started by triggering the START task.

The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU. The watchdog is implemented as a down-counter that generates a TIMEOUT event when it wraps over after counting down to 0. When the watchdog timer is started through the START task, the watchdog counter is loaded with the value specified in the CRV register. This counter is also reloaded with the value specified in the CRV register when a reload request is granted.

The watchdog's timeout period is given by:

```
timeout [s] = ( CRV + 1 ) / 32768
```

When started, the watchdog will automatically force the 32.768 kHz RC oscillator on as long as no other 32.768 kHz clock source is running and generating the 32.768 kHz system clock, see chapter *CLOCK*—*Clock control* on page 141.

39.1 Reload criteria

The watchdog has eight separate reload request registers, which shall be used to request the watchdog to reload its counter with the value specified in the CRV register. To reload the watchdog counter, the special value 0x6E524635 needs to be written to all enabled reload registers.

One or more RR registers can be individually enabled through the RREN register.

39.2 Temporarily pausing the watchdog

By default, the watchdog will be active counting down the down-counter while the CPU is sleeping and when it is halted by the debugger. It is however possible to configure the watchdog to automatically pause while the CPU is sleeping as well as when it is halted by the debugger.

39.3 Watchdog reset

A TIMEOUT event will automatically lead to a watchdog reset.

See *Reset* on page 73 for more information about reset sources. If the watchdog is configured to generate an interrupt on the TIMEOUT event, the watchdog reset will be postponed with two 32.768 kHz clock cycles after the TIMEOUT event has been generated. Once the TIMEOUT event has been generated, the impending watchdog reset will always be effectuated.

The watchdog must be configured before it is started. After it is started, the watchdog's configuration registers, which comprise registers CRV, RREN, and CONFIG, will be blocked for further configuration.

The watchdog can be reset from several reset sources, see *Reset behavior* on page 74.

When the device starts running again, after a reset, or waking up from OFF mode, the watchdog configuration registers will be available for configuration again.



39.4 Registers

Table 87: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40010000	WDT	WDT	Watchdog timer		

Table 88: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start the watchdog
EVENTS_TIMEOUT	0x100	Watchdog timeout
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RUNSTATUS	0x400	Run status
REQSTATUS	0x404	Request status
CRV	0x504	Counter reload value
RREN	0x508	Enable register for reload request registers
CONFIG	0x50C	Configuration register
RR[0]	0x600	Reload request 0
RR[1]	0x604	Reload request 1
RR[2]	0x608	Reload request 2
RR[3]	0x60C	Reload request 3
RR[4]	0x610	Reload request 4
RR[5]	0x614	Reload request 5
RR[6]	0x618	Reload request 6
RR[7]	0x61C	Reload request 7

39.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	umbe	er		31	1 30	29	2	8 2	7 :	26	25	24	23	22	2 2	1 2	0 :	19	18	17	16	1	5 1	4 1	3 :	12 :	11	10	9	8	7	6	5	4	3	2	1	0
Id																																						Α
Rese	t 0x0	0000000		0	0	0	C) ()	0	0	0	0	0	C) (0	0	0	0	0	C) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	:							De	scr	ript	tio	n																					
Α	RW	TIMEOUT											W	rite	· '1	' to	Er	nab	le	int	err	up'	t fo	r T	IMI	ΕOι	JT	eve	nt									
													Se	e <i>E</i>	VE	NT	S _	TIN	1EC	טט'	Т																	
			Set	1									En	abl	le																							
			Disabled	0									Re	ad	: D	isa	ble	d																				
			Enabled	1									Re	ad:	: Er	nak	oled	b																				

39.4.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit	numbe	r		31	1 30	29	2	8 2	7	26	25	24	23	3 2:	2 2	1 2	20	19	18	1	7 1	6 :	15	14	13	3 1	2 1	1	10	9	8	7	6	5	4	3	2	1	0
Id																																							Α
Res	et 0x0	0000000		0	0	0	C) (0	0	0	0	0	0	()	0	0	0	0	()	0	0	0	() (0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	:							D	esc	rip	tio	n																						
Α	RW	TIMEOUT											W	rite	e '1	.' to	D D	isa	ble	in	ter	ru	pt	for	· TI	M	Οι	JT	eve	ent									
													Se	e E	VE	N7	s_	TΙΛ	1E (วบ	Т																		
			Clear	1									Di	sak	le																								
			Disabled	0									Re	ead	: D	isa	ble	d																					
			Enabled	1									Re	ead	: E	nal	ole	d																					



39.4.3 RUNSTATUS

Address offset: 0x400

Run status

Bitı	numbe	r		3:	1 30	29	28	8 27	7 26	6 2	5 24	4 2	3 2	2 2	1 2	0 1	.9 1	L8 1	.7 1	.6 1	5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0) (0	0) (0 (0	0	0	0 () () (0 () (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	е						D	esc	ript	tior	n																		
Α	R	RUNSTATUS										lr	ndic	ate	s w	/he	the	r oı	no	t th	e w	ato	hdo	og i	s ru	nnir	ng							
			NotRunning	0								٧	Vato	chd	og	not	ru	nni	ng															
			Running	1								٧	Vato	chd	og i	is r	unr	ning																

39.4.4 REQSTATUS

Address offset: 0x404

Request status

																									_							
	numbe	er		31	. 30	29	28	27	26	25	24 2	23	22 2	21 2	0 19	18	17	16	15 1	4 1	3 12	11	10	9				4	- 3	2	1	0
Id																													D			
Res	et 0x0	0000001		0	0	0	0	0	0	0	_	•	0 (0	0	0	0 () (0	0	0	0	0 () (0	0	0	0	0	1
Id	RW	Field	Value Id	Va	llue						ı	Des	scrip	tior	1																	
Α	R	RRO									ı	Rec	ques	t sta	itus	for	RR[C] re	gist	er												
			DisabledOrRequested	0							ı	RR[[0] re	egist	ter is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			${\sf EnabledAndUnrequested}$	1							ı	RR[[0] re	egist	ter is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
В	R	RR1									ı	Rec	ques	t sta	itus	for	RR[1] re	gist	er												
			DisabledOrRequested	0							ı	RR[[1] re	egist	ter is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			${\sf EnabledAndUnrequested}$	1							ı	RR[[1] re	egist	er is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
С	R	RR2									F	Rec	ques	t sta	itus	for	RR[2] re	gist	er												
			DisabledOrRequested	0							ı	RR[[2] re	egist	ter is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			EnabledAndUnrequested	1							ı	RR[[2] re	egist	ter is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
D	R	RR3									ı	Rec	ques	t sta	atus	for	RR[3] re	gist	er												
			DisabledOrRequested	0							ı	RR[[3] re	egist	ter is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			${\sf EnabledAndUnrequested}$	1							ſ	RR[[3] re	egist	ter is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
E	R	RR4									ı	Rec	ques	t sta	itus	for	RR[4] re	gist	er												
			DisabledOrRequested	0							ı	RR[[4] re	egist	er is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			${\sf EnabledAndUnrequested}$	1							ı	RR[[4] re	egist	ter is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
F	R	RR5									ı	Rec	ques	t sta	atus	for	RR[5] re	gist	er												
			DisabledOrRequested	0							ı	RR[[5] re	egist	ter is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			EnabledAndUnrequested	1							ı	RR[[5] re	egist	ter is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
G	R	RR6									ı	Rec	ques	t sta	itus	for	RR[6] re	gist	er												
			DisabledOrRequested	0							ı	RR[[6] re	egist	ter is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			EnabledAndUnrequested	1							ı	RR[[6] re	egist	er is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
Н	R	RR7									ı	Rec	ques	t sta	itus	for	RR[7	'] re	gist	er												
			DisabledOrRequested	0							ı	RR[[7] re	egist	er is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			EnabledAndUnrequested	1							ı	RR[[7] re	egist	ter is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					

39.4.5 CRV

Address offset: 0x504 Counter reload value

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16 :	15 1	L4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3 .	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α Α	A A	A	Α	Α	Α	Α	Α	Α	Α /	4 4	A A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	. 1	1	1	1	1	1	1	1 :	1 1	l 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	CRV		[0	x00	000	000	0	xFF	FFF	FFF	Со	unt	er r	elo	ad v	/alu	e in	nu	mb	er c	f cy	cles	of	the	32.7	768	kHz	2				

clock



39.4.6 RREN

Address offset: 0x508

Enable register for reload request registers

Bit r	numbe	er _		31	30 2	29 :	28 2	7 2	6 2	5 2	4 23	3 22	21	20	19	18	17 :	16	15 :	14 1	3 1	2 11	10	9	8	7	6	5 4	1 3	2	1	0
Id																										Н	G	F	E D	С	В	Α
Res	et 0x0	0000001		0	0	0	0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	1
Id	RW	Field	Value Id	Va	lue						De	escr	iptic	on																		
Α	RW	RR0									En	nabl	e or	dis	able	e RF	R[0]	re	giste	er												
			Disabled	0							Di	isab	le Ri	R[0]	reg	gist	er															
			Enabled	1							En	nabl	e RR	(0]	reg	iste	er															
В	RW	RR1									En	nabl	e or	dis	able	e RF	R[1]	re	giste	er												
			Disabled	0							Di	isab	le Ri	R[1]	reg	gist	er															
			Enabled	1							En	nabl	e RR	(1)	reg	iste	er															
С	RW	RR2									En	nabl	e or	dis	able	e RF	R[2]	re	giste	er												
			Disabled	0							Di	isab	le Ri	R[2	reg	gist	er															
			Enabled	1							En	nabl	e RR	[2]	reg	iste	er															
D	RW	RR3									En	nabl	e or	dis	able	e RF	R[3]	re	giste	er												
			Disabled	0							Di	isab	le Ri	R[3	reg	gist	er															
			Enabled	1							En	nabl	e RR	(3]	reg	iste	er															
Ε	RW	RR4									En	nabl	e or	dis	able	e RF	R[4]	re	giste	er												
			Disabled	0							Di	isab	le Ri	R[4]	reg	gist	er															
			Enabled	1							En	nabl	e RR	(4)	reg	iste	er															
F	RW	RR5									En	nabl	e or	dis	able	e RF	R[5]	re	giste	er												
			Disabled	0							Di	isab	le Ri	R[5]	reg	gist	er															
			Enabled	1							En	nabl	e RR	[5]	reg	iste	er															
G	RW	RR6									En	nabl	e or	dis	able	e RF	R[6]	re	giste	er												
			Disabled	0							Di	isab	le Ri	R[6	reg	gist	er															
			Enabled	1							En	nabl	e RR	(6]	reg	iste	er															
Н	RW	RR7									En	nabl	e or	dis	able	e RF	R[7]	re	giste	er												
			Disabled	0							Di	isab	le Ri	R[7	reg	gist	er															
			Enabled	1							Er	nabl	e RR	[7]	reg	iste	er															

39.4.7 CONFIG

Address offset: 0x50C Configuration register

																															_	
Bit	numbe	er		31	. 30	29	28 .	27 .	26 2	25 2	24 .	23 2	22 2	21 2	0 1	9 1	8 1.	7 16	5 15	14	13	12	11 1	.0 9	9 8	3 7	6	5	4	3	2 :	1 0
Id																														С		Α
Res	et 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0 0) () (0	0	0	0	0	0	0 () (0 (0	0	0	0	0	0 (0 1
Id	RW	Field	Value Id	Va	lue						1	Des	crip	tion																		
Α	RW	SLEEP									(Con	figu	ıre t	he	wat	chd	log	to e	ithe	r b	e pa	used	d, o	r ke	pt r	unr	ning,	,			
											١	whil	e tł	ne C	PU	is s	leep	oing														
			Pause	0							-	Paus	se v	vatc	hdo	og v	vhil	e th	e Cl	PU i	s sle	eepi	ng									
			Run	1							-	Kee	p th	ne w	atc	hdc	g rı	unn	ing	whi	le tl	ne C	PU i	s sle	eep	ing						
С	RW	HALT									(Con	figu	ire t	he	wat	chd	log	to e	ithe	r b	e pa	used	d, o	r ke	pt r	unr	ning,	,			
											,	whil	e tł	ne C	PU	is h	alte	ed b	y th	e d	ebu	gge										
			Pause	0							1	Paus	se v	vatc	hdo	og v	vhil	e th	e Cl	PU i	s ha	altec	by	the	de	bug	ger					
			Run	1								Kee	p th	ne w	atc	hdc	g ru	unn	ing	whi	le tl	ne C	PU i	s ha	alte	d by	th.	е				
											(deb	ugg	er																		

39.4.8 RR[0]

Address offset: 0x600 Reload request 0



E	Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1 0
1	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	4 А
1	Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
ı	ld	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
,	Д	W	RR										Re	oac	l re	que	st r	egi	stei	r															
				Reload	0x	6E5	246	35					Va	lue 1	to r	eau	ıest	ar	elo	ad (of t	he v	wat	cho	log	tim	er								

39.4.9 RR[1]

Address offset: 0x604 Reload request 1

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0)
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0)
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																				ı
Α	W	RR										Re	loa	d re	qu	est i	regi	iste	r																
			Reload	0x	6E5	246	35					Va	lue	to	rea	uesi	taı	relo	ad	of t	the	wa	tch	dos	tin	ner									

39.4.10 RR[2]

Address offset: 0x608 Reload request 2

Bit	numb	er		31 30 29 28 27 26 25	4 23 22 21 20 19 18 17	7 16 15 14 13 12 11 10 9 8 7 6 5 4 :	3 2 1 0
Id				A A A A A A	A A A A A A A		A A A A
Res	et 0x	00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0000000000000000	0 0 0 0
Id	RW	Field	Value Id	Value	Description		
Α	W	RR			Reload request registe	er	
			Reload	0x6E524635		load of the watchdog timer	

39.4.11 RR[3]

Address offset: 0x60C Reload request 3

Bitı	num	nbe	r		31 30 29 28 27 26 25 24 23	22 21 20 19 18 1	17 16 1	5 14	13 12	11 1	0 9	8	7	6	5	4	3 2	1	0
Id					A A A A A A A A	AAAAA	AAA	4 A	A A	A	4 A	Α	Α	Α	Α	Α	АА	A	Α
Res	et 0	0x0	000000		0 0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0	0 0	0 0	0 (0 0	0	0	0	0	0	0 0	0	0
Id	R	w	Field	Value Id	Value Des	scription													
Α	W	V	RR		Rel	oad request regis	ter												
				Reload	0x6E524635 Val	lue to request a re	eload o	f the v	watch	ndog t	ime	-							

39.4.12 RR[4]

Address offset: 0x610 Reload request 4

Bitı	numb	er		31	. 30	29	28	3 2	7 26	5 2	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Δ	A	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et 0x0	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue	:						De	scr	ipti	on																			
Α	W	RR										Re	loa	d re	qu	est i	regi	iste	r															
			Reload	Ох	6E5	524	635	;				Va	lue	to i	rea	uest	taı	relo	ad	of t	he	wat	cho	dog	tin	ner								

39.4.13 RR[5]

Address offset: 0x614 Reload request 5



Bit	numb	er		31	1 30	29	9 2	8 2	7 2	26 :	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	. Α			Δ.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0x(00000000		0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	o
Id	RW	Field	Value Id	Va	alue	9							De	cri	otic	on																				
Α	W	RR											Rel	oad	re	que	est r	egis	ster																	
			Reload	0>	(6E!	524	63	5					Val	ue 1	o r	equ	uest	ar	elo	ad o	of t	he	wat	cho	log	tim	ner									

39.4.14 RR[6]

Address offset: 0x618 Reload request 6

Bit r	iumb	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et OxC	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description
Α	W	RR		Reload request register
			Reload	0x6E524635 Value to request a reload of the watchdog timer

39.4.15 RR[7]

Address offset: 0x61C Reload request 7

Bit r	numb	er		31	. 30	29	28	3 27	7 26	5 2	5 2	4 2	3 2	2 21	. 20	19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	2	1 0
Id				Α	Α	Α	Α	. A	A	. 4	\ <i>A</i>	A A		4 A	Α	Α	Α	Α	Α	Α	Α	Α.	A /	A	Α	Α	Α	Α	Α	Α	A A	١,	A A
Res	et Ox	00000000		0	0	0	0	0	0	C) () () (0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	alue	•						D	esc	ript	ion																		
Α	W	RR										R	elo	ad r	equ	est	reg	iste	r														
			Reload	0x	6E5	524	635	5				٧	alu	e to	req	ues	t a	relo	ad	of t	he v	wato	hdo	g tii	ner								

39.5 Electrical specification

39.5.1 Watchdog Timer Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{WDT}	Run current for watchdog timer		0.3	2	μΑ
t _{WDT}	Time out interval	458 μs		36 h	



40 SWI — Software interrupts

A set of interrupts have been reserved for use as software interrupts.

40.1 Registers

Table 89: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40014000	SWI	SWI0	Software interrupt 0		
0x40015000	SWI	SWI1	Software interrupt 1		
0x40016000	SWI	SWI2	Software interrupt 2		
0x40017000	SWI	SWI3	Software interrupt 3		
0x40018000	SWI	SWI4	Software interrupt 4		
0x40019000	SWI	SWI5	Software interrupt 5		



41 NFCT — Near field communication tag

The NFCT peripheral is an implementation of an NFC Forum compliant listening device NFC-A.

With appropriate software, the NFCT peripheral can be used as the listening device NFC-A as specified by the *NFC Forum*.

Listed here are the main features for the NFCT peripheral:

- NFC-A listen mode operation
 - 13.56 MHz input frequency
 - Bit rate 106 kbps
- Wake-on-field low power field detection (SENSE) mode
- · Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum
- Programmable frame timing controller
- Integrated automatic collision resolution, cyclic redundancy check (CRC), and parity functions

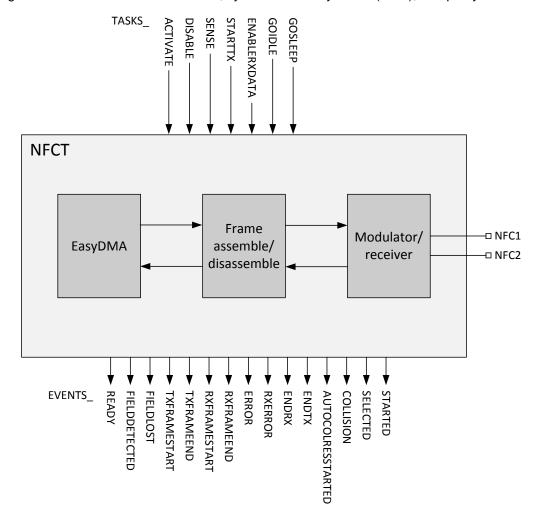


Figure 126: NFCT block diagram

41.1 Overview

The NFCT peripheral contains a 13.56 MHz AM receiver and a 13.56 MHz load modulator with 106 kbps data rate as defined by the NFC Forum.



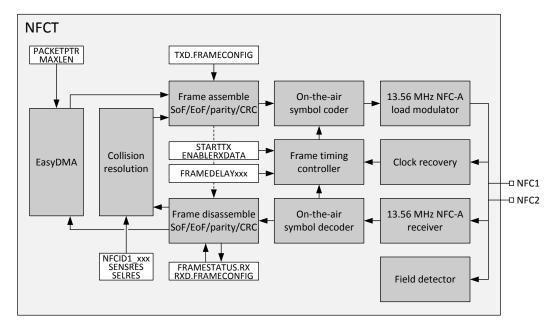


Figure 127: NFCT overview

When transmitting, the frame data will be transferred directly from RAM and transmitted with configurable frame type and delay timing. The system will be notified by an event whenever a complete frame is received or sent. The received frames will be automatically disassembled and the data part of the frame transferred to RAM.

The NFCT peripheral also supports the collision detection and resolution ("anticollision") as defined by the NFC Forum.

Wake-on-field is supported in SENSE mode while the device is either in System OFF or System ON mode. When the antenna enters an NFC field, an event will be triggered notifying the system to activate the NFCT functionality for incoming frames. In System ON, if the energy detected at the antenna increases beyond a threshold value, the module will generate a *FIELDDETECTED* event. When the strength of the field no longer supports NFC communication, the module will generate a *FIELDLOST* event. For the Low Power Field Detect threshold values, refer to *NFCT Electrical Specification* on page 498.

In System OFF, the NFCT Low Power Field Detect function can wake the system up through a reset. The NFC bit in the RESETREAS register in *POWER* — *Power supply* on page 66 will be set as the cause of the wake-up.

If the system is put into System OFF mode while a field is already present, the NFCT Low Power Field Detect function will wake the system up right away and generate a reset.

Important: As a consequence of a reset, NFCT is disabled, and therefore the reset handler will have to activate NFCT again and set it up properly.

The HFXO must be running before the NFCT peripheral goes into ACTIVATED state. Note that the NFCT peripheral calibration is automatically done on *ACTIVATE* task. The HFXO can be turned off when the NFCT peripheral goes into SENSE mode. The shortcut FIELDDETECTED_ACTIVATE can be used when the HFXO is already running while in SENSE mode.

Outgoing data will be collected from RAM with the EasyDMA function and assembled according to the TXD.FRAMECONFIG on page 494 register. Incoming data will be disassembled according to the RXD.FRAMECONFIG register and the data section in the frame will be written to RAM via the EasyDMA function.

The NFCT peripheral includes a frame timing controller that can be used to accurately control the interframe delay between the incoming frame and a corresponding outgoing frame. It also includes optional CRC functionality.



41.2 Operating states

Tasks and events are used to control the operating state of the peripheral. The module can change state by triggering a task, or when specific operations are finalized. Events and tasks allow software to keep track of and change the current state.

See Figure 126: NFCT block diagram on page 477 and Figure 128: NFCT state diagram, automatic collision resolution enabled on page 479 for more information.

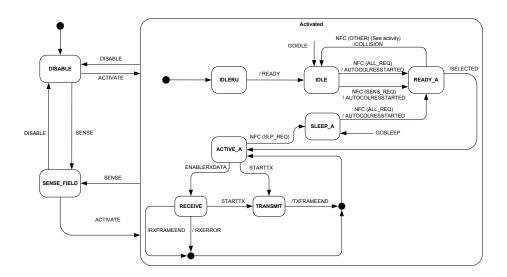


Figure 128: NFCT state diagram, automatic collision resolution enabled

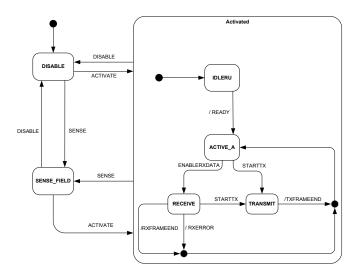


Figure 129: NFCT state diagram, automatic collision resolution disabled

Important:

- FIELDLOST event will not be reflected in the state machine (for instance by going back to the DISABLE state). It is up to software to decide on the actions to take when a field lost occurs.
- FIELDLOST event is not generated in SENSE mode.
- Sending SENSE task while field is still present does not generate FIELDDETECTED event.
- If the FIELDDETECTED event is cleared before sending the *ACTIVATE* task, then the FIELDDETECTED event shows up again after sending the ACTIVATE task. The shortcut FIELDDETECTED_ACTIVATE can be used to avoid this condition.



41.3 Pin configuration

NFCT uses two pins to connect the antenna and these pins are shared with GPIOs.

The PROTECT field in the NFCPINS register in *UICR* defines the usage of these pins and their protection level against excessive voltages. The content of the NFCPINS register is reloaded at every reset. See *Pin assignments* on page 13 for the pins used by the NFCT peripheral.

When NFCPINS.PROTECT=NFC, a protection circuit will be enabled on the dedicated pins, preventing the chip from being damaged in the presence of a strong NFC field. The protection circuit will short the two pins together if voltage difference exceeds approximately 2V. The GPIO function on those pins will also be disabled.

When NFCPINS.PROTECT=Disabled, the device will not be protected against strong NFC field damages caught by a connected NFCT antenna, and the NFCT peripheral will not operate as expected, as it will never leave the DISABLE state.

The pins dedicated to the NFCT antenna function will have some limitation when the pins are configured for normal GPIO operation. The pin capacitance will be higher on those (refer to C_{PAD_NFC} in the Electrical Specification of *GPIO* — *General purpose input/output* on page 154), and some increased leakage current between the two pins is to be expected if they are used in GPIO mode, and are driven to different logical values. To save power, the two pins should always be set to the same logical value whenever entering one of the device power saving modes. For details, refer to I_{NFC_LEAK} in the Electrical Specification of *GPIO* — *General purpose input/output* on page 154.

41.4 EasyDMA

The NFCT peripheral implements EasyDMA for reading and writing of data packets from and to the Data RAM.

The NFCT EasyDMA utilizes a pointer called *PACKETPTR* on page 494 for receiving and transmitting packets.

The NFCT peripheral uses EasyDMA to read or write RAM, but not both at the same time. The event *RXFRAMESTART* indicates that the EasyDMA has started writing to the RAM for a receive frame and the event *RXFRAMEND* indicates that the EasyDMA has completed writing to the RAM. Similarly, the event *TXFRAMESTART* indicates that the EasyDMA has started reading from the RAM for a transmit frame and the event *TXFRAMEND* indicates that the EasyDMA has completed reading from the RAM. If a transmit and a receive operation is issued at the same time, the transmit operation would be prioritized.

Starting a transmit operation while the EasyDMA is writing a receive frame to the RAM will result in unpredictable behavior. Starting an EasyDMA operation when there is an ongoing EasyDMA operation may result in unpredictable behavior. It is recommended to wait for the TXFRAMEEND or RXFRAMEEND event for the ongoing transmit or receive before starting a new receive or transmit operation.

The *MAXLEN* on page 494 register determines the maximum number of bytes that can be read from or written to the RAM. This feature can be used to ensure that the NFCT peripheral does not overwrite, or read beyond, the RAM assigned to a packet. Note that if the *RXD.AMOUNT* or *TXD.AMOUNT* register indicates longer data packets than set in MAXLEN, the frames sent to or received from the physical layer will be incomplete. In that situation, in RX, the OVERRUN bit in the *FRAMESTATUS.RX* register will be set and an *RXERROR* event will be triggered.

Important: The RXD.AMOUNT and TXD.AMOUNT define a frame length in bytes and bits excluding start of frame (SoF), end of frame (EoF), and parity, but including CRC for RXD.AMOUNT only. Make sure to take potential additional bits into account when setting MAXLEN.

Only sending task *ENABLERXDATA* ensures that a new value in PACKETPTR pointing to the RX buffer in Data RAM is taken into account.

If PACKETPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a hard fault or RAM corruption. For more information about the different memory regions, see Chapter *Memory* on page 20.



The NFCT peripherals normally do alternative receive and transmit frames. Therefore, to prepare for the next frame, the PACKETPTR, MAXLEN, *TXD.FRAMECONFIG* and TXD.AMOUNT can be updated while the receive is in progress, and, similarly, the PACKETPTR, MAXLEN and *RXD.FRAMECONFIG* can be updated while the transmit is in progress. They can be updated and prepared for the next NFC frame immediately after the *STARTED* event of the current frame has been received. Updating the TXD.FRAMECONFIG and TXD.AMOUNT during the current transmit frame or updating RXD.FRAMECONFIG during current receive frame may cause unpredictable behaviour.

In accordance with *NFC Forum, NFC Digital Protocol Technical Specification*, the least significant bit (LSB) from the least significant byte (LSByte) is sent on air first. The bytes are stored in increasing order, starting at the lowest address in the EasyDMA buffer in RAM.

41.5 Frame assembler

The NFCT peripheral implements a frame assembler in hardware.

When the NFCT peripheral is in the ACTIVE_A state, the software can decide to enter RX or TX mode. For RX, see *Frame disassembler* on page 482. For TX, the software must indicate the address of the source buffer in Data RAM and its size through programming the *PACKETPTR* and MAXLEN registers respectively, then issuing a STARTTX task.

MAXLEN must be set so that it matches the size of the frame to be sent.

The *STARTED* event indicates that the PACKETPTR and MAXLEN registers have been captured by the frame assembler EasyDMA.

When asserting the *STARTTX* task, the frame assembler module will start reading TXD.AMOUNT.TXDATABYTES bytes (plus one additional byte if TXD.AMOUNT.TXDATABITS > 0) from the RAM position set by the PACKETPTR.

The NFCT peripheral transmits the data as read from RAM, adding framing and the CRC calculated on the fly if set in TXD.FRAMECONFIG. The NFCT peripheral will take (8*TXD.AMOUNT.TXDATABYTES + TXD.AMOUNT.TXDATABITS) bits and assemble a frame according to the settings in *TXD.FRAMECONFIG*. Both short frames, standard frames, and bit-oriented SDD frames as specified in the *NFC Forum*, *NFC Digital Protocol Technical Specification* can be assembled by the correct setting of the TXD.FRAMECONFIG register.

The bytes will be transmitted on air in the same order as they are read from RAM with a rising bit order within each byte, least significant bit (LSB) first. That is, b0 will be transmitted on air before b1, and so on. The bits read from RAM will be coded into symbols as defined in the *NFC Forum, NFC Digital Protocol Technical Specification*.

Important: Some NFC Forum documents, such as *NFC Forum, NFC Digital Protocol Technical Specification*, define bit numbering in a byte from b1 (LSB) to b8 (most significant bit (MSB)), while most other technical documents from the NFC Forum, and also the Nordic Semiconductor documentation, traditionally number them from b0 to b7. The present document uses the b0–b7 numbering scheme. Be aware of this when comparing the *NFC Forum, NFC Digital Protocol Technical Specification* to others.

The frame assembler can be configured in TXD.FRAMECONFIG to add SoF symbol, calculate and add parity bits, and calculate and add CRC to the data read from RAM when assembling the frame. The total frame will then be longer than what is defined by TXD.AMOUNT.TXDATABYTES. TXDATABITS. DISCARDMODE will select if the first bits in the first byte read from RAM or the last bits in the last byte read from RAM will be discarded if TXD.AMOUNT.TXDATABITS are not equal to zero. Note that if TXD.FRAMECONFIG.PARITY = Parity and TXD.FRAMECONFIG.DISCARDMODE=DiscardStart, a parity bit will be included after the non-complete first byte. No parity will be added after a non-complete last byte.

The frame assemble operation is illustrated in *Figure 130: Frame assemble illustration* on page 482 for different settings in TXD.FRAMECONFIG. All shaded bit fields are added by the frame assembler. Some of these bits are optional and appearances are configured in TXD.FRAMECONFIG. Note that the frames illustrated do not necessarily comply with the NFC specification. The figure is only to illustrate the behavior of the NFCT peripheral.



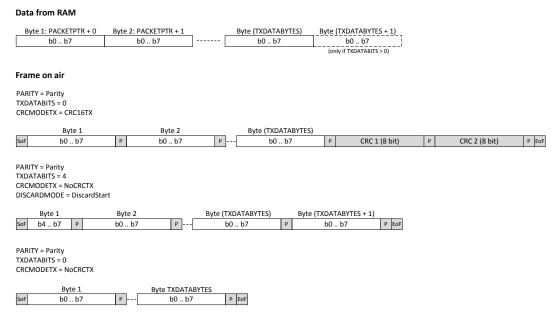


Figure 130: Frame assemble illustration

The accurate timing for transmitting the frame on air is set using the frame timing controller settings.

41.6 Frame disassembler

The NFCT peripheral implements a frame disassembler in hardware.

When the NFCT peripheral is in the ACTIVE_A state, the software can decide to enter RX or TX mode. For TX, see *Frame assembler* on page 481. For RX, the software must indicate the address and size of the destination buffer in Data RAM through programming the *PACKETPTR* and MAXLEN registers before issuing an *ENABLERXDATA* task.

The *STARTED* event indicates that the PACKETPTR and MAXLEN registers have been captured by the frame disassembler EasyDMA.

When an incoming frame starts, the *RXFRAMESTART* event will get issued and data will be written to the buffer in Data RAM. The frame disassembler will verify and remove any parity bits, start of frame (SoF) and end of frame (EoF) symbols on the fly based on *RXD.FRAMECONFIG* register configuration. It will, however, verify and transfer the CRC bytes into RAM, if the CRC is enabled through RXD.FRAMECONFIG.

When an EoF symbol is detected, the NFCT peripheral will assert the *RXFRAMEEND* event and write the *RXD.AMOUNT* register to indicate numbers of received bytes and bits in the data packet. The module does not interpret the content of the data received from the remote NFC device, except for SoF, EoF, parity, and CRC checking, as described above. The frame disassemble operation is illustrated below.



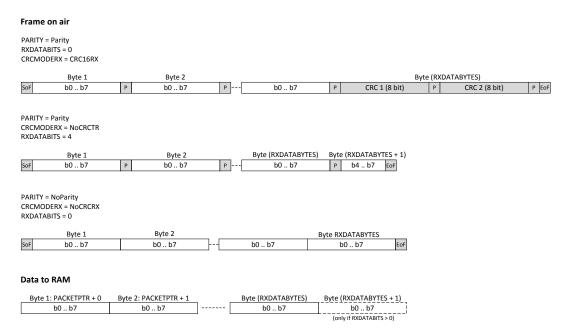


Figure 131: Frame disassemble illustration

Per NFC specification, the time between EoF to the next SoF can be as short as 86 µs, and thefore care must be taken that PACKETPTR and MAXLEN are ready and ENABLERXDATA is issued on time after the end of previous frame. The use of a PPI shortcut from *TXFRAMEEND* to ENABLERXDATA is recommended.

41.7 Frame timing controller

The NFCT peripheral includes a frame timing controller that continuously keeps track of the number of the 13.56 MHz RF carrier clock periods since the end of the EoF of the last received frame.

The NFCT peripheral can be programmed to send a responding frame within a time window or at an exact count of RF carrier periods. In case of *FRAMEDELAYMODE* = Window, a *STARTTX* task triggered before the frame timing controller counter is equal to *FRAMEDELAYMIN* will force the transmission to halt until the counter is equal to FRAMEDELAYMIN. If the counter is within FRAMEDELAYMIN and *FRAMEDELAYMAX* when the STARTTX task is triggered, the NFCT peripheral will start the transmission straight away. In case of FRAMEDELAYMODE = ExactVal, a STARTTX task triggered before the frame delay counter is equal to FRAMEDELAYMAX will halt the actual transmission start until the counter is equal to FRAMEDELAYMAX.

In case of FRAMEDELAYMODE = WindowGrid, the behaviour is similar to the FRAMEDELAYMODE = Window, but the actual transmission between FRAMEDELAYMIN and FRAMEDELAYMAX starts on a bit grid as defined for NFC-A Listen frames (slot duration of 128 RF carrier periods).

An *ERROR* event (with FRAMEDELAYTIMEOUT cause in *ERRORSTATUS*) will be asserted if the frame timing controller counter reaches FRAMEDELAYMAX without any STARTTX task triggered. This may happen even when the response is not required as per *NFC Forum, NFC Digital Protocol Technical Specification*. Any commands handled by the automatic collision resolution that don't involve a response being generated may also result in an ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS). The FRAMEDELAYMIN and FRAMEDELAYMAX values shall only be updated before the STARTTX task is triggered. Failing to do so may cause unpredictable behaviour.

The frame timing controller operation is illustrated in *Figure 132: Frame timing controller* (*FRAMEDELAYMODE=Window*) on page 484. The frame timing controller automatically adjusts the frame timing counter based on the last received data bit according to NFC-A technology in the *NFC Forum, NFC Digital Protocol Technical Specification*.



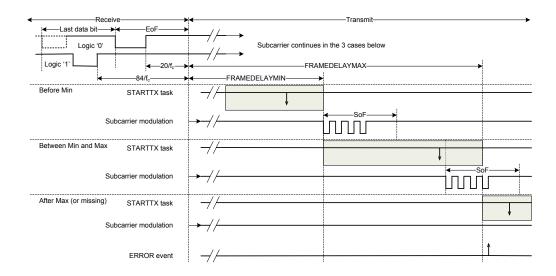


Figure 132: Frame timing controller (FRAMEDELAYMODE=Window)

41.8 Collision resolution

The NFCT peripheral implements an automatic collision resolution function as defined by the NFC Forum.

Automatic collision resolution is enabled by default, and it is recommended that the feature is used since it is power efficient and reduces the complexity of software handling the collision resolution sequence. This feature can be disabled through the MODE field in the *AUTOCOLRESCONFIG* register. When the automatic collision resolution is disabled, all commands will be sent over EasyDMA as defined in frame disassembler.

The SENSRES and SELRES registers need to be programmed upfront in order for the collision resolution to behave correctly. Depending on the NFCIDSIZE field in SENSRES, the following registers also need to be programmed upfront:

- NFCID1_LAST if NFCID1SIZE=NFCID1Single (ID = 4 bytes);
- NFCID1_2ND_LAST and NFCID1_LAST if NFCID1SIZE=NFCID1Double (ID = 7 bytes);
- NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST if NFCID1SIZE=NFCID1Triple (ID = 10 bytes);

A pre-defined set of registers, NFC.TAGHEADER0..3, containing a valid NFCID1 value, is available in *FICR* and can be used by software to populate the NFCID1_3RD_LAST, NFCID1_2ND_LAST, and NFCID1_LAST registers.

Table 90: NFCID1 byte allocation (top sent first on air) on page 484 explains the position of the ID bytes in NFCID1_3RD_LAST, NFCID1_2ND_LAST, and NFCID1_LAST, depending on the ID size, and as compared to the definition used in the NFC Forum, NFC Digital Protocol Technical Specification.

Table 90: NFCID1 byte allocation (top sent first on air)

	ID = 4 bytes	ID = 7 bytes	ID = 10 bytes
NFCID1_Q			nfcid1 ₀
NFCID1_R			nfcid1 ₁
NFCID1_S			nfcid1 ₂
NFCID1_T		nfcid1 ₀	nfcid1 ₃
NFCID1_U		nfcid1 ₁	nfcid1 ₄
NFCID1_V		nfcid1 ₂	nfcid1 ₅
NFCID1_W	nfcid1 ₀	nfcid1 ₃	nfcid1 ₆
NFCID1_X	nfcid1 ₁	nfcid1 ₄	nfcid1 ₇
NFCID1_Y	nfcid1 ₂	nfcid1 ₅	nfcid1 ₈
NFCID1 Z	nfcid1 ₂	nfcid1 _e	nfcid1 _o

The hardware implementation can handle the states from IDLE to ACTIVE_A automatically as defined in the *NFC Forum, NFC Activity Technical Specification*, and the other states are to be handled by software. The software keeps track of the state through events. The collision resolution will trigger an



AUTOCOLRESSTARTED event when it has started. Reaching the ACTIVE_A state is indicated by the SELECTED event.

If collision resolution fails, a *COLLISION* event is triggered. Note that errors occurring during automatic collision resolution may also cause *ERROR* and/or *RXERROR* events to be generated. Other events may also get generated. It is recommended that the software ignores any event except COLLISION, SELECTED and FIELDLOST during automatic collision resolution. Software shall also make sure that any unwanted SHORT or PPI shortcut is disabled during automatic collision resolution.

The automatic collision resolution will be restarted, if the packets are received with CRC or parity errors while in ACTIVE_A state. The automatic collision resolution feature can be disabled while in ACTIVE_A state to avoid this.

The SLP_REQ is automatically handled by the NFCT peripheral when the automatic collision resolution is enabled. However, this results in an ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS) since the SLP_REQ has no response. This error must be ignored until the SELECTED event is triggered and this error should be cleared by the software when the SELECTED event is triggered.

41.9 Antenna interface

In ACTIVATED state, an amplitude regulator will adjust the voltage swing on the antenna pins to a value that is within the V_{swing} limit.

Refer to NFCT Electrical Specification on page 498.

41.10 NFCT antenna recommendations

The NFCT antenna coil must be connected differential between NFC1 and NFC2 pins of the device.

Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56 MHz.

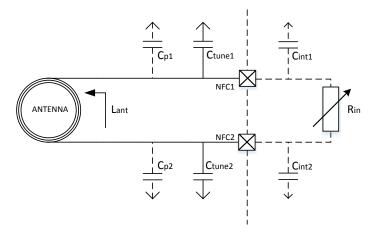


Figure 133: NFCT antenna recommendations

The required tuning capacitor value is given by the below equations:



$$C'_{tune} = \frac{1}{(2\pi \cdot 13.56 \text{ MHz})^2 \cdot L_{ant}} \quad where \ C'_{tune} = \frac{1}{2} \cdot \left(C_p + C_{int} + C_{tune}\right)$$

$$and \ C_{tune1} = C_{tune2} = C_{tune} \qquad C_{p1} = C_{p2} = C_p \qquad C_{int1} = C_{int2} = C_{int}$$

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56 \text{ MHz})^2 \cdot L_{ant}} - C_p - C_{int}$$

An antenna inductance of $L_{ant} = 2 \mu H$ will give tuning capacitors in the range of 130 pF on each pin. The total capacitance on **NFC1** and **NFC2** must be matched.

41.11 Battery protection

If the antenna is exposed to a strong NFC field, current may flow in the opposite direction on the supply due to parasitic diodes and ESD structures.

If the battery used does not tolerate return current, a series diode must be placed between the battery and the device in order to protect the battery.

41.12 References

NFC Forum, NFC Analog Specification version 1.0, www.nfc-forum.org

NFC Forum, NFC Digital Protocol Technical Specification version 1.1, www.nfc-forum.org

NFC Forum, NFC Activity Technical Specification version 1.1, www.nfc-forum.org

41.13 Registers

Table 91: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40005000	NFCT	NFCT	Near field communication tag		

Table 92: Register Overview

Register	Offset	Description
TASKS_ACTIVATE	0x000	Activate NFCT peripheral for incoming and outgoing frames, change state to activated
TASKS_DISABLE	0x004	Disable NFCT peripheral
TASKS_SENSE	0x008	Enable NFC sense field mode, change state to sense mode
TASKS_STARTTX	0x00C	Start transmission of an outgoing frame, change state to transmit
TASKS_ENABLERXDATA	0x01C	Initializes the EasyDMA for receive.
TASKS_GOIDLE	0x024	Force state machine to IDLE state
TASKS_GOSLEEP	0x028	Force state machine to SLEEP_A state
EVENTS_READY	0x100	The NFCT peripheral is ready to receive and send frames
EVENTS_FIELDDETECTED	0 0x104	Remote NFC field detected
EVENTS_FIELDLOST	0x108	Remote NFC field lost
EVENTS_TXFRAMESTART	0x10C	Marks the start of the first symbol of a transmitted frame
EVENTS_TXFRAMEEND	0x110	Marks the end of the last transmitted on-air symbol of a frame
EVENTS_RXFRAMESTAR	I 0x114	Marks the end of the first symbol of a received frame
EVENTS_RXFRAMEEND	0x118	Received data has been checked (CRC, parity) and transferred to RAM, and EasyDMA has ended
		accessing the RX buffer
EVENTS_ERROR	0x11C	NFC error reported. The ERRORSTATUS register contains details on the source of the error.



Register	Offset	Description
EVENTS_RXERROR	0x128	NFC RX frame error reported. The FRAMESTATUS.RX register contains details on the source of the
		error.
EVENTS_ENDRX	0x12C	RX buffer (as defined by PACKETPTR and MAXLEN) in Data RAM full.
EVENTS_ENDTX	0x130	Transmission of data in RAM has ended, and EasyDMA has ended accessing the TX buffer
EVENTS_AUTOCOLRESS	T 0x138	Auto collision resolution process has started
EVENTS_COLLISION	0x148	NFC auto collision resolution error reported.
EVENTS_SELECTED	0x14C	NFC auto collision resolution successfully completed
EVENTS_STARTED	0x150	EasyDMA is ready to receive or send frames.
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSTATUS	0x404	NFC Error Status register
FRAMESTATUS.RX	0x40C	Result of last incoming frame
NFCTAGSTATE	0x410	NfcTag state register
FIELDPRESENT	0x43C	Indicates the presence or not of a valid field
FRAMEDELAYMIN	0x504	Minimum frame delay
FRAMEDELAYMAX	0x508	Maximum frame delay
FRAMEDELAYMODE	0x50C	Configuration register for the Frame Delay Timer
PACKETPTR	0x510	Packet pointer for TXD and RXD data storage in Data RAM
MAXLEN	0x514	Size of the RAM buffer allocated to TXD and RXD data storage each
TXD.FRAMECONFIG	0x518	Configuration of outgoing frames
TXD.AMOUNT	0x51C	Size of outgoing frame
RXD.FRAMECONFIG	0x520	Configuration of incoming frames
RXD.AMOUNT	0x524	Size of last incoming frame
NFCID1_LAST	0x590	Last NFCID1 part (4, 7 or 10 bytes ID)
NFCID1_2ND_LAST	0x594	Second last NFCID1 part (7 or 10 bytes ID)
NFCID1_3RD_LAST	0x598	Third last NFCID1 part (10 bytes ID)
AUTOCOLRESCONFIG	0x59C	Controls the auto collision resolution function. This setting must be done before the NFCT peripheral
		is enabled.
SENSRES	0x5A0	NFC-A SENS_RES auto-response settings
SELRES	0x5A4	NFC-A SEL_RES auto-response settings

41.13.1 SHORTS

Address offset: 0x200

Shortcut register

		J																														
Bit r	numbe	er		31	30 2	9 2	28 2	7 2	6 25	24	23 2	22 2	21 20	19	9 18	17	16	15	14	13	12	11	10	9	8	7	6	5	4 3	3 2	1	0
Id																												F			В	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	tion																			
Α	RW	FIELDDETECTED_ACTIVAT	E								Sho	rtcu	ıt be	twe	en	FIEL	DD	ETE	CTE	D e	ver	ıt aı	nd /	ACT	IVA	ATE	tas	k				
											See	EVE	ENTS	_FI	ELD	DET	ECT	ED	and	I TA	SKS	5_A	СТІ	VA1	E							
			Disabled	0							Disa	ble	sho	rtcı	ıt																	
			Enabled	1							Enal	ble	shor	tcu	t																	
В	RW	FIELDLOST_SENSE									Sho	rtcu	ıt be	twe	een	FIEL	DLO	OST	eve	nt	and	SE	NSE	ta	sk							
											See	EVE	ENTS	_FI	ELD	LOS	T aı	nd 1	TASI	(S	SΕΛ	ISE										
			Disabled	0							Disa	ble	sho	rtcı	ıt																	
			Enabled	1							Enal	ble	shor	tcu	t																	
F	RW	TXFRAMEEND_ENABLERX	[Sho	rtcu	ıt be	twe	en	TXF	RAN	ИEE	ND	eve	ent	and	l EN	IAB	LER	RXD	ATA	4 ta	sk			
											See	EVE	ENTS		(FR)	4ME	EN	D a	nd 7	AS	KS_	ENA	4 <i>BL</i>	ER)	(DA	TA						
			Disabled	0							Disa	ble	sho	rtcı	ıt																	
			Enabled	1							Enal	ble	shor	tcu	t																	



41.13.2 INTEN

Address offset: 0x300

Enable or disable interrupt

L11	abic	e or disable interru	ирг		
Bitı	numbe	er		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					TSR NMLK HGFEDCBA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	READY			Enable or disable interrupt for READY event
					See EVENTS_READY
			Disabled	0	Disable
			Enabled	1	Enable
В	RW	FIELDDETECTED			Enable or disable interrupt for FIELDDETECTED event
					See EVENTS_FIELDDETECTED
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	FIELDLOST			Enable or disable interrupt for FIELDLOST event
					Son EVENTS EIELDLOST
			Disabled	0	See EVENTS_FIELDLOST Disable
			Enabled	1	Enable
D	RW	TXFRAMESTART	Lilabica	1	Enable or disable interrupt for TXFRAMESTART event
	11.00	TATIO WILLS IT WIT			·
				_	See EVENTS_TXFRAMESTART
			Disabled	0	Disable
_	DIA	TVEDALAEEAID	Enabled	1	Enable
E	RW	TXFRAMEEND			Enable or disable interrupt for TXFRAMEEND event
					See EVENTS_TXFRAMEEND
			Disabled	0	Disable
			Enabled	1	Enable
F	RW	RXFRAMESTART			Enable or disable interrupt for RXFRAMESTART event
					See EVENTS_RXFRAMESTART
			Disabled	0	Disable
			Enabled	1	Enable
G	RW	RXFRAMEEND			Enable or disable interrupt for RXFRAMEEND event
					See EVENTS_RXFRAMEEND
			Disabled	0	Disable
			Enabled	1	Enable
Н	RW	ERROR			Enable or disable interrupt for ERROR event
					See EVENTS_ERROR
			Disabled	0	Disable
			Enabled	1	Enable
K	RW	RXERROR			Enable or disable interrupt for RXERROR event
			Disabled	0	See EVENTS_RXERROR
			Disabled Enabled	0	Disable Enable
L	R\M/	ENDRX	Eliableu	1	Enable or disable interrupt for ENDRX event
-	11.00	LIVOIX			
					See EVENTS_ENDRX
			Disabled	0	Disable
	Ditt	FNDTV	Enabled	1	Enable Facility or disable interrupt for ENDTY quant
М	ĸW	ENDTX			Enable or disable interrupt for ENDTX event
					See EVENTS_ENDTX
			Disabled	0	Disable
			Enabled	1	Enable
N	RW	AUTOCOLRESSTARTED			Enable or disable interrupt for AUTOCOLRESSTARTED event
					See EVENTS_AUTOCOLRESSTARTED



Bitı	numbe	er		31	1 30	29	28	27	26	25 2	24 :	23 2:	2 21	20	19	18	17	16	15	14	13	12	11	10 !	9	8 7	7	6 5	5 4	3	2	1	O
Id														Т	S	R				N		M	L	K		H	+ (G F	E	D	С	В	Δ
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()	0 (0	0	0	0	o
Id	RW	Field	Value Id	Va	alue)					ı	Desc	ripti	on																			
			Disabled	0							- 1	Disak	ole																				
			Enabled	1							- 1	Enab	le																				
R	RW	COLLISION									- 1	Enab	le o	r dis	sabl	le ir	teri	rup	t fo	r CC	DLLI	ISIO	N e	ven	t								
												See	EVEN	NTS_	_co	LLIS	5101	V															
			Disabled	0							ı	Disab	ole																				
			Enabled	1							- 1	Enab	le																				
S	RW	SELECTED									ı	Enab	le o	r dis	sabl	le ir	iteri	rup	t fo	r SE	LEC	CTEI	D e	vent									
											:	See E	EVEN	NTS_	SE	LEC	TED																
			Disabled	0							ı	Disab	ole																				
			Enabled	1							- 1	Enab	le																				
Т	RW	STARTED									ı	Enab	le o	r dis	sabl	le ir	iteri	rup	t fo	r ST	AR	TED	ev	ent									
											:	See E	EVEN	NTS_	ST	ART	ED																
			Disabled	0							- 1	Disab	ole																				
			Enabled	1							ı	Enab	le																				

41.13.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numb	er		31	30 2	9 28	8 27	26.2	25 2	4 2	3 2	22 21	20	19	18	17	16	15	14	13	12	2 1	1 10) 9	8	7	6	5	4	3	2 .	1 0
Id														S					N				. K									 В А
	et 0x0	0000000		0	0 (0 0	0	0	0 (0 () (0 0				0	0	0							0							
Id		Field	Value Id	Val								criptic			_	_	Ť	Ť	_		Ť						Ť					
Α	RW	READY								٧	/rit	e '1' t	to E	nab	le i	nte	rru	pt '	or	RE/	۱D	Y e	ven	t								
										ς	مم	EVEN	TS	RF4	אַחוּ	,																
			Set	1							nak		,5_	,,,,,																		
			Disabled	0								d: Disa	able	-d																		
			Enabled	1								d: Ena																				
В	RW	FIELDDETECTED										e '1' t			le i	nte	rru	pt ·	or	FIEI	LDI	DE.	TEC	TED	eve	ent						
			.									EVEN	15_	FIEL	LDL)E I I	CI	ΈD														
			Set	1							nak																					
			Disabled Enabled	0								d: Disa d: Ena																				
С	D\A/	FIELDLOST	Enabled	1								u: Ena :e '1' t			i ما	nto	rri	nt:	or	CIEI	וח	0	ST c	won	+							
C	NVV	FIELDLOST								٧	VIIL	ет	LO E	IIau	ne i	me	110	ıμι	UI	FIE	וטו	LO.) i e	ven	t							
												EVEN	TS_	FIEL	LDL	OST	Γ															
			Set	1						Ε	nak	ble																				
			Disabled	0								d: Disa																				
			Enabled	1								d: Ena																				
D	RW	TXFRAMESTART								٧	/rit	:e '1' t	to E	nab	le i	nte	rru	pt '	or	TXF	RA	M	EST	ART	eve	ent						
										S	ee i	EVEN	TS_	TXF	RA	ME.	STA	4RT														
			Set	1						Ε	nak	ble																				
			Disabled	0						R	eac	d: Disa	able	ed																		
			Enabled	1						R	eac	d: Ena	ble	d																		
Ε	RW	TXFRAMEEND								٧	/rit	e '1' t	to E	nab	le i	nte	rru	pt '	or	TXF	RA	M	EEN	ID e	ven	t						
										S	ee	EVEN	TS_	TXF	RA	ME	ΕN	D														
			Set	1							nak																					
			Disabled	0						R	eac	d: Disa	able	ed																		
			Enabled	1						R	eac	d: Ena	ble	d																		
F	RW	RXFRAMESTART								٧	/rit	e '1' t	to E	nab	le i	nte	rru	pt '	or	RXF	R.A	١M	EST	ART	eve	ent						
										S	ee	EVEN	TS	RXF	RΔ	MF	STA	4 <i>R</i> 7														
			Set	1							nak		.5_				- 17	,														
				-						-																						



Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					TSR NMLK HGFEDCBA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	RXFRAMEEND			Write '1' to Enable interrupt for RXFRAMEEND event
					See EVENTS_RXFRAMEEND
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	ERROR			Write '1' to Enable interrupt for ERROR event
					See EVENTS_ERROR
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
K	RW	RXERROR			Write '1' to Enable interrupt for RXERROR event
					See EVENTS_RXERROR
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
L	RW	ENDRX			Write '1' to Enable interrupt for ENDRX event
					See EVENTS_ENDRX
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
М	RW	ENDTX			Write '1' to Enable interrupt for ENDTX event
					See EVENTS_ENDTX
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
N	RW	AUTOCOLRESSTARTED			Write '1' to Enable interrupt for AUTOCOLRESSTARTED event
					See EVENTS_AUTOCOLRESSTARTED
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
R	RW	COLLISION			Write '1' to Enable interrupt for COLLISION event
					See EVENTS_COLLISION
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
S	RW	SELECTED	2.100.00	-	Write '1' to Enable interrupt for SELECTED event
			Cat	1	See EVENTS_SELECTED
			Set Disabled	0	Enable Read: Disabled
			Enabled	1	Read: Enabled
Т	RW	STARTED	Litablea	-	Write '1' to Enable interrupt for STARTED event
•					
			C-4	4	See EVENTS_STARTED
			Set	1	Enable Death Disabled
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

41.13.4 INTENCLR

Address offset: 0x308



Disable interrupt

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 T S R N M L K H G F E D C B A
	et 0x0	000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	READY			Write '1' to Disable interrupt for READY event
					See EVENTS_READY
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	FIELDDETECTED			Write '1' to Disable interrupt for FIELDDETECTED event
			Clear	1	See EVENTS_FIELDDETECTED Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	FIELDLOST	Eliablea	-	Write '1' to Disable interrupt for FIELDLOST event
•					
					See EVENTS_FIELDLOST
			Clear	1	Disable
			Disabled	0	Read: Disabled
_			Enabled	1	Read: Enabled
D	RW	TXFRAMESTART			Write '1' to Disable interrupt for TXFRAMESTART event
					See EVENTS_TXFRAMESTART
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Ε	RW	TXFRAMEEND			Write '1' to Disable interrupt for TXFRAMEEND event
					See EVENTS_TXFRAMEEND
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	RXFRAMESTART			Write '1' to Disable interrupt for RXFRAMESTART event
					See EVENTS_RXFRAMESTART
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	RXFRAMEEND			Write '1' to Disable interrupt for RXFRAMEEND event
					See EVENTS_RXFRAMEEND
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	ERROR			Write '1' to Disable interrupt for ERROR event
					See EVENTS_ERROR
			Clear	1	Disable Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
K	RW	RXERROR	Eliablea	-	Write '1' to Disable interrupt for RXERROR event
					·
			Clear	1	See EVENTS_RXERROR
			Clear	1	Disable Pead: Disabled
			Disabled	0	Read: Disabled
L	D\A/	ENDRX	Enabled	1	Read: Enabled Write '1' to Disable interrupt for ENDRX event
	IVV	LINDINA			
					See EVENTS_ENDRX
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled



Bit r	number			31 30	29 :	28 27	7 26 2	5 24	23	22 21	. 20	19	18	17 1	l6 1	L5 1	4 13	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id											Т	S	R			١	1	M	L	K			н	G	F	ΕI) C	В	Α
Res	et 0x000	00000		0 0	0	0 0	0 0	0	0	0 0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW Fi	ield	Value Id	Value	:				Des	scripti	ion																		
М	RW E	NDTX							Wri	ite '1'	to [Disa	ble	inte	rru	pt fo	r Eľ	NDT	Хe	ven	t								
									See	e EVEN	VTS_	EN	DTX																
			Clear	1					Disa	able																			
			Disabled	0					Rea	ad: Dis	sabl	ed																	
			Enabled	1					Rea	ad: En	able	ed																	
N	RW A	UTOCOLRESSTARTED							Wri	ite '1'	to [Disa	ble	inte	rru	pt fo	r Al	UTC	СО	LRE	SST	ART	ED (eve	nt				
									See	e EVEN	VTS_	AU	тос	OLF	RESS	STAF	RTEL	ס											
			Clear	1					Disa	able																			
			Disabled	0					Rea	ad: Dis	sabl	ed																	
			Enabled	1					Rea	ad: En	able	ed																	
R	RW C	OLLISION							Wri	ite '1'	to [Disa	ble	inte	rru	pt fo	or Co	OLL	ISIC)N e	ven	t							
									See	e EVEN	VTS_	co	LLIS	ION															
			Clear	1					Disa	able																			
			Disabled	0					Rea	ad: Dis	sabl	ed																	
			Enabled	1					Rea	ad: En	able	ed																	
S	RW SE	ELECTED							Wri	ite '1'	to [Disa	ble	inte	rru	pt fo	or SE	ELEC	CTE	D ev	/ent								
									See	e EVEN	NTS_	SEL	EC1	ED															
			Clear	1					Disa	able																			
			Disabled	0					Rea	ad: Dis	sabl	ed																	
			Enabled	1					Rea	ad: En	able	ed																	
Т	RW ST	TARTED							Wri	ite '1'	to [Disa	ble	inte	rru	pt fo	or ST	ΓAR	TEC	eve	ent								
									See	e EVEN	VTS_	STA	\RTI	ED															
			Clear	1					Disa	able																			
			Disabled	0					Rea	ad: Dis	sabl	ed																	
			Enabled	1					Rea	ad: En	able	ed																	

41.13.5 ERRORSTATUS

Address offset: 0x404

NFC Error Status register

Write a bit to '1' to clear it. Writing '0' has no effect.

Bit r	umbe	er		33	1 30	29	28	27 2	26 2	25 2	4 2	23 2	2 2	1 2	0 19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 :	2 :	1 ()
Id																																	A	4
Res	t 0x0	0000000		0	0	0	0	0	0	0 () (0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () ()
Id	RW	Field	Value Id	V	alue	•					C	Desc	rip	tior	ı																			ı
Α	RW	FRAMEDELAYTIMEOUT									Ν	No S	TAF	RTT.	X tas	sk t	rigg	ere	d be	for	e e	xpir	atio	on c	of th	ne t	ime	e se	t in					
											F	RAI	MEI	DEL	AYN	1AX																		

41.13.6 FRAMESTATUS.RX

Address offset: 0x40C

Result of last incoming frame

Write a bit to '1' to clear it. Writing '0' has no effect.

Bit	numbe	er		31 30	29	28	27 2	26 2	25 24	4 23	3 22	2 21	20	19	18 :	17 1	16 1	5 14	13	12	11 1	0 9	8	7	6	5	4	3	2 1	0
Id																												С	3	Α
Res	et 0x0	0000000		0 0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0	0	0	0 (0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Value	•					D	esci	ripti	on																	
Α	RW	CRCERROR								Ν	o va	alid	end	of f	ram	e (I	EoF)	det	ecte	d										
			CRCCorrect	0						V	alid	CRO	C de	tect	ed															
			CRCError	1						CI	RC r	ece	ivec	d do	es n	ot r	mate	h lo	cal	chec	k									



Bit r	numbe	er		31	1 30	29	2	8 27	7 2	6 2	5 2	24	23 :	22	21	20	19	18	17	7 16	5 1	5 1	4 1	3 1	2 1	1 1	0 9	8	7	6	5	4	3	2	1	0
Id																																	С	В		Α
Rese	et 0x0	0000000		0	0	0	0	0	(0 ()	0	0	0	0	0	0	0	0	0	C	0) () (0 () (0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue								Des	cri	ipti	on																				
В	RW	PARITYSTATUS											Pari	ity	sta	tus	of	rec	eiv	ed	fra	me														
			ParityOK	0									Frai	me	re	ceiv	ved	l wi	th	pari	ity	ОК														
			ParityError	1									Frai	me	re	ceiv	ved	l wi	th	pari	ity	erro	or													
С	RW	OVERRUN											Ove	erru	un d	det	ect	ed																		
			NoOverrun	0									No	ove	errı	un (det	ect	ed																	
			Overrun	1									Ove	erru	un e	erro	or																			

41.13.7 NFCTAGSTATE

Address offset: 0x410 NfcTag state register

Bit	numb	er		3:	1 30	29	28	27	26 2	5 2	4 23	3 22	21 2	20 :	19 1	18	17 1	16	15 1	.4 1	13 :	12 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																														Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 (0	0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	V	alue						De	escr	iptio	n																		
Α	R	NFCTAGSTATE									Nf	сТа	g sta	te																		
			Disabled	0							Di	sab	ed o	r se	ense	9																
			RampUp	2							Ra	mp	Up																			
			Idle	3							Idl	le																				
			Receive	4							Re	cei	/e																			
			FrameDelay	5							Fra	ame	Dela	ay																		
			Transmit	6							Tra	ans	mit																			

41.13.8 FIELDPRESENT

Address offset: 0x43C

Indicates the presence or not of a valid field

Bitı	numbe	er		31	30	29	28	27	20	5 25	5 2	4 2	3 2	22 :	21	20	19	18	17	7 16	5 1	5 1	4 1	3 1	2 1	1 1	.0 9	9 1	3 7	' (5 5	5 4	1 3	2	1	0
Id																																			В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	C) (0	0	0	0	0	0	0	0	C) () () () (0	0 () () () () () (0	0	0	0
Id	RW	Field	Value Id	Va	lue							D)es	crip	otic	on																				
Α	R	FIELDPRESENT										Ir	ndi	cat	es	if a	va	lid	fiel	d is	pr	ese	nt.	Αv	aila	ble	on	ly iı	th	e a	ctiv	ate	d			
												S	tat	e.																						
			NoField	0								Ν	lo۱	vali	d fi	ield	l de	ete	cte	d																
			FieldPresent	1								٧	/ali	d fi	eld	de	ete	cte	b																	
В	R	LOCKDETECT										Ir	ndi	cat	es	if th	he	low	le	vel	has	s lo	cke	d to	o th	ne f	ield									
			NotLocked	0								Ν	lot	loc	ke	d to	o fi	eld																		
			Locked	1								L	ocl	ked	to	fie	ld																			

41.13.9 FRAMEDELAYMIN

Address offset: 0x504 Minimum frame delay

Bit r	numbe	r		31	30	29	28	27	26	25 :	24 :	23 :	22 2	21 2	20 1	19 1	8 1	7 1	6 1	5 1	4 1	3 12	2 11	. 10	9	8	7	6	5	4	3	2 1	1 0
Id																			A	A A	Α Α	. Δ	. A	Α	Α	Α	Α	Α	Α	Α	Α /	A A	A A
Res	et 0x0	0000480		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	1	0	0	1	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	tio	n																		
Α	RW	FRAMEDELAYMIN										Min	imu	ım	frar	ne	dela	ıy ir	า ทน	ımb	er (of 1	3.56	5 M	Hz c	locl	(S						

Minimum frame delay in number of 13.56 MHz clocks

41.13.10 FRAMEDELAYMAX

Address offset: 0x508



Maximum frame delay

Bit	numbe	er		31	L 30	29	28	27	26	25 :	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et OxC	0001000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																			
Δ	R\M	ERAMEDEL AVMAY										NΛο	vin	าเเท	fr	m	a da	ıləv	, in	nur	nhe	r o	f 13	56	N/I	-17 C	·loc	Ьc						

41.13.11 FRAMEDELAYMODE

Address offset: 0x50C

Configuration register for the Frame Delay Timer

																																			_
Bit	numb	er		33	1 30	29	28	27	26	25	24	23	22 2	21 2	0 1	19 1	18 1	17 1	.6 1	15 :	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		Α	Α
Res	et 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0 ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Id	RW	Field	Value Id	V	alue	•						Des	scrip	otio	1																				
Α	RW	FRAMEDELAYMODE										Cor	nfigu	urati	on	reg	giste	er f	or t	he	Fra	me	e De	elay	Tin	ner									
			FreeRun	0								Tra	nsm	nissio	on	is ir	nde	pen	de	nt c	of f	ran	ne t	ime	er a	nd	will	sta	art v	vhe	en				
												the	STA	ART1	Χt	ask	is	trig	ger	ed.	No	tir	ne	out.											
			Window	1								Fra	me	is tr	ans	mi	ttec	d be	tw	eer	n FR	RAN	ΛEC	DEL	٩YN	ΛIN	and	t							
												FR/	٩ME	DEL	ΑY	MA	Х																		
			ExactVal	2								Fra	me	is tr	ans	mi	ttec	d ex	act	ly a	it F	RAI	ME	DEL	IYA	MΑ	X								
			WindowGrid	3								Fra	me	is tr	ans	mi	ttec	d or	a l	oit (gric	l be	etw	eer	FR	AN	1ED	EL/	NΥ	1IN					
												and	d FR	AME	DE	ELA'	YΜ	AX																	

41.13.12 PACKETPTR

Address offset: 0x510

Packet pointer for TXD and RXD data storage in Data RAM

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20 :	19 :	18 1	7 1	6 1	5 1	4 1	3 1	2 1:	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ /	4 4	۱ ۸	Δ Δ	. 4	A	. A	Α	Α	Α	Α	Α	Α	A	Δ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 () (0	•	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	PTR										Pac	ket	poi	inte	r fo	r TX	(D a	nd	RXI	D da	ita	stor	age	in I	Dat	a RA	١M.	Thi	is			
												adr	Iroc	c ic	a h	vto.	-alia	nor	1 R /	LΛ	hhc	roc	c										

41.13.13 MAXLEN

Address offset: 0x514

Size of the RAM buffer allocated to TXD and RXD data storage each

Bitı	numb	er		31	L 30	29	28 2	27 26	5 2	5 24	1 23	22	21	20	19	18 :	17 1	6 1	5 14	4 13	12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id																									A .	Α,	Α,	4 Δ	A	Α	Α	Α
Res	et 0x0	00000000		0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0
Id	RW	Field	Value Id	Va	alue						De	scri	iptio	on																		
Α	RW	MAXLEN		[0	25	7]					Siz	e o	f th	e RA	MA	buff	er a	lloc	ate	d to	TXE	an)	d RX	(D	data	sto	ora	ge				
											ea	ch																				

41.13.14 TXD.FRAMECONFIG

Address offset: 0x518

Configuration of outgoing frames

Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Id			D	СВА
Reset 0x00000017		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 1
ld RW Field	Value Id	Value	Description	
A RW PARITY			Indicates if parity is added to the frame	



Bitı	numbe	er		31	30 2	29 :	28 2	7 2	26 2	5 2	24	23 2	22 2	21 2	0 :	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	! 1	0
Id																															D	(В	Α
Res	et 0x0	0000017		0	0	0	0 ()	0 (0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0 1	. 1	. 1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			
			NoParity	0								Pari	ty i	s no	t a	dde	ed 1	to T	Χf	ran	nes													
			Parity	1								Pari	ty i	s ad	lde	d to	o TX	X fr	am	es														
В	RW	DISCARDMODE										Disc	ard	ling	un	use	ed b	oits	at	sta	t o	r er	d c	f a	frar	ne								
			DiscardEnd	0								Unu	sec	d bit	s a	re o	disc	card	ded	at	enc	lof	fra	me	(Eo	F)								
			DiscardStart	1								Unu	sec	d bit	s a	re o	disc	card	ded	at	sta	rt o	f fra	ame	(So	oF)								
С	RW	SOF										Add	ing	SoF	10	no	t ir	ι TX	(fr	am	es													
			NoSoF	0								SoF	syn	nbo	l n	ot a	dd	ed																
			SoF	1								SoF	syn	nbo	l ad	dde	d																	
D	RW	CRCMODETX										CRC	mo	ode	for	ou	itgo	oing	g fra	ame	es													
			NoCRCTX	0								CRC	is i	not	ado	ded	to	the	e fr	am	е													
			CRC16TX	1								16 b	it C	CRC	ad	ded	l to	the	e fr	am	e b	ase	d o	n all	the	e da	ata ı	rea	d fr	om				
												RAN	1 th	nat i	s u	sed	l in	the	fra	am	9													

41.13.15 TXD.AMOUNT

Address offset: 0x51C Size of outgoing frame

Bitı	numbe	er		31 3	0 29	28	27	26 2	5 24	4 2	3 2	2 2	1 2	0 19	9 18	3 17	16	15	14	13	12 1	1 1	9	8	7	6	5	4	3 2	2 1	١ 0
Id																					E	3 E	В	В	В	В	В	В	ВА	A A	A A
Res	et 0x0	0000000		0 (0	0	0	0 0	0	0) (0 (0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0 (
Id	RW	Field	Value Id	Valu	e					D	esc	crip	tion	١																	
A	RW	TXDATABITS		[07]					b TI bi	e ir he its	nclu DIS is d	ided CAR	l in RDIV rde	the IOD d at	frar E fie	ne (eld i e sta	exc n Ff	ludi RAM or at	ing MEC	oarit ONF e end	y bi IG.1	rom t). 'X se a fra	lect	s if	unı	ısed	d			
В	RW	TXDATABYTES		[02	57]								r of ng C								be	incl	uded	l in t	the	frai	me,				

41.13.16 RXD.FRAMECONFIG

Address offset: 0x520

Configuration of incoming frames

Bit r	numbe	er		31	30	29	28 2	27 :	26 2	25 2	24 2	23 2:	2 2:	1 20	19	18	17	16	15	14	13	12 :	11 1	0 9	8	7	6	5	4 3	3 2	1	0
Id																													С	В		Α
Res	et 0x0	0000015		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	1 () 1	0	1
Id	RW	Field	Value Id	Va	lue							Desc	ript	ion																		
Α	RW	PARITY									- 1	ndic	ate	s if p	arit	y e	хре	cte	d in	RX	fra	me										$\overline{}$
			NoParity	0							F	Parit	y is	not	exp	ect	ed i	n R	X fr	am	es											
			Parity	1							F	Parit	y is	ехр	ecte	d ii	n R)	(fra	ame	es												
В	RW	SOF									S	SoF e	expe	ecte	d or	no	t in	RX	fra	mes	,											
			NoSoF	0							S	oF s	ym	bol i	s no	ot e	хре	cte	d in	RX	fra	mes	5									
			SoF	1							S	oF s	ym	bol i	s ex	рес	cted	d in	RX	frar	nes											
С	RW	CRCMODERX									(CRC	mod	de fo	or in	cor	nin	g fr	ame	es												
			NoCRCRX	0							(CRC i	is n	ot ex	фес	tec	l in	RX	frai	nes												
			CRC16RX	1							L	.ast	16 k	oits i	n R	X fr	ame	e is	CRO	c, CI	RC i	is ch	eck	ed a	nd	CRC	STA	TUS	,			
											ι	ıpda	ted																			

41.13.17 RXD.AMOUNT

Address offset: 0x524

Size of last incoming frame



Bit	numbe	er		31	. 30	29	28	8 27	7 2	6 2	5 2	4 2	3 22	2 21	L 20	19	18	17	16	15	14	13	12 :	11 :	10 9) ;	8 7	6	5	4	3	2	1	0
Id																								В	ВЕ	3	ВВ	В	В	В	В	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	(0 0) (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	llue							D	esc	ripti	ion																			
Α	R	RXDATABITS										N	um	ber	of b	its	in t	he	last	byt	e ir	the	e fra	me	, if I	ess	tha	n 8						
												(i	nclu	ıdin	g CF	RC,	but	ex	cluc	ling	pai	ity	and	Sol	-/Ec	F f	ram	ing)).					
												F	ram	es v	with	0 0	data	by	tes	and	les	s th	an '	7 da	ata b	oits	are	inv	alid	ı				
												a	nd a	are i	not	rec	eive	ed p	rop	erly	<i>/</i> .													
В	R	RXDATABYTES										N	um	ber	of c	om	ple	te k	oyte	s re	cei	ved	in t	he i	fram	ne ((incl	udii	ng C	CRC,				
												b	ut e	xclu	udin	g p	arit	y aı	nd S	oF/	EoF	fra	min	g)										

41.13.18 NFCID1_LAST

Address offset: 0x590

Last NFCID1 part (4, 7 or 10 bytes ID)

Bit r	iumbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 :	LO	9 8	3 7	' 6	5	4	3	2	1	0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	В	В	В	В	В	В	В	3 <i>A</i>	Α	Α	Α	Α	Α	Α	Α
Rese	et 0x0	0006363		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1 :	LC) 1	1	0	0	0	1	1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	NFCID1_Z										NF	CID	1 by	yte	Z (v	/ery	/ las	st b	yte	ser	ıt)												
В	RW	NFCID1_Y										NF	CID	1 by	yte	Υ																		
С	RW	NFCID1_X										NF	CID	1 by	yte	Х																		
D	RW	NFCID1_W										NF	CID	1 by	yte	W																		

41.13.19 NFCID1_2ND_LAST

Address offset: 0x594

Second last NFCID1 part (7 or 10 bytes ID)

Bit r	iumbe	r		31 30	29	28	27	26	25	24	23	22 :	21 2	0 1	9 18	3 17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3	2 1	0
Id											С	С	С	С (C C	С	С	В	В	В	ВВ	В	В	В	Α	Α	Α	Α	Α	Д Д	A
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Value	9						De	scrip	otio	n																	
Α	RW	NFCID1_V									NF	CID1	l by	te V																	
В	RW	NFCID1_U									NF	CID1	l by	te U																	
С	RW	NFCID1_T									NF	CID1	l by	e T																	

41.13.20 NFCID1_3RD_LAST

Address offset: 0x598

Third last NFCID1 part (10 bytes ID)

Bitı	numbe	er		31	30	29	28	3 27	7 2	6 2	25 :	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id													С	С	С	С	С	С	С	С	В	В	В	В	В	В	В	В	Α	Α	Α	Α	A A	۱	A
Res	et 0x0	0000000		0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue								De	cri	pti	on																			
Α	RW	NFCID1_S											NF	CID	1 b	yte	S																		
В	RW	NFCID1_R											NF	CID	1 b	yte	R																		
_	R\M	NFCID1 Q											NF	חו־	1 h	νtο	Λ																		

41.13.21 AUTOCOLRESCONFIG

Address offset: 0x59C

Controls the auto collision resolution function. This setting must be done before the NFCT peripheral is enabled.



Bitı	numbe	er		31 30	29	28 2	27 2	26 2	.5 24	1 23	3 22	21	20 1	L9 1	8 17	7 16	15	14	13 1	2 1	1 10	9	8	7	6	5	4 3	2	1 0
Id																													А
Res	et 0x0	0000002		0 0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	1 0
Id	RW	Field	Value Id	Value						D	escri	iptio	on																
Α	RW	MODE								Er	able	es/d	lisab	les a	auto	col	lisic	n re	solu	ıtior	1								
			Enabled	0						Αι	uto d	colli	sion	reso	oluti	on e	enal	bled											
	Disabled			1						Αι	uto d	colli	sion	reso	oluti	on (disa	bled											

41.13.22 SENSRES

Address offset: 0x5A0

NFC-A SENS_RES auto-response settings

Bit	numbe	er		31	30	29	28	27	26	25	24	23 2	22 :	21	20	19	18	17	16	15	14	13	12	2 11	10	9	8	7	6	5	4	3 2	1	. 0
Id																				Ε	Ε	Ε	Ε	D	D	D	D	С	С	В	Α /	Δ Δ	. Α	A
Res	et 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	1
Id	RW	Field	Value Id	Va	lue							Des	cri	otic	n																			
Α	RW	BITFRAMESDD										Bit f	frar	ne:	SDI	D as	de	efin	ed	by ·	the	b5	:b1	of	byte	e 1 i	n Sl	NS.	_RE	S				
												resp	oon	se i	in t	he	NF	C Fo	ru	m, I	۷F	C Di	gita	al P	roto	col	Tec	hni	cal					
												Spe	cifi	cati	ion																			
			SDD00000	0								SDD) pa	itte	rn (000	00																	
			SDD00001	1								SDD) pa	itte	rn (000	01																	
			SDD00010	2								SDD) pa	itte	rn (000	10																	
			SDD00100	4								SDD) pa	itte	rn (001	.00																	
			SDD01000	8								SDD) pa	itte	rn (010	00																	
			SDD10000	16								SDD) pa	itte	rn :	100	00																	
В	RW	RFU5										Res	erv	ed	for	fut	ure	us	e. S	hal	Ιb	e 0.												
С	RW	NFCIDSIZE										NFC	CID1	l siz	ze.	Thi	s va	lue	is	use	d l	y tl	ne a	aut	о со	llisi	on r	eso	luti	on				
												eng	ine																					
			NFCID1Single	0								NFC	CID1	l siz	ze:	sing	gle	(4 k	yte	es)														
			NFCID1Double	1								NFC	CID1	l siz	ze:	dοι	ıble	e (7	by	tes)													
			NFCID1Triple	2								NFC	CID1	l siz	ze:	trip	le (10	byt	es)														
D	RW	PLATFCONFIG										Tag	pla	tfo	rm	coı	nfig	ura	tio	n a	s d	efin	ed	by	the	b4:	b1 c	of by	yte	2				
												in S	ENS	S_R	ES	res	por	ise	in t	he	NF	C F	oru	m,	NFC	Dig	gital	Pro	otoc	ol				
												Tecl	hni	cal	Spe	ecif	icat	ion																
Е	RW	RFU74										Res	erv	ed	for	fut	ure	us	e. S	hal	Ιb	e 0.												

41.13.23 SELRES

Address offset: 0x5A4

NFC-A SEL_RES auto-response settings

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												Ε	D	D	С	С	В	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scr	iptio	on																				
Α	RW	RFU10										Re	ser	ved	for	r fut	ure	e us	e. S	hal	Ιb	e 0.													Γ
В	RW	CASCADE										Ca	sca	de a	as c	lefir	nec	l by	the	b3	of	SEI	_R	ES 1	esp	ons	e ir	n th	e N	FC					
												Fo	run	1, N	FC	Dig	ital	Pro	too	ol -	Гес	hni	cal	Spe	cifi	cati	on ((coı	ntro	lle	d				
												by	hai	rdw	are	, sh	all	be	0)																
С	RW	RFU43										Re	ser	ved	for	r fut	ure	e us	e. S	ha	Ιb	e 0.													
D	RW	PROTOCOL										Pr	oto	col a	as c	defi	nec	d by	the	e bī	7:b(of	SE	L_R	ES 1	resp	ons	se i	n th	e					
												NF	C F	oru	m,	NFC	Di	igita	l Pi	oto	СО	l Te	chi	nica	l Sp	ecit	icat	tior	1						
Е	RW	RFU7										Re	ser	ved	for	fut	ure	e us	e. S	hal	Ιb	e 0.													



41.14 Electrical specification

41.14.1 NFCT Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
	•		7.7		
t _c	Frequency of operation		13.56		MHz
C _{MI}	Carrier modulation index	95			%
DR	Data Rate		106		kbps
V _{sense}	Peak differential Field detect threshold level on NFC1-NFC2 ³²		0.59		Vp
I _{sense}	Current in SENSE STATE ³³		100		nA
I _{activated}	Current in ACTIVATED STATE		400		μΑ
I _{max}	Maximum input current on NFCT pins			80	mA

41.14.2 NFCT Timing Parameters

Symbol	Description	Min.	Тур.	Max.	Units
t _{activate}	Time from task_ACTIVATE in SENSE or DISABLE state to			500	μs
	ACTIVATE_A or IDLE state ³⁴				
t _{sense}	Time from remote field is present in SENSE mode to			20	μs
	FIELDDETECTED event is asserted				

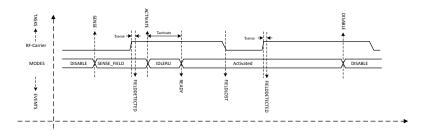


Figure 134: NFCT timing parameters (Shortcuts for FIELDDETECTED and FIELDLOST are disabled)

Input is high impedance in sense mode
This current does not apply when in NFC field
Does not account for voltage supply and oscillator startup times



42 PDM — Pulse density modulation interface

The pulse density modulation (PDM) module enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. The PDM module generates the PDM clock and supports single-channel or dual-channel (Left and Right) data input. Data is transferred directly to RAM buffers using EasyDMA.

Listed here are the main features for PDM:

- Up to two PDM microphones configured as a Left/Right pair using the same data input
- 16 kHz output sample rate, 16-bit samples
- EasyDMA support for sample buffering
- · HW decimation filters
- Selectable ratio of 64 or 80 between PDM_CLK and output sample rate

The PDM module illustrated in *Figure 135: PDM module* on page 499 is interfacing up to two digital microphones with the PDM interface. It implements EasyDMA, which relieves real-time requirements associated with controlling the PDM slave from a low priority CPU execution context. It also includes all the necessary digital filter elements to produce PCM samples. The PDM module allows continuous audio streaming.

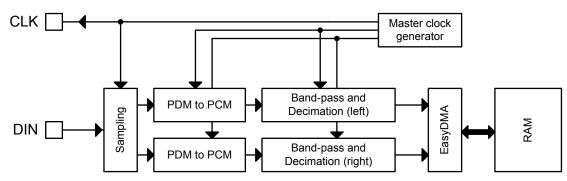


Figure 135: PDM module

42.1 Master clock generator

The FREQ field in the master clock's PDMCLKCTRL register allows adjusting the PDM clock's frequency.

The master clock generator does not add any jitter to the HFCLK source chosen. It is recommended (but not mandatory) to use the Xtal as HFCLK source.

42.2 Module operation

By default, bits from the left PDM microphone are sampled on PDM_CLK falling edge, bits for the right are sampled on the rising edge of PDM_CLK, resulting in two bitstreams. Each bitstream is fed into a digital filter which converts the PDM stream into 16-bit PCM samples, and filters and down-samples them to reach the appropriate sample rate.

The EDGE field in the MODE register allows swapping Left and Right, so that Left will be sampled on rising edge, and Right on falling.

The PDM module uses EasyDMA to store the samples coming out from the filters into one buffer in RAM.

Depending on the mode chosen in the OPERATION field in the MODE register, memory either contains alternating left and right 16-bit samples (Stereo), or only left 16-bit samples (Mono).

To ensure continuous PDM sampling, it is up to the application to update the EasyDMA destination address pointer as the previous buffer is filled.



The continuous transfer can be started or stopped by sending the START and STOP tasks. STOP becomes effective after the current frame has finished transferring, which will generate the STOPPED event. The STOPPED event indicates that all activity in the module are finished, and that the data is available in RAM (EasyDMA has finished transferring as well). Attempting to restart before receiving the STOPPED event may result in unpredictable behaviour.

42.3 Decimation filter

In order to convert the incoming data stream into PCM audio samples, a decimation filter is included in the PDM interface module.

The input of the filter is the two-channel PDM serial stream (with left channel on clock high, right channel on clock low). Depending on the RATIO selected, its output is 2×16 -bit PCM samples at a sample rate either 64 times or 80 times (depending on the RATIO register) lower than the PDM clock rate.

The filter stage of each channel is followed by a digital volume control, to attenuate or amplify the output samples in a range of -20 dB to +20 dB around the default (reset) setting, defined by $G_{PDM,default}$. The gain is controlled by the GAINL and GAINR registers.

As an example, if the goal is to achieve 2500 RMS output samples (16 bit) with a 1 kHz 90 dBA signal into a -26 dBFS sensitivity PDM microphone, the user will have to sum the PDM module's default gain ($G_{PDM,default}$) and the gain introduced by the microphone and acoustic path of his implementation (an attenuation would translate into a negative gain), and adjust GAINL and GAINR by this amount. Assuming that only the PDM module influences the gain, GAINL and GAINR must be set to - $G_{PDM,default}$ dB to achieve the requirement.

With G_{PDM,default}=3.2 dB, and as GAINL and GAINR are expressed in 0.5 dB steps, the closest value to program would be 3.0 dB, which can be calculated as:

```
GAINL = GAINR = (DefaultGain - (2 * 3))
```

Remember to check that the resulting values programmed into GAINL and GAINR fall within MinGain and MaxGain.

42.4 EasyDMA

Samples will be written directly to RAM, and EasyDMA must be configured accordingly.

The address pointer for the EasyDMA channel is set in SAMPLE.PTR register. If the destination address set in SAMPLE.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

DMA supports Stereo (Left+Right 16-bit samples) and Mono (Left only) data transfer, depending on setting in the OPERATION field in the MODE register. The samples are stored little endian.

Table 93: DMA sample storage

MODE.OPERATION	Bits per sample	Result stored per RAM word	Physical RAM allocated (32 bit words)	Result boundary indexes in RAM	Note
Stereo	32 (2x16)	L+R	ceil(SAMPLE.MAXCNT/2)	R0=[31:16]; L0=[15:0]	Default
Mono	16	2xL	ceil(SAMPLE.MAXCNT/2)	L1=[31:16]; L0=[15:0]	

The destination buffer in RAM consists of one block, the size of which is set in SAMPLE.MAXCNT register. Format is number of 16-bit samples. The physical RAM allocated is always:

```
(RAM allocation, in bytes) = SAMPLE.MAXCNT * 2;
```

(but the mapping of the samples depends on MODE.OPERATION.

If OPERATION=Stereo, RAM will contain a succession of Left and Right samples.

If OPERATION=Mono, RAM will contain a succession of mono samples.



For a given value of SAMPLE.MAXCNT, the buffer in RAM can contain half the stereo sampling time as compared to the mono sampling time.

The PDM acquisition can be started by the START task, after the SAMPLE.PTR and SAMPLE.MAXCNT registers have been written. When starting the module, it will take some time for the filters to start outputting valid data. Transients from the PDM microphone itself may also occur. The first few samples (typically around 50) might hence contain invalid values or transients. It is therefore advised to discard the first few samples after a PDM start.

As soon as the STARTED event is received, the firmware can write the next SAMPLE.PTR value (this register is double-buffered), to ensure continuous operation.

When the buffer in RAM is filled with samples, an END event is triggered. The firmware can start processing the data in the buffer. Meanwhile, the PDM module starts acquiring data into the new buffer pointed to by SAMPLE.PTR, and sends a new STARTED event, so that the firmware can update SAMPLE.PTR to the next buffer address.

42.5 Hardware example

Connect the microphone clock to CLK, and data to DIN.



Figure 136: Example of a single PDM microphone, wired as left



Figure 137: Example of a single PDM microphone, wired as right

Note that in a single-microphone (mono) configuration, depending on the microphone's implementation, either the left or the right channel (sampled at falling or rising CLK edge respectively) will contain reliable data. If two microphones are used, one of them has to be set as left, the other as right (L/R pin tied high or to GND on the respective microphone). It is strongly recommended to use two microphones of exactly the same brand and type so that their timings in left and right operation match.

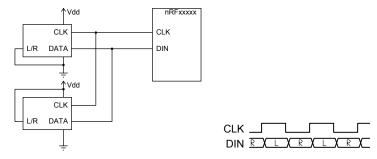


Figure 138: Example of two PDM microphones

42.6 Pin configuration

The CLK and DIN signals associated to the PDM module are mapped to physical pins according to the configuration specified in the PSEL.CLK and PSEL.DIN registers respectively. If the CONNECT field in any PSEL register is set to Disconnected, the associated PDM module signal will not be connected to the required physical pins, and will not operate properly.



The PSEL.CLK and PSEL.DIN registers and their configurations are only used as long as the PDM module is enabled, and retained only as long as the device is in System ON mode. See *POWER* — *Power supply* on page 66 for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register.

To ensure correct behaviour in the PDM module, the pins used by the PDM module must be configured in the GPIO peripheral as described in *Table 94: GPIO configuration before enabling peripheral* on page 502 before enabling the PDM module. This is to ensure that the pins used by the PDM module are driven correctly if the PDM module itself is temporarily disabled or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the PDM module is supposed to be connected to an external PDM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behaviour.

Table 94: GPIO configuration before enabling peripheral

PDM signal	PDM pin	Direction	Output value	Comment
CLK	As specified in PSEL.CLK	Output	0	
DIN	As specified in PSEL.DIN	Input	Not applicable	

42.7 Registers

Table 95: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001D000	PDM	PDM	Pulse Density modulation (digital	
			microphone) interface	

Table 96: Register Overview

Register	Offset	Description
TASKS_START	0x000	Starts continuous PDM transfer
TASKS_STOP	0x004	Stops PDM transfer
EVENTS_STARTED	0x100	PDM transfer has started
EVENTS_STOPPED	0x104	PDM transfer has finished
EVENTS_END	0x108	The PDM has written the last sample specified by SAMPLE.MAXCNT (or the last sample after a STOP
		task has been received) to Data RAM
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	PDM module enable register
PDMCLKCTRL	0x504	PDM clock generator control
MODE	0x508	Defines the routing of the connected PDM microphones' signals
GAINL	0x518	Left output gain adjustment
GAINR	0x51C	Right output gain adjustment
RATIO	0x520	Selects the ratio between PDM_CLK and output sample rate. Change PDMCLKCTRL accordingly.
PSEL.CLK	0x540	Pin number configuration for PDM CLK signal
PSEL.DIN	0x544	Pin number configuration for PDM DIN signal
SAMPLE.PTR	0x560	RAM address pointer to write samples to with EasyDMA
SAMPLE.MAXCNT	0x564	Number of samples to allocate memory for in EasyDMA mode

42.7.1 INTEN

Address offset: 0x300

Enable or disable interrupt



Bit n	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				СВА
Rese	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW STARTED			Enable or disable interrupt for STARTED event
				See EVENTS_STARTED
		Disabled	0	Disable
		Enabled	1	Enable
В	RW STOPPED			Enable or disable interrupt for STOPPED event
				See EVENTS_STOPPED
		Disabled	0	Disable
		Enabled	1	Enable
С	RW END			Enable or disable interrupt for END event
				See EVENTS_END
		Disabled	0	Disable
		Enabled	1	Enable

42.7.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				СВА
Res	set 0x00000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW STARTED			Write '1' to Enable interrupt for STARTED event
				See EVENTS_STARTED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW STOPPED			Write '1' to Enable interrupt for STOPPED event
				See EVENTS_STOPPED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW END			Write '1' to Enable interrupt for END event
				See EVENTS_END
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

42.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0													
Id			СВА													
Reset 0x00000000		0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$													
Id RW Field	Value Id	Value	Description													
A RW STARTED			Write '1' to Disable interrupt for STARTED event													
			See EVENTS_STARTED													
	Clear	1	Disable													
	Disabled	0	Read: Disabled													
	Enabled	1	Read: Enabled													
B RW STOPPED			Write '1' to Disable interrupt for STOPPED event													



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 C B A													
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0													
Id RW Field	Value Id	Value	Description													
			See EVENTS_STOPPED													
	Clear	1	Disable													
	Disabled	0	Read: Disabled													
	Enabled	1	Read: Enabled													
C RW END			Write '1' to Disable interrupt for END event													
			See EVENTS_END													
	Clear	1	Disable													
	Disabled	0	Read: Disabled													
	Enabled	1	Read: Enabled													

42.7.4 ENABLE

Address offset: 0x500

PDM module enable register

Bitı	numbe	er		3	1 30	29	28	3 27	7 26	6 2	5 24	4 2	3 2	2 2	1 2	0 1	9 1	8 17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0) (0 0	() (0	(0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	٧	alue	2						D	esc	ript	ior	,																		
Α	RW	ENABLE										Е	nab	ole c	r d	isal	ole	PDN	/1 m	odu	le													
			Disabled	0								D	isal	ble																				
			Enabled	1								Е	nab	ole																				

42.7.5 PDMCLKCTRL

Address offset: 0x504

PDM clock generator control

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x08400000		$\begin{smallmatrix} 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0$
Id RW Field	Value Id	Value Description
A RW FREQ		PDM_CLK frequency
	1000K	0x08000000 PDM_CLK = 32 MHz / 32 = 1.000 MHz
	Default	0x08400000 PDM_CLK = 32 MHz / 31 = 1.032 MHz. Nominal clock for
		RATIO=Ratio64.
	1067K	0x08800000 PDM_CLK = 32 MHz / 30 = 1.067 MHz
	1231K	0x09800000 PDM_CLK = 32 MHz / 26 = 1.231 MHz
	1280K	0x0A000000 PDM_CLK = 32 MHz / 25 = 1.280 MHz. Nominal clock for
		RATIO=Ratio80.
	1333K	0x0A800000 PDM_CLK = 32 MHz / 24 = 1.333 MHz

42.7.6 MODE

Address offset: 0x508

Defines the routing of the connected PDM microphones' signals

Bit	numbe	er		31 30	29	28	27 2	26 2	25 24	1 23	3 22	2 21	20	19	18 17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id																													Е	3 A
Res	et 0x0	0000000		0 0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 () (0
Id	RW	Field	Value Id	Value						D	esci	ripti	on																	
Α	RW	OPERATION								M	lone	o or	ster	eo	opera	itio	า													
			Stereo	0 Sample and store one pair (Left + Right) of 16bit samples per								er																		
				RAM word R=[31:16]: L=[15:0]																										



Bit num	ber		31 30 29 28 27	26 25 24	23 22	21 20	19 :	18 1	.7 16	15	14 13	3 12	11 10	9	8	7	6	5 4	3	2	1 0
Id																					ВА
Reset 0	x00000000		0 0 0 0 0	0 0 0	0 0	0 0	0	0 (0 0	0	0 0	0	0 0	0	0	0	0	0 0	0	0	0 0
Id RV	V Field	Value Id	Value		Descri	ption															
		Mono	1		Sample	e and	store	e tw	o su	ccess	ive L	eft sa	mpl	es (1	6 bit	ea	ch)	per			
					RAM w	vord L	1=[3	1:16	5]; LO	=[15	:0]										
B RV	V EDGE				Define	s on v	vhich	PD	M_C	LK e	dge L	eft (d	r mo	no)	is sa	mp	led				
		LeftFalling	0		Left (o	r mon	o) is	sam	pled	l on	fallin	g edg	e of	PDIV	I_CL	K					
		LeftRising	1		Left (o	r mon	o) is	sam	pled	on	rising	edge	of F	DM	_CLk	(

42.7.7 GAINL

Address offset: 0x518

Left output gain adjustment

42.7.8 GAINR

Address offset: 0x51C

Right output gain adjustment

Bit r	numbe	er		33	1 30	29	28	3 27	26	25	24	23	22 :	21 2	0 1	9 1	8 1	7 16	5 15	14	13	12 1	1 10	9	8	7	6	5	4	3 :	2 1	0 1
Id																										Α	Α	Α	Α	A A	Δ ,	А А
Res	et 0x0	0000028		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0 0	0	0	0	0	1	0	1 (0 (0 0
Id	RW	Field	Value Id	V	alue							Des	crip	ptio	n																	
Α	RW	GAINR										Rigl	nt o	utp	ut g	gain	adj	ustr	nen	t, in	0.5	dB	steps	, ard	oun	d tł	ne					
												def	ault	t mo	dul	le ga	ain ((see	ele	ctri	cal p	araı	nete	rs)								
			MinGain	0>	x00							-20	dB 8	gain	adj	just	mei	nt (r	nini	mui	n)											
			DefaultGain	0>	x28							0dE	ga	in a	djus	stm	ent	('25	00 1	RMS	s' re	quir	emer	ıt)								
			MaxGain	0>	x50							+20	dB	gair	ad	ljust	me	nt (max	imu	ım)											

42.7.9 RATIO

Address offset: 0x520

Selects the ratio between PDM_CLK and output sample rate. Change PDMCLKCTRL accordingly.



Bit	numb	ber			31 3	0 29	28	3 27	26	25	24	23 :	22 2	21 2	0 1	9 18	3 17	16	15	14	13 1	2 1:	10	9	8	7	6	5 -	4 3	2	1	0
Id																																Α
Res	et 0x	x00	000000		0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	V	Field	Value Id	Valu	е						Des	crip	tio	n																	
Α	RW	٧	RATIO								:	Sele	ects	the	rati	io b	etw	een	PDI	M_C	CLK a	nd	outp	ut s	am	ple	rate	9				
				ratio64	0							Rat	io o	f 64																		
				ratio80	1							Rat	io o	f 80																		

42.7.10 PSEL.CLK

Address offset: 0x540

Pin number configuration for PDM CLK signal

Bit r	numbe	er		31 30 29 28 27 26 25 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	B A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

42.7.11 PSEL.DIN

Address offset: 0x544

Pin number configuration for PDM DIN signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ВАААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

42.7.12 SAMPLE.PTR

Address offset: 0x560

RAM address pointer to write samples to with EasyDMA

1	Bit n	umb	er		31	1 30	29	28	3 27	7 26	25	24	1 23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ö
1	d				Α	Α	Α	Α	Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4
ı	Rese	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	כ
ı	d	RW	Field	Value Id	Va	alue							De	escr	ipti	on																				
7	Δ	RW	SAMPI FPTR										Αr	ldre	ss t	o w	/rite	PL	M	am	nle	s to	ΩV	er l	DΜ	Α										_

42.7.13 SAMPLE.MAXCNT

Address offset: 0x564

Number of samples to allocate memory for in EasyDMA mode

Reset 0x000000000	
Id A A A A A A A A A A A A A A A A A A A	
	0 0 0 0
51 50 25 20 27 20 25 21 20 15 10 17 10 15 11 10 5 0 7 0 5	AAAA
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5	3 2 1 0



42.8 Electrical specification

42.8.1 PDM Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{PDM,stereo}	PDM module active current, stereo operation ³⁵		250		μΑ
f _{PDM,CLK,64}	PDM clock speed, RATIO of 64		1.032		MHz
f _{PDM,CLK,80}	PDM clock speed, RATIO of 80				MHz
t _{PDM,JITTER}	Jitter in PDM clock output			20	ns
T _{dPDM,CLK}	PDM clock duty cycle	40	50	60	%
t _{PDM,DATA}	Decimation filter delay			5	ms
t _{PDM,cv}	Allowed clock edge to data valid			125	ns
t _{PDM,ci}	Allowed (other) clock edge to data invalid	0			ns
t _{PDM,s}	Data setup time at f _{PDM,CLK} =1.024 MHz or 1.280 MHz	65			ns
t _{PDM,h}	Data hold time at f _{PDM,CLK} =1.024 MHz or 1.280 MHz	0			ns
G _{PDM} default	Default (reset) absolute gain of the PDM module		3.2		dB

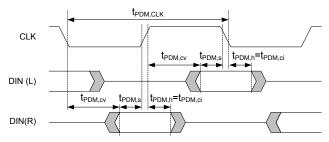


Figure 139: PDM timing diagram

³⁵ Average current including PDM and DMA transfers, excluding clock and power supply base currents



43 I²S — Inter-IC sound interface

The I²S (Inter-IC Sound) module, supports the original two-channel I²S format, and left or right-aligned formats. It implements EasyDMA for sample transfer directly to and from RAM without CPU intervention.

The I²S peripheral has the following main features:

- Master and Slave mode
- Simultaneous bi-directional (TX and RX) audio streaming
- Original I²S and left- or right-aligned format
- 8, 16 and 24-bit sample width
- · Low-jitter Master Clock generator
- · Various sample rates

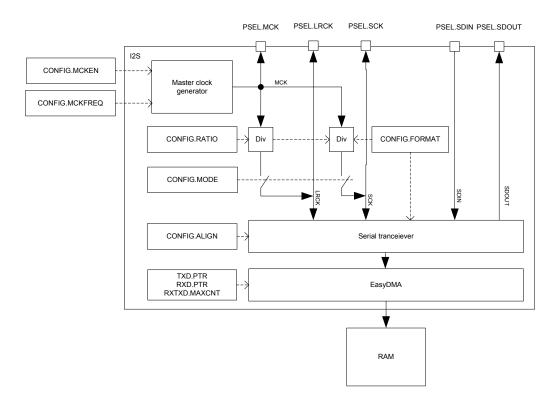


Figure 140: I²S master

43.1 Mode

The I²S protocol specification defines two modes of operation, Master and Slave.

The I²S mode decides which of the two sides (Master or Slave) shall provide the clock signals LRCK and SCK, and these signals are always supplied by the Master to the Slave.

43.2 Transmitting and receiving

The I²S module supports both transmission (TX) and reception (RX) of serial data. In both cases the serial data is shifted synchronously to the clock signals SCK and LRCK.



TX data is written to the SDOUT pin on the falling edge of SCK, and RX data is read from the SDIN pin on the rising edge of SCK. The most significant bit (MSB) is always transmitted first.

TX and RX are available in both Master and Slave modes and can be enabled/disabled independently in the CONFIG.TXEN on page 518 and CONFIG.RXEN on page 518.

Transmission and/or reception is started by triggering the START task. When started and transmission is enabled (in *CONFIG.TXEN* on page 518), the TXPTRUPD event will be generated for every *RXTXD.MAXCNT* on page 521 number of transmitted data words (containing one or more samples). Similarly, when started and reception is enabled (in *CONFIG.RXEN* on page 518), the RXPTRUPD event will be generated for every *RXTXD.MAXCNT* on page 521 received data words.

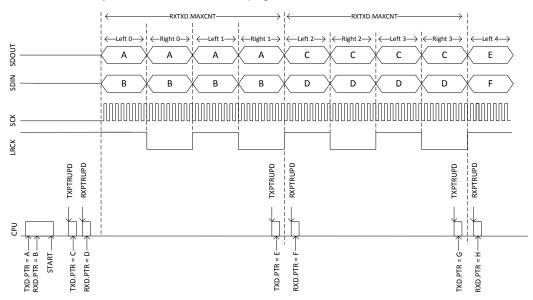


Figure 141: Transmitting and receiving. CONFIG.FORMAT = Aligned, CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo, RXTXD.MAXCNT = 1.

43.3 Left right clock (LRCK)

The Left Right Clock (LRCK), often referred to as "word clock", "sample clock" or "word select" in I²S context, is the clock defining the frames in the serial bit streams sent and received on SDOUT and SDIN, respectively.

In I2S mode, each frame contains one left and right sample pair, with the left sample being transferred during the low half period of LRCK followed by the right sample being transferred during the high period of LRCK.

In Aligned mode, each frame contains one left and right sample pair, with the left sample being transferred during the high half period of LRCK followed by the right sample being transferred during the low period of LRCK.

Consequently, the LRCK frequency is equivalent to the audio sample rate.

When operating in Master mode, the LRCK is generated from the MCK, and the frequency of LRCK is then given as:

```
LRCK = MCK / CONFIG.RATIO
```

LRCK always toggles around the falling edge of the serial clock SCK.

43.4 Serial clock (SCK)

The serial clock (SCK), often referred to as the serial bit clock, pulses once for each data bit being transferred on the serial data lines SDIN and SDOUT.



When operating in Master mode the SCK is generated from the MCK, and the frequency of SCK is then given as:

```
SCK = 2 * LRCK * CONFIG.SWIDTH
```

The falling edge of the SCK falls on the toggling edge of LRCK.

When operating in Slave mode SCK is provided by the external I²S master.

43.5 Master clock (MCK)

The master clock (MCK) is the clock from which LRCK and SCK are derived when operating in Master mode.

The MCK is generated by an internal MCK generator. This generator always needs to be enabled when in Master mode, but the generator can also be enabled when in Slave mode. Enabling the generator when in slave mode can be useful in the case where the external Master is not able to generate its own master clock.

The MCK generator is enabled/disabled in the register *CONFIG.MCKEN* on page 519, and the generator is started or stopped by the START or STOP tasks.

In Master mode the LRCK and the SCK frequencies are closely related, as both are derived from MCK and set indirectly through *CONFIG.RATIO* on page 519 and *CONFIG.SWIDTH* on page 520.

When configuring these registers, the user is responsible for fulfilling the following requirements:

1. SCK frequency can never exceed the MCK frequency, which can be formulated as:

```
CONFIG.RATIO >= 2 * CONFIG.SWIDTH
```

2. The MCK/LRCK ratio shall be a multiple of 2 * CONFIG.SWIDTH, which can be formulated as:

```
Integer = (CONFIG.RATIO / (2 * CONFIG.SWIDTH))
```

The MCK signal can be routed to an output pin (specified in PSEL.MCK) to supply external I²S devices that require the MCK to be supplied from the outside.

When operating in Slave mode, the I²S module does not use the MCK and the MCK generator does not need to be enabled.

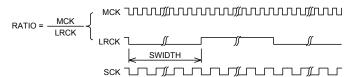


Figure 142: Relation between RATIO, MCK and LRCK.

Table 97: Configuration examples

Desired LRCK [Hz]	CONFIG.SWIDTH	CONFIG.RATIO	CONFIG.MCKFREQ	MCK [Hz]	LRCK [Hz]	LRCK error [%]
16000	16Bit	32X	32MDIV63	507936.5	15873.0	-0.8
16000	16Bit	64X	32MDIV31	1032258.1	16129.0	0.8
16000	16Bit	256X	32MDIV8	4000000.0	15625.0	-2.3
32000	16Bit	32X	32MDIV31	1032258.1	32258.1	0.8
32000	16Bit	64X	32MDIV16	2000000.0	31250.0	-2.3
32000	16Bit	256X	32MDIV4	8000000.0	31250.0	-2.3
44100	16Bit	32X	32MDIV23	1391304.3	43478.3	-1.4
44100	16Bit	64X	32MDIV11	2909090.9	45454.5	3.1
44100	16Bit	256X	32MDIV3	10666666.7	41666.7	-5.5

43.6 Width, alignment and format

The CONFIG.SWIDTH register primarily defines the sample width of the data written to memory. In master mode, it then also sets the amount of bits per frame. In Slave mode it controls padding/trimming if required. Left, right, transmitted, and received samples always have the same width. The CONFIG.FORMAT register specifies the position of the data frames with respect to the LRCK edges in both Master and Slave modes.



When using I²S format, the first bit in a half-frame (containing one left or right sample) gets sampled on the second rising edge of the SCK after a LRCK edge. When using Aligned mode, the first bit in a half-frame gets sampled on the first rising edge of SCK following a LRCK edge.

For data being received on SDIN the sample value can be either right or left-aligned inside a half-frame, as specified in *CONFIG.ALIGN* on page 520. *CONFIG.ALIGN* on page 520 affects only the decoding of the incoming samples (SDIN), while the outgoing samples (SDOUT) are always left-aligned (or justified).

When using left-alignment, each half-frame starts with the MSB of the sample value (both for data being sent on SDOUT and received on SDIN).

When using right-alignment, each half-frame of data being received on SDIN ends with the LSB of the sample value, while each half-frame of data being sent on SDOUT starts with the MSB of the sample value (same as for left-alignment).

In Master mode, the size of a half-frame (in number of SCK periods) equals the sample width (in number of bits), and in this case the alignment setting does not care as each half-frame in any case will start with the MSB and end with the LSB of the sample value.

In slave mode, however, the sample width does not need to equal the frame size. This means you might have extra or fewer SCK pulses per half-frame than what the sample width specified in *CONFIG.SWIDTH* requires.

In the case where we use **left-alignment** and the number of SCK pulses per half-frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits after the LSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0.

In the case where we use **left-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

· Data sent and received on SDOUT and SDIN will be truncated with the LSBs being removed first.

In the case where we use **right-alignment** and the number of SCK pulses per frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits before the MSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0 (same behavior as for left-alignment).

In the case where we use **right-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

- Data received on SDIN will be sign-extended to "sample width" number of bits before being written to memory.
- Data sent on SDOUT will be truncated with the LSBs being removed first (same behavior as for leftalignment).

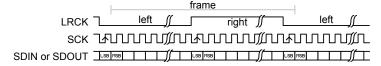


Figure 143: I²S format. CONFIG.SWIDTH equalling half-frame size.

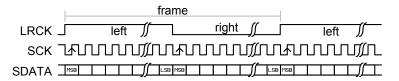


Figure 144: Aligned format. CONFIG.SWIDTH equalling half-frame size.



43.7 EasyDMA

The I²S module implements EasyDMA for accessing internal Data RAM without CPU intervention.

The source and destination pointers for the TX and RX data are configured in *TXD.PTR* on page 521 and *RXD.PTR* on page 521. The memory pointed to by these pointers will only be read or written when TX or RX are enabled in *CONFIG.TXEN* on page 518 and *CONFIG.RXEN* on page 518.

The addresses written to the pointer registers *TXD.PTR* on page 521 and *RXD.PTR* on page 521 are double-buffered in hardware, and these double buffers are updated for every *RXTXD.MAXCNT* on page 521 words (containing one or more samples) read/written from/to memory. The events TXPTRUPD and RXPTRUPD are generated whenever the TXD.PTR and RXD.PTR are transferred to these double buffers.

If *TXD.PTR* on page 521 is not pointing to the Data RAM region when transmission is enabled, or *RXD.PTR* on page 521 is not pointing to the Data RAM region when reception is enabled, an EasyDMA transfer may result in a HardFault and/or memory corruption. See *Memory* on page 20 for more information about the different memory regions.

Due to the nature of I²S, where the number of transmitted samples always equals the number of received samples (at least when both TX and RX are enabled), one common register *RXTXD.MAXCNT* on page 521 is used for specifying the sizes of these two memory buffers. The size of the buffers is specified in a number of 32-bit words. Such a 32-bit memory word can either contain four 8-bit samples, two 16-bit samples or one right-aligned 24-bit sample sign extended to 32 bit.

In stereo mode (CONFIG.CHANNELS=Stereo), the samples are stored as "left and right sample pairs" in memory. Figure Figure 145: Memory mapping for 8 bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo. on page 512, Figure 147: Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo. on page 513 and Figure 149: Memory mapping for 24 bit stereo. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo. on page 513 show how the samples are mapped to memory in this mode. The mapping is valid for both RX and TX.

In mono mode (CONFIG.CHANNELS=Left or Right), RX sample from only one channel in the frame is stored in memory, the other channel sample is ignored. Illustrations *Figure 146: Memory mapping for 8 bit mono.* CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left. on page 513, *Figure 148: Memory mapping for 16 bit mono, left channel only.* CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left. on page 513 and *Figure 150: Memory mapping for 24 bit mono, left channel only.* CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left. on page 514 show how RX samples are mapped to memory in this mode.

For TX, the same outgoing sample read from memory is transmitted on both left and right in a frame, resulting in a mono output stream.

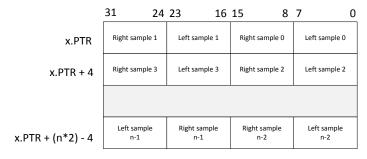


Figure 145: Memory mapping for 8 bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo.



	31 24	23 16	15 8	7 0
x.PTR	Left sample 3	Left sample 2	Left sample 1	Left sample 0
x.PTR + 4	Left sample 7	Left sample 6	Left sample 5	Left sample 4
x.PTR + n - 4	Left sample n-1	Left sample n-2	Left sample n-3	Left sample n-4

Figure 146: Memory mapping for 8 bit mono. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left.

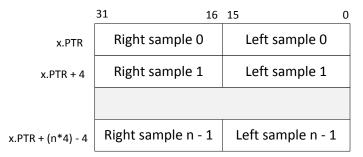


Figure 147: Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo.

	31 16	15 0
x.PTR	Left sample 1	Left sample 0
x.PTR + 4	Left sample 3	Left sample 2
x.PTR + (n*2) - 4	Left sample n - 1	Left sample n - 2

Figure 148: Memory mapping for 16 bit mono, left channel only. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left.

	31	23 0
x.PTR	Sign ext.	Left sample 0
x.PTR + 4	Sign ext.	Right sample 0
x.PTR + (n*8) - 8	Sign ext.	Left sample n - 1
x.PTR + (n*8) - 4	Sign ext.	Right sample n - 1

Figure 149: Memory mapping for 24 bit stereo. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo.



	31	23	0
x.PTR	Sign ext.	Left sample 0	
x.PTR + 4	Sign ext.	Left sample 1	
x.PTR + (n*4) - 4	Sign ext.	Left sample n - 1	

Figure 150: Memory mapping for 24 bit mono, left channel only. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left.

43.8 Module operation

Described here is a typical operating procedure for the I²S module.

1. Configure the I²S module using the CONFIG registers

```
// Enable reception
NRF I2S->CONFIG.RXEN = (I2S CONFIG RXEN RXEN Enabled <<
                                        I2S_CONFIG_RXEN_RXEN_Pos);
// Enable transmission
NRF_I2S->CONFIG.TXEN = (I2S_CONFIG_TXEN TXEN Enabled <<
                                        I2S CONFIG TXEN TXEN Pos);
// Enable MCK generator
NRF_I2S->CONFIG.MCKEN = (I2S_CONFIG_MCKEN_MCKEN_Enabled <<</pre>
                                        12S CONFIG MCKEN MCKEN Pos);
// MCKFREQ = 4 MHz
NRF_12S->CONFIG.MCKFREQ = 12S_CONFIG_MCKFREQ_MCKFREQ_32MDIV8 <<
                                        12S CONFIG MCKFREQ MCKFREQ Pos;
// Ratio = 256
NRF I2S->CONFIG.RATIO = I2S CONFIG RATIO RATIO 256X <<
                                       12S CONFIG RATIO RATIO Pos;
// MCKFREQ = 4 MHz and Ratio = 256 gives sample rate = 15.625 ks/s
// Sample width = 16 bit
NRF I2S->CONFIG.SWIDTH = I2S CONFIG SWIDTH SWIDTH 16Bit <<
                                        12S CONFIG SWIDTH SWIDTH Pos;
// Alignment = Left
NRF I2S->CONFIG.ALIGN = I2S CONFIG ALIGN ALIGN Left <<
                                       12S CONFIG ALIGN ALIGN Pos;
// Format = I2S
NRF I2S->CONFIG.FORMAT = I2S CONFIG FORMAT FORMAT I2S <<
                                        12S CONFIG FORMAT FORMAT Pos;
// Use stereo
NRF I2S->CONFIG.CHANNELS = I2S CONFIG CHANNELS CHANNELS Stereo <<
                                        12S CONFIG CHANNELS CHANNELS Pos;
```

2. Map IO pins using the PINSEL registers



3. Configure TX and RX data pointers using the TXD, RXD and RXTXD registers

```
NRF_I2S->TXD.PTR = my_tx_buf;
NRF_I2S->RXD.PTR = my_rx_buf;
NRF_I2S->TXD.MAXCNT = MY_BUF_SIZE;
```

4. Enable the I²S module using the ENABLE register

```
NRF_I2S->ENABLE = 1;
```

5. Start audio streaming using the START task

```
NRF_I2S->TASKS_START = 1;
```

6. Handle received and transmitted data when receiving the TXPTRUPD and RXPTRUPD events

```
if (NRF_I2S->EVENTS_TXPTRUPD != 0)
{
    NRF_I2S->TXD.PTR = my_next_tx_buf;
    NRF_I2S->EVENTS_TXPTRUPD = 0;
}

if (NRF_I2S->EVENTS_RXPTRUPD != 0)
{
    NRF_I2S->RXD.PTR = my_next_rx_buf;
    NRF_I2S->EVENTS_RXPTRUPD = 0;
}
```

43.9 Pin configuration

The MCK, SCK, LRCK, SDIN and SDOUT signals associated with the I²S module are mapped to physical pins according to the pin numbers specified in the PSEL.x registers.

These pins are acquired whenever the I²S module is enabled through the register *ENABLE* on page 518.

When a pin is acquired by the I²S module, the direction of the pin (input or output) will be configured automatically, and any pin direction setting done in the GPIO module will be overridden. The directions for the various I²S pins are shown below in *Table 98: GPIO configuration before enabling peripheral (master mode)* on page 515 and *Table 99: GPIO configuration before enabling peripheral (slave mode)* on page 516.

To secure correct signal levels on the pins when the system is in OFF mode, and when the I²S module is disabled, these pins must be configured in the GPIO peripheral directly.

Table 98: GPIO configuration before enabling peripheral (master mode)

I ² S signal	I ² S pin	Direction	Output value	Comment
MCK	As specified in PSEL.MCK	Output	0	
LRCK	As specified in PSEL.LRCK	Output	0	



I ² S signal	I ² S pin	Direction	Output value	Comment
SCK	As specified in PSEL.SCK	Output	0	
SDIN	As specified in PSEL.SDIN	Input	Not applicable	
SDOUT	As specified in PSEL.SDOUT	Output	0	

Table 99: GPIO configuration before enabling peripheral (slave mode)

I ² S signal	I ² S pin	Direction	Output value	Comment
MCK	As specified in PSEL.MCK	Output	0	
LRCK	As specified in PSEL.LRCK	Input	Not applicable	
SCK	As specified in PSEL.SCK	Input	Not applicable	
SDIN	As specified in PSEL.SDIN	Input	Not applicable	
SDOUT	As specified in PSEL.SDOUT	Output	0	

43.10 Registers

Table 100: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40025000	125	I2S	Inter-IC sound interface		

Table 101: Register Overview

Register	Offset	Description
TASKS_START	0x000	Starts continuous I2S transfer. Also starts MCK generator when this is enabled.
TASKS_STOP	0x004	Stops I2S transfer. Also stops MCK generator. Triggering this task will cause the {event:STOPPED}
		event to be generated.
EVENTS_RXPTRUPD	0x104	The RXD.PTR register has been copied to internal double-buffers. When the I2S module is started
		and RX is enabled, this event will be generated for every RXTXD.MAXCNT words that are received on
		the SDIN pin.
EVENTS_STOPPED	0x108	12S transfer stopped.
EVENTS_TXPTRUPD	0x114	The TDX.PTR register has been copied to internal double-buffers. When the I2S module is started
		and TX is enabled, this event will be generated for every RXTXD.MAXCNT words that are sent on the
		SDOUT pin.
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable I2S module.
CONFIG.MODE	0x504	I2S mode.
CONFIG.RXEN	0x508	Reception (RX) enable.
CONFIG.TXEN	0x50C	Transmission (TX) enable.
CONFIG.MCKEN	0x510	Master clock generator enable.
CONFIG.MCKFREQ	0x514	Master clock generator frequency.
CONFIG.RATIO	0x518	MCK / LRCK ratio.
CONFIG.SWIDTH	0x51C	Sample width.
CONFIG.ALIGN	0x520	Alignment of sample within a frame.
CONFIG.FORMAT	0x524	Frame format.
CONFIG.CHANNELS	0x528	Enable channels.
RXD.PTR	0x538	Receive buffer RAM start address.
TXD.PTR	0x540	Transmit buffer RAM start address.
RXTXD.MAXCNT	0x550	Size of RXD and TXD buffers.
PSEL.MCK	0x560	Pin select for MCK signal.
PSEL.SCK	0x564	Pin select for SCK signal.
PSEL.LRCK	0x568	Pin select for LRCK signal.
PSEL.SDIN	0x56C	Pin select for SDIN signal.
PSEL.SDOUT	0x570	Pin select for SDOUT signal.

43.10.1 INTEN

Address offset: 0x300 Enable or disable interrupt



Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F C B
Rese	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
В	RW RXPTRUPD			Enable or disable interrupt for RXPTRUPD event
				See EVENTS_RXPTRUPD
		Disabled	0	Disable
		Enabled	1	Enable
С	RW STOPPED			Enable or disable interrupt for STOPPED event
				See EVENTS_STOPPED
		Disabled	0	Disable
		Enabled	1	Enable
F	RW TXPTRUPD			Enable or disable interrupt for TXPTRUPD event
				See EVENTS_TXPTRUPD
		Disabled	0	Disable
		Enabled	1	Enable

43.10.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31 3	30 29	9 28	27	26 2	5 24	23 2	22 21	L 20	19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4 3	2	1 (
Id																										F		С	В
Res	et 0x0	0000000		0	0 0	0	0	0 0	0	0	0 0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0 0	0	0 (
Id	RW	Field	Value Id	Valu	ıe					Des	cript	ion																	
В	RW	RXPTRUPD								Writ	te '1'	to E	nab	le i	nte	rru	pt f	or F	RXPT	RU	PD e	ven	t						
										See	EVEI	NTS_	RXF	PTR	UPL)													
			Set	1						Enal	ble																		
			Disabled	0						Read	d: Di	sabl	ed																
			Enabled	1						Read	d: En	able	d																
С	RW	STOPPED								Writ	te '1'	to E	nab	le i	nte	rru	pt f	or S	TOP	PEI	D ev	ent							
										See	EVEI	NTS_	STO	PP	ED														
			Set	1						Enal	ble																		
			Disabled	0						Read	d: Di	sabl	ed																
			Enabled	1						Read	d: En	able	d																
F	RW	TXPTRUPD								Writ	te '1'	to E	nab	le i	nte	rru	pt f	or T	XPT	RU	PD e	ven	t						
										See	EVEI	NTS_	TXP	TR	UPE)													
			Set	1						Enal	ble																		
			Disabled	0						Read	d: Di	sabl	ed																
			Enabled	1						Read	d: En	able	d																

43.10.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	er		31	. 30	29	28	3 27	7 2	6 25	5 2	4 2	3 2	2 2	21 2	0 1	19 1	8 2	17 1	6 1	5 1	.4 1	13 1	12 1	1 1) 9	8	7	6	5	4	3	2	1 0
Id																														F			С	В
Res	et 0x0	0000000		0	0	0	0	0	0	0	C) () (0	0 0)	0 (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	llue							D	esc	rip	tior	ı																		
В	RW	RXPTRUPD										V	/rit	e '1	1' to	Di	sab	le i	nte	rru	pt f	or I	RXP	TRU	JPD	eve	nt							
												S	ee	EVE	ENT	S_ <i>F</i>	RXP	TRU	JPD															
			Clear	1								D	isa	ble																				
			Disabled	0								R	eac	d: D	isat	ole	d																	
			Enabled	1								R	eac	d: E	nab	lec	i																	
С	RW	STOPPED										V	/rit	e '1	1' to	Di	sab	le i	nte	rru	pt f	or S	STO	PPE	D e	ven	t							



Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 F C B
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
			See EVENTS_STOPPED
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
F RW TXPTRUPD			Write '1' to Disable interrupt for TXPTRUPD event
			See EVENTS_TXPTRUPD
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

43.10.4 ENABLE

Address offset: 0x500 Enable I2S module.

Bitı	numb	er		31 30	29	28	27	26 :	25 2	24 2	23 2	22 2	1 20) 19	18	17	16	15	14 :	13 1	2 11	. 10	9	8	7	6	5	4	3	2 :	1 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 (0 0
ld	RW	Field	Value Id	Value	2					0	Desc	crip	tion																		
Α	RW	ENABLE								E	nal	ole I	2S r	nod	ule.																
			Disabled	0						0	Disa	ble																			
			Enabled	1						Е	nal	ble																			

43.10.5 CONFIG.MODE

Address offset: 0x504

I2S mode.

Bitı	numbe	er		31	1 30	29	28	27	26	25	24	1 23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							De	scr	ipti	on																			
Α	RW	MODE										12:	S m	ode																				
			Master	0								М	aste	er m	ode	e. S	CK a	and	LR	CK į	gen	era	ted	fro	n ir	iter	nal	ma	este	er				
												clo	ok	(MC	CK)	and	ou	tpu	t or	n pi	ns c	lefi	ned	by	PSE	L.x	κx.							
			Slave	1								Sla	ive	mo	de.	SCK	an	d L	RCK	ge	ner	ate	d b	y ex	terr	nal	ma:	ste	r ar	nd				
												re	ceiv	ed	on	pins	de	fine	ed b	у Р	SEL	.xx	K											

43.10.6 CONFIG.RXEN

Address offset: 0x508 Reception (RX) enable.

Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A
Reset 0x00000000	0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field Value Id	Value	Description
A RW RXEN		Reception (RX) enable.
Disabled	0	Reception disabled and now data will be written to the RXD.PTR
		address.
Enabled	1	Reception enabled.

43.10.7 CONFIG.TXEN

Address offset: 0x50C



Transmission (TX) enable.

Bit	numbe	er		3	1 30	29	28	3 27	7 26	5 25	5 24	1 2	3 22	21	20	19	18	17	16	15	14	13	12	11 1	0 9	9 8	3 7	' 6	5	4	3	2	1	0
Id																																		Α
Res	et 0x0	0000001		0	0	0	0	0	0	0	0	C	0	0	0	0	0	0	0	0	0	0	0	0) (0 () (0	0	0	0	0	0	1
Id	RW	Field	Value Id	٧	'alu	е						D	escr	ipti	on																			
Α	RW	TXEN										Т	rans	mis	sior	1 (T)	K) e	nab	ole.															
			Disabled	0								Т	rans	miss	sior	n dis	abl	led	and	l nc	w c	lata	wi	ll be	rea	d f	om	the	ē					
												R	XD.T	XD	adc	ires	s.																	
			Enabled	1								Т	rans	mis	sior	n en	abl	ed.																

43.10.8 CONFIG.MCKEN

Address offset: 0x510

Master clock generator enable.

Bit	numbe	er		3	1 30	29	28	27	26	25	24	23	22	21 2	20 :	19 1	8 1	.7 1	5 15	5 14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																																Α
Res	et 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 1
Id	RW	Field	Value Id	٧	alue	:						De	scri	ptio	n																	
Α	RW	MCKEN										Ma	ste	r clo	ck	gen	era	tor e	enal	ole.												
			Disabled	0								Ma	ste	r clo	ck	gen	era	tor o	lisa	bled	l an	d PS	EL.N	1CK	not							
												cor	nne	cted	l(av	aila	ble	as G	PIC)).												
			Enabled	1								Ma	ste	r clo	ck	gen	era	tor r	unr	ning	and	MC	κ οι	itpu	it or	PS	EL.N	ИCК	ί.			

43.10.9 CONFIG.MCKFREQ

Address offset: 0x514

Master clock generator frequency.

	numbe	er		3:	1 3	0 29	28	27	26	25	24	23 :	22 :	21 20) 19	9 18	3 17	16	15	14	13 1	2 11	10	9	8	7	6	5	4 :	3 2	1	0
Id				Α	Δ	A A	Α	Α	Α	Α	Α	Α	Α	A A	Α	\ A	Α	Α	Α	Α	A A	A A	Α	Α	Α	Α	Α	Α	Α /	A A	Α	Α
Res	et 0x2	20000000		0	0) 1	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	V	alu	e						Des	crip	otion																		
Α	RW	MCKFREQ										Ma	ster	cloc	k g	ene	rato	or fr	equ	enc	y.											
			32MDIV2	0:	x80	000	000)				32 [ИΗ	z / 2	= 1	6.0	МН	Z														
			32MDIV3	0:	x50	000	000)				32 [ИΗ	z/3	= 1	0.66	666	567	МН	z												
			32MDIV4	0:	x40	000	000)				32 [ИΗ	z / 4	= 8	.0 N	1Hz															
			32MDIV5	0:	x30	000	000)				32 [ИΗ	z / 5	= 6	.4 N	1Hz															
			32MDIV6	0	x28	000	000)				32 [ИΗ	z / 6	= 5	.333	333	33 N	ЛHz													
			32MDIV8	0	x20	000	000)				32 [ИΗ	z / 8	= 4	.0 N	1Hz															
			32MDIV10	0	x18	000	000)				32 [ИΗ	z / 10) = 1	3.2	МН	Z														
			32MDIV11	0	x16	000	000)				32 [ИΗ	z / 11	L = 1	2.90	909	909	МН	z												
			32MDIV15	0	x11	000	000)				32 [ИΗ	z / 15	5 = 1	2.13	333	333	МН	z												
			32MDIV16	0	x10	000	000)				32 [ИΗ	z / 16	5 = 1	2.0	МН	Z														
			32MDIV21	0	x0C	000	000)				32 [ИΗ	z / 21	L =	1.52	2380	095														
			32MDIV23	0:	хОВ	000	000)				32 [ИΗ	z / 23	3 =	1.39	9130	043	МН	z												
			32MDIV30	0:	x08	800	000)				32 [ИΗ	z / 30) =	1.06	666	567	МН	z												
			32MDIV31	0:	x08	400	000)				32 [ИΗ	z / 31	L =	1.03	322	581	МН	z												
			32MDIV32	0:	x08	000	000)				32 [ИΗ	z / 32	2 =	1.0	МН	Z														
			32MDIV42	0	x06	000	000)				32 [ИΗ	z / 42	2 =	0.76	519	048	МН	z												
			32MDIV63	0	x04	100	000)				32 [ИΗ	z / 63	3 =	0.50	79	365	МН	z												
			32MDIV125	0:	x02	0C0	000)				32 [ИΗ	z / 12	25 =	0.2	256	МН	Z													

43.10.10 CONFIG.RATIO

Address offset: 0x518 MCK / LRCK ratio.



Bit number	31 30 29 28 27 26	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		ААА
Reset 0x00000006	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Valu	e Id Value	Description
A RW RATIO		MCK / LRCK ratio.
32X	0	LRCK = MCK / 32
48X	1	LRCK = MCK / 48
64X	2	LRCK = MCK / 64
96X	3	LRCK = MCK / 96
128	4	LRCK = MCK / 128
192	5	LRCK = MCK / 192
2562	6	LRCK = MCK / 256
3842	7	LRCK = MCK / 384
512	(8	LRCK = MCK / 512

43.10.11 CONFIG.SWIDTH

Address offset: 0x51C

Sample width.

Bit numbe	r		31	. 30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	.8 1	7 1	6 1	5 14	13	12	11	10	9	8	7	6	5 .	4 3	2	1	0
Id																															Α	Α
Reset 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	1
Id RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
A RW	SWIDTH										San	nple	wi	dth																		
		8Bit	0								8 b	it.																				
		16Bit	1								16	bit.																				
		24Bit	2								24	bit.																				

43.10.12 CONFIG.ALIGN

Address offset: 0x520

Alignment of sample within a frame.

Bit	nuı	mbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																																			Α
Res	et	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	F	RW	Field	Value Id	Va	lue							De	scri	ptio	on																			
Α	F	RW	ALIGN										Ali	gnn	nen	t of	sar	npl	e w	ithi	n a	fra	me												
				Left	0								Lef	t-al	ign	ed.																			
				Right	1								Rig	ht-	alig	ned	١.																		

43.10.13 CONFIG.FORMAT

Address offset: 0x524

Frame format.

Bit r	numbe	er		31 3	29	28	3 27	26	25	24	23 2	22 2	21 2) 19	18	17	16 :	15 1	4 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1 0
Id																														Α
Res	et OxO	0000000		0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0	0	0 0
Id	RW	Field	Value Id	Valu	е						Des	crip	tion																	
Α	RW	FORMAT									Fran	ne f	orm	at.																
			I2S	0							Orig	gina	l I2S	for	nat.															
			Aligned	1							Alte	rna	te (I	eft-	or r	ight	-alig	nec	d) fo	rma	t.									

43.10.14 CONFIG.CHANNELS

Address offset: 0x528 Enable channels.



Bi	t nı	umbe	r		3:	1 30	29	2	8 2	7 2	6 2	5 2	24 :	23 2	2 2	1 2	0 1	.9 1	18 1	L7 1	16 1	15 :	14 1	13 :	12 :	11 1	0 9	9 :	3	7	6	5	4	3	2	1 0
Id																																			,	4 А
R	se	t 0x0	0000000		0	0	0	C) () () (0	0	0	0 (0) (0 (0	0	0	0	0	0	0	0 () (0 () (0	0	0	0	0	0 (0 0
Id		RW	Field	Value Id	V	'alu	9						- 1	Des	crip	tior	า																			
Α		RW	CHANNELS										- 1	Enal	ole (cha	nne	els.																		
				Stereo	0								:	Ster	eo.																					
				Left	1								-	Left	onl	y.																				
				Right	2								ı	Righ	t or	nly.																				

43.10.15 RXD.PTR

Address offset: 0x538

Receive buffer RAM start address.

Bit	numb	er		31	. 30	29	28	3 27	7 26	5 25	24	23	22	21 2	20 1	9 1	8 17	16	15	14	13 1	2 13	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 4	A	Α	Α	Α	A A	A A	Α	Α	Α	Α	Α	Α	Α	А А	Α	Α
Res	et 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	otio	n																	
Α	RW	PTR										Re	eiv	e bı	ıffeı	r Da	ta R	AM	sta	t ac	dre	s. V	Vhe	n re	ceiv	/ing	, w	ord	s			
												100	ntair	ning	san	nple	s w	ill be	e wi	itte	n to	this	ado	Ires	s. T	his	add	Ires	S			
												is a	wo	rd a	ilign	ed I	Data	RΔ	M a	ddr	200											

43.10.16 TXD.PTR

Address offset: 0x540

Transmit buffer RAM start address.

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21 2	20 1	9 18	3 17	16	15	14	13 1	2 13	. 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	A A	A	Α	Α	Α	Α	A	4 A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							De	scri	ptio	n																	
Α	RW	PTR										Tra	nsn	nit b	uffe	r Da	ıta F	RAN	1 sta	art a	ddr	ess.	Whe	en ti	rans	smi	ttin	ıg,				
												wo	rds	con	taini	ing s	am	ples	wi	ll be	feto	hed	fro	m th	nis a	addı	res	s. T	his			
												ado	dres	s is	a wo	ord a	aligr	ned	Dat	a R	AM a	addr	ess.									

43.10.17 RXTXD.MAXCNT

Address offset: 0x550

Size of RXD and TXD buffers.

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1
Id				AAAAA	A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A RW MAXCNT	words.				

43.10.18 PSEL.MCK

Address offset: 0x560

Pin select for MCK signal.

Bit r	numbe	er		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id				С	B AAAA
Rese	et OxF	FFFFFF		1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect



43.10.19 PSEL.SCK

Address offset: 0x564

Pin select for SCK signal.

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	B AAAAA
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

43.10.20 PSEL.LRCK

Address offset: 0x568

Pin select for LRCK signal.

Bit r	umbe	er		31	30	29	28 2	27 :	26 2	25 2	24 :	23 2	2 2	1 20) 19	18	17	16	15	14 1	l3 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id				С																					В				Α	A A	A	Α
Rese	t 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1 :	1 1	۱ 1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Va	lue						- 1	Des	cript	ion																		
Α	RW	PIN		[0.	.31]						- 1	Pin ı	num	ber																		
В	RW	PORT		[0.	.1]						- 1	Port	nun	nbe	r																	
С	RW	CONNECT									(Con	nect	ion																		
			Disconnected	1							- 1	Disc	onn	ect																		
			Connected	0							(Con	nect																			

43.10.21 PSEL.SDIN

Address offset: 0x56C

Pin select for SDIN signal.

Bit r	iumbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	B AAAA
Rese	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

43.10.22 PSEL.SDOUT

Address offset: 0x570

Pin select for SDOUT signal.

Bit r	iumbe	er		31 30 29 28 27 26 2	25 24	4 23	3 22	21	20	19	18	17 :	16 1	15 1	4 1	3 12	11	10	9	8	7	6	5	4	3	2	1 0
Id				С																В				Α	Α	Α.	А А
Rese	et OxF	FFFFFF		1 1 1 1 1 1	1 1	. 1	1	1	1	1	1	1	1	1 :	1 1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Value		De	escr	ipti	on																		
Α	RW	PIN		[031]		Pi	n nı	ımb	er																		
В	RW	PORT		[01]		Po	rt r	ıum	ber	r																	
С	RW	CONNECT				Co	nn	ectio	on																		
			Disconnected	1		Di	sco	nne	ct																		
			Connected	0		Co	nn	ect																			



43.11 Electrical specification

43.11.1 I2S timing specification

Symbol	Description	Min.	Тур.	Max.	Units
t_{S_SDIN}	SDIN setup time before SCK rising	20			ns
t _{H_SDIN}	SDIN hold time after SCK rising	15			ns
t_{S_SDOUT}	SDOUT setup time after SCK falling	40			ns
t _{H_SDOUT}	SDOUT hold time before SCK falling	6			ns
t _{SCK_LRCK}	SCLK falling to LRCK edge	-5	0	5	ns
f _{MCK}	MCK frequency			4000	kHz
f _{LRCK}	LRCK frequency			48	kHz
f _{SCK}	SCK frequency			2000	kHz
DC _{CK}	Clock duty cycle (MCK, LRCK, SCK)	45		55	%

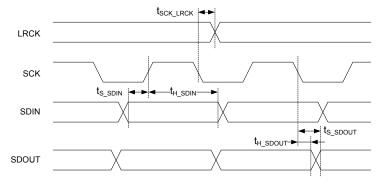


Figure 151: I2S timing diagram



44 MWU — Memory watch unit

The Memory watch unit (MWU) can be used to generate events when a memory region is accessed by the CPU. The MWU can be configured to trigger events for access to Data RAM and Peripheral memory segments. The MWU allows an application developer to generate memory access events during development for debugging or during production execution for failure detection and recovery.

Listed here are the main features for MWU:

- Six memory regions, four user-configurable and two fixed regions in peripheral address space
- Flexible configuration of regions with START and END addresses
- Generate events on CPU read and/or write to a defined region of Data RAM or peripheral memory address space
- Programmable maskable or non-maskable (NMI) interrupt on events
- Peripheral interfaces can be watched for read and write access using subregions of the two fixed memory regions

Table 102: Memory regions

Memory region	START address	END address
REGION[03]	Configurable	Configurable
PREGION[0]	0x4000000	0x4001FFFF
PREGION[1]	0x40020000	0x4003FFFF

Each MWU region is defined by a start address and an end address, configured by the START and END registers respectively. These addresses are byte aligned and inclusive. The END register value has to be greater or equal to the START register value. Each region is associated with a pair of events that indicate that either a write access or a read access from the CPU has been detected inside the region.

For regions containing subregions (see below), a set of status registers PERREGION[0..1].SUBSTATWA and PERREGION[0..1].SUBSTATRA indicate which subregion(s) caused the EVENT_PREGION[0..1].WA and EVENT_PREGION[0..1].RA respectively.

The MWU is only able to detect memory accesses in the Data RAM and Peripheral memory segments from the CPU, see *Memory* on page 20 for more information about the different memory segments. EasyDMA accesses are not monitored by the MWU. The MWU requires two HCLK cycles to detect and generate the event.

The peripheral regions, PREGION[0...1], are divided into 32 equally sized subregions, SR[0...31]. All subregions are excluded in the main region by default, and any can be included by specifying them in the SUBS register. When a subregion is excluded from the main region, the memory watch mechanism will not trigger any events when that subregion is accessed.

Subregions in PREGION[0..1] cannot be individually configured for read or write access watch. Watch configuration is only possible for a region as a whole. The PRGNiRA and PRGNiWA (i=0..1) fields in the REGIONEN register control watching read and write access.

REGION[0..3] can be individually enabled for read and/or write access watching through their respective RGNiRA and RGNiWA (i=0..3) fields in the REGIONEN register.

REGIONENSET and REGIONENCLR allow respectively enabling and disabling one or multiple REGIONs or PREGIONs watching in a single write access.

44.1 Registers

Table 103: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40020000	MWU	MWU	Memory watch unit	



Table 104: Register Overview

Register	Offset	Description
EVENTS_REGION[0].W	A 0x100	Write access to region 0 detected
EVENTS_REGION[0].RA	0x104	Read access to region 0 detected
EVENTS_REGION[1].WA	A 0x108	Write access to region 1 detected
EVENTS_REGION[1].RA	0x10C	Read access to region 1 detected
EVENTS_REGION[2].W/	A 0x110	Write access to region 2 detected
EVENTS_REGION[2].RA	0x114	Read access to region 2 detected
EVENTS_REGION[3].WA	A 0x118	Write access to region 3 detected
EVENTS_REGION[3].RA	0x11C	Read access to region 3 detected
EVENTS_PREGION[0].V	VA 0x160	Write access to peripheral region 0 detected
EVENTS_PREGION[0].R	A 0x164	Read access to peripheral region 0 detected
EVENTS_PREGION[1].V	VA 0x168	Write access to peripheral region 1 detected
EVENTS_PREGION[1].R	A 0x16C	Read access to peripheral region 1 detected
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
NMIEN	0x320	Enable or disable non-maskable interrupt
NMIENSET	0x324	Enable non-maskable interrupt
NMIENCLR	0x328	Disable non-maskable interrupt
PERREGION[0].SUBSTA	7 1 0x400	Source of event/interrupt in region 0, write access detected while corresponding subregion was
		enabled for watching
PERREGION[0].SUBSTA	T/ 0x404	Source of event/interrupt in region 0, read access detected while corresponding subregion was
		enabled for watching
PERREGION[1].SUBSTA	7 1 0x408	Source of event/interrupt in region 1, write access detected while corresponding subregion was
		enabled for watching
PERREGION[1].SUBSTA	T/ 0x40C	Source of event/interrupt in region 1, read access detected while corresponding subregion was
		enabled for watching
REGIONEN	0x510	Enable/disable regions watch
REGIONENSET	0x514	Enable regions watch
REGIONENCLR	0x518	Disable regions watch
REGION[0].START	0x600	Start address for region 0
REGION[0].END	0x604	End address of region 0
REGION[1].START	0x610	Start address for region 1
REGION[1].END	0x614	End address of region 1
REGION[2].START	0x620	Start address for region 2
REGION[2].END	0x624	End address of region 2
REGION[3].START	0x630	Start address for region 3
REGION[3].END	0x634	End address of region 3
PREGION[0].START	0x6C0	Reserved for future use
PREGION[0].END	0x6C4	Reserved for future use
PREGION[0].SUBS	0x6C8	Subregions of region 0
PREGION[1].START	0x6D0	Reserved for future use
PREGION[1].END	0x6D4	Reserved for future use
PREGION[1].SUBS	0x6D8	Subregions of region 1

44.1.1 INTEN

Address offset: 0x300 Enable or disable interrupt

Bitı	numbe	er		31	1 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 1	.1 10	9	8	7	6	5	4	3	2 :	1 0
Id								L	K	J	1																Н	G	F	Ε	D	C E	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	V	alue	•						De	scri	otic	n																		
Α	RW	REGION0WA										Ena	ble	or	dis	able	e in	teri	rup	t fo	r RE	GIO	ON[()].W	A e	/ent	:						
												See	e EV	EN	TS_	REC	310	N[0	J. N	/A													
			Disabled	0								Dis	able	ē																			



	number			25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld Res	et 0x00000000		L K	J I H G F E D C B A 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description Description
		Enabled	1	Enable
В	RW REGIONORA			Enable or disable interrupt for REGION[0].RA event
				See EVENTS_REGION[0].RA
		Disabled	0	Disable
		Enabled	1	Enable
С	RW REGION1WA			Enable or disable interrupt for REGION[1].WA event
				See EVENTS REGION[1].WA
		Disabled	0	Disable
		Enabled	1	Enable
D	RW REGION1RA			Enable or disable interrupt for REGION[1].RA event
				See EVENTS_REGION[1].RA
		Disabled	0	Disable
		Enabled	1	Enable
E	RW REGION2WA		_	Enable or disable interrupt for REGION[2].WA event
		Disabled	0	See EVENTS_REGION[2].WA Disable
		Enabled	1	Enable
F	RW REGION2RA		_	Enable or disable interrupt for REGION[2].RA event
		Disabled	0	See EVENTS_REGION[2].RA Disable
		Enabled	1	Enable
G	RW REGION3WA		_	Enable or disable interrupt for REGION[3].WA event
				See EVENTS_REGION[3].WA
		Disabled	0	Disable
		Enabled	1	Enable
Н	RW REGION3RA			Enable or disable interrupt for REGION[3].RA event
				Con EVENTS DECION[2] DA
		Disabled	0	See EVENTS_REGION[3].RA Disable
		Enabled	1	Enable
ı	RW PREGIONOWA			Enable or disable interrupt for PREGION[0].WA event
				See EVENTS_PREGION[0].WA
		Disabled	0	Disable
		Enabled	1	Enable
J	RW PREGIONORA			Enable or disable interrupt for PREGION[0].RA event
				See EVENTS_PREGION[0].RA
		Disabled	0	Disable
		Enabled	1	Enable
K	RW PREGION1WA			Enable or disable interrupt for PREGION[1].WA event
				See EVENTS_PREGION[1].WA
		Disabled	0	Disable
		Enabled	1	Enable
L	RW PREGION1RA			Enable or disable interrupt for PREGION[1].RA event
				See EVENTS_PREGION[1].RA
		Disabled	0	Disable
		Enabled	1	Enable

44.1.2 INTENSET

Address offset: 0x304 Enable interrupt



Bit r	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L K	J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW REGIONOWA			Write '1' to Enable interrupt for REGION[0].WA event
				See EVENTS_REGION[0].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW REGIONORA			Write '1' to Enable interrupt for REGION[0].RA event
				See EVENTS_REGION[0].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW REGION1WA			Write '1' to Enable interrupt for REGION[1].WA event
				See EVENTS_REGION[1].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW REGION1RA			Write '1' to Enable interrupt for REGION[1].RA event
		C-1	4	See EVENTS_REGION[1].RA Enable
		Set Disabled	1 0	
		Enabled	1	Read: Disabled Read: Enabled
E	RW REGION2WA	Ellableu	1	Write '1' to Enable interrupt for REGION[2].WA event
L	NW REGIONZWA			write 1 to Enable Interrupt for REGION[2].WA event
				See EVENTS_REGION[2].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
_		Enabled	1	Read: Enabled
F	RW REGION2RA			Write '1' to Enable interrupt for REGION[2].RA event
				See EVENTS_REGION[2].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW REGION3WA			Write '1' to Enable interrupt for REGION[3].WA event
				See EVENTS_REGION[3].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW REGION3RA			Write '1' to Enable interrupt for REGION[3].RA event
				See EVENTS_REGION[3].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
ı	RW PREGIONOWA			Write '1' to Enable interrupt for PREGION[0].WA event
				See EVENTS_PREGION[0].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
J	RW PREGIONORA			Write '1' to Enable interrupt for PREGION[0].RA event
		Cat	4	See EVENTS_PREGION[0].RA
		Set	1	Enable Read: Disabled
		Disabled	0	Read: Disabled
V	DW DDECIONALIA	Enabled	1	Read: Enabled
K	RW PREGION1WA			Write '1' to Enable interrupt for PREGION[1].WA event



Bit n	umbe	er		3:	1 30	29	28	27	26	25	24	23 2	22	21	20	19	18	17	16 1	15 1	14 1	.3 1	2 11	. 10	9	8	7	6	5	4	3 2	1	0
Id								L	K	J	1																Н	G	F	E I) C	В	Α
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	٧	alue							Des	cri	ptio	n																		
												See	EV	/EN	TS_	PRE	GIO]NC	1].V	VA													
			Set	1								Ena	ble	è																			
			Disabled	0								Rea	ıd: I	Disa	ble	ed																	
			Enabled	1								Rea	ıd: I	Ena	ble	d																	
L	RW	PREGION1RA										Wri	te '	'1' t	o E	nab	le i	nte	rrup	ot fo	or P	REG	SION	[1].	RA e	ever	nt						
												See	ΕV	/EN	TS_	PRE	GIO]NC	1].F	A													
			Set	1								Ena	ble	9																			
			Disabled	0								Rea	d: I	Disa	ble	ed																	
			Enabled	1								Rea	ıd: I	Ena	ble	d																	

44.1.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number			6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
d			(JI H G F E D C B A
Reset 0x0000000			
d RW Field	Value Id	Value	Description
A RW REGIO	NOWA		Write '1' to Disable interrupt for REGION[0].WA event
			See EVENTS_REGION[0].WA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
RW REGIO	NORA		Write '1' to Disable interrupt for REGION[0].RA event
			See EVENTS_REGION[0].RA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW REGIO	N1WA		Write '1' to Disable interrupt for REGION[1].WA event
			See EVENTS_REGION[1].WA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
O RW REGIO		-	Write '1' to Disable interrupt for REGION[1].RA event
			See EVENTS_REGION[1].RA
	Clear	1	Disable
	Disabled	0	Read: Disabled
- 014 05010	Enabled	1	Read: Enabled
RW REGIO	N2WA		Write '1' to Disable interrupt for REGION[2].WA event
			See EVENTS_REGION[2].WA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
RW REGIO	N2RA		Write '1' to Disable interrupt for REGION[2].RA event
			See EVENTS_REGION[2].RA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
G RW REGIO	N3WA		Write '1' to Disable interrupt for REGION[3].WA event
			See EVENTS_REGION[3].WA
	Clear	1	Disable



Bitı	number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L K J I	HGFEDCBA
Res	set 0x00000000		0 0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field Val	lue Id	Value	Description
	Dis	sabled	0	Read: Disabled
	Ena	abled	1	Read: Enabled
Н	RW REGION3RA			Write '1' to Disable interrupt for REGION[3].RA event
				See EVENTS_REGION[3].RA
	Cle	ear		Disable
				Read: Disabled
				Read: Enabled
ı	RW PREGIONOWA			Write '1' to Disable interrupt for PREGION[0].WA event
				See EVENTS_PREGION[0].WA
	Cle	-ar		Disable
				Read: Disabled
				Read: Enabled
J	RW PREGIONORA			Write '1' to Disable interrupt for PREGION[0].RA event
				C EVENTS DOECIONIOLDA
	Cla			See EVENTS_PREGION[0].RA Disable
	Cle			
				Read: Disabled
	RW PREGION1WA	abled		Read: Enabled
K	RW PREGIONIWA			Write '1' to Disable interrupt for PREGION[1].WA event
				See EVENTS_PREGION[1].WA
	Cle	ear	1	Disable
	Dis	sabled	0	Read: Disabled
	Ena	abled	1	Read: Enabled
L	RW PREGION1RA			Write '1' to Disable interrupt for PREGION[1].RA event
				See EVENTS_PREGION[1].RA
	Cle	ear	1	Disable
	Dis	sabled	0	Read: Disabled
	Ena	abled	1	Read: Enabled

44.1.4 NMIEN

Address offset: 0x320

Enable or disable non-maskable interrupt

Bitı	numbe	r		31 30	29	28 2	7 2	6 25	5 24	1 23 22	21 20	0 19	9 18	3 17	16	15	14 :	13 1	2 13	10	9	8	7 6	5	4	3	2	1 0
Id						l	L I	K J	-1														H G	F	E	D	С	ВА
Res	et 0x0	0000000		0 0	0	0 (0 (0 0	0	0 0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value	•					Descri	iption	1																
Α	RW	REGION0WA								Enable	e or d	isab	ole n	non-	mas	kat	le i	nter	rupt	for	REG	ION	۱[0].۱	WΑ				
										event																		
										See EV	VENTS	S_RI	EGIC	ON[)]. N	/A												
			Disabled	0						Disabl	e																	
			Enabled	1						Enable	e																	
В	RW	REGIONORA								Enable	e or d	isab	ole n	non-	mas	kab	le i	nter	rupt	for	REG	ION	[0].	RA				
										event																		
										See EV	VENTS		EGIC	ON[0].R	4												
			Disabled	0						Disabl	e																	
			Enabled	1						Enable	e																	
С	RW	REGION1WA								Enable	e or d	isab	ole n	non-	mas	kat	le i	nter	rupt	for	REG	ION	۱[1].۱	WA				
										event																		
										See E	/ENTS	S_RI	EGIC)NC	1]. W	/A												
			Disabled	0						Disabl	e																	
			Enabled	1						Enable	e																	



Bit	numbe	er		31 30	29 28	27 20	5 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id							J	
Res	et 0x0	0000000		0 0	0 0	0 0	0 (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
D	RW	REGION1RA						Enable or disable non-maskable interrupt for REGION[1].RA event See EVENTS_REGION[1].RA
			Disabled	0				Disable
			Enabled	1				Enable
Е	RW	REGION2WA						Enable or disable non-maskable interrupt for REGION[2].WA event
			Disabled	0				See EVENTS_REGION[2].WA
			Disabled Enabled	0				Disable Enable
F	D\A/	REGION2RA	Enabled	1				Enable or disable non-maskable interrupt for REGION[2].RA
	11.00	REGIONZIA						event
			Disabled	0				See EVENTS_REGION[2].RA
			Disabled Enabled	0				Disable Enable
G	R\M	REGION3WA	Enableu	1				Enable or disable non-maskable interrupt for REGION[3].WA
J	11.00	REGIONSWA						event
								See EVENTS_REGION[3].WA
			Disabled	0				Disable
	DVA	REGION3RA	Enabled	1				Enable
Н	KVV	REGIONSKA						Enable or disable non-maskable interrupt for REGION[3].RA event
								See EVENTS_REGION[3].RA
			Disabled	0				Disable
			Enabled	1				Enable
'	KW	PREGIONOWA						Enable or disable non-maskable interrupt for PREGION[0].WA event
								See EVENTS_PREGION[0].WA
			Disabled	0				Disable
			Enabled	1				Enable
J	RW	PREGIONORA						Enable or disable non-maskable interrupt for PREGION[0].RA event
								See EVENTS_PREGION[0].RA
			Disabled	0				Disable
			Enabled	1				Enable
K	RW	PREGION1WA						Enable or disable non-maskable interrupt for PREGION[1].WA event
								See EVENTS_PREGION[1].WA
			Disabled	0				Disable
			Enabled	1				Enable
L	RW	PREGION1RA						Enable or disable non-maskable interrupt for PREGION[1].RA event
								See EVENTS_PREGION[1].RA
			Disabled	0				Disable
			Enabled	1				Enable

44.1.5 NMIENSET

Address offset: 0x324

Enable non-maskable interrupt



	number			6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	at 0::0000000			H G F E D C B A
Res	et 0x00000000 RW Field	Value Id	Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
A	RW REGIONOWA	value lu	value	Write '1' to Enable non-maskable interrupt for REGION[0].WA event
		Set	1	See <i>EVENTS_REGION[0].WA</i> Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW REGIONORA			Write '1' to Enable non-maskable interrupt for REGION[0].RA event
		Set	1	See EVENTS_REGION[0].RA Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW REGION1WA			Write '1' to Enable non-maskable interrupt for REGION[1].WA event
				See EVENTS_REGION[1].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW REGION1RA			Write '1' to Enable non-maskable interrupt for REGION[1].RA event
				See EVENTS_REGION[1].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
E	RW REGION2WA	Enabled	1	Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[2].WA event
				See EVENTS_REGION[2].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW REGION2RA			Write '1' to Enable non-maskable interrupt for REGION[2].RA event
				See EVENTS_REGION[2].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW REGION3WA			Write '1' to Enable non-maskable interrupt for REGION[3].WA event
				See EVENTS_REGION[3].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
	D	Enabled	1	Read: Enabled
Н	RW REGION3RA			Write '1' to Enable non-maskable interrupt for REGION[3].RA event
				See EVENTS_REGION[3].RA
		Set	1	Enable People Disabled
		Disabled	0	Read: Disabled
	RW PREGIONOWA	Enabled	1	Read: Enabled Write '1' to Enable non-markable interrupt for PREGIONIO WA
•	NVV PREGIONUWA			Write '1' to Enable non-maskable interrupt for PREGION[0].WA event
				See EVENTS_PREGION[0].WA



Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		L K	J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
ld RW Field	Value Id	Value	Description
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
J RW PREGION	ORA		Write '1' to Enable non-maskable interrupt for PREGION[0].RA
			event
			See EVENTS_PREGION[0].RA
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
K RW PREGION	1WA		Write '1' to Enable non-maskable interrupt for PREGION[1].WA
			event
			See EVENTS_PREGION[1].WA
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
L RW PREGION			Write '1' to Enable non-maskable interrupt for PREGION[1].RA
			event
			C EVENTS DDECION(A) DA
	C-L	1	See EVENTS_PREGION[1].RA
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

44.1.6 NMIENCLR

Address offset: 0x328

Disable non-maskable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		L K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW REGIONOWA		Write '1' to Disable non-maskable interrupt for REGION[0].WA
		event
		See EVENTS_REGION[0].WA
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
B RW REGIONORA		Write '1' to Disable non-maskable interrupt for REGION[0].RA
		event
		See EVENTS_REGION[0].RA
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
C RW REGION1WA		Write '1' to Disable non-maskable interrupt for REGION[1].WA
		event
		C CICITO DECIDATE LIVE
	CI.	See EVENTS_REGION[1].WA
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
D RW REGION1RA		Write '1' to Disable non-maskable interrupt for REGION[1].RA
		event
		See EVENTS_REGION[1].RA



Bitı	number		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L K J	
Res	set 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Clear	1	Disable
		Disabled	0	Read: Disabled
_	DIV. DECIONAVA	Enabled	1	Read: Enabled
Ε	RW REGION2WA			Write '1' to Disable non-maskable interrupt for REGION[2].WA
				event
				See EVENTS_REGION[2].WA
		Clear	1	Disable
		Disabled	0	Read: Disabled
F	RW REGION2RA	Enabled	1	Read: Enabled
r	RW REGIONZRA			Write '1' to Disable non-maskable interrupt for REGION[2].RA event
				event
				See EVENTS_REGION[2].RA
		Clear	1	Disable
		Disabled	0	Read: Disabled
	DIV. DECIONAVA	Enabled	1	Read: Enabled
G	RW REGION3WA			Write '1' to Disable non-maskable interrupt for REGION[3].WA
				event
				See EVENTS_REGION[3].WA
		Clear	1	Disable
		Disabled	0	Read: Disabled
	DIAL DECIGNIZA	Enabled	1	Read: Enabled
Н	RW REGION3RA			Write '1' to Disable non-maskable interrupt for REGION[3].RA
				event
				See EVENTS_REGION[3].RA
		Clear	1	Disable
		Disabled	0	Read: Disabled
1	RW PREGIONOWA	Enabled	1	Read: Enabled Write '1' to Disable non-maskable interrupt for PREGION[0].WA
'	RW PREGIONOWA			event
				See EVENTS_PREGION[0].WA
		Clear	1	Disable
		Disabled Enabled	0 1	Read: Disabled Read: Enabled
1	RW PREGIONORA	Ellableu	1	Write '1' to Disable non-maskable interrupt for PREGION[0].RA
,	RW FREGIONORA			event
				See EVENTS_PREGION[0].RA
		Clear	1	Disable Pand: Disabled
		Disabled	0	Read: Disabled
K	RW PREGION1WA	Enabled	1	Read: Enabled Write '1' to Disable non-maskable interrupt for PREGION[1].WA
K	RW FREGIONIWA			event
		Class	1	See EVENTS_PREGION[1].WA
		Clear Disabled	1 0	Disable Read: Disabled
		Enabled	1	Read: Enabled
L	RW PREGION1RA	LIIADICU	1	Write '1' to Disable non-maskable interrupt for PREGION[1].RA
-	THEOLOGICA			event
		Class	1	See EVENTS_PREGION[1].RA
		Clear	1	Disable Pead: Disabled
		Disabled Enabled	1	Read: Disabled Read: Enabled
		LITUDICU	1	nedd. Ellabied



44.1.7 PERREGION[0].SUBSTATWA

Address offset: 0x400

Source of event/interrupt in region 0, write access detected while corresponding subregion was enabled for watching

Signature Sign	I H G	F E D C B
Id RW Field Value Id Value Description A RW SRO Subregion 0 in region 0 (write '1' to clear) No Access 0 No write access occurred in this subregion B RW SR1 Write access(es) occurred in this subregion B RW SR1 No Access 0 No write access occurred in this subregion C RW SR2 Subregion 2 in region 0 (write '1' to clear) No Access 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion D RW SR3 Subregion 3 in region 0 (write '1' to clear) No Access 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion E RW SR4 Subregion 4 in region 0 (write '1' to clear)	0 0 0	0 0 0 0 0
A RW SR0 NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion B RW SR1 NoAccess 0 No write access occurred in this subregion NoAccess 1 Write access(es) occurred in this subregion Access 1 Write access(es) occurred in this subregion Write access(es) occurred in this subregion Access 1 Write access(es) occurred in this subregion No write access occurred in this subregion No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion Write access(es) occurred in this subregion No write access occurred in this subregion NoAccess 1 Write access(es) occurred in this subregion NoAccess 1 Write access occurred in this subregion Access 1 Write access(es) occurred in this subregion NoAccess 1 Write access(es) occurred in this subregion Access 1 Write access(es) occurred in this subregion No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion		
NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion B RW SR1 Subregion 1 in region 0 (write '1' to clear) NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion Write access(es) occurred in this subregion Access 1 Write access occurred in this subregion NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion Write access(es) occurred in this subregion Access 1 Write access(es) occurred in this subregion NoAccess 1 Write access occurred in this subregion Access 1 Write access occurred in this subregion NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion		
Access 1 Write access(es) occurred in this subregion B RW SR1 Subregion 1 in region 0 (write '1' to clear) NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion Subregion 2 in region 0 (write '1' to clear) NoAccess 0 No write access occurred in this subregion NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion Write access(es) occurred in this subregion No write access occurred in this subregion NoAccess 1 Write access(es) occurred in this subregion NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion Subregion 4 in region 0 (write '1' to clear)		
B RW SR1 Subregion 1 in region 0 (write '1' to clear) NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion Subregion 2 in region 0 (write '1' to clear) NoAccess 0 No write access occurred in this subregion NoAccess 1 Write access(es) occurred in this subregion Access 1 Write access(es) occurred in this subregion D RW SR3 Subregion 3 in region 0 (write '1' to clear) NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion Subregion 4 in region 0 (write '1' to clear)		
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C RW SR2 Subregion 2 in region 0 (write '1' to clear) NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion D RW SR3 Subregion 3 in region 0 (write '1' to clear) NoAccess 0 No write access occurred in this subregion NoAccess 1 Write access occurred in this subregion Roberts 1 Write access(es) occurred in this subregion Subregion 4 in region 0 (write '1' to clear)		
NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion D RW SR3 Subregion 3 in region 0 (write '1' to clear) NoAccess 0 No write access occurred in this subregion NoAccess 1 Write access(es) occurred in this subregion Access 1 Write access(es) occurred in this subregion Subregion 4 in region 0 (write '1' to clear)		
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D RW SR3 Subregion 3 in region 0 (write '1' to clear) NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion E RW SR4 Subregion 4 in region 0 (write '1' to clear)		
NoAccess 0 No write access occurred in this subregion Access 1 Write access(es) occurred in this subregion E RW SR4 Subregion 4 in region 0 (write '1' to clear)		
Access 1 Write access(es) occurred in this subregion E RW SR4 Subregion 4 in region 0 (write '1' to clear)		
E RW SR4 Subregion 4 in region 0 (write '1' to clear)		
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NOACCESS 0 NO WITE access occurred in this subregion		
Access 1 Write access(es) occurred in this subregion		
F RW SR5 Subregion 5 in region 0 (write '1' to clear)		
NoAccess 0 No write access occurred in this subregion		
Access 1 Write access(es) occurred in this subregion		
G RW SR6 Subregion 6 in region 0 (write '1' to clear)		
NoAccess 0 No write access occurred in this subregion		
Access 1 Write access(es) occurred in this subregion		
H RW SR7 Subregion 7 in region 0 (write '1' to clear)		
NoAccess 0 No write access occurred in this subregion		
Access 1 Write access(es) occurred in this subregion		
I RW SR8 Subregion 8 in region 0 (write '1' to clear)		
NoAccess 0 No write access occurred in this subregion		
Access 1 Write access(es) occurred in this subregion		
J RW SR9 Subregion 9 in region 0 (write '1' to clear)		
NoAccess 0 No write access occurred in this subregion		
Access 1 Write access(es) occurred in this subregion		
K RW SR10 Subregion 10 in region 0 (write '1' to clear)		
NoAccess 0 No write access occurred in this subregion		
Access 1 Write access(es) occurred in this subregion		
L RW SR11 Subregion 11 in region 0 (write '1' to clear)		
NoAccess 0 No write access occurred in this subregion		
Access 1 Write access(es) occurred in this subregion		
M RW SR12 Subregion 12 in region 0 (write '1' to clear)		
NoAccess 0 No write access occurred in this subregion		
Access 1 Write access(es) occurred in this subregion		
N RW SR13 Subregion 13 in region 0 (write '1' to clear)		
NoAccess 0 No write access occurred in this subregion		
Access 1 Write access(es) occurred in this subregion		
O RW SR14 Subregion 14 in region 0 (write '1' to clear)		
NoAccess 0 No write access occurred in this subregion		
Access 1 Write access(es) occurred in this subregion		
P RW SR15 Subregion 15 in region 0 (write '1' to clear)		
NoAccess 0 No write access occurred in this subregion		
Noncess of the write access occurred in this sauregion		
Access 1 Write access(es) occurred in this subregion Q RW SR16 Subregion 16 in region 0 (write '1' to clear)		



Bit r	numbe	er		31 30	29 28	27	26 25	24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id				f e	d c	b	a Z	Υ	/ X W V U T S R Q P O N M L K J I H G F E D C B
Res	et 0x0	0000000		0 0	0 0	0	0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
R	RW	SR17							Subregion 17 in region 0 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
S	RW	SR18							Subregion 18 in region 0 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Т	RW	SR19							Subregion 19 in region 0 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
U	RW	SR20							Subregion 20 in region 0 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
٧	RW	SR21							Subregion 21 in region 0 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
W	RW	SR22							Subregion 22 in region 0 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Х	RW	SR23	7100033	•					Subregion 23 in region 0 (write '1' to clear)
^		51125	NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Υ	R\M	SR24	7100033	-					Subregion 24 in region 0 (write '1' to clear)
	11.00	31/24	NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Z	D\A/	SR25	Access	1					Subregion 25 in region 0 (write '1' to clear)
_	11.00	31/23	NoAccess	0					
				1					No write access occurred in this subregion Write access(as) accurred in this subregion
	D\A/	SR26	Access	1					Write access(es) occurred in this subregion
a	NVV	3N20	NaAssass	0					Subregion 26 in region 0 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
L	DVA	CD27	Access	1					Write access(es) occurred in this subregion
b	KVV	SR27	N-A	0					Subregion 27 in region 0 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
C	RW	SR28		_					Subregion 28 in region 0 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
d	RW	SR29							Subregion 29 in region 0 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
е	RW	SR30							Subregion 30 in region 0 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
f	RW	SR31							Subregion 31 in region 0 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion

44.1.8 PERREGION[0].SUBSTATRA

Address offset: 0x404

Source of event/interrupt in region 0, read access detected while corresponding subregion was enabled for watching



The color	Bit r	numbe	er		31 30	29 28	27 26	25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
March Marc									
No.	Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
No.	Id	RW	Field	Value Id	Value				Description
Read accessiciency coursed in this subregion Read accessiciency coursed in this subregion Received Rec	Α	RW	SR0						Subregion 0 in region 0 (write '1' to clear)
B RW SR1 NoAccess 0 No read access occurred in this subregion C RW SS2 Subregion 1 in region 0 (pwire "1" to clean") D RW SS2 Subregion 2 in region 0 (pwire "1" to clean") D RW SS3 No read access occurred in this subregion D RW SS3 No read access occurred in this subregion E RW SS4 No read access occurred in this subregion E RW SS4 No read access occurred in this subregion E RW SS4 No read access occurred in this subregion B RW SS5 1 Read accessed occurred in this subregion B RW SS5 1 Read accessed occurred in this subregion B RW SS5 1 Read accessed occurred in this subregion B RW SS6 1 Read accessed occurred in this subregion B RW SS6 1 Read accessed occurred in this subregion B RW SS7 Subregion 1 in region 0 (w				NoAccess	0				No read access occurred in this subregion
No.				Access	1				Read access(es) occurred in this subregion
Read access[es] occurred in this subregion Read access[es] occurred in this subregion Access 1	В	RW	SR1						Subregion 1 in region 0 (write '1' to clear)
No				NoAccess	0				No read access occurred in this subregion
No read access occurred in this subregion Access 1 Read access[e] occurred in this subregion Read ac				Access	1				Read access(es) occurred in this subregion
	С	RW	SR2						Subregion 2 in region 0 (write '1' to clear)
New SR3				NoAccess	0				No read access occurred in this subregion
No				Access	1				Read access(es) occurred in this subregion
Rev	D	RW	SR3						Subregion 3 in region 0 (write '1' to clear)
E RW SR4 Subregion 4 in region 0 (write '1' to clear) F RW SR5 1 Read accesses occurred in this subregion F RW SR5 SR5 Subregion 5 in region 0 (write '1' to clear) G RW SR6 1 Read access (see) occurred in this subregion G RW SR6 1 Read access (see) occurred in this subregion H RW SR7 Subregion 5 in region 0 (write '1' to clear) NoAccess 1 Read access (see) occurred in this subregion Access 1 Read access (see) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access (see) occurred in this subregion No RW SR8 1 Read access occurred in this subregion No Read access occurred in Region 0 (write '1' to clear) No Read access occurred in this subregion No RW SR1 No Read access occurred in this subregion No Read access occurred in Read access occurred				NoAccess	0				No read access occurred in this subregion
No.				Access	1				Read access(es) occurred in this subregion
Access 1	E	RW	SR4						Subregion 4 in region 0 (write '1' to clear)
Subsection Sub				NoAccess	0				No read access occurred in this subregion
No. No. Rev. No. No. Rev. No. Red. Courted in this subregion				Access	1				Read access(es) occurred in this subregion
	F	RW	SR5						Subregion 5 in region 0 (write '1' to clear)
G RW SR6 NoAccess 0 No read access occurred in this subregion H RW SR7 Subregion 7 in region 0 (write "1" to clear) H RW SR7 Subregion 7 in region 0 (write "1" to clear) I RW SR8 1 Read access (es) occurred in this subregion I RW SR8 1 Read access (es) occurred in this subregion J RW SR8 1 Read access (es) occurred in this subregion J RW SR9 1 Read access (es) occurred in this subregion J RW SR9 1 Read access (es) occurred in this subregion J RW SR9 1 Read access (es) occurred in this subregion J RW SR10 1 Read access (es) occurred in this subregion K RW SR10 1 Read access (es) occurred in this subregion L RW SR11 1 Read access (es) occurred in this subregion M RW SR12 1 Read access (es) occurred in this subregion<				NoAccess	0				No read access occurred in this subregion
No. Access				Access	1				Read access(es) occurred in this subregion
No.	G	RW	SR6						Subregion 6 in region 0 (write '1' to clear)
Note				NoAccess	0				No read access occurred in this subregion
NoAccess No No read access occurred in this subregion RW SR8				Access	1				Read access(es) occurred in this subregion
RW SRB	Н	RW	SR7						Subregion 7 in region 0 (write '1' to clear)
RW SR8				NoAccess	0				No read access occurred in this subregion
No. No. read access occurred in this subregion				Access	1				Read access(es) occurred in this subregion
Read access(es) occurred in this subregion Subregi	I	RW	SR8						Subregion 8 in region 0 (write '1' to clear)
Subregion 9 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subr				NoAccess	0				No read access occurred in this subregion
No Access No A				Access	1				Read access(es) occurred in this subregion
RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC	J	RW	SR9						Subregion 9 in region 0 (write '1' to clear)
K RW SR10 NoAccess 0 No No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion				NoAccess	0				No read access occurred in this subregion
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion L RW SR11 Sourcess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion				Access	1				Read access(es) occurred in this subregion
L RW SR11 Subregion 11 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion No RW SR12 Subregion 12 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion No RW SR13 Subregion 12 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion No Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion No Read access occurred in this subregion No Read access occurred in this subregion No Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion	K	RW	SR10						Subregion 10 in region 0 (write '1' to clear)
L RW SR11 NoAccess 0 No No read access occurred in this subregion 0 (write '1' to clear) RW RW SR12 Subregion 12 in region 0 (write '1' to clear) NoAccess 1 No read access occurred in this subregion No RW SR13 Read access(se) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(se) occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(se) occurred in this subregion No read access occurred in this subregion				NoAccess	0				No read access occurred in this subregion
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M RW SR12 Subregion 12 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion No No read access occurred in this subregion Read access(es) occurred in this subregion No No read access occurred in this subregion No read access occurred in this subregion				NoAccess	0				No read access occurred in this subregion
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N RW SR13 N ACCESS 1 NOACCESS 0 NO Read access(es) occurred in this subregion NOACCESS 0 NO Read access occurred in this subregion ACCESS 1 Read access(es) occurred in this subregion NO RW SR14 NOACCESS 0 NO Read access occurred in this subregion NO RW SR15 Read access(es) occurred in this subregion NO READ SR15 NOACCESS 0 NO Read access occurred in this subregion Read access(es) occurred in this subregion NO Read access occurred in this subregion Read access(es) occurred in this subregion NO Read access occurred in this subregion NO Read access occurred in this subregion Read access occurred in this subregion NO Read access occurred in this subregion Read access occurred in this subregion NO Read access occurred in this subregion NO Read access occurred in this subregion	М	RW	SR12						Subregion 12 in region 0 (write '1' to clear)
N RW SR13 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion O RW SR14 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion Read access(es) occurred in this subregion No Read access(es) occurred in this subregion No Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access occurred in this subregion Read access occurred in this subregion NoAccess 1 Read access occurred in this subregion No Read access occurred in this subregion No Read access occurred in this subregion				NoAccess	0				No read access occurred in this subregion
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion No RW SR14 SR14 Subregion 14 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion No Read access(es) occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion Read access occurred in this subregion No read access occurred in this subregion				Access	1				Read access(es) occurred in this subregion
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Subregion 14 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion P RW SR15 NoAccess 0 No read access occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion Subregion 16 in region 0 (write '1' to clear) NoAccess No No read access occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion				NoAccess	0				No read access occurred in this subregion
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion P RW SR15 Subregion 15 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 16 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion No read access occurred in this subregion Subregion 16 in region 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion R RW SR17 Subregion 17 in region 0 (write '1' to clear) NoAccess 1 Read access occurred in this subregion R Read access occurred in this subregion R Read access occurred in this subregion R Read access occurred in this subregion				Access	1				Read access(es) occurred in this subregion
Access 1 Read access(es) occurred in this subregion P RW SR15 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 16 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion No Read access occurred in this subregion No Read access occurred in this subregion Read access(es) occurred in this subregion Subregion 17 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Read access(es) occurred in this subregion Read access occurred in this subregion Read access occurred in this subregion Read access occurred in this subregion	0	RW	SR14						Subregion 14 in region 0 (write '1' to clear)
P RW SR15 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Q RW SR16 NoAccess 0 No read access occurred in this subregion NoAccess 1 Subregion 16 in region 0 (write '1' to clear) NoAccess 1 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion R RW SR17 NoAccess 0 No read access occurred in this subregion No read access occurred in this subregion R Read access(es) occurred in this subregion R Read access occurred in this subregion				NoAccess	0				No read access occurred in this subregion
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Access 1 Read access(es) occurred in this subregion Q RW SR16 Subregion 16 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 17 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access occurred in this subregion Read access occurred in this subregion Read access occurred in this subregion	Р	RW	SR15						Subregion 15 in region 0 (write '1' to clear)
Q RW SR16 Subregion 16 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 17 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion R RW SR17 Subregion 17 in region 0 (write '1' to clear) NoAccess 1 Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion				NoAccess	0				No read access occurred in this subregion
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion R RW SR17 Subregion 17 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion				Access	1				Read access(es) occurred in this subregion
Access 1 Read access(es) occurred in this subregion R RW SR17 Subregion 17 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion	Q	RW	SR16						Subregion 16 in region 0 (write '1' to clear)
R RW SR17 Subregion 17 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion				NoAccess	0				No read access occurred in this subregion
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion				Access	1				Read access(es) occurred in this subregion
Access 1 Read access(es) occurred in this subregion	R	RW	SR17						Subregion 17 in region 0 (write '1' to clear)
* * * * * * * * * * * * * * * * * * * *				NoAccess	0				No read access occurred in this subregion
S RW SR18 Subregion 18 in region 0 (write '1' to clear)				Access	1				Read access(es) occurred in this subregion
	S	RW	SR18						Subregion 18 in region 0 (write '1' to clear)



Bit r	numbe	er		31 30	29	9 28	27	26	25	24	23	3 22 2:	1 2	0 19	9 1	8 1	7 1	6 1	5 :	14	13	12	2 1	1 1	0	9	8	7	6	5	4	3	2	1
Id				f e	d	С	b	а	Z	Υ	Χ	w v	/ l	U T		S F	₹ (QΙ	D	О	N	М		L F	<	J		н	G	F	E	D	С	В.
	et 0x0	0000000										0 0																						
Id		Field	Value Id	Value								escript																						
			NoAccess	0								o read			00	cur	rec	l in	thi	is	sub	reg	gio	n										
			Access	1							Re	ead ac	ces	s(es) o	ccu	rre	d ir	ı th	nis	suk	re	gio	on										
Т	RW	SR19									Su	ıbregio	on	19 ir	re	egio	n () (w	rit	e	1' t	o c	le	ar)										
			NoAccess	0							No	o read	ac	cess	00	cur	rec	lin	thi	is	sub	reg	gio	n										
			Access	1							Re	ead ac	ces	s(es) o	ccu	rre	d ir	ı th	ıis	sub	re	gio	on										
U	RW	SR20									Su	ıbregio	on	20 ir	n re	egio	n () (w	rit	e '	1' t	o c	le	ar)										
			NoAccess	0							No	o read	ac	cess	00	cur	rec	l in	thi	is	sub	reg	gio	n										
			Access	1							Re	ead ac	ces	s(es) o	ccu	rre	d ir	th	iis	sub	re	gio	on										
٧	RW	SR21									Su	ıbregio	on	21 ir	n re	egio	n () (w	rit	e '	1' t	о с	le	ar)										
			NoAccess	0							No	o read	ac	cess	00	cur	rec	l in	thi	is	sub	reg	gio	n										
			Access	1							Re	ead ac	ces	s(es) o	ccu	rre	d ir	th	iis	sub	re	gio	on										
W	RW	SR22									Su	ıbregio	on	22 ir	n re	gio	n ((w	rit	e '	1' t	о с	le	ar)										
			NoAccess	0							No	o read	ac	cess	00	cur	rec	l in	thi	is	sub	reg	gio	n										
			Access	1							Re	ead ac	ces	s(es) o	ccu	rre	d ir	th	iis	suk	re	gio	on										
Χ	RW	SR23									Su	ıbregio	on	23 ir	n re	egio	n ((w	rit	e '	1' t	о с	le	ar)										
			NoAccess	0							No	o read	ac	cess	00	cur	rec	l in	thi	is	sub	reg	gio	n										
			Access	1							Re	ead ac	ces	s(es) o	ccu	rre	d ir	th	iis	sub	re	gio	on										
Υ	RW	SR24									Su	ıbregio	on	24 ir	n re	egio	n ((w	rit	e '	1' t	о с	le	ar)										
			NoAccess	0							No	o read	ac	cess	00	cur	rec	l in	thi	is	sub	reg	gio	n										
			Access	1							Re	ead ac	ces	s(es) o	ccu	rre	d ir	th	iis	suk	re	gio	on										
Z	RW	SR25									Su	ıbregio	on	25 ir	n re	egio	n () (w	rit	e '	1' t	о с	le	ar)										
			NoAccess	0							No	o read	ac	cess	00	cur	rec	l in	thi	is	sub	reg	gio	n										
			Access	1							Re	ead ac	ces	ss(es) o	ccu	rre	d ir	th	iis	suk	re	gio	on										
а	RW	SR26									Su	ıbregio	on	26 ir	n re	egio	n () (w	rit	e '	1' t	o c	le	ar)										
			NoAccess	0							No	o read	ac	cess	00	cur	rec	l in	thi	is	sub	reg	gio	n										
			Access	1							Re	ead ac	ces	s(es) o	ccu	rre	d ir	th	iis	suk	re	gio	on										
b	RW	SR27									Su	ıbregio	on	27 ir	n re	egio	n () (w	rit	e '	1' t	o c	le	ar)										
			NoAccess	0							No	o read	ac	cess	00	cur	rec	l in	thi	is:	sub	reg	gio	n										
			Access	1								ead ac											-											
С	RW	SR28		_								ıbregio				-																		
			NoAccess	0								o read																						
			Access	1								ead ac											_											
d	RW	SR29		•								ıbregio				-		•																
			NoAccess	0								o read																						
	D	cnao	Access	1								ead ac											_											
е	кW	SR30	NaAaaaa	0								ıbregio				-		•						•										
			NoAccess	0								o read																						
	DIA	CD24	Access	1								ead ac		•									•											
Т	KW	SR31	NaAaaaa	0								ıbregio				-																		
			NoAccess	0								o read																						
			Access	1							ке	ead ac	ces	s(es) 0	ccu	rre	u Ir	rtr	IIS	sut	re	gi	ווכ										

44.1.9 PERREGION[1].SUBSTATWA

Address offset: 0x408

Source of event/interrupt in region 1, write access detected while corresponding subregion was enabled for watching

Bit	numbe	er		3	1 30	29	28	3 27	7 26	25	24	23	22	21 2	20 1	.9 1	.8 1	7 16	5 15	14	13 3	12 :	11 1	0 9	8	7	6	5	4	3	2	1 0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U .	Т :	S R	Q	P	0	N	М	LI	()	-1	Н	G	F	Ε	D	С	ВА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	٧	alue	•						De	scrip	otio	n																	
Α	RW	SR0										Sul	oreg	ion	0 ir	re	gion	1 (\	writ	e '1'	to c	lea	r)									
			NoAccess	0								No	wri	te a	cce	ss o	ccu	red	in t	his	subr	egi	on									
			Access	1								Wr	ite a	ассе	ess(e	es) (occu	rre	d in	this	sub	reg	ion									



Rit r	numbe	or .		31 30	29 28	3 27	26.2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	iuiiibo	-1							X W V U T S R Q P O N M L K J I H G F E D C B A
	et 0x0	0000000							0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
В	RW	SR1							Subregion 1 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
С	RW	SR2							Subregion 2 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
D	RW	SR3							Subregion 3 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Е	RW	SR4							Subregion 4 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
F	RW	SR5							Subregion 5 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
G	RW	SR6							Subregion 6 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Н	RW	SR7							Subregion 7 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
I	RW	SR8							Subregion 8 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
J	RW	SR9							Subregion 9 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
K	RW	SR10							Subregion 10 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
	DIA	CD11	Access	1					Write access(es) occurred in this subregion
L	KW	SR11	NaAssass	0					Subregion 11 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
N 4	D\A/	CD12	Access	1					Write access(es) occurred in this subregion
М	KVV	SR12	NoAccors	0					Subregion 12 in region 1 (write '1' to clear)
			NoAccess Access	0					No write access occurred in this subregion Write access(es) occurred in this subregion
N	R\M	SR13	Access	1					Subregion 13 in region 1 (write '1' to clear)
IN	IVV	31(13	NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
0	RW	SR14	recess	-					Subregion 14 in region 1 (write '1' to clear)
_			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Р	RW	SR15		-					Subregion 15 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Q	RW	SR16							Subregion 16 in region 1 (write '1' to clear)
-			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
R	RW	SR17							Subregion 17 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
S	RW	SR18							Subregion 18 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Т	RW	SR19							Subregion 19 in region 1 (write '1' to clear)



Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			Y X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	NoAccess	0	No write access occurred in this subregion
	Access	1	Write access(es) occurred in this subregion
U RW SR20			Subregion 20 in region 1 (write '1' to clear)
5 III 51125	NoAccess	0	No write access occurred in this subregion
	Access	1	Write access(es) occurred in this subregion
V RW SR21	, 100000	-	Subregion 21 in region 1 (write '1' to clear)
	NoAccess	0	No write access occurred in this subregion
	Access	1	Write access(es) occurred in this subregion
W RW SR22	Access	±	Subregion 22 in region 1 (write '1' to clear)
W IWW SINZZ	NoAccess	0	No write access occurred in this subregion
	Access	1	Write access(es) occurred in this subregion
X RW SR23	Access	1	Subregion 23 in region 1 (write '1' to clear)
A I(W 3I(23	NoAccess	0	No write access occurred in this subregion
	Access	1	Write access(es) occurred in this subregion
Y RW SR24	Access	1	Subregion 24 in region 1 (write '1' to clear)
1 NW 3N24	NoAccess	0	No write access occurred in this subregion
	Access	1	Write access(es) occurred in this subregion
Z RW SR25	Access	1	Subregion 25 in region 1 (write '1' to clear)
Z IVW SIVZS	NoAccess	0	No write access occurred in this subregion
	Access	1	Write access(es) occurred in this subregion
a RW SR26	Access	1	Subregion 26 in region 1 (write '1' to clear)
d NVV 3N2U	NoAccess	0	No write access occurred in this subregion
	Access	1	Write access(es) occurred in this subregion
b RW SR27	Access	1	Subregion 27 in region 1 (write '1' to clear)
D NVV 3N27	NoAccess	0	No write access occurred in this subregion
	Access	1	Write access(es) occurred in this subregion
c RW SR28	Access	1	Subregion 28 in region 1 (write '1' to clear)
C NVV 3NZO	NoAccord	0	No write access occurred in this subregion
	NoAccess Access	1	Write access(es) occurred in this subregion
d RW SR29	Access	1	· · · · · · · · · · · · · · · · · · ·
d RW SR29	No Accord	0	Subregion 29 in region 1 (write '1' to clear)
	NoAccess		No write access occurred in this subregion
o DW CD20	Access	1	Write access(es) occurred in this subregion
e RW SR30	No Accord	0	Subregion 30 in region 1 (write '1' to clear)
	NoAccess		No write access occurred in this subregion
f DW CD21	Access	1	Write access(es) occurred in this subregion
f RW SR31	No Accord	0	Subregion 31 in region 1 (write '1' to clear)
	NoAccess	0	No write access occurred in this subregion
	Access	1	Write access(es) occurred in this subregion

44.1.10 PERREGION[1].SUBSTATRA

Address offset: 0x40C

Source of event/interrupt in region 1, read access detected while corresponding subregion was enabled for watching

Bit nu	ımbe	r		31	30	29	28 2	27 :	26 2	25 2	24 2	3 2	2 21	20	19	18	17 :	16	15 1	.4 1	3 12	2 11	10	9	8	7	6	5 -	4 3	2	1	0
Id				f	e	d	С	b	a Z	Z	Υ 2	X V	V V	U	Т	S	R	Q	Р (1 C	N N	1 L	K	J	1	Н	G	F	E C	С	В	Α
Reset	0x0	0000000		0	0	0	0	0	0 (0	0 (0 (0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	lue						C	esc	ript	ion																		
Α	RW	SR0									S	ubr	egio	n 0	in r	egic	on 1	(w	rite	'1' t	o cl	ear)										
			NoAccess	0							١	lo r	ead	acce	ess (occi	ırre	d in	thi	s su	bre	gion										
			Access	1							R	lead	dacc	ess	(es)	occ	urre	d i	n th	is sı	ubre	gior	n									
В	RW	SR1									S	ubr	egio	n 1	in r	egic	on 1	(w	rite	'1' t	o cl	ear)										
			NoAccess	0							١	lo r	ead	acce	ess (occi	urre	d in	thi	s su	bre	gion										
			Access	1							R	lead	acc	ess	(es)	occ	urre	d i	n th	is sı	ubre	gior	ı									



F e d c b a Z Y X W V U T S R Q P O N M L K J I Reset 0x000000000					
Id RW Field Value Id Value Description C RW SR2 Subregion 2 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion D RW SR3 Subregion 3 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion E RW SR4 Subregion 4 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion for pagion 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion for pagion 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion for pagion 1 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion for pagion 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion for pagion 1 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion for pagion 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion for pagion 1 (write '1' to clear) NoAccess 1 Read access(es) oc	0 0	0 0	0 0	0 0	0 0 0
C RW SR2 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access occurred					
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D RW SR3 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access (es) occurred in this subregion Access 1 Read access (es) occurred in this subregion Access 1 Read access (es) occurred in this subregion Access 1 Read access (es) occurred in this subregion Access 1 Read access (es) occurred in this subregion Access 1 Read access (es) occurred in this subregion Access 1 Read access (es) occurred in this subregion Access 1 Read access (es) occurred in this subregion Access 1 Read access (es) occurred in this subregion Access 1 Read access (es) occurred in this subregi					
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Access 1 Read access(es) occurred in this subregion E RW SR4 SR4 SR4 SR4 Subregion 4 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion F RW SR5 Subregion 5 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion H RW SR7 Subregion 7 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion Subregion 8 in region 1 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion					
E RW SR4 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion F RW SR5 NoAccess 0 No read access occurred in this subregion Subregion 5 in region 1 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 6 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access Access 1 Read access(es) occurred in this subregion Access Access 1 Read access(es) occurred in this subregion Access Acc					
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Access 1 Read access(es) occurred in this subregion F RW SR5 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 6 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 7 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion					
F RW SR5 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 6 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion					
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Access 1 Read access(es) occurred in this subregion G RW SR6 Subregion 6 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 8 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 9 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion					
G RW SR6 NoAccess O No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 7 in region 1 (write '1' to clear) NoAccess O No read access occurred in this subregion NoAccess O No read access occurred in this subregion Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 8 in region 1 (write '1' to clear) NoAccess O No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 9 in region 1 (write '1' to clear) NoAccess NoAccess O No read access occurred in this subregion					
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Access 1 Read access(es) occurred in this subregion H RW SR7 Subregion 7 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 8 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 9 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion					
H RW SR7 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 8 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 9 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion					
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Access 1 Read access(es) occurred in this subregion Subregion 8 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 9 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion					
Subregion 8 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 9 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion					
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion J RW SR9 Subregion 9 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion					
Access 1 Read access(es) occurred in this subregion J RW SR9 Subregion 9 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion					
J RW SR9 Subregion 9 in region 1 (write '1' to clear) NoAccess 0 No read access occurred in this subregion					
NoAccess 0 No read access occurred in this subregion					
The state of the s					
Access 1 Read access(es) occurred in this subregion					
, , , , , , , , , , , , , , , , , , , ,					
K RW SR10 Subregion 10 in region 1 (write '1' to clear)					
NoAccess 0 No read access occurred in this subregion					
Access 1 Read access(es) occurred in this subregion					
L RW SR11 Subregion 11 in region 1 (write '1' to clear)					
NoAccess 0 No read access occurred in this subregion					
Access 1 Read access(es) occurred in this subregion					
M RW SR12 Subregion 12 in region 1 (write '1' to clear)					
NoAccess 0 No read access occurred in this subregion					
Access 1 Read access(es) occurred in this subregion					
N RW SR13 Subregion 13 in region 1 (write '1' to clear)					
NoAccess 0 No read access occurred in this subregion					
Access 1 Read access(es) occurred in this subregion					
O RW SR14 Subregion 14 in region 1 (write '1' to clear)					
NoAccess 0 No read access occurred in this subregion					
Access 1 Read access(es) occurred in this subregion					
P RW SR15 Subregion 15 in region 1 (write '1' to clear)					
NoAccess 0 No read access occurred in this subregion					
Access 1 Read access(es) occurred in this subregion					
Q RW SR16 Subregion 16 in region 1 (write '1' to clear)					
NoAccess 0 No read access occurred in this subregion					
Access 1 Read access(es) occurred in this subregion					
R RW SR17 Subregion 17 in region 1 (write '1' to clear)					
NoAccess 0 No read access occurred in this subregion					
Access 1 Read access(es) occurred in this subregion					
S RW SR18 Subregion 18 in region 1 (write '1' to clear)					
NoAccess 0 No read access occurred in this subregion					
Access 1 Read access(es) occurred in this subregion					
needs 1 nead access(es) occurred in this sublegion					
T RW SR19 Subregion 19 in region 1 (write '1' to clear)					
T RW SR19 Subregion 19 in region 1 (write '1' to clear)					



Bit ı	number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				X W V U T S R Q P O N M L K J I H G F E D C B A
Res	set 0x00000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
٧	RW SR21		:	Subregion 21 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
W	RW SR22		:	Subregion 22 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
Χ	RW SR23		3	Subregion 23 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
Υ	RW SR24		;	Subregion 24 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
Z	RW SR25		;	Subregion 25 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
а	RW SR26		!	Subregion 26 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
b	RW SR27		:	Subregion 27 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
С	RW SR28		;	Subregion 28 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
d	RW SR29		:	Subregion 29 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
e	RW SR30		:	Subregion 30 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
f	RW SR31			Subregion 31 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion

44.1.11 REGIONEN

Address offset: 0x510

Enable/disable regions watch

Bit r	numbe	r		31	30 2	29 2	28 2	7 2	6 25	5 24	23	3 22	21 2	20 1	19 1	.8 1	7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6 !	5 4	3	2	1	0
Id							L	_ K	(J	-1															1	4	G I	F E	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0 (0	0 (0 () () () (0	0	0	0	0	0	כ	0 (0 0	0	0	0	0
Id	RW	Field	Value Id	Val	lue						De	escri	ptio	n																		
Α	RW	RGN0WA									En	able	e/dis	abl	e wi	rite	acc	ess	wa	tch	in re	egio	n[0]									
			Disable	0							Dis	sabl	e wri	ite	acce	ess	wat	ch i	n t	his r	egic	n										
			Enable	1							En	able	e wri	te a	ассе	ss v	vat	:h i	n th	is re	egio	n										
В	RW	RGNORA									En	able	e/dis	abl	e re	ad	acc	ess	wat	ch i	n re	gior	1[0]									
			Disable	0							Dis	sabl	e rea	ad a	ссе	ss v	vato	h ii	n th	is re	egio	n										
			Enable	1							En	able	e rea	d a	cces	ss w	atc	h in	th	is re	gior	١										
С	RW	RGN1WA									En	able	e/dis	abl	e wi	rite	acc	ess	wa	tch	in re	egio	n[1]									
			Disable	0							Dis	sabl	e wri	ite	ассе	ess	wat	ch i	n t	his r	egic	n										
			Enable	1							En	able	e wri	te a	ассе	ss v	vat	:h i	n th	is re	egio	n										
D	RW	RGN1RA									En	able	e/dis	abl	e re	ad	acc	ess	wat	ch i	n re	gior	1[1]									



Bit r	numbe	er		3	1 30	29	28	27	26	25	24	23	3 2	22 2	21 2	0 :	19 1	18	17 1	16	15	14	13	12	2 13	1 1) 9) {	3 7	' (ŝ	5 4	4	3 2	2 1	1 0
Id								L	K	J	-1																		H	1 (ŝ	FI	ΕI) (C E	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0)	0	0 (0	0	0	0	0	0	0	0	0	0	C	0) (0) ()	0 (0	0 () (0 (
Id	RW	Field	Value Id	٧	alue	:						D	es	crip	otio	n																				
			Disable	0								Di	isa	able	rea	ıd a	ссе	ess	wat	ch	in	this	re	gio	n											
			Enable	1								Er	nal	ble	rea	d a	cce	SS	wat	ch	n t	his	reg	gior	n											
Е	RW	RGN2WA										Er	nal	ble,	/dis	abl	e w	rit	e ac	ces	s v	/at	:h i	n r	egi	on	[2]									
			Disable	0								Di	isa	able	wri	ite	acc	ess	wa	tcł	in	thi	s re	gio	on											
			Enable	1								Er	nal	ble	wri	te a	ассе	ess	wat	ch	in	thi	re	gio	n											
F	RW	RGN2RA										Er	nal	ble,	/dis	abl	e re	ad	acc	es	s w	atc	h ir	re	egic	n[2]									
			Disable	0								Di	isa	able	rea	ıd a	ссе	ess	wat	ch	in	this	re	gio	n											
			Enable	1								Er	nal	ble	rea	d a	cce	SS	wat	ch	n t	his	reg	gior	n											
G	RW	RGN3WA										Er	nal	ble,	/dis	abl	e w	rit	e ac	ces	s v	/at	:h i	n r	egi	on	[3]									
			Disable	0								Di	isa	able	wri	ite	acc	ess	wa	tcł	in	thi	s re	gio	on											
			Enable	1								Er	nal	ble	wri	te a	ассе	ess	wat	ch	in	thi	re	gio	n											
Н	RW	RGN3RA										Er	nal	ble	/dis	abl	e re	ad	acc	es	s w	atc	h ir	re	egic	n[3]									
			Disable	0								Di	isa	able	rea	nd a	ссе	ess	wat	ch	in	this	re	gio	n											
			Enable	1								Er	nal	ble	rea	d a	cce	SS	wat	ch	in t	his	reg	gior	n											
1	RW	PRGN0WA										Er	nal	ble,	/dis	abl	e w	rit	e ac	ces	s v	/at	:h i	n P	PRE	GIC	N[0]								
			Disable	0								Di	isa	able	wri	ite	acc	ess	wa	tcł	in	thi	s P	REC	GIC	N										
			Enable	1								Er	nal	ble	wri	te a	ассе	ess	wat	ch	in	thi	PF	REG	SIO	N										
J	RW	PRGNORA										Er	nal	ble,	/dis	abl	e re	ad	acc	es	s w	atc	h ir	PF	REC	GIO	N[C)]								
			Disable	0								Di	isa	able	rea	nd a	ссе	ess	wat	ch	in	this	PR	EG	οlo	N										
			Enable	1								Er	nal	ble	rea	d a	cce	SS	wat	ch	in t	his	PR	EG	101	١										
K	RW	PRGN1WA										Er	nal	ble,	/dis	abl	e w	rit	e ac	ces	s v	/at	:h i	n P	PRE	GIC	N[1]								
			Disable	0								Di	isa	able	wri	ite	acc	ess	wa	tcł	in	thi	s P	REC	GIC	N										
			Enable	1								Er	nal	ble	wri	te a	ассе	ess	wat	ch	in	thi	PF	REG	610	N										
L	RW	PRGN1RA										Er	nal	ble	/dis	abl	e re	ad	acc	es	s w	atc	h ir	PF	REC	SIO	N[1	.]								
			Disable	0								Di	isa	able	rea	nd a	ассе	ess	wat	ch	in	this	PR	EG	ίO	N										
			Enable	1								Er	nal	ble	rea	d a	cce	SS '	wat	ch	n t	his	PR	EG	101	٧										

44.1.12 REGIONENSET

Address offset: 0x514 Enable regions watch

Bit	numbe	r		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				L K J I	HGFEDCBA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	RGN0WA			Enable write access watch in region[0]
			Set	1	Enable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
В	RW	RGNORA			Enable read access watch in region[0]
			Set	1	Enable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
С	RW	RGN1WA			Enable write access watch in region[1]
			Set	1	Enable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
D	RW	RGN1RA			Enable read access watch in region[1]
			Set	1	Enable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
Е	RW	RGN2WA			Enable write access watch in region[2]
			Set	1	Enable write access watch in this region
			Disabled	0	Write access watch in this region is disabled



Bit	number			31 30	29 28 2	27 26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id						L K	J I	HGFEDCBA
Res	et 0x000	000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW F	Field	Value Id	Value				Description
			Enabled	1				Write access watch in this region is enabled
F	RW F	RGN2RA						Enable read access watch in region[2]
			Set	1				Enable read access watch in this region
			Disabled	0				Read access watch in this region is disabled
			Enabled	1				Read access watch in this region is enabled
G	RW F	RGN3WA						Enable write access watch in region[3]
			Set	1				Enable write access watch in this region
			Disabled	0				Write access watch in this region is disabled
			Enabled	1				Write access watch in this region is enabled
Н	RW F	RGN3RA						Enable read access watch in region[3]
			Set	1				Enable read access watch in this region
			Disabled	0				Read access watch in this region is disabled
			Enabled	1				Read access watch in this region is enabled
1	RW F	PRGN0WA						Enable write access watch in PREGION[0]
			Set	1				Enable write access watch in this PREGION
			Disabled	0				Write access watch in this PREGION is disabled
			Enabled	1				Write access watch in this PREGION is enabled
J	RW F	PRGN0RA						Enable read access watch in PREGION[0]
			Set	1				Enable read access watch in this PREGION
			Disabled	0				Read access watch in this PREGION is disabled
			Enabled	1				Read access watch in this PREGION is enabled
K	RW F	PRGN1WA						Enable write access watch in PREGION[1]
			Set	1				Enable write access watch in this PREGION
			Disabled	0				Write access watch in this PREGION is disabled
			Enabled	1				Write access watch in this PREGION is enabled
L	RW F	PRGN1RA						Enable read access watch in PREGION[1]
			Set	1				Enable read access watch in this PREGION
			Disabled	0				Read access watch in this PREGION is disabled
			Enabled	1				Read access watch in this PREGION is enabled

44.1.13 REGIONENCLR

Address offset: 0x518 Disable regions watch

Bit	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				L K J I	H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	RGN0WA			Disable write access watch in region[0]
			Clear	1	Disable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
В	RW	RGNORA			Disable read access watch in region[0]
			Clear	1	Disable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
С	RW	RGN1WA			Disable write access watch in region[1]
			Clear	1	Disable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
D	RW	RGN1RA			Disable read access watch in region[1]
			Clear	1	Disable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled



Bit	numbe	er		31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					L K J I	H G F E D C B A
Res	et 0x0	0000000		0 0 0 0	0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value		Description
Ε	RW	RGN2WA				Disable write access watch in region[2]
			Clear	1		Disable write access watch in this region
			Disabled	0		Write access watch in this region is disabled
			Enabled	1		Write access watch in this region is enabled
F	RW	RGN2RA				Disable read access watch in region[2]
			Clear	1		Disable read access watch in this region
			Disabled	0		Read access watch in this region is disabled
			Enabled	1		Read access watch in this region is enabled
G	RW	RGN3WA				Disable write access watch in region[3]
			Clear	1		Disable write access watch in this region
			Disabled	0		Write access watch in this region is disabled
			Enabled	1		Write access watch in this region is enabled
Н	RW	RGN3RA				Disable read access watch in region[3]
			Clear	1		Disable read access watch in this region
			Disabled	0		Read access watch in this region is disabled
			Enabled	1		Read access watch in this region is enabled
1	RW	PRGN0WA				Disable write access watch in PREGION[0]
			Clear	1		Disable write access watch in this PREGION
			Disabled	0		Write access watch in this PREGION is disabled
			Enabled	1		Write access watch in this PREGION is enabled
J	RW	PRGNORA				Disable read access watch in PREGION[0]
			Clear	1		Disable read access watch in this PREGION
			Disabled	0		Read access watch in this PREGION is disabled
			Enabled	1		Read access watch in this PREGION is enabled
K	RW	PRGN1WA				Disable write access watch in PREGION[1]
			Clear	1		Disable write access watch in this PREGION
			Disabled	0		Write access watch in this PREGION is disabled
			Enabled	1		Write access watch in this PREGION is enabled
L	RW	PRGN1RA				Disable read access watch in PREGION[1]
			Clear	1		Disable read access watch in this PREGION
			Disabled	0		Read access watch in this PREGION is disabled
			Enabled	1		Read access watch in this PREGION is enabled

44.1.14 REGION[0].START

Address offset: 0x600 Start address for region 0

	Bit number			31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	16	15	14	13	12 :	11 1	0 9	8 (7	6	5	4	3	2	1 ()
	Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	. 4	A A	Α	Α	Α	Α	Α	A A	۸ 4	Α Δ	A	Α	Α	Α	Α	Α.	Α /	٨
1	Reset 0x000	00000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 ()
ı	ld RW F	ield	Value Id	Va	lue							Des	crip	tio	n																		
	A RW S	TART										Stai	rt ac	ddre	ess f	or r	egio	on															

44.1.15 REGION[0].END

Address offset: 0x604 End address of region 0

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW END		End address of region.

End address of region.



44.1.16 REGION[1].START

Address offset: 0x610 Start address for region 1

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW START	Start address for region

44.1.17 REGION[1].END

Address offset: 0x614 End address of region 1

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW END		End address of region.

44.1.18 REGION[2].START

Address offset: 0x620 Start address for region 2

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Re	set 0x	0000000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	/ Field	Value Id	Val	ue							De	scri	ptic	on																			
Α	RW	/ START										Sta	rt a	ddr	ess	for	re	gior	า															

44.1.19 REGION[2].END

Address offset: 0x624 End address of region 2

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW END		End address of region.

44.1.20 REGION[3].START

Address offset: 0x630 Start address for region 3

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW START		Start address for region

44.1.21 REGION[3].END

Address offset: 0x634 End address of region 3



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW FND		End address of region

44.1.22 PREGION[0].START

Address offset: 0x6C0

Reserved for future use

Bit r	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	А А
Res	et Ox(00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW Field Value Id			Va	lue							De	scri	pti	on																			
	_											_			,	٠.																		_

A R START Reserved for future use

44.1.23 PREGION[0].END

Address offset: 0x6C4

Reserved for future use

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A R END		Reserved for future use

44.1.24 PREGION[0].SUBS

Address offset: 0x6C8 Subregions of region 0

Bitı	numbe	er		31 30	29	28 2	7 26	25	24 2	23 :	22 2	21 2	20 1	9 18	3 17	16	15 1	.4 1	.3 12	2 11	10	9	8	7 (5 5	4	3	2	1 0
Id				f e	d	С	b a	Z	Υ	X	W١	VΙ	U T	S	R	Q	Р) I	N M	l L	K	J	1 1	4 (3 F	Ε	D	C	3 A
Res	et 0x0	0000000		0 0	0	0	0 0	0	0	0	0 (0 (0 0	0	0	0	0	0	0 0	0	0	0	0	0 (0	0	0	0 (0 0
Id	RW	Field	Value Id	Value	9					Des	crip	tio	n																
Α	RW	SR0							- 1	ncl	ude	or	excl	ude	sub	reg	on () in	regio	on									
			Exclude	0					E	Excl	lude	:																	
			Include	1					I	ncl	ude																		
В	RW	SR1							I	ncl	ude	or	excl	ude	sub	reg	ion 1	. in	regio	on									
			Exclude	0					E	Excl	lude	:																	
			Include	1					I	ncl	ude																		
С	RW	SR2							I	ncl	ude	or	excl	ude	sub	reg	ion 2	! in	regio	on									
			Exclude	0					E	Excl	lude	:																	
			Include	1					I	ncl	ude																		
D	RW	SR3							I	ncl	ude	or	excl	ude	sub	reg	on 3	in	regio	on									
			Exclude	0					E	Excl	lude	:																	
			Include	1					- 1	ncl	ude																		
E	RW	SR4							ı	ncl	ude	or	excl	ude	sub	reg	ion 4	l in	regio	on									
			Exclude	0					E	Excl	lude	:																	
			Include	1					I	ncl	ude																		
F	RW	SR5							I	ncl	ude	or	excl	ude	sub	reg	on 5	in	regio	on									
			Exclude	0					E	Excl	lude	:																	
			Include	1					I	ncl	ude																		
G	RW	SR6							I	ncl	ude	or	excl	ude	sub	reg	on 6	in	regio	on									
			Exclude	0					E	Excl	lude	:																	
			Include	1					1	ncl	ude																		



Bit r	numbe	er		31 30	29 28	27	26 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et OxO	0000000							0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
Н	RW	SR7							Include or exclude subregion 7 in region
			Exclude	0					Exclude
			Include	1					Include
I	RW	SR8							Include or exclude subregion 8 in region
			Exclude	0					Exclude
			Include	1					Include
J	RW	SR9							Include or exclude subregion 9 in region
			Exclude	0					Exclude
.,			Include	1					Include
K	RW	SR10	Fredrick	0					Include or exclude subregion 10 in region
			Exclude	0					Exclude
L	D\A/	SR11	Include	1					Include Include or exclude subregion 11 in region
_	KVV	2411	Exclude	0					Exclude Exclude
			Include	1					Include
М	RW	SR12	meidde	-					Include or exclude subregion 12 in region
		31112	Exclude	0					Exclude
			Include	1					Include
N	RW	SR13							Include or exclude subregion 13 in region
			Exclude	0					Exclude
			Include	1					Include
0	RW	SR14							Include or exclude subregion 14 in region
			Exclude	0					Exclude
			Include	1					Include
Р	RW	SR15							Include or exclude subregion 15 in region
			Exclude	0					Exclude
			Include	1					Include
Q	RW	SR16							Include or exclude subregion 16 in region
			Exclude	0					Exclude
			Include	1					Include
R	RW	SR17		_					Include or exclude subregion 17 in region
			Exclude	0					Exclude
_	D\A/	SR18	Include	1					Include
S	KVV	2819	Exclude	0					Include or exclude subregion 18 in region Exclude
			Include	1					Include
Т	RW	SR19	meidde	_					Include or exclude subregion 19 in region
•		5.125	Exclude	0					Exclude
			Include	1					Include
U	RW	SR20							Include or exclude subregion 20 in region
			Exclude	0					Exclude
			Include	1					Include
V	RW	SR21							Include or exclude subregion 21 in region
			Exclude	0					Exclude
			Include	1					Include
W	RW	SR22							Include or exclude subregion 22 in region
			Exclude	0					Exclude
			Include	1					Include
Х	RW	SR23							Include or exclude subregion 23 in region
			Exclude	0					Exclude
			Include	1					Include
Υ	RW	SR24		_					Include or exclude subregion 24 in region
			Exclude	0					Exclude
-	Divi	CDOF	Include	1					Include
Z	КW	SR25							Include or exclude subregion 25 in region



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
Exclude	0 Exclude
Include	1 Include
a RW SR26	Include or exclude subregion 26 in region
Exclude	0 Exclude
Include	1 Include
b RW SR27	Include or exclude subregion 27 in region
Exclude	0 Exclude
Include	1 Include
c RW SR28	Include or exclude subregion 28 in region
Exclude	0 Exclude
Include	1 Include
d RW SR29	Include or exclude subregion 29 in region
Exclude	0 Exclude
Include	1 Include
e RW SR30	Include or exclude subregion 30 in region
Exclude	0 Exclude
Include	1 Include
f RW SR31	Include or exclude subregion 31 in region
Exclude	0 Exclude
Include	1 Include

44.1.25 PREGION[1].START

Address offset: 0x6D0

Reserved for future use

Bitı	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	R	START										Res	erv	/ed	for	fut	ure	use	•															

44.1.26 PREGION[1].END

Address offset: 0x6D4

Reserved for future use

Bit	num	be	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2 :	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	А А
Re	set 0	x00	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RV	N	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	R		END										Res	serv	/ed	for	fut	ure	use	e															

44.1.27 PREGION[1].SUBS

Address offset: 0x6D8 Subregions of region 1

Bit r	numb	er		31	. 30	29	28	3 27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				f	е	d	С	b	а	Z	Υ	Х	W	٧	U	Т	S	R	Q	Р	О	N	M	L	K	J	1	н	G	F	Е	D C	В	Α
Res	et 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	SR0										Ind	lud	e oı	r ex	cluc	de s	ubr	egi	on	0 in	ı re	gioi	า										
			Exclude	0								Ex	clud	le																				



Bit n	umbe	er		31 30	29 28	27	26 25	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b	a Z	Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	t 0x0	0000000		0 0	0 0	0	0 0	0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value					Description
			Include	1					Include
В	RW	SR1							Include or exclude subregion 1 in region
			Exclude	0					Exclude
			Include	1					Include
С	RW	SR2							Include or exclude subregion 2 in region
			Exclude	0					Exclude
			Include	1					Include
D	RW	SR3							Include or exclude subregion 3 in region
			Exclude	0					Exclude
			Include	1					Include
E	RW	SR4							Include or exclude subregion 4 in region
			Exclude	0					Exclude
			Include	1					Include
F	RW	SR5							Include or exclude subregion 5 in region
			Exclude	0					Exclude
			Include	1					Include
G	RW	SR6							Include or exclude subregion 6 in region
			Exclude	0					Exclude
	D) 4 /	507	Include	1					Include
Н	RW	SR/	5 1 1						Include or exclude subregion 7 in region
			Exclude	0					Exclude
	D\A/	CDO	Include	1					Include
1	KVV	SR8	Exclude	0					Include or exclude subregion 8 in region Exclude
			Include	1					Include
J	D\A/	SR9	include	1					Include or exclude subregion 9 in region
,	11.00	31(9	Exclude	0					Exclude
			Include	1					Include
K	RW	SR10	meidde	-					Include or exclude subregion 10 in region
		SKID	Exclude	0					Exclude
			Include	1					Include
L	RW	SR11							Include or exclude subregion 11 in region
			Exclude	0					Exclude
			Include	1					Include
М	RW	SR12							Include or exclude subregion 12 in region
			Exclude	0					Exclude
			Include	1					Include
N	RW	SR13							Include or exclude subregion 13 in region
			Exclude	0					Exclude
			Include	1					Include
0	RW	SR14							Include or exclude subregion 14 in region
			Exclude	0					Exclude
			Include	1					Include
Р	RW	SR15							Include or exclude subregion 15 in region
			Exclude	0					Exclude
			Include	1					Include
Q	RW	SR16							Include or exclude subregion 16 in region
			Exclude	0					Exclude
			Include	1					Include
R	RW	SR17							Include or exclude subregion 17 in region
			Exclude	0					Exclude
			Include	1					Include
S	RW	SR18							Include or exclude subregion 18 in region
			Exclude	0					Exclude
			Include	1					Include



Bit	numb	er		31 30	29	28	27 20	6 2	5 24	2	3 22 21 2	20 19	18	17	16	15	14	13	3 12	2 1	1 10	9	8	7	6 !	5 4	4 3	3 2	2 1	. 0
Id				f e	d	С	b a	1 2	Z Y	>	(W V I	U T	S	R	Q	Р	0	N	М	1 L	. K	J	ī	Н	G I	FI	E [) (В	8 A
Res	et 0x0	0000000		0 0	0	0	0 0) (0 0	c	000	0 0	0	0	0	0	0	0	0	C	0 (0	0	0	0 (0 (0 () (0	0
Id		Field	Value Id	Value						D	escriptio	n																		
Т	RW	SR19								lr	clude or	exclu	de	sub	re	gion	19	in	reg	ior	1									
			Exclude	0						E	kclude																			
			Include	1						lr	clude																			
U	RW	SR20								lr	clude or	exclu	de	sub	reg	gion	20) in	reg	ior	n									
			Exclude	0						E:	kclude																			
			Include	1						lr	ıclude																			
V	RW	SR21								lr	clude or	exclu	de	sub	re	gion	21	. in	reg	ior	n									
			Exclude	0						E	kclude																			
			Include	1						Ir	ıclude																			
W	RW	SR22								Ir	clude or	exclu	de	sub	re	gion	22	! in	reg	ior	ı									
			Exclude	0						E	kclude																			
			Include	1						lr	ıclude																			
Χ	RW	SR23								lr	clude or	exclu	de	sub	re	gion	23	in	reg	ior	1									
			Exclude	0						E	kclude																			
			Include	1						lr	ıclude																			
Υ	RW	SR24								lr	clude or	exclu	de	sub	re	gion	24	in	reg	ior	n									
			Exclude	0						E:	kclude																			
			Include	1						lr	ıclude																			
Z	RW	SR25								lr	iclude or	exclu	de	sub	re	gion	25	in	reg	ior	1									
			Exclude	0						E	kclude																			
			Include	1							ıclude																			
а	RW	SR26									iclude or	exclu	de	sub	re	gion	26	in	reg	ior	1									
			Exclude	0							kclude																			
			Include	1							ıclude																			
b	RW	SR27									iclude or	exclu	de	sub	re	gion	27	' in	reg	ior	1									
			Exclude	0							kclude																			
			Include	1							iclude																			
С	RW	SR28									iclude or	exclu	ide	sub	re	gion	28	in	reg	ior	1									
			Exclude	0							kclude																			
	D\4/	CD20	Include	1							iclude						20													
d	RW	SR29	Fuelude	0							iclude or	exciu	ae	sub	re	gion	29	ın	reg	gior	1									
			Exclude Include	1							kclude iclude																			
e	D\A/	SR30	include	1							iclude iclude or	ovelu	de	cub	ror	ion	30	l in	roc	ior	,									
٦	IL AA	31130	Exclude	0							kclude or	CXCIU	ue	งนม	ıe	51011	50	, 111	ıeg	iUI	'									
			Include	1							iclude																			
f	B/V	SR31	include	1							iclude iclude or	evelu	ahı	cub	rer	ion	21	in	rec	ior	1									
	ΝVV	JUST	Exclude	0							kclude or	exciu	ue	่อนม	ı e	51011	31	. 111	reg	,101										
			Include	1							iclude																			
			meiuue	1						II	iciuue																			



45 EGU — Event generator unit

The Event generator unit (EGU) provides support for inter-layer signaling. This means support for atomic triggering of both CPU execution and hardware tasks from both firmware (by CPU) and hardware (by PPI). This feature can, for instance, be used for triggering CPU execution at a lower priority execution from a higher priority execution, or to handle a peripheral's ISR execution at a lower priority for some of its events. However, triggering any priority from any priority is possible.

Listed here are the main EGU features:

- · Enables SW triggering of interrupts
- Separate interrupt vectors for every EGU instance
- Up to 16 separate event flags per interrupt for multiplexing

Each instance of The EGU implements a set of tasks which can individually be triggered to generate the corresponding event, i.e., the corresponding event for TASKS_TRIGGER[n] is EVENTS_TRIGGERED[n].

Refer to Table 105: Instances on page 551 for a list of the various EGU instances

45.1 Registers

Table 105: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40014000	EGU	EGU0	Event generator unit 0	
0x40015000	EGU	EGU1	Event generator unit 1	
0x40016000	EGU	EGU2	Event generator unit 2	
0x40017000	EGU	EGU3	Event generator unit 3	
0x40018000	EGU	EGU4	Event generator unit 4	
0x40019000	EGU	EGU5	Event generator unit 5	

Table 106: Register Overview

Register	Offset	Description
TASKS_TRIGGER[0]	0x000	Trigger 0 for triggering the corresponding TRIGGERED[0] event
TASKS_TRIGGER[1]	0x004	Trigger 1 for triggering the corresponding TRIGGERED[1] event
TASKS_TRIGGER[2]	0x008	Trigger 2 for triggering the corresponding TRIGGERED[2] event
TASKS_TRIGGER[3]	0x00C	Trigger 3 for triggering the corresponding TRIGGERED[3] event
TASKS_TRIGGER[4]	0x010	Trigger 4 for triggering the corresponding TRIGGERED[4] event
TASKS_TRIGGER[5]	0x014	Trigger 5 for triggering the corresponding TRIGGERED[5] event
TASKS_TRIGGER[6]	0x018	Trigger 6 for triggering the corresponding TRIGGERED[6] event
TASKS_TRIGGER[7]	0x01C	Trigger 7 for triggering the corresponding TRIGGERED[7] event
TASKS_TRIGGER[8]	0x020	Trigger 8 for triggering the corresponding TRIGGERED[8] event
TASKS_TRIGGER[9]	0x024	Trigger 9 for triggering the corresponding TRIGGERED[9] event
TASKS_TRIGGER[10]	0x028	Trigger 10 for triggering the corresponding TRIGGERED[10] event
TASKS_TRIGGER[11]	0x02C	Trigger 11 for triggering the corresponding TRIGGERED[11] event
TASKS_TRIGGER[12]	0x030	Trigger 12 for triggering the corresponding TRIGGERED[12] event
TASKS_TRIGGER[13]	0x034	Trigger 13 for triggering the corresponding TRIGGERED[13] event
TASKS_TRIGGER[14]	0x038	Trigger 14 for triggering the corresponding TRIGGERED[14] event
TASKS_TRIGGER[15]	0x03C	Trigger 15 for triggering the corresponding TRIGGERED[15] event
EVENTS_TRIGGERED[0]	0x100	Event number 0 generated by triggering the corresponding TRIGGER[0] task
EVENTS_TRIGGERED[1]	0x104	Event number 1 generated by triggering the corresponding TRIGGER[1] task
EVENTS_TRIGGERED[2]	0x108	Event number 2 generated by triggering the corresponding TRIGGER[2] task
EVENTS_TRIGGERED[3]	0x10C	Event number 3 generated by triggering the corresponding TRIGGER[3] task
EVENTS_TRIGGERED[4]	0x110	Event number 4 generated by triggering the corresponding TRIGGER[4] task
EVENTS_TRIGGERED[5]	0x114	Event number 5 generated by triggering the corresponding TRIGGER[5] task
EVENTS_TRIGGERED[6]	0x118	Event number 6 generated by triggering the corresponding TRIGGER[6] task



Register	Offset	Description
EVENTS_TRIGGERED[7]	0x11C	Event number 7 generated by triggering the corresponding TRIGGER[7] task
EVENTS_TRIGGERED[8]	0x120	Event number 8 generated by triggering the corresponding TRIGGER[8] task
EVENTS_TRIGGERED[9]	0x124	Event number 9 generated by triggering the corresponding TRIGGER[9] task
EVENTS_TRIGGERED[10)] 0x128	Event number 10 generated by triggering the corresponding TRIGGER[10] task
EVENTS_TRIGGERED[11	l] 0x12C	Event number 11 generated by triggering the corresponding TRIGGER[11] task
EVENTS_TRIGGERED[12	2] 0x130	Event number 12 generated by triggering the corresponding TRIGGER[12] task
EVENTS_TRIGGERED[13	B] 0x134	Event number 13 generated by triggering the corresponding TRIGGER[13] task
EVENTS_TRIGGERED[14	l] 0x138	Event number 14 generated by triggering the corresponding TRIGGER[14] task
EVENTS_TRIGGERED[15	5] 0x13C	Event number 15 generated by triggering the corresponding TRIGGER[15] task
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt

45.1.1 INTEN

Address offset: 0x300

Enable or disable interrupt

Enable of disable interrupt	•		
Bit number		31 30 29 28 27 26 25 24	$23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0$
Id			PONMLKJIHGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
ld RW Field Va	alue Id	Value	Description
A RW TRIGGEREDO			Enable or disable interrupt for TRIGGERED[0] event
			See EVENTS_TRIGGERED[0]
Dis	isabled	0	Disable
En	nabled	1	Enable
B RW TRIGGERED1			Enable or disable interrupt for TRIGGERED[1] event
			See EVENTS_TRIGGERED[1]
Di:	isabled	0	Disable
En	nabled	1	Enable
C RW TRIGGERED2			Enable or disable interrupt for TRIGGERED[2] event
			See EVENTS_TRIGGERED[2]
Di	isabled	0	Disable
		1	Enable
D RW TRIGGERED3			Enable or disable interrupt for TRIGGERED[3] event
			Son EVENTS TRICCEREDISI
Di	isabled	0	See EVENTS_TRIGGERED[3] Disable
		1	Enable
E RW TRIGGERED4	labica	-	Enable or disable interrupt for TRIGGERED[4] event
2.		0	See EVENTS_TRIGGERED[4]
		0	Disable Enable
F RW TRIGGERED5	lableu	1	Enable or disable interrupt for TRIGGERED[5] event
1 KW TRIGGEREDS			
			See EVENTS_TRIGGERED[5]
		0	Disable
	nabled	1	Enable
G RW TRIGGERED6			Enable or disable interrupt for TRIGGERED[6] event
			See EVENTS_TRIGGERED[6]
		0	Disable
	nabled	1	Enable
H RW TRIGGERED7			Enable or disable interrupt for TRIGGERED[7] event
			See EVENTS_TRIGGERED[7]
Di	isabled	0	Disable
En	nabled	1	Enable
I RW TRIGGERED8			Enable or disable interrupt for TRIGGERED[8] event



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id	P O N M L K J I H G F E D C B .
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
	See EVENTS_TRIGGERED[8]
Disabled	0 Disable
Enabled	1 Enable
J RW TRIGGERED9	Enable or disable interrupt for TRIGGERED[9] event
	See EVENTS_TRIGGERED[9]
Disabled	0 Disable
Enabled	1 Enable
K RW TRIGGERED10	Enable or disable interrupt for TRIGGERED[10] event
	See EVENTS_TRIGGERED[10]
Disabled	0 Disable
Enabled	1 Enable
L RW TRIGGERED11	Enable or disable interrupt for TRIGGERED[11] event
	See EVENTS_TRIGGERED[11]
Disabled	0 Disable
Enabled	1 Enable
M RW TRIGGERED12	Enable or disable interrupt for TRIGGERED[12] event
	See EVENTS_TRIGGERED[12]
Disabled	0 Disable
Enabled	1 Enable
N RW TRIGGERED13	Enable or disable interrupt for TRIGGERED[13] event
	See EVENTS_TRIGGERED[13]
Disabled	0 Disable
Enabled	1 Enable
O RW TRIGGERED14	Enable or disable interrupt for TRIGGERED[14] event
	See EVENTS_TRIGGERED[14]
Disabled	0 Disable
Enabled	1 Enable
P RW TRIGGERED15	Enable or disable interrupt for TRIGGERED[15] event
8: 11.1	See EVENTS_TRIGGERED[15]
Disabled	0 Disable
Enabled	1 Enable

45.1.2 INTENSET

Address offset: 0x304 Enable interrupt

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	1	8 1	7 1	6 :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																					Р	О	N	M	L	K	J	1	Н	G	F	Ε	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ipti	on																					
Α	RW	TRIGGERED0										Wr	rite	'1'	to I	Ena	ble	e in	ter	rup	ot f	or 1	RIC	GGE	RE	D[0] ev	/en	t							
												See	e <i>E</i> \	VEN	ITS_	_TF	RIG	GEI	REL	0]0	1															
			Set	1								Ena	able	e																						
			Disabled	0								Rea	ad:	Dis	abl	ed																				
			Enabled	1								Rea	ad:	Ena	able	ed																				
В	RW	TRIGGERED1										Wr	rite	'1'	to I	Ena	ble	e in	ter	rup	ot f	or 1	RIC	GGE	RE	D[1] ev	/en	t							
												See	e <i>E</i> \	VEN	ITS_	_TF	RIG	GEI	REL	0[1]															
			Set	1								Ena	able	е																						
			Disabled	0								Rea	ad:	Dis	abl	ed																				
			Enabled	1								Rea	ad:	Ena	able	ed																				
С	RW	TRIGGERED2										Wr	rite	'1'	to I	Ena	ble	e in	ter	rup	ot f	or 1	RIC	GGE	RE	D[2] ev	/en	t							



Bitı	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				PONMLKJIHGFEDCBA
Res	set 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
				See EVENTS_TRIGGERED[2]
		Set	1	Enable
		Disabled Enabled	0 1	Read: Disabled Read: Enabled
D	RW TRIGGERED3	Eliableu	1	Write '1' to Enable interrupt for TRIGGERED[3] event
	NW THIOGENEDS			
		C-+	4	See EVENTS_TRIGGERED[3]
		Set Disabled	1	Enable Read: Disabled
		Enabled	1	Read: Enabled
E	RW TRIGGERED4	Enablea	-	Write '1' to Enable interrupt for TRIGGERED[4] event
		Set	1	See EVENTS_TRIGGERED[4] Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW TRIGGERED5	Endoica	-	Write '1' to Enable interrupt for TRIGGERED[5] event
		Set	1	See EVENTS_TRIGGERED[5] Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW TRIGGERED6	Endoica	-	Write '1' to Enable interrupt for TRIGGERED[6] event
		Set	1	See EVENTS_TRIGGERED[6] Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW TRIGGERED7			Write '1' to Enable interrupt for TRIGGERED[7] event
				See EVENTS_TRIGGERED[7]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
I	RW TRIGGERED8			Write '1' to Enable interrupt for TRIGGERED[8] event
				See EVENTS_TRIGGERED[8]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
J	RW TRIGGERED9			Write '1' to Enable interrupt for TRIGGERED[9] event
				See EVENTS_TRIGGERED[9]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
K	RW TRIGGERED10			Write '1' to Enable interrupt for TRIGGERED[10] event
				See EVENTS_TRIGGERED[10]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
L	RW TRIGGERED11			Write '1' to Enable interrupt for TRIGGERED[11] event
				See EVENTS_TRIGGERED[11]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
М	RW TRIGGERED12			Write '1' to Enable interrupt for TRIGGERED[12] event

See EVENTS_TRIGGERED[12]



Bit number			31 30 2	29 28 2	27 26	25 24	4 23	3 22 2	21 20	0 19	18	17 1	16 1	.5 14	13	12 1	1 10	9	8	7	6 5	5 4	3	2	1 0
Id													F	РО	N	М	L K	J	1	Н	G I	: E	D	C I	ВА
Reset 0x0000	00000		0 0	0 0	0 0	0 0	0	0 (0 0	0	0	0 (0 (0 0	0	0	0 0	0	0	0	0 () (0	0 (0 0
Id RW Fie	eld	Value Id	Value				D	escrip	tion	ı															
		Set	1				Er	nable																	
		Disabled	0				Re	ead: D	isab	led															
		Enabled	1				Re	ead: E	nabl	led															
N RW TR	RIGGERED13						W	/rite '1	l' to	Enal	ble i	nter	rup	t for	TRI	GGEI	RED[13] (ever	t					
							Se	ee <i>EVE</i>	NTS	TR.	IGGI	EREL	D[13	31											
		Set	1					nable		_															
		Disabled	0				Re	ead: D	isab	led															
		Enabled	1				Re	ead: E	nabl	led															
O RW TR	RIGGERED14						W	/rite '1	l' to	Enal	ble i	nter	rup	t for	TRI	GGEI	RED[:	14] (ever	t					
							Se	ee <i>EVE</i>	NTS	TR	IGGI	FRFI	D[14	11											
		Set	1					nable					-1-	• •											
		Disabled	0					ead: D	isab	led															
		Enabled	1				Re	ead: E	nabl	led															
P RW TR	RIGGERED15						W	/rite '1	l' to	Enal	ble i	nter	rup	t for	TRI	GGEI	RED[:	15] (ever	it					
							۲.	51/1	- N.T.C		100	-0-1	D[4]	-1											
								ee <i>EVE</i>	:N13	_ / K	IGGI	EKEL	בנוןע	>]											
		Set	1					nable																	
		Disabled	0					ead: D																	
		Enabled	1				Re	ead: E	nabl	led															

45.1.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bitı	numbe	er		31 3	0 29	9 28	8 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	3 12	2 1:	1 10	9	8	7	6	5	4 3	3 2	1	0
Id																			Р	0	Ν	ΙN	1 L	. K	J	ī	н	G	F	E [) C	В	Α
Res	et 0x0	0000000		0	0 0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0
Id	RW	Field	Value Id	Valu	e						Des	scri	ptic	on																			
Α	RW	TRIGGERED0									Wri	rite '	'1' t	to [Disa	ble	int	err	upt	t fo	r Tl	RIG	GEF	RED[0] €	ever	ıt						
											See	e <i>EV</i>	/FN	TS	TRI	GG	FRE	וחי	กา														
			Clear	1								able		_					-,														
			Disabled	0							Rea	ad: I	Disa	abl	ed																		
			Enabled	1							Rea	ad: ۱	Ena	ble	ed																		
В	RW	TRIGGERED1									Wri	rite '	'1' t	to [Disa	ble	int	err	upt	t fo	r Tl	RIG	GEF	RED[1] €	ever	nt						
											Soo	e <i>EV</i>	/ENI	TC	TDI	cc	EDI	יח: זח:	11														
			Clear	1								able		13_	-111	GG	ENL	υį	ıj														
			Disabled	0								ad: I		abl	ed																		
			Enabled	1								ad: I																					
С	RW	TRIGGERED2									Wri	rite '	'1' t	to [Disa	ble	int	err	upt	t fo	r Tl	RIG	GEF	RED[2] €	ever	nt						
											۲.,	e <i>EV</i>	/ENI	TC	TDI		CDI	יחי	21														
			Clear	1								e <i>E v</i> sable		13_	_IKI	GG	EKL	υĮ.	2]														
			Disabled	0								ad: I		ahl	ha																		
			Enabled	1								ad: I																					
D	RW	TRIGGERED3	Z. i do i d	-								rite '				ble	int	err	upt	t fo	r Tl	RIG	GEF	REDÍ	31 e	ever	nt						
																								ľ									
			Class									e <i>EV</i>		15_	_IRI	GG	ERE	:DĮ.	3]														
			Clear Disabled	1								able ad: I		اماء	~ d																		
			Enabled	0								ad: ad:																					
E	D\A/	TRIGGERED4	Eliablea	1								au. i rite '				hla	int	orr	unt	f fo	r Ti	DIC.	CEL	EDI	/11 c	wor	+						
-	11.44	THIOGENEDA																		. 10		NIO'	JLF	יבטן	→ 1 €	.vei	16						
												e <i>EV</i>		TS_	TRI	GG	ERE	D[·	4]														
			Clear	1								able																					
			Disabled	0							Rea	ad:	Disa	abl	ed																		



Bit r	numbe	r		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					PONMLKJIHGFEDCBA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Enabled	1	Read: Enabled
F	RW	TRIGGERED5			Write '1' to Disable interrupt for TRIGGERED[5] event
					See EVENTS_TRIGGERED[5]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	TRIGGERED6			Write '1' to Disable interrupt for TRIGGERED[6] event
					See EVENTS_TRIGGERED[6]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	TRIGGERED7			Write '1' to Disable interrupt for TRIGGERED[7] event
					See EVENTS_TRIGGERED[7]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
I	RW	TRIGGERED8			Write '1' to Disable interrupt for TRIGGERED[8] event
					See EVENTS_TRIGGERED[8]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
J	RW	TRIGGERED9			Write '1' to Disable interrupt for TRIGGERED[9] event
					See EVENTS_TRIGGERED[9]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
K	RW	TRIGGERED10			Write '1' to Disable interrupt for TRIGGERED[10] event
					See EVENTS_TRIGGERED[10]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
L	RW	TRIGGERED11			Write '1' to Disable interrupt for TRIGGERED[11] event
					See EVENTS_TRIGGERED[11]
			Clear	1	Disable
			Disabled	0	Read: Disabled
	D14/	TRICCEPEDAG	Enabled	1	Read: Enabled
М	кW	TRIGGERED12			Write '1' to Disable interrupt for TRIGGERED[12] event
					See EVENTS_TRIGGERED[12]
			Clear	1	Disable
			Disabled	0	Read: Disabled
NI	DIA	TRICCERED13	Enabled	1	Read: Enabled Write '4' to Disable interrupt for TRICGERED[12] event
N	KW	TRIGGERED13			Write '1' to Disable interrupt for TRIGGERED[13] event
					See EVENTS_TRIGGERED[13]
			Clear	1	Disable
			Disabled	0	Read: Disabled
0	D\A/	TRIGGERED14	Enabled	1	Read: Enabled Write '1' to Disable interrupt for TRIGGERED[14] event
0	KVV	TRIGGERED14			Write '1' to Disable interrupt for TRIGGERED[14] event
					See EVENTS_TRIGGERED[14]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled



Bitı	numbe	r		31	1 30	29	2	8 2	7 2	26	25	24	23	22	2 21	L 20	0 1	9 1	8	17	16	15	14	13	3 1	2 1	11:	10	9	8	7	6	5	4	3	2	1	0
Id																						Р	0	Ν	ΙN	Λ	L	K	J	1	Н	G	F	Ε	D	С	В	Α
Res	et 0x0	0000000		0	0	0	C	0)	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	()	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•							De	SCI	ript	ion	1																					
Р	RW	TRIGGERED15											W	rite	'1'	to	Dis	sab	le	int	err	upt	fo	r TI	RIG	GE	RE	D[1	5]	eve	nt							
													Se	e <i>E</i>	VEI	NTS	5_ <i>T</i>	RIC	iGI	ERE	D[15]																
			Clear	1									Di	sab	le																							
			Disabled	0									Re	ad	: Di	sab	lec	t																				
			Enabled	1									Re	ad	: En	ab	led																					

45.2 Electrical specification

45.2.1 EGU Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{EGU,EVT}	Latency between setting an EGU event flag and the system		1		cycles
	setting an interrupt				



46 PWM — Pulse width modulation

The PWM module enables the generation of pulse width modulated signals on GPIO. The module implements an up or up-and-down counter with four PWM channels that drive assigned GPIOs.

Three PWM modules can provide up to 12 PWM channels with individual frequency control in groups of up to four channels. Furthermore, a built-in decoder and EasyDMA capabilities make it possible to manipulate the PWM duty cycles without CPU intervention. Arbitrary duty-cycle sequences are read from Data RAM and can be chained to implement ping-pong buffering or repeated into complex loops.

Listed here are the main features of one PWM module:

- Fixed PWM base frequency with programmable clock divider
- Up to four PWM channels with individual polarity and duty-cycle values
- Edge or center-aligned pulses across PWM channels
- · Multiple duty-cycle arrays (sequences) defined in Data RAM
- · Autonomous and glitch-free update of duty cycle values directly from memory through EasyDMA
- · Change of polarity, duty-cycle, and base frequency possibly on every PWM period
- Data RAM sequences can be repeated or connected into loops

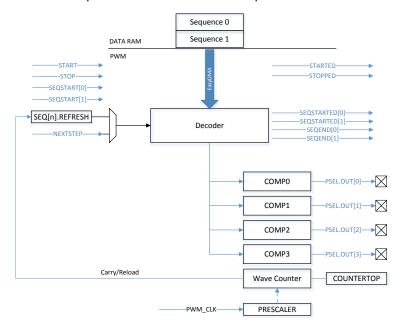


Figure 152: PWM Module

46.1 Wave counter

The wave counter is responsible for generating the pulses at a duty-cycle that depends on the compare values, and at a frequency that depends on COUNTERTOP.

There is one common 15-bit counter with four compare channels. Thus, all four channels will share the same period (PWM frequency), but can have individual duty-cycle and polarity. The polarity is set by the value read from RAM (see *Figure 155: Decoder memory access modes* on page 561), while the MODE register controls if the counter counts up, or up and down. The timer top value is controlled by the COUNTERTOP register. This register value in conjunction with the selected PRESCALER of the PWM_CLK will result in a given PWM period. A COUNTERTOP value smaller than the compare setting will result in a state where no PWM edges are generated. Respectively, OUT[n] is held high, given that the polarity is set to FallingEdge. All the compare registers are internal and can only be configured through the decoder presented later.

COUNTERTOP can be safely written at any time. It will get sampled following a START task. If DECODER.LOAD is anything else than WaveForm, it will also get sampled following a STARTSEQ[n] task,



and when loading a new value from RAM during a sequence playback. If DECODER.LOAD=WaveForm, the register value is ignored, and taken from RAM instead (see *Decoder with EasyDMA* on page 561 below).

Figure 153: PWM up counter example - FallingEdge polarity on page 559 shows the counter operating in up (MODE=PWM_MODE_Up) mode with three PWM channels with the same frequency but different duty cycle. The counter is automatically reset to zero when COUNTERTOP is reached and OUT[n] will invert. OUT[n] is held low if the compare value is 0 and held high respectively if set to COUNTERTOP given that the polarity is set to FallingEdge. Running in up counter mode will result in pulse widths that are edge-aligned. See the code example below:

```
uint16 t pwm seq[4] = {PWM CH0 DUTY, PWM CH1 DUTY, PWM CH2 DUTY,
PWM CH3 DUTY);
NRF PWM0->PSEL.OUT[0] = (first pin << PWM PSEL OUT PIN Pos)
                        (PWM PSEL OUT CONNECT Connected <<
                                                  PWM PSEL OUT CONNECT Pos);
NRF PWM0->PSEL.OUT[1] = (second pin << PWM PSEL OUT PIN Pos) |
                        (PWM PSEL OUT CONNECT Connected <<
                                                 PWM_PSEL_OUT_CONNECT_Pos);
                      = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
NRF PWM0->ENABLE
NRF PWM0->MODE
                      = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
NRF PWM0->PRESCALER = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                  PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM COUNTERTOP COUNTERTOP Pos); //1 msec
NRF PWM0->LOOP
                    = (PWM LOOP CNT Disabled << PWM LOOP CNT Pos);
NRF PWM0->DECODER
                   = (PWM DECODER LOAD Individual << PWM DECODER LOAD Pos)
                      (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF PWM0->SEQ[0].PTR = ((uint32_t)(pwm_seq) << PWM_SEQ_PTR_PTR_Pos);
NRF PWM0->SEQ[0].CNT = ((sizeof(pwm seq) / sizeof(uint16_t)) < < 
                                                 PWM SEQ CNT CNT Pos);
NRF_PWM0 \rightarrow SEQ[0].REFRESH = 0;
NRF PWM0 -> SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

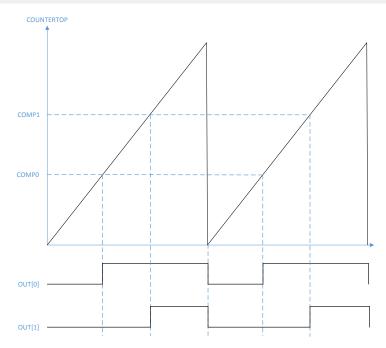


Figure 153: PWM up counter example - FallingEdge polarity

In up counting mode, the following formula can be used to compute PWM period and step size:

```
PWM period: T<sub>PWM</sub> (U<sub>p</sub>) = T<sub>PWM</sub> C<sub>LK</sub> * COUNTERTOP
```

Step width/Resolution: $T_{\text{steps}} = T_{\text{PWM_CLK}}$



Figure 154: PWM up-and-down counter example on page 560 shows the counter operating in up and down mode with (MODE=PWM_MODE_UpAndDown) two PWM channels with the same frequency but different duty cycle and output polarity. The counter starts decrementing to zero when COUNTERTOP is reached and will invert the OUT[n] when compare value is hit for the second time. This results in a set of pulses that are center- aligned.

```
uint16 t pwm seq[4] = {PWM CHO DUTY, PWM CH1 DUTY, PWM CH2 DUTY,
 PWM CH3 DUTY);
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |</pre>
                                                                      (PWM PSEL OUT CONNECT Connected <<
                                                                                                                                              PWM PSEL OUT CONNECT Pos);
NRF PWM0->PSEL.OUT[1] = (second pin << PWM PSEL OUT PIN Pos) |
                                                                      (PWM PSEL OUT CONNECT Connected <<
                                                                                                                                             PWM PSEL OUT CONNECT Pos);
NRF PWM0->ENABLE
                                                               = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
                                                               = (PWM MODE UPDOWN UpAndDown << PWM MODE UPDOWN Pos);
NRF PWM0->MODE
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                                                                                                                             PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
                                                               = (PWM LOOP CNT Disabled << PWM LOOP CNT Pos);
NRF
          PWM0->LOOP
NRF PWM0->DECODER
                                                          = (PWM DECODER LOAD Individual << PWM DECODER LOAD Pos)
                                                               (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF_PWM0->SEQ[0].PTR = ((uint32_t)(pwm_seq) << PWM_SEQ PTR PTR Pos);
NRF_PWM0 - SEQ[0].CNT = ((sizeof(pwm_seq) / sizeof(uint16_t)) < < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < colspan="2">(sizeof(uint16_t)) < col
                                                                                                                                             PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0 \rightarrow SEQ[0].REFRESH = 0;
NRF PWM0 -> SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

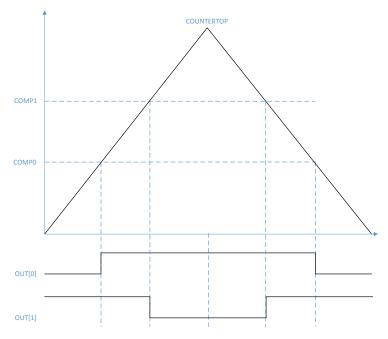


Figure 154: PWM up-and-down counter example

In up-and-down counting modes, the following formula can be used to compute PWM period and step size:

```
T_{PWM}(Up And Down) = T_{PWM} CLK * 2 * COUNTERTOP
```

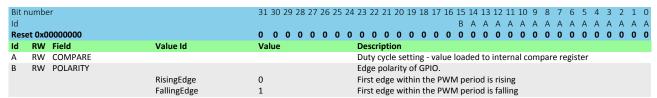
Step width/Resolution: $T_{\text{Steps}} = T_{\text{PWM CLK}} * 2$



46.2 Decoder with EasyDMA

The decoder uses EasyDMA to take PWM parameters stored in Data RAM by ways of EasyDMA and updates the internal compare registers of the wave counter based on the mode of operation.

The mentioned PWM parameters are organized into a sequence containing at least one half word (16 bit). Its most significant bit[15] denotes the polarity of the OUT[n] while bit[14:0] is the 15-bit compare value. See below for further details of these RAM defined registers.



The DECODER register controls how the RAM content is interpreted and loaded to the internal compare registers. The LOAD field can be used to control if the RAM values are loaded to all compare channels - or alternatively to update a group or all channels with individual values. *Figure 155: Decoder memory access modes* on page 561 illustrates how the parameters stored in RAM are organized and routed to the various compare channels in the different modes.

A special mode of operation is available when DECODER.LOAD is set to WaveForm. In this mode, up to three PWM channels can be enabled - OUT[0] to OUT[2]. In RAM, four values are loaded at a time: the first, second and third location are used to load the values, and the fourth RAM location is used to load the COUNTERTOP register. This way one can have up to three PWM channels with a frequency base that changes on a per PWM period basis. This mode of operation is useful for arbitrary wave form generation in applications such as LED lighting.

The register SEQ[n].REFRESH=N (one per sequence n=0 or 1) will instruct a new RAM stored pulse width value on every (N+1)th PWM period. Setting the register to zero will result in a new duty cycle update every PWM period as long as the minimum PWM period is observed.

Note that registers SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored when DECODER.MODE=NextStep . The next value is loaded upon receiving every NEXTSTEP task.

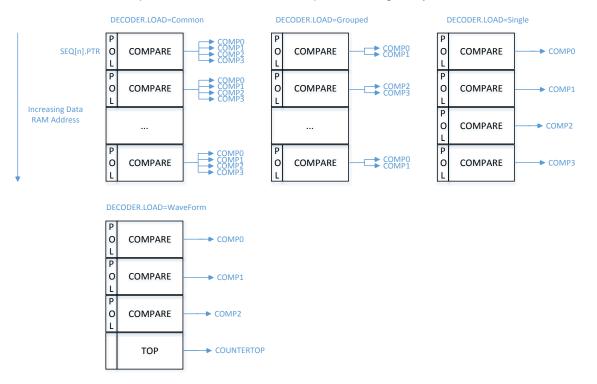


Figure 155: Decoder memory access modes



SEQ[n].PTR is the pointer used to fetch COMPARE values from RAM. If the SEQ[n].PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

After the SEQ[n].PTR is set to the desired RAM location, the SEQ[n].CNT register must be set to the number of 16-bit half words in the sequence. It is important to observe that the Grouped and Single modes require one half word per group or one half word per channel respectively, and thus increases RAM size occupation. If PWM generation was not running yet at that point, sending the SEQSTART[n] task will load the first value from RAM, then start the PWM generation. A SEQSTARTED[n] event is generated as soon as the EasyDMA has read the first PWM parameter from RAM and the wave counter has started executing it. When LOOP.CNT=0, sequence n=0 or 1 is played back once. After the last value in the sequence has been loaded and started executing, a SEQEND[n] event is generated. The PWM generation will then continue with the last loaded value. See *Figure 156: Simple sequence example* on page 563 for an example of such simple playback.

To completely stop the PWM generation and force the associated pins to a defined state, a STOP task can be fired at any time. A STOPPED event is generated when the PWM generation has stopped at the end of currently running PWM period, and the pins go into their idle state as defined in GPIO->OUT. PWM generation can then only be restarted through a SEQSTART[n] task. SEQSTART[n] will resume PWM generation after having loaded the first value from the RAM buffer defined in the SEQ[n].PTR register.

The table below provides indication of when specific registers get sampled by the hardware. Care should be taken when updating these registers to avoid values to be applied earlier than expected.

Table 107: When to safely update PWM registers

Register	Taken into account by hardware	Recommended (safe) update
SEQ[n].PTR	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[n].CNT	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[0].ENDDELAY	When sending the SEQSTART[0] task	Before starting sequence [0] through a SEQSTART[0] task
	Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the	When no more value from sequence [0] gets loaded from RAM (indicated by the SEQEND[0] event)
	PWMPERIODEND event)	At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired) $$
SEQ[1].ENDDELAY	When sending the SEQSTART[1] task	Before starting sequence [1] through a SEQSTART[1] task
	Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the	When no more value from sequence [1] gets loaded from RAM (indicated by the SEQEND[1] event)
	PWMPERIODEND event)	At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired)
SEQ[0].REFRESH	When sending the SEQSTART[0] task	Before starting sequence [0] through a SEQSTART[0] task
	Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired)
SEQ[1].REFRESH	When sending the SEQSTART[1] task	Before starting sequence [1] through a SEQSTART[1] task
	Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired)
COUNTERTOP	In DECODER.LOAD=WaveForm: this register is ignored.	Before starting PWM generation through a SEQSTART[n] task
	In all other LOAD modes: at the end of current PWM period (indicated by the PWMPERIODEND event)	After a STOP task has been issued, and the STOPPED event has been received.
MODE	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
DECODER	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
PRESCALER	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
LOOP	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
PSEL.OUT[n]	Immediately	Before enabling the PWM instance through the ENABLE register

Important: SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored at the end of a complex sequence, indicated by a LOOPSDONE event. The reason for this is that the last value loaded from RAM is maintained until further action from software (restarting a new sequence, or stopping PWM generation).



Figure 156: Simple sequence example on page 563 depicts the source code used for configuration and timing details in a sequence where only sequence 0 is used and only run once with a new PWM duty cycle for each period.

```
NRF PWM0->PSEL.OUT[0] = (first pin << PWM_PSEL_OUT_PIN_Pos)</pre>
                            (PWM PSEL OUT CONNECT Connected <<
                                                        PWM PSEL OUT CONNECT Pos);
NRF PWM0->ENABLE
                         = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
                         = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
NRF PWM0->MODE
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                                         PWM PRESCALER PRESCALER Pos);
NRF_PWM0->COUNTERTOP = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec NRF_PWM0->LOOP = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF PWM0->DECODER
                       = (PWM DECODER LOAD Common << PWM DECODER LOAD Pos)
                         (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF PWM0->SEQ[0].PTR = ((uint32 t) (seq0 ram) << PWM SEQ PTR PTR Pos);
NRF PWM0->SEQ[0].CNT = ((sizeof(seq0 ram) / sizeof(uint16 t))) < < (sizeof(seq0 ram) / sizeof(uint16 t))
                                                         PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[0].REFRESH = 0;
NRF PWM0->SEQ[0].ENDDELAY = 0;
NRF_PWM0 \rightarrow TASKS_SEQSTART[0] = 1;
```

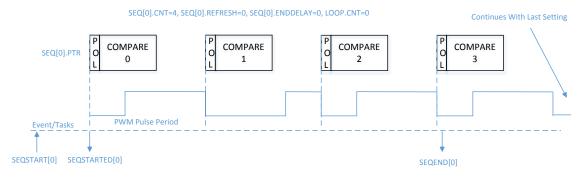


Figure 156: Simple sequence example

A more complex example is shown in *Figure 157: Example using two sequences* on page 564, where LOOP.CNT>0. In this case, an automated playback takes place, consisting of SEQ[0], delay 0, SEQ[1], delay 1, then again SEQ[0], etc. The user can choose to start a complex playback with SEQ[0] or SEQ[1] through sending the SEQSTART[0] or SEQSTART[1] task.

The complex playback always ends with delay 1.

The two sequences 0 and 1 are defined with address of values tables in Data RAM (pointed by SEQ[n].PTR) and respective buffer size (SEQ[n].CNT). The rate at which a new value is loaded is defined individually for each sequence by SEQ[n].REFRESH . The chaining of sequence 1 following sequence 0 is implicit, the LOOP.CNT register allows the chaining of sequence 1 to sequence 0 for a determined number of times. In other words, it allows to repeat a complex sequence a number of times in a fully automated way.

In the example below, sequence 0 is defined with SEQ[0].REFRESH set to one - that means that a new PWM duty cycle is pushed every second PWM period. This complex sequence is started with the SEQSTART[0] task, so SEQ[0] is played first. Since SEQ[0].ENDDELAY=1 there will be one PWM period delay between last period on sequence 0 and the first period on sequence 1. Since SEQ[1].ENDDELAY=0 there is no delay 1, so SEQ[0] would be started immediately after the end of SEQ[1]. However, as LOOP.CNT is one, the playback stops after having played only once SEQ[1], and both SEQEND[1] and LOOPSDONE are generated (their order is not guaranteed in this case).



```
NRF PWM0->PSEL.OUT[0] = (first pin << PWM PSEL OUT PIN Pos)
                       (PWM PSEL OUT CONNECT Connected <<
                                              PWM PSEL OUT CONNECT Pos);
NRF PWM0->ENABLE
                    = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_
   PWM0->MODE
                    = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                              PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM COUNTERTOP COUNTERTOP Pos); //1 msec
                   = (1 \ll PWM LOOP CNT Pos);
NRF PWM0->LOOP
NRF PWM0->DECODER
                  = (PWM DECODER LOAD Common << PWM DECODER LOAD Pos) |
                    (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF PWM0->SEQ[0].PTR = ((uint32 t)(seq0 ram) << PWM SEQ PTR PTR Pos);
PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[0].REFRESH = 1;
NRF PWM0->SEQ[0].ENDDELAY = 1;
NRF PWM0->SEQ[1].PTR = ((uint32 t)(seq1 ram) << PWM SEQ PTR PTR Pos);
NRF PWM0->SEQ[1].CNT = ((sizeof(seq1 ram) / sizeof(uint16 t)) <<
                                              PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[1].REFRESH = 0;
NRF PWM0->SEQ[1].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

SEQ[0].CNT=2, SEQ[1].CNT=3, SEQ[0].REFRESH=1, SEQ[1].REFRESH=0, SEQ[0].ENDDELAY=1, SEQ[1].ENDDELAY=0, LOOP.CNT=1

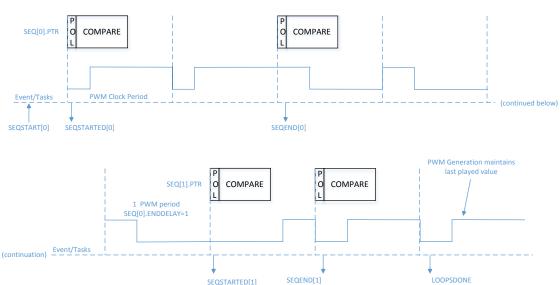


Figure 157: Example using two sequences

The decoder can also be configured to asynchronously load a new PWM duty cycle. If the DECODER.MODE register is set to NextStep - then the NEXTSTEP task will cause an update of the internal compare registers on the next PWM period.

The figures below provide an overview of each part of an arbitrary sequence, in various modes (LOOP.CNT=0 and LOOP.CNT>0). In particular are represented:

- Initial and final duty cycle on the PWM output(s)
- Chaining of SEQ[0] and SEQ[1] if LOOP.CNT>0
- · Influence of registers on the sequence
- · Events fired during a sequence
- DMA activity (loading of next value and applying it to the output(s))

Note that the single-shot example applies also to SEQ[1], only SEQ[0] is represented for simplicity.



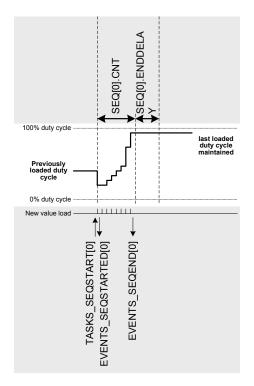


Figure 158: Single shot (LOOP.CNT=0)

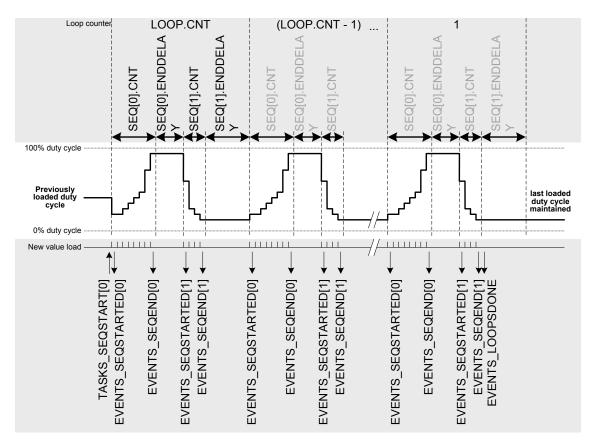


Figure 159: Complex sequence (LOOP.CNT>0) starting with SEQ[0]



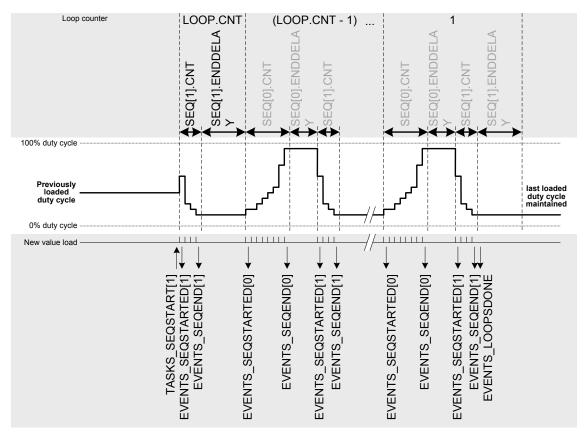


Figure 160: Complex sequence (LOOP.CNT>0) starting with SEQ[1]

Note that if a sequence is in use in a simple or complex sequence, it must have a length of SEQ[n].CNT > 0.

46.3 Limitations

The previous compare value will be repeated if the PWM period is selected to be shorter than the time it takes for the EasyDMA to fetch from RAM and update the internal compare registers.

This is to ensure a glitch-free operation even if very short PWM periods are chosen.

46.4 Pin configuration

The OUT[n] (n=0..3) signals associated to each channel of the PWM module are mapped to physical pins according to the configuration specified in the respective PSEL.OUT[n] registers. If a PSEL.OUT[n].CONNECT is set to Disconnected, the associated PWM module signal will not be connected to any physical pins.

The PSEL.OUT[n] registers and their configurations are only used as long as the PWM module is enabled and PWM generation is active (wave counter started), and retained only as long as the device is in System ON mode, see *POWER* chapter for more information about power modes.

To ensure correct behaviour in the PWM module, the pins used by the PWM module must be configured in the GPIO peripheral as described in *Table 108: Recommended GPIO configuration before starting PWM generation* on page 567 before enabling the PWM module. The pins' idle state is defined by the OUT registers in the GPIO module. This is to ensure that the pins used by the PWM module are driven correctly, if PWM generation is stopped through a STOP task, the PWM module itself is temporarily disabled, or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected IOs as long as the PWM module is supposed to be connected to an external PWM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behaviour.



Table 108: Recommended GPIO configuration before starting PWM generation

PWM signal	PWM pin	Direction	Output value	Comment
OUT[n]	As specified in PSEL.OUT[n]	Output	0	Idle state defined in GPIO->OUT
	(n=0, 3)			

46.5 Registers

Table 109: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x4001C000	PWM	PWM0	Pulse width modulation unit 0		
0x40021000	PWM	PWM1	Pulse width modulation unit 1		
0x40022000	PWM	PWM2	Pulse width modulation unit 2		
0x4002D000	PWM	PWM3	Pulse width modulation unit 3		

Table 110: Register Overview

Register	Offset	Description
TASKS_STOP	0x004	Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence
		playback
TASKS_SEQSTART[0]	0x008	Loads the first PWM value on all enabled channels from sequence 0, and starts playing that
		sequence at the rate defined in SEQ[0]REFRESH and/or DECODER.MODE. Causes PWM generation to
		start it was not running.
TASKS_SEQSTART[1]	0x00C	Loads the first PWM value on all enabled channels from sequence 1, and starts playing that
		sequence at the rate defined in SEQ[1]REFRESH and/or DECODER.MODE. Causes PWM generation to
		start it was not running.
TASKS_NEXTSTEP	0x010	Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep.
		Does not cause PWM generation to start it was not running.
EVENTS_STOPPED	0x104	Response to STOP task, emitted when PWM pulses are no longer generated
EVENTS_SEQSTARTED[0	0x108	First PWM period started on sequence 0
EVENTS_SEQSTARTED[1] 0x10C	First PWM period started on sequence 1
EVENTS_SEQEND[0]	0x110	Emitted at end of every sequence 0, when last value from RAM has been applied to wave counter
EVENTS_SEQEND[1]	0x114	Emitted at end of every sequence 1, when last value from RAM has been applied to wave counter
EVENTS_PWMPERIODE	N 0x118	Emitted at the end of each PWM period
EVENTS_LOOPSDONE	0x11C	Concatenated sequences have been played the amount of times defined in LOOP.CNT
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	PWM module enable register
MODE	0x504	Selects operating mode of the wave counter
COUNTERTOP	0x508	Value up to which the pulse generator counter counts
PRESCALER	0x50C	Configuration for PWM_CLK
DECODER	0x510	Configuration of the decoder
LOOP	0x514	Amount of playback of a loop
SEQ[0].PTR	0x520	Beginning address in Data RAM of this sequence
SEQ[0].CNT	0x524	Amount of values (duty cycles) in this sequence
SEQ[0].REFRESH	0x528	Amount of additional PWM periods between samples loaded into compare register
SEQ[0].ENDDELAY	0x52C	Time added after the sequence
SEQ[1].PTR	0x540	Beginning address in Data RAM of this sequence
SEQ[1].CNT	0x544	Amount of values (duty cycles) in this sequence
SEQ[1].REFRESH	0x548	Amount of additional PWM periods between samples loaded into compare register
SEQ[1].ENDDELAY	0x54C	Time added after the sequence
PSEL.OUT[0]	0x560	Output pin select for PWM channel 0
PSEL.OUT[1]	0x564	Output pin select for PWM channel 1
PSEL.OUT[2]	0x568	Output pin select for PWM channel 2
PSEL.OUT[3]	0x56C	Output pin select for PWM channel 3



46.5.1 SHORTS

Address offset: 0x200 Shortcut register

Bit r	number	•		31 30	29	28 2	27 2	26 2	5 2	4 23	3 2	2 2	21 2	0 1	9 18	3 17	16	15	14	13 1	.2 1	1 10	9	8	7	6 5	4	3	2	1 0
Id																											Е	D	С	ВА
Rese	et 0x00	000000		0 0	0	0	0	0 (0	0) (0	0 (0	0	0	0	0	0	0	0 (0	0	0	0	0 0	0	0	0	0 0
Id	RW	Field	Value Id	Value	:					D	esc	crip	tior	1																
Α	RW	SEQENDO_STOP								Sł	hor	tcu	ıt be	etwe	een	SEC	ĮΕΝ	D[0]	eve	ent a	and	STO	P ta	sk						
										Se	ee l	EVE	NT.	s_si	EQE	ND[0] a	nd	TAS	KS	STO	P								
			Disabled	0						Di	isal	ble	sho	rtcı	ut															
			Enabled	1						Er	nab	ole	sho	rtcu	it															
В	RW	SEQEND1_STOP								Sł	hor	tcu	ıt be	etwe	een	SEC	ĮΕΝ	D[1]	eve	ent a	and	STO	P ta	sk						
										Se	ee l	EVE	ENT.	s_si	EQE	ND[1] a	nd	TAS	KS	sto	P								
			Disabled	0						Di	isal	ble	sho	rtcı	ut															
			Enabled	1						Er	nab	ole	sho	rtcu	it															
С	RW	LOOPSDONE_SEQSTARTO								Sł	hor	tcu	ıt be	etwe	een	LOC	PS	100	IE e	ven	t an	d SE	QS1	ART	[0]	task				
										Se	ee l	EVE	NT.	S_L	00F	SDC	ONE	and	d <i>TA</i>	SKS	_SE	QST,	4RT	[0]						
			Disabled	0						Di	isal	ble	sho	rtcı	ut															
			Enabled	1						Er	nab	ole	sho	rtcu	it															
D	RW	LOOPSDONE_SEQSTART1								Sł	hor	tcu	ıt be	etwe	een	LOC	PS	100	IE e	ven	t an	d SE	QS1	ART	[1]	task				
										Se	ee l	EVE	NT.	S_ <i>L</i> (00F	SDC	ONE	and	d <i>TA</i>	SKS	_SE	QST,	4RT	[1]						
			Disabled	0						Di	isal	ble	sho	rtcı	ut															
			Enabled	1						Er	nab	ole	sho	rtcu	it															
E	RW	LOOPSDONE_STOP								Sł	hor	tcu	ıt be	etwe	een	LOC	PS	100	IE e	ven	t an	d ST	OP	task						
										Se	ee l	EVE	ENT.	S_L	00F	SDC	ONE	and	d <i>TA</i>	SKS	_ST	OP								
			Disabled	0						Di	isal	ble	sho	rtcı	ut															
			Enabled	1						Er	nab	ole	sho	rtcu	it															

46.5.2 INTEN

Address offset: 0x300 Enable or disable interrupt

	umbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld Rese	ተ በሂበ	000000		0 0 0 0 0 0 0 0	H G F E D C B
Id		Field	Value Id	Value	Description
В	RW	STOPPED			Enable or disable interrupt for STOPPED event
					See EVENTS_STOPPED
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	SEQSTARTED0			Enable or disable interrupt for SEQSTARTED[0] event
					See EVENTS_SEQSTARTED[0]
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	SEQSTARTED1			Enable or disable interrupt for SEQSTARTED[1] event
					See EVENTS_SEQSTARTED[1]
			Disabled	0	Disable
			Enabled	1	Enable
E	RW	SEQEND0			Enable or disable interrupt for SEQEND[0] event
					See EVENTS_SEQEND[0]
			Disabled	0	Disable
			Enabled	1	Enable
F	RW	SEQEND1			Enable or disable interrupt for SEQEND[1] event



Bit r	numbe	er		31	30	29	28 :	27	26 2	5 2	4 23	22	21 2	20 1	9 1	8 1	7 16	5 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id																										Н	G	F	Е	D (С Е	3
Res	et OxO	0000000		0	0	0	0	0	0 (0 (0 0	0	0	0	0 0) (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	Va	lue						De	escr	iptio	n																		
											Se	e E	VENT	S_ S	EQE	NL	0[1]															
			Disabled	0							Dis	sabl	le																			
			Enabled	1							En	able	e																			
G	RW	PWMPERIODEND								Enable Enable or disable interrupt for P See EVENTS PWMPERIODEND							lW	ИРΕ	RIO	DEN	ID (evei	nt									
											Se	e E	VENT	S_F	PWN	1PE	RIO	DEI	VD													
			Disabled	0							Dis	sabl	le																			
			Enabled	1							En	able	e																			
Н	RW	LOOPSDONE									En	able	e or o	disa	ble	int	erru	pt f	or L	.00	PSD	ON	E ev	en	t							
											Se	e E	VENT	S_L	.001	PSE	ON	Ε														
			Disabled	0							Dis	sabl	le																			
			Enabled	1							En	able	e																			

46.5.3 INTENSET

Address offset: 0x304

Enable interrupt

	ioro irritorrapt			
Bit nur	ımber		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				HGFEDCB
Reset	t 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id R	RW Field	Value Id	Value	Description
B R	RW STOPPED			Write '1' to Enable interrupt for STOPPED event
				See EVENTS_STOPPED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
C R	RW SEQSTARTED0			Write '1' to Enable interrupt for SEQSTARTED[0] event
				See EVENTS_SEQSTARTED[0]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D R	RW SEQSTARTED1			Write '1' to Enable interrupt for SEQSTARTED[1] event
				See EVENTS_SEQSTARTED[1]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E R	RW SEQENDO			Write '1' to Enable interrupt for SEQEND[0] event
				See EVENTS_SEQEND[0]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F R	RW SEQEND1			Write '1' to Enable interrupt for SEQEND[1] event
				See EVENTS_SEQEND[1]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G R	RW PWMPERIODEND			Write '1' to Enable interrupt for PWMPERIODEND event
				See EVENTS_PWMPERIODEND
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
H R	RW LOOPSDONE			Write '1' to Enable interrupt for LOOPSDONE event



Bit numbe	r											21 2	0 19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3	2 1	١ 0
Id																								Н	G	F	Ε	D	СВ	3
Reset 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 0	0 (0	0	0	0	0	0	0	0 0	0 (
ld RW	Field	Value Id							De	scrip	otio	1																		
			Se						See	EV	ENT	S_LC	OP.	SDC	NE															
		Set								Ena	ble																			
		Disabled								ad: E	Disal	oled																		
		Enabled	1							Rea	ad: E	Enab	led																	

46.5.4 INTENCLR

Address offset: 0x308

Disable interrupt

	abio iiito			
	number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				H G F E D C B
	et 0x0000000			
Id	RW Field	Value Id	Value	Description
В	RW STOP	PED		Write '1' to Disable interrupt for STOPPED event
				See EVENTS_STOPPED
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW SEQST	ARTEDO		Write '1' to Disable interrupt for SEQSTARTED[0] event
				See EVENTS_SEQSTARTED[0]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW SEQST	ARTED1		Write '1' to Disable interrupt for SEQSTARTED[1] event
				See EVENTS_SEQSTARTED[1]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Ε	RW SEQE	IDO		Write '1' to Disable interrupt for SEQEND[0] event
				See EVENTS_SEQEND[0]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW SEQE	ID1		Write '1' to Disable interrupt for SEQEND[1] event
				See EVENTS_SEQEND[1]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW PWM	PERIODEND		Write '1' to Disable interrupt for PWMPERIODEND event
				See EVENTS_PWMPERIODEND
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW LOOP:	DONE		Write '1' to Disable interrupt for LOOPSDONE event
				See EVENTS_LOOPSDONE
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

46.5.5 ENABLE

Address offset: 0x500



PWM module enable register

Bit	numbe	er		31 30	29	28	3 27	26	25	24	23	22	21 2	20 1	9 1	8 17	7 16	5 15	14	13	12	11 1	.0 9	9 8	3 7	7 6	5	4	3	2	1 0)
Id																															A	
Res	et 0x0	0000000		0 0 0 0 0 0 0 0						0	0	0	0 () (0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0 0	,	
Id	RW	Field	Value Id	Value							De	scri	otio	n																		ı
Α	RW	ENABLE									Ena	able	or (disa	ble	PW	M r	nod	ule													
			Disabled	0							Dis	able	ed																			
			Enabled							Ena	able																					

46.5.6 MODE

Address offset: 0x504

Selects operating mode of the wave counter

Bit r	numb	er		31 30 29 28 27 26 25 24 23 22 2	21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A
Res	et Ox	0000000		0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Descript	otion
Α	RW	UPDOWN		Selects (up or up and down as wave counter mode
			Up	0 Up coun	nter - edge aligned PWM duty-cycle
			UpAndDown	1 Up and	down counter - center aligned PWM duty cycle

46.5.7 COUNTERTOP

Address offset: 0x508

Value up to which the pulse generator counter counts

Bit	numb	er		31 30	29	28 2	7 26	5 25	24	23	22 2	1 20	19	18 1	17 :	16 1	15 1	4 13	3 12	11	10	9	8	7	6 !	5 4	4 3	2	1)
Id																	,	Α Α	Α	Α	Α	Α	Α	Α	A	A A	4 A	Α	Α .	
Res	et 0x0	000003FF		0 0	0	0 (0 0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	1	1	1	1 :	1 :	1 1	1	1	
Id	RW	Field	Value Id	Value						Des	crip	tion																		ı
Α	RW	COUNTERTOP		[332	767]]				Valı	ue u	p to	whi	h th	ie p	ulse	e ge	nera	tor	cοι	ınte	r cc	ount	s. T	his					
										regi	ister	is ig	nore	ed w	her	n DE	СО	DER	.MO	DE:	-Wa	veF	orn	n ar	nd o	nly				
										بامير			RAN	4:	II h															

46.5.8 PRESCALER

Address offset: 0x50C

Configuration for PWM_CLK

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		ААА
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PRESCALER		Pre-scaler of PWM_CLK
	DIV_1	0 Divide by 1 (16MHz)
	DIV_2	1 Divide by 2 (8MHz)
	DIV_4	2 Divide by 4 (4MHz)
	DIV_8	3 Divide by 8 (2MHz)
	DIV_16	4 Divide by 16 (1MHz)
	DIV_32	5 Divide by 32 (500kHz)
	DIV_64	6 Divide by 64 (250kHz)
	DIV_128	7 Divide by 128 (125kHz)

46.5.9 DECODER

Address offset: 0x510

Configuration of the decoder



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	B A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW LOAD	How a sequence is read from RAM and spread to the compare
	register
Common	0 1st half word (16-bit) used in all PWM channels 03
Grouped	1 1st half word (16-bit) used in channel 01; 2nd word in channel
	23
Individual	2 1st half word (16-bit) in ch.0; 2nd in ch.1;; 4th in ch.3
WaveForm	3 1st half word (16-bit) in ch.0; 2nd in ch.1;; 4th in
	COUNTERTOP
B RW MODE	Selects source for advancing the active sequence
RefreshCount	0 SEQ[n].REFRESH is used to determine loading internal compare
	registers
NextStep	1 NEXTSTEP task causes a new value to be loaded to internal
	compare registers

46.5.10 LOOP

Address offset: 0x514

Amount of playback of a loop

Bit r	umber		31 30 29 28 2	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0x00000000		0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW Field	Value Id	Value	Description
Α	RW CNT			Amount of playback of pattern cycles
		Disabled	0	Looping disabled (stop at the end of the sequence)

46.5.11 SEQ[0].PTR

Address offset: 0x520

Beginning address in Data RAM of this sequence

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW PTR		Beginning address in Data RAM of this sequence

46.5.12 SEQ[0].CNT

Address offset: 0x524

Amount of values (duty cycles) in this sequence

Bitı	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW CNT			Amount of values (duty cycles) in this sequence
		Disabled	0	Sequence is disabled, and shall not be started as it is empty

46.5.13 SEQ[0].REFRESH

Address offset: 0x528

Amount of additional PWM periods between samples loaded into compare register



Bit number		31	. 30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	.8 1	7 16	5 15	14	13	12	11 :	10	9	8	7 6	5 5	4	3	2	1	0
Id										Α	Α	Α	A	A A	4 Δ	A	. A	Α	Α	Α	Α	A	A	Δ,	4 Α	\ A	A	Α	Α	Α	Α
Reset 0x00000001		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	1
ld RW Field	Value Id	Va	lue							Des	crip	otio	n																		
A RW CNT										Am	oun	t of	fad	ditio	onal	PW	/M	peri	ods	bet	wee	en s	am	ples	loa	de	t				
										into	о со	mp	are	reg	iste	r (lo	ad (eve	y R	EFRI	ESH	.CN	T+1	PV	٧M						
										per	iods	5)																			
	Continuous	0								Upo	date	ev	ery	PW	M p	erio	od														

46.5.14 SEQ[0].ENDDELAY

Address offset: 0x52C

Time added after the sequence

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 1	8 17 16 15 14 13	12 11 10 9 8	7 6 5 4	3 2 1 0
Id			A A A A A	A A A A A	A A A A A	A A A A	. A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0	00000	0 0 0 0 0	0 0 0 0	0 0 0 0
ld RW Field	Value Id	Value	Description				
A RW CNT			Time added after	the sequence in P\	WM periods		

46.5.15 SEQ[1].PTR

Address offset: 0x540

Beginning address in Data RAM of this sequence

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Beginning address in Data RAM of this sequence

46.5.16 SEQ[1].CNT

Address offset: 0x544

Amount of values (duty cycles) in this sequence

Bitı	numb	er		31 30	29	28 2	7 26	25	24	23	22	21 2	0 19	9 18	3 17	16	15	14	13	12 :	1 1	9	8	7	6	5	4	3 2	2 1	. 0
Id																		Α	Α	Α	A A	A	Α	Α	Α	Α	Α	A A	Α Δ	A A
Res	et Ox	0000000		0 0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value						De	scrip	ptio	n																	
Α	RW	CNT								Am	nour	nt of	valu	ıes	(dut	у су	cles	s) ir	thi	s se	que	nce								
			Disabled	0						Sec	quer	nce i	s dis	sabl	ed,	and	sha	all n	ot k	e si	arte	d a	s it i	s er	npt	У				

46.5.17 SEQ[1].REFRESH

Address offset: 0x548

Amount of additional PWM periods between samples loaded into compare register

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000001		$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value Description
A RW CNT		Amount of additional PWM periods between samples loaded
		into compare register (load every REFRESH.CNT+1 PWM
		periods)
	Continuous	0 Update every PWM period

46.5.18 SEQ[1].ENDDELAY

Address offset: 0x54C



Time added after the sequence

Bi	t nui	mbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0	l
Id													Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	А А	
Re	eset	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	l
Id	F	RW	Field	Value Id	Va	lue							De	scr	ptic	on																				l
Α	F	RW	CNT										Tin	ne a	add	ed a	afte	r th	ie s	eau	ien	ce i	n P	WΝ	1 pe	erio	ds									

46.5.19 PSEL.OUT[0]

Address offset: 0x560

Output pin select for PWM channel 0

Bit r	numbe	er		31 3	0 29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 :	12 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				С																								В	Α	Α	Α	А А
Res	et OxF	FFFFFF		1	1 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Valu	e						De	scri	ptic	on																		
Α	RW	PIN		[03	1]						Pin	nu	mb	er																		
В	RW	PORT		[01	.]						Por	rt n	uml	ber																		
С	RW	CONNECT									OO	nne	ctic	n																		
			Disconnected	1							Dis	con	nne	ct																		
			Connected	0							OO	nne	ct																			

46.5.20 PSEL.OUT[1]

Address offset: 0x564

Output pin select for PWM channel 1

Bit r	numbe	er		31 3	30 29	9 28	8 27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	0 9	8 (. 7	6	5	4	3	2	1	0
Id				С																								В	Α	Α	Α	Α	Α
Res	et OxF	FFFFFF		1	1 1	l 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	. 1	. 1	1	1	1	1	1	1
Id	RW	Field	Value Id	Valu	ıe						De	scr	ipti	on																			
Α	RW	PIN		[03	31]						niq	า ทเ	umb	er																			
В	RW	PORT		[01	1]						Ро	rt r	num	bei	r																		
С	RW	CONNECT									Co	nne	ecti	on																			
			Disconnected	1							Di	sco	nne	ct																			
			Connected	0							Co	nne	ect																				

46.5.21 PSEL.OUT[2]

Address offset: 0x568

Output pin select for PWM channel 2

Bit r	numbe	er		31	30 2	9 28	8 27	26	25	24	23 :	22 2	21 2	0 19	18	17	16	15	14 1	3 12	11	10	9 8	7	6	5	4	3	2	1 0
Id				С																						В	Α	Α	A	А А
Res	et OxF	FFFFFF		1	1 1	l 1	. 1	1	1	1	1	1	1 :	l 1	1	1	1	1	1 :	l 1	1	1	1 1	. 1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Val	ue						Des	crip	tio	ı																
Α	RW	PIN		[0	31]						Pin	nun	nbe	r																
В	RW	PORT		[0	1]						Por	t nu	mb	er																
С	RW	CONNECT									Con	nec	tior	1																
			Disconnected	1							Disc	conr	nect																	
			Connected	0							Con	nec	t																	

46.5.22 PSEL.OUT[3]

Address offset: 0x56C

Output pin select for PWM channel 3



Bit r	numbe	er		31	30 2	9 2	8 27	7 26	25	24	23	22	21	20	19	18 1	l7 1	6 15	5 14	13	12 :	11 10	9	8	7	6	5	4	3 2	2 1	. 0
Id				С																							В	Α	A A	Α Δ	АА
Res	et OxF	FFFFFF		1	1 1	L 1	l 1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1 1	1	1	1	1	1	1	1 1	1	. 1
Id	RW	Field	Value Id	Val	ue						De	scr	iptio	on																	
Α	RW	PIN		[0	31]						Pin	า ทน	ımb	er																	
В	RW	PORT		[0	1]						Poi	rt n	um	ber																	
С	RW	CONNECT									Coi	nne	ectio	n																	
			Disconnected	1							Dis	100	nne	ct																	
			Connected	0							Coi	nne	ect																		

46.6 Electrical specification

46.6.1 PWM Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{PWM,16MHz}	PWM run current, Prescaler set to DIV_1 (16 MHz), excluding		200		μΑ
	DMA and GPIO				
I _{PWM,8MHz}	PWM run current, Prescaler set to DIV_2 (8 MHz), excluding		100		μΑ
	DMA and GPIO				
I _{PWM,125kHz}	PWM run current, Prescaler set to DIV_128 (125 kHz), excluding		50		μΑ
	DMA and GPIO				



47 SPI — Serial peripheral interface master

The SPI master provides a simple CPU interface which includes a TXD register for sending data and an RXD register for receiving data. This section is added for legacy support for now.

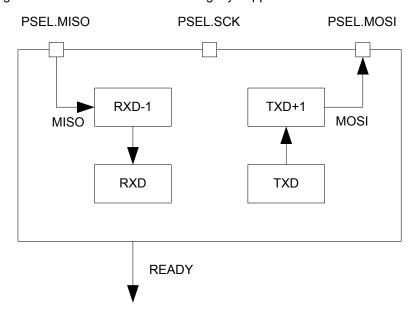


Figure 161: SPI master

RXD-1 and TXD+1 illustrate the double buffered version of RXD and TXD respectively.

47.1 Functional description

The TXD and RXD registers are double-buffered to enable some degree of uninterrupted data flow in and out of the SPI master.

The SPI master does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master. The SPI master supports SPI modes 0 through 3.

Table 111: SPI modes

Mode	Clock polarity	Clock phase
	CPOL	СРНА
SPI_MOI	DE 0 (Leading)	0 (Active High)
SPI_MOI	DE 0 (Leading)	1 (Active Low)
SPI_MOI	DE 1 (Trailing)	0 (Active High)
SPI MOI	DE 1 (Trailing)	1 (Active Low)

47.1.1 SPI master mode pin configuration

The different signals SCK, MOSI, and MISO associated with the SPI master are mapped to physical pins.

This mapping is according to the configuration specified in the PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If the CONNECT field of a PSEL.xxx register is set to Disconnected, the associated SPI master signal is not connected to any physical pin. The PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI master is disabled.

To secure correct behavior in the SPI, the pins used by the SPI must be configured in the GPIO peripheral as described in *Table 112: GPIO configuration* on page 577 prior to enabling the SPI. The SCK must



always be connected to a pin, and that pin's input buffer must always be connected for the SPI to work. This configuration must be retained in the GPIO for the selected IOs as long as the SPI is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 112: GPIO configuration

SPI master signal	SPI master pin	Direction	Output value
SCK	As specified in PSEL.SCK	Output	Same as CONFIG.CPOL
MOSI	As specified in PSEL.MOSI	Output	0
MISO	As specified in PSEL.MISO	Input	Not applicable

47.1.2 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.

Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 23 for details on peripherals and their IDs.

47.1.3 SPI master transaction sequence

An SPI master transaction is started by writing the first byte, which is to be transmitted by the SPI master, to the TXD register.

Since the transmitter is double buffered, the second byte can be written to the TXD register immediately after the first one. The SPI master will then send these bytes in the order they are written to the TXD register.

The SPI master is a synchronous interface, and for every byte that is sent, a different byte will be received at the same time; this is illustrated in *Figure 162: SPI master transaction* on page 578. Bytes that are received will be moved to the RXD register where the CPU can extract them by reading the register. The RXD register is double buffered in the same way as the TXD register, and a second byte can therefore be received at the same time as the first byte is being extracted from RXD by the CPU. The SPI master will generate a READY event every time a new byte is moved to the RXD register. The double buffered byte will be moved from RXD-1 to RXD as soon as the first byte is extracted from RXD. The SPI master will stop when there are no more bytes to send in TXD and TXD+1.



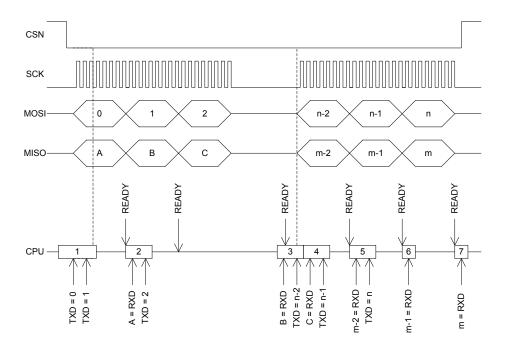


Figure 162: SPI master transaction

The READY event of the third byte transaction is delayed until B is extracted from RXD in occurrence number 3 on the horizontal lifeline. The reason for this is that the third event is generated first when C is moved from RXD-1 to RXD after B is read.

The SPI master will move the incoming byte to the RXD register after a short delay following the SCK clock period of the last bit in the byte. This also means that the READY event will be delayed accordingly, see *Figure 163: SPI master transaction* on page 578. Therefore, it is important that you always clear the READY event, even if the RXD register and the data that is being received is not used.

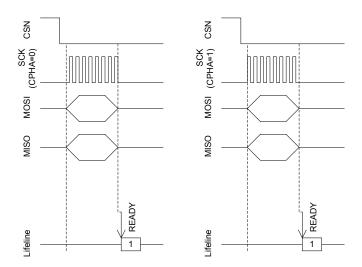


Figure 163: SPI master transaction



47.2 Registers

Table 113: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	SPI	SPI0	SPI master 0		Deprecated
0x40004000	SPI	SPI1	SPI master 1		Deprecated
0x40023000	SPI	SPI2	SPI master 2		Deprecated

Table 114: Register Overview

Register	Offset	Description
EVENTS_READY	0x108	TXD byte sent and RXD byte received
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable SPI
PSEL.SCK	0x508	Pin select for SCK
PSEL.MOSI	0x50C	Pin select for MOSI signal
PSEL.MISO	0x510	Pin select for MISO signal
RXD	0x518	RXD register
TXD	0x51C	TXD register
FREQUENCY	0x524	SPI frequency. Accuracy depends on the HFCLK source selected.
CONFIG	0x554	Configuration register

47.2.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	r		31	30 2	9 :	28 2	27 2	26	25	24	23	22	21	20	19	18	3 17	7 10	5 1	5 1	4 1	.3 1	12 1	11 1	.0	9	8	7	6	5	4	3	2	1	0
Id																																		Α		
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C) () (0	0	0 (0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Val	ue							De	scr	ipti	on																					
Α	RW	READY										Wr	ite	'1'	to E	Ena	ble	int	terr	up	t fo	r R	EAI	DY 6	evei	nt										_
												See	e <i>E</i> I	/EΝ	ITS_	RE	AD	Υ																		
			Set	1								Ena	able	е																						
			Disabled	0								Rea	ad:	Dis	abl	ed																				
			Enabled	1								Rea	ad:	Ena	able	ed																				

47.2.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bitı	numbe	er		31	1 30	29	2	8 2	7 2	6 2	5 2	4 2	3 2	2 2	1 2	0 1	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		Α		
Res	et 0x0	0000000		0	0	0	C) (0) (0) (0 () (0 ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	:						C	eso	rip	tio	า																				
Α	RW	READY										٧	Vrit	e '1	l' to	Di	sab	le	int	erru	ıpt	for	RE	AD'	Y e	/en	t									
												S	ee	EVE	NT	S_F	REA	DΥ	,																	
			Clear	1								C	isa	ble																						
			Disabled	0								R	lead	d: D	isal	ole	d																			
			Enabled	1								R	lead	d: E	nab	led	ł																			

47.2.3 ENABLE

Address offset: 0x500

Enable SPI



Bitı	numl	ber			31 3	0 29	9 28	8 27	26	25	24	23	22	21 :	20 1	19 1	8 1	7 1	5 15	14	13	12	1 1	9	8	7	6	5	4	3	2	1 0
Id																														Α	Α	А А
Res	et 0	x00	000000		0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id	RV	N	Field	Value Id	Valu	e						De	scri	ptio	n																	
Α	RV	Ν	ENABLE									Ena	able	or	disa	ble	SPI															
				Disabled	0							Dis	able	s SP	l l																	
				Enabled	1							Ena	able	SPI																		

47.2.4 PSEL.SCK

Address offset: 0x508 Pin select for SCK

Bitı	numbe	er		31	30 2	29 2	28 2	7 2	6 2	5 2	4 2	23 2	22 2	21 2	20 1	L9 1	8 1	7 1	6 1	5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1	0
Id				С																									В	Α	Α	Α	Α	Α
Res	et 0xF	FFFFFF		1	1	1	1 1	1 :	L 1	L 1	1	1	1 :	1 :	1	1	1 :	1 :	L 1	L 1	1 1	1	. 1	. 1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																			
Α	RW	PIN		[0.	.31]						F	Pin ı	nun	nbe	r																			
В	RW	PORT		[0.	.1]						F	ort	nu	mb	er																			
С	RW	CONNECT									(Con	nec	tior	n																			
			Disconnected	1								Disc	onr	nect	t																			
			Connected	0							(Con	nec	t																				

47.2.5 PSEL.MOSI

Address offset: 0x50C Pin select for MOSI signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ВАААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

47.2.6 PSEL.MISO

Address offset: 0x510

Pin select for MISO signal

Bit r	umbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	вааа
Rese	t OxF	FFFFFF		1 1 1 1 1 1 1 1	$1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

47.2.7 RXD

Address offset: 0x518

RXD register



Bit	numb	er		31	30 2	29	28	27 :	26	25 2	24	23 2	22 2	1 2	0 19	18	3 17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3	2 1	L 0
Id																										Α	Α	Α	Α	Α.	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0
Id	RW	Field	Value Id	Va	lue							Des	crip	tior	1																	
Α	R	RXD										RX c	lata	rec	eive	d. I	Dou	ble	buf	fere	d											

47.2.8 TXD

Address offset: 0x51C

TXD register

Bitı	numbe	er		31	30 2	9 :	28 2	7 26	5 25	24	23	22	21	20	19 1	.8 1	7 1	6 1	5 1	4 1	3 12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id																										Α	Α	Α	Α	A	4 A	А
Res	et 0x0	0000000		0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Va	lue						De	scri	otic	n																		
Α	RW	TXD									ΤX	data	a to	sei	nd. I	Dou	ble	buf	fer	ed												

47.2.9 FREQUENCY

Address offset: 0x524

SPI frequency. Accuracy depends on the HFCLK source selected.

Bit r	numbe	er		31	. 30	29	28	8 27	26	5 25	5 24	23	22	21	20	19	18 1	l7 1	6 1	5 14	1 13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	A	Α	A	Α	Α	Α	Α	Α	Α	Α	A A	A A	A	Α	Α	Α	Α	Α	A	Α	Α	Α .	Α /	A A	Α	Α
Rese	et 0x0	400000		0	0	0	0	0	1	. 0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0 (0 (0	0
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	n																		
Α	RW	FREQUENCY										SPI	ma	ste	r da	ata r	ate																
			K125	0x	:020	0000	000)				12	5 kb	ps																			
			K250	0x	040	0000	000)				250) kb	ps																			
			K500	0x	:080	0000	000)				500) kb	ps																			
			M1	0x	100	0000	000)				1 N	1bp	S																			
			M2	0x	200	0000	000)				2 N	1bp	S																			
			M4	0x	400	0000	000)				4 N	1bp	S																			
			M8	0x	800	0000	000)				8 N	1bp	S																			

47.2.10 CONFIG

Address offset: 0x554 Configuration register

																									_	_	_	_		_	
Bit r	numbe	er		31	30	29	28 2	27 2	26 2	5 2	4 2	3 22	21	20	19	18	17	16	15	14 1	.3 1	2 11	. 10	9	8	7	6	5 4	1 3	2	1 0
Id																														С	В А
Res	et 0x0	0000000		0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0 0
Id	RW	Field	Value Id	Va	lue						D	escr	iptic	n																	
Α	RW	ORDER									В	it or	der																		
			MsbFirst	0							Ν	/lost	signi	ifica	ant	bit	shif	ted	ou	t fir	st										
			LsbFirst	1							Le	east	signi	ifica	ant	bit	shit	ted	ou	t fir	st										
В	RW	СРНА									S	erial	cloc	k (S	SCK) ph	nase	:													
			Leading	0							S	amp	le or	ı le	adir	ng e	edge	e of	clc	ck,	shift	ser	ial d	ata	on t	rai	ling				
											е	dge																			
			Trailing	1							S	amp	le or	n tra	ailir	ng e	dge	e of	clo	ck,	hift	seri	al d	ata	on l	eac	ling				
											е	dge																			
С	RW	CPOL									S	erial	cloc	k (S	SCK) pc	olari	ty													
			ActiveHigh	0							Α	ctive	hig	h																	
			ActiveLow	1							Α	ctive	low	,																	



47.3 Electrical specification

47.3.1 SPI master interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{SPI}	Bit rates for SPI ³⁶			8 ³⁷	Mbps
I _{SPI,2Mbps}	Run current for SPI, 2 Mbps			50	μΑ
I _{SPI,8Mbps}	Run current for SPI, 8 Mbps			50	μΑ
I _{SPI,IDLE}	Idle current for SPI (STARTed, no CSN activity)		<1		μΑ
t _{SPI.START}	Time from writing TXD register to transmission started		1		μs

47.3.2 Serial Peripheral Interface (SPI) Master timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{SPI,CSCK}	SCK period	125			ns
t _{SPI,RSCK,LD}	SCK rise time, standard drive ^a			t _{RF,25pF}	
t _{SPI,RSCK,HD}	SCK rise time, high drive ^a			t _{HRF,25pF}	
t _{SPI,FSCK,LD}	SCK fall time, standard drive ^a			t _{RF,25pF}	
t _{SPI,FSCK,HD}	SCK fall time, high drive ^a			t _{HRF,25pF}	
t _{SPI,WHSCK}	SCK high time ^a	(0.5*t _{CSC}	κÌ		
		- t _{RSCK}			
t _{SPI,WLSCK}	SCK low time ^a	(0.5*t _{CSC}	κÌ		
		- t _{FSCK}			
t _{SPI,SUMI}	MISO to CLK edge setup time	19			ns
t _{SPI,HMI}	CLK edge to MISO hold time	18			ns
t _{SPI,VMO}	CLK edge to MOSI valid			59	ns
t _{SPI,HMO}	MOSI hold time after CLK edge	20			ns

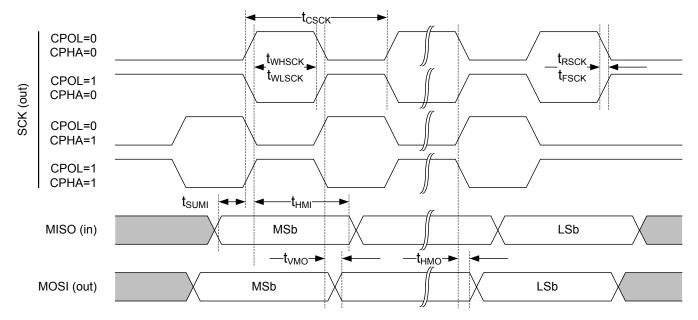


Figure 164: SPI master timing diagram

 $^{^{36}}$ High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.

^a At 25pF load, including GPIO capacitance, see GPIO spec.



48 TWI — I²C compatible two-wire interface

The TWI master is compatible with I²C operating at 100 kHz and 400 kHz.

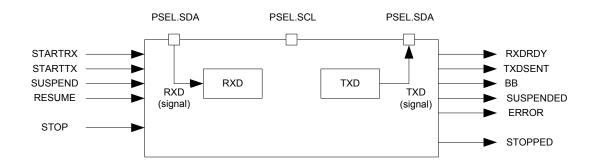


Figure 165: TWI master's main features

48.1 Functional description

This TWI master is not compatible with CBUS. The TWI transmitter and receiver are single buffered.

See, Figure 165: TWI master's main features on page 583.

A TWI setup comprising one master and three slaves is illustrated in *Figure 166: A typical TWI setup comprising one master and three slaves* on page 583. This TWI master is only able to operate as the only master on the TWI bus.

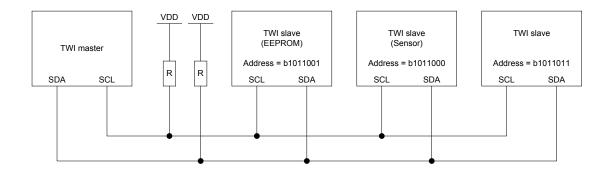


Figure 166: A typical TWI setup comprising one master and three slaves

This TWI master supports clock stretching performed by the slaves. The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

48.2 Master mode pin configuration

The different signals SCL and SDA associated with the TWI master are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

If the CONNECT field of a PSEL.xxx register is set to Disconnected, the associated TWI signal is not connected to any physical pin. The PSEL.SCL and PSEL.SDA registers and their configurations are



only used as long as the TWI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCL and PSEL.SDA must only be configured when the TWI is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table 115: GPIO configuration* on page 584.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 115: GPIO configuration

TWI master signal	TWI master pin	Direction	Drive strength	Output value
SCL	As specified in PSEL.SCL	Input	SOD1	Not applicable
SDA	As specified in PSEL.SDA	Input	SOD1	Not applicable

48.3 Shared resources

The TWI shares registers and other resources with other peripherals that have the same ID as the TWI.

Therefore, you must disable all peripherals that have the same ID as the TWI before the TWI can be configured and used. Disabling a peripheral that has the same ID as the TWI will not reset any of the registers that are shared with the TWI. It is therefore important to configure all relevant TWI registers explicitly to secure that it operates correctly.

The Instantiation table in *Instantiation* on page 23 shows which peripherals have the same ID as the TWI.

48.4 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes that are written to the TXD register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave. A TXDSENT event will be generated each time the TWI master has clocked out a TXD byte, and the associated ACK/NACK bit has been clocked in from the slave.

The TWI master transmitter is single buffered, and a second byte can only be written to the TXD register after the previous byte has been clocked out and the ACK/NACK bit clocked in, that is, after the TXDSENT event has been generated.

If the CPU is prevented from writing to TXD when the TWI master is ready to clock out a byte, the TWI master will stretch the clock until the CPU has written a byte to the TXD register.

A typical TWI master write sequence is illustrated in *Figure 167: The TWI master writing data to a slave* on page 585. Occurrence 3 in the figure illustrates delayed processing of the TXDSENT event associated with TXD byte 1. In this scenario the TWI master will stretch the clock to prevent writing erroneous data to the slave.



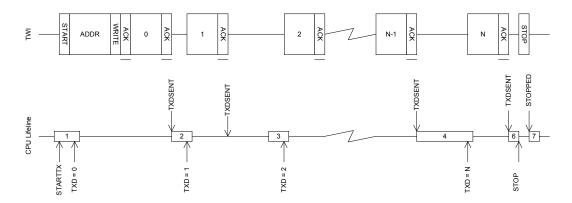


Figure 167: The TWI master writing data to a slave

The TWI master write sequence is stopped when the STOP task is triggered whereupon the TWI master will generate a stop condition on the TWI bus.

48.5 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1).

The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

The TWI master will generate a RXDRDY event every time a new byte is received in the RXD register.

After receiving a byte, the TWI master will delay sending the ACK/NACK bit by stretching the clock until the CPU has extracted the received byte, that is, by reading the RXD register.

The TWI master read sequence is stopped by triggering the STOP task. This task must be triggered before the last byte is extracted from RXD to ensure that the TWI master sends a NACK back to the slave before generating the stop condition.

A typical TWI master read sequence is illustrated in *Figure 168: The TWI master reading data from a slave* on page 586. Occurrence 3 in this figure illustrates delayed processing of the RXDRDY event associated with RXD byte B. In this scenario the TWI master will stretch the clock to prevent the slave from overwriting the contents of the RXD register.



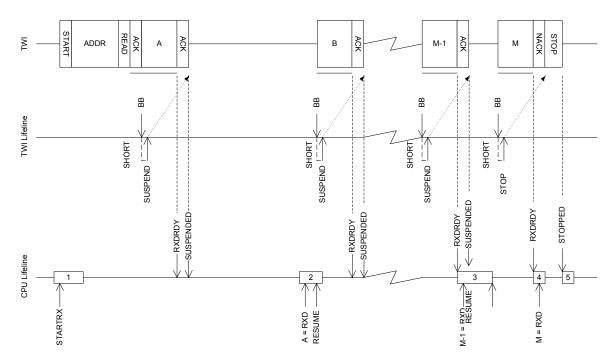


Figure 168: The TWI master reading data from a slave

48.6 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes one byte to the slave followed by reading M bytes from the slave. Any combination and number of transmit and receive sequences can be combined in this fashion. Only one shortcut to STOP can be enabled at any given time.

The figure below illustrates a repeated start sequence where the TWI master writes one byte, followed by reading M bytes from the slave without performing a stop in-between.

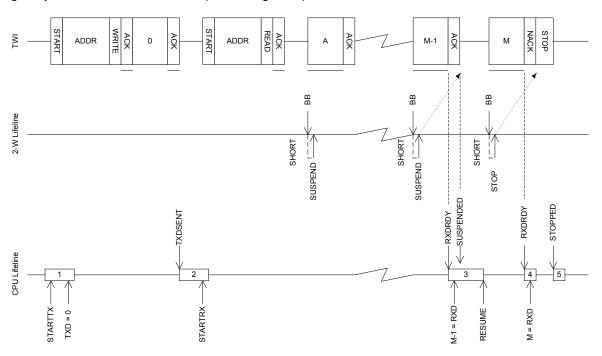


Figure 169: A repeated start sequence, where the TWI master writes one byte, followed by reading M bytes from the slave without performing a stop in-between



To generate a repeated start after a read sequence, a second start task must be triggered instead of the STOP task, that is, STARTRX or STARTTX. This start task must be triggered before the last byte is extracted from RXD to ensure that the TWI master sends a NACK back to the slave before generating the repeated start condition.

48.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

48.8 Registers

Table 116: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	TWI	TWI0	Two-wire interface master 0		Deprecated
0x40004000	TWI	TWI1	Two-wire interface master 1		Deprecated

Table 117: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start TWI receive sequence
TASKS_STARTTX	0x008	Start TWI transmit sequence
TASKS_STOP	0x014	Stop TWI transaction
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_RXDREADY	0x108	TWI RXD byte received
EVENTS_TXDSENT	0x11C	TWI TXD byte sent
EVENTS_ERROR	0x124	TWI error
EVENTS_BB	0x138	TWI byte boundary, generated before each byte that is sent or received
EVENTS_SUSPENDED	0x148	TWI entered the suspended state
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4C4	Error source
ENABLE	0x500	Enable TWI
PSEL.SCL	0x508	Pin select for SCL
PSEL.SDA	0x50C	Pin select for SDA
RXD	0x518	RXD register
TXD	0x51C	TXD register
FREQUENCY	0x524	TWI frequency. Accuracy depends on the HFCLK source selected.
ADDRESS	0x588	Address used in the TWI transfer

48.8.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number		31	30	29	28 2	7 2	6 25	24	23	22 2	21 2	0 19	9 18	17	16	15	14	13	12	11	10 9	9 8	3 7	' 6	5	4	3	2	1 ()
Id																													В	٨
Reset 0x00000000		0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0 ()
ld RW Field	Value Id	Va	lue						Des	crip	otio	1																		

A RW BB_SUSPEND

Shortcut between BB event and SUSPEND task



Bit number		31 30 29 28 27 26 25 24 23 22 21 2	0 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			В
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description	n
		See <i>EVENT</i> :	S_BB and TASKS_SUSPEND
	Disabled	0 Disable sho	ortcut
	Enabled	1 Enable sho	rtcut
B RW BB_STOP		Shortcut be	etween BB event and STOP task
		See EVENTS	S_BB and TASKS_STOP
	Disabled	0 Disable sho	ortcut
	Enabled	1 Enable sho	rtcut

48.8.2 INTENSET

Address offset: 0x304

Enable interrupt

		у и поттарт																															
	numb	er		3:	1 30	29	28 2	27 2	6 25	5 24	1 2	3 22	2 21 2	0 1			.7 1	6 1			13 1	2 :	11 1					5 5	5 4	3			0
Id															F					Ε)	(Α	
Res		00000000		0			0	0 (0	0			0		0 0) (0 (כ	0	0	0	0	0 () () () () (0 () (0	0	0	0
Id		Field	Value Id	V	alue								riptio																				
Α	RW	STOPPED									W	Vrite	e '1' to	En	nable	e in	iter	rup	ot fo	or S	TOI	PE	D e	ven	t								
											S	ee E	VENT	s_s	TOF	PE	D																
			Set	1							Е	nab	le																				
			Disabled	0							R	ead	: Disa	ble	d																		
			Enabled	1							R	ead	: Enat	oled	ł																		
В	RW	RXDREADY									W	Vrite	e '1' to	En	nable	e in	iter	rup	ot fo	or F	RXDI	RE/	ADY	eve	nt								
											S	ee E	VENT	S F	RXDI	RE/	ADY																
			Set	1								nab		_																			
			Disabled	0							R	ead	: Disa	ble	d																		
			Enabled	1							R	ead	: Enat	oled	ł																		
С	RW	TXDSENT									W	Vrite	e '1' to	En	nable	e in	iter	rup	ot fo	or 1	XDS	SEN	IT e	/en	t								
											S	ee E	VENT	· S_1	TXDS	EΝ	IT																
			Set	1								nab		-																			
			Disabled	0							R	ead	: Disa	ble	d																		
			Enabled	1							R	ead	: Enab	oled	ł																		
D	RW	ERROR									W	Vrite	e '1' to	En	nable	e in	iter	rup	ot fo	or E	RRC	OR	eve	nt									
											S	ee E	VENT	S_E	RRC	DR																	
			Set	1							Е	nab	le																				
			Disabled	0							R	ead	: Disa	ble	d																		
			Enabled	1							R	ead	: Enak	oled	ł																		
Ε	RW	ВВ									W	Vrite	e '1' to	En	nable	e in	iter	rup	ot fo	or E	ВВ е	ver	nt										
											S	ee E	VENT	S_E	3 <i>B</i>																		
			Set	1							Е	nab	le																				
			Disabled	0							R	ead	: Disa	ble	d																		
			Enabled	1							R	ead	: Enat	oled	ł																		
F	RW	SUSPENDED									W	Vrite	e '1' to	En	nable	e in	iter	rup	ot fo	or S	USF	PEN	IDE) ev	en	t							
											S	ee E	VENT	s_s	SUSF	EΝ	IDE	D															
			Set	1							Е	nab	le																				
			Disabled	0							R	ead	: Disa	ble	d																		
			Enabled	1							R	ead	: Enak	oled	ł																		

48.8.3 INTENCLR

Address offset: 0x308 Disable interrupt



Bit	numb	er		31	30 2	29 2	28 27	7 26	25	24	23	3 22 2	1 2	0 1	9 1	.8 1	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (
Id															- 1	F				Ε					D		С					В.	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0 () () (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Val	ue						De	escrip	tio	ı																			
Α	RW	STOPPED									W	rite '1	' to	Dis	sab	le i	nte	rru	ıpt	for	STC	PP	ED	eve	ent								
											Se	e <i>EVE</i>	NT.	s_s	ΤΟΙ	PPE	D																
			Clear	1							Di	sable																					
			Disabled	0							Re	ead: D	isal	oled	b																		
			Enabled	1							Re	ead: E	nab	led	I																		
В	RW	RXDREADY									W	rite '1	' to	Dis	sab	le i	nte	erru	ıpt	for	RXI	ORE	ΑC)Y e	ver	t							
											Se	e <i>EVE</i>	NT.	S_R	XD	REA	4D	Y															
			Clear	1							Di	sable																					
			Disabled	0							Re	ead: D	isal	oled	b																		
			Enabled	1							Re	ead: E	nab	led	ı																		
С	RW	TXDSENT									W	rite '1	' to	Dis	sab	le i	nte	rrı	ıpt	for	TXI	SE	NT	eve	ent								
											Se	e <i>EVE</i>	NT.	S_T	XD:	SEN	٧T																
			Clear	1							Di	sable																					
			Disabled	0							Re	ead: D	isal	oled	b																		
			Enabled	1							Re	ead: E	nab	led	1																		
D	RW	ERROR									W	rite '1	'to	Dis	sab	le i	nte	erru	ıpt	for	ERF	ROF	? e	/ent	t								
											Se	e <i>EVE</i>	NT.	S_E	RR	OR																	
			Clear	1							Di	sable																					
			Disabled	0							Re	ead: D	isal	oled	d																		
			Enabled	1							Re	ead: E	nab	led	I																		
Ε	RW	ВВ									W	rite '1	'to	Dis	sab	le i	nte	erru	ıpt	for	BB	eve	ent										
											Se	e <i>EVE</i>	NT.	S_B	BB																		
			Clear	1							Di	sable																					
			Disabled	0							Re	ead: D	isal	oled	b																		
			Enabled	1							Re	ead: E	nab	led	I																		
F	RW	SUSPENDED									W	rite '1	' to	Dis	sab	le i	nte	erru	ıpt	for	SUS	PE	ND	ED	eve	nt							
											Se	e <i>EVE</i>	NT.	s_s	USI	PEN	VDI	D															
			Clear	1							Di	sable																					
			Disabled	0							Re	ead: D	isal	oled	d																		
			Enabled	1							Re	ead: E	nab	led	ı																		

48.8.4 ERRORSRC

Address offset: 0x4C4

Error source

Bit r	numbe	er		31	30.2	29 :	28 2	7 2	6 2	5 24	1 23	22	21 2	20 1	19 1	18	17 ·	16	15	14 ^	3 1	2 1	1 1	0 9	9 8	3 7	' 6	5	4	3	2	1 0
Id																															C	ВА
Res	et 0x0	0000000		0	0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0) (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Val	ue						De	scri	ptio	n																		
Α	RW	OVERRUN									Ov	erru	ın er	rror	-																	
											A n	new	byte	e w	as r	ece	eive	d b	efo	re p	rev	iou	s by	/te	got	rea	d by	,				
											sof	ftwa	re fi	ron	n th	e R	XD	reg	iste	er. (Prev	/iou	ıs d	ata	is l	ost)						
			NotPresent	0							Rea	ad: ı	no o	ver	run	00	cur	ed														
			Present	1							Rea	ad: d	over	rur	oc	cui	ed															
В	RW	ANACK									NA	ACK r	rece	ive	d af	fter	sei	ndir	ng t	he a	add	ress	(w	rite	'1'	to	lea	r)				
			NotPresent	0							Rea	ad:	erro	r no	ot p	res	ent															
			Present	1							Rea	ad:	erro	r pı	rese	ent																
С	RW	DNACK									NA	ACK r	rece	ive	d af	ter	sei	ndir	ng a	da	ta b	yte	(w	rite	'1'	to c	lear	-)				
			NotPresent	0							Rea	ad:	erro	r no	ot p	res	ent															
			Present	1							Rea	ad:	erro	r pı	rese	ent																



48.8.5 ENABLE

Address offset: 0x500

Enable TWI

Bitı	numb	ber			31	30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																																Α	A	А А
Res	et 0x	(00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	V	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	V I	ENABLE										En	able	or	dis	able	e T\	N۱															
				Disabled	0								Di	sabl	e T\	N۱																		
				Enabled	5								En	able	: TV	VI																		

48.8.6 PSEL.SCL

Address offset: 0x508
Pin select for SCL

Bit r	iumbe	r		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ваааа
Rese	et OxF	FFFFFF		1 1 1 1 1 1 1 1	$1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

48.8.7 PSEL.SDA

Address offset: 0x50C Pin select for SDA

Bit r	numbe	er		31	30 2	29 2	28 2	7 26	5 25	5 24	23	3 22	21	20	19	18	17	16	15	14 1	13 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	1 0
Id				С																								В	Α.	ΑА	A A	Α Α
Res	et OxF	FFFFFF		1	1	1	1 1	l 1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	l 1	1	1	1	1	1	1	1 1	1	l 1
Id	RW	Field	Value Id	Va	lue						De	escr	ipti	on																		
Α	RW	PIN		[0.	.31]						Pi	n nı	ımb	er																		
В	RW	PORT		[0.	.1]						Po	rt r	um	bei	r																	
С	RW	CONNECT									Co	nne	ectio	on																		
			Disconnected	1							Di	sco	nne	ct																		
			Connected	0							Co	nne	ect																			

48.8.8 RXD

Address offset: 0x518

RXD register

Bit nu	mber		31 30 29 28 27	26 25 24	23 2	2 21 2	0 19	18 17	7 16	15 1	4 13	12 13	10	9	8	7	6 5	4	3	2 :	1 0
Id																Δ,	Д Д	A	Α	A A	4 А
Reset	0x00000000		0 0 0 0 0	0 0 0	0 0	0 (0 0	0 0	0	0 (0 0	0 0	0	0	0	0	0 0	0	0	0 (0 0
Id	RW Field	Value Id	Value		Desc	riptio	1														
Α	R RXD				RXD	registe	er														

48.8.9 TXD

Address offset: 0x51C

TXD register



Reset 0x00000000				0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id RW Field A RW TXD	Value Id	Value	Description TXD register		

48.8.10 FREQUENCY

Address offset: 0x524

TWI frequency. Accuracy depends on the HFCLK source selected.

Bit	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 1	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	Α	Α	Α	Α	Α	Α	Α	A	4 A	Α	Α
Res	et 0x0	4000000		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	FREQUENCY										TW	/I m	aste	er c	locl	k fr	equ	end	у													
			K100	0x	019	800	000					100) kb	ps																			
			K250	0x	040	0000	000					250) kb	ps																			
			K400	0x	066	800	000					400) kb	ps	(act	ual	rat	e 4:	10.	256	kbp	5)											

48.8.11 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

E	3it n	umbe	er		31	30 2	29 :	28 2	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 :	10	9	8	7	6	5	4	3	2	1)
1	d																												Α	Α	Α	Α .	Δ,	Α	4
F	Rese	t 0x0	0000000		0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0)
ı	ld	RW	Field	Value Id	Va	lue						De	scri	ptic	on																				
-	Δ	RW	ADDRESS									Αd	dre	SS 11	iser	lin	the	TW	/I tr	ans	fer														

48.9 Electrical specification

48.9.1 TWI interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWI,SCL}	Bit rates for TWI ³⁸	100		400	kbps
I _{TWI,100kbps}	Run current for TWI, 100 kbps		50		μΑ
I _{TWI,400kbps}	Run current for TWI, 400 kbps		50		μΑ
t _{TWI,START}	Time from STARTRX/STARTTX task to transmission started		1.5		μs

48.9.2 Two Wire Interface (TWI) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{TWI,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t _{TWI,HD_DAT}	Data hold time after negative edge on SCL – all modes	500			ns
t _{TWI,HD_STA,100kbps}	TWI master hold time for START and repeated START condition,	10000			ns
	100 kbps				
t _{TWI,HD_STA,250kbps}	TWI master hold time for START and repeated START condition,	4000			ns
	250kbps				
t _{TWI,HD_STA,400kbps}	TWI master hold time for START and repeated START condition,	2500			ns
	400 kbps				
t _{TWI,SU_STO,100kbps}	TWI master setup time from SCL high to STOP condition, 100	5000			ns
	kbps				
t _{TWI,SU_STO,250kbps}	TWI master setup time from SCL high to STOP condition, 250	2000			ns
	kbps				

High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Symbol	Description	Min.	Тур.	Max.	Units
t _{TWI,SU_STO,400kbps}	TWI master setup time from SCL high to STOP condition, 400	1250			ns
	kbps				
t _{TWI,BUF,100kbps}	TWI master bus free time between STOP and START conditions,	5800			ns
	100 kbps				
t _{TWI,BUF,250kbps}	TWI master bus free time between STOP and START conditions,	2700			ns
	250 kbps				
t _{TWI,BUF,400kbps}	TWI master bus free time between STOP and START conditions,	2100			ns
	400 kbps				

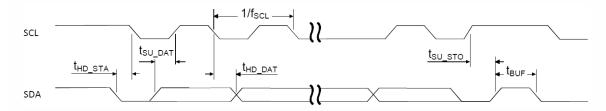


Figure 170: TWI timing diagram, 1 byte transaction



49 UART — Universal asynchronous receiver/ transmitter

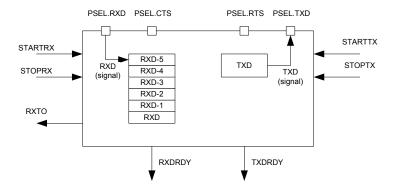


Figure 171: UART configuration

49.1 Functional description

Listed here are the main features of UART.

The UART implements support for the following features:

- Full-duplex operation
- · Automatic flow control
- Parity checking and generation for the 9th data bit

As illustrated in *Figure 171: UART configuration* on page 593, the UART uses the TXD and RXD registers directly to transmit and receive data. The UART uses one stop bit.

49.2 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UART are mapped to physical pins according to the configuration specified in the PSEL.RXD, PSEL.RTS, and PSEL.TXD registers respectively.

If the CONNECT field of a PSEL.xxx register is set to Disconnected, the associated UART signal will not be connected to any physical pin. The PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers and their configurations are only used as long as the UART is enabled, and retained only for the duration the device is in ON mode. PSEL.RXD, PSEL.CTS, PSEL.RTS and PSEL.TXD must only be configured when the UART is disabled.

To secure correct signal levels on the pins by the UART when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Pin configuration* on page 593.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 118: GPIO configuration

UART pin	Direction	Output value
RXD	In	put Not applicable
CTS	In	put Not applicable
RTS	Ou	itput 1
TXD	Ou	tput 1



49.3 Shared resources

The UART shares registers and other resources with other peripherals that have the same ID as the UART.

Therefore, you must disable all peripherals that have the same ID as the UART before the UART can be configured and used. Disabling a peripheral that has the same ID as the UART will not reset any of the registers that are shared with the UART. It is therefore important to configure all relevant UART registers explicitly to ensure that it operates correctly.

See the Instantiation table in *Instantiation* on page 23 for details on peripherals and their IDs.

49.4 Transmission

A UART transmission sequence is started by triggering the STARTTX task.

Bytes are transmitted by writing to the TXD register. When a byte has been successfully transmitted the UART will generate a TXDRDY event after which a new byte can be written to the TXD register. A UART transmission sequence is stopped immediately by triggering the STOPTX task.

If flow control is enabled a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in *Figure 172: UART transmission* on page 594. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended. For more information, see *Suspending the UART* on page 595.

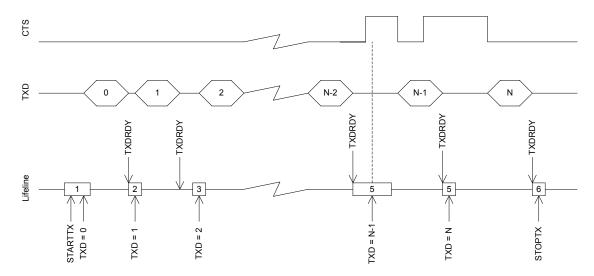


Figure 172: UART transmission

49.5 Reception

A UART reception sequence is started by triggering the STARTRX task.

The UART receiver chain implements a FIFO capable of storing six incoming RXD bytes before data is overwritten. Bytes are extracted from this FIFO by reading the RXD register. When a byte is extracted from the FIFO a new byte pending in the FIFO will be moved to the RXD register. The UART will generate an RXDRDY event every time a new byte is moved to the RXD register.

When flow control is enabled, the UART will deactivate the RTS signal when there is only space for four more bytes in the receiver FIFO. The counterpart transmitter is therefore able to send up to four bytes after the RTS signal is deactivated before data is being overwritten. To prevent overwriting data in the FIFO, the counterpart UART transmitter must therefore make sure to stop transmitting data within four bytes after the RTS line is deactivated.



The RTS signal will first be activated again when the FIFO has been emptied, that is, when all bytes in the FIFO have been read by the CPU, see *Figure 173: UART reception* on page 595.

The RTS signal will also be deactivated when the receiver is stopped through the STOPRX task as illustrated in *Figure 173: UART reception* on page 595. The UART is able to receive four to five additional bytes if they are sent in succession immediately after the RTS signal has been deactivated. This is possible because the UART is, even after the STOPRX task is triggered, able to receive bytes for an extended period of time dependent on the configured baud rate. The UART will generate a receiver timeout event (RXTO) when this period has elapsed.

To prevent loss of incoming data the RXD register must only be read one time following every RXDRDY event.

To secure that the CPU can detect all incoming RXDRDY events through the RXDRDY event register, the RXDRDY event register must be cleared before the RXD register is read. The reason for this is that the UART is allowed to write a new byte to the RXD register, and therefore can also generate a new event, immediately after the RXD register is read (emptied) by the CPU.

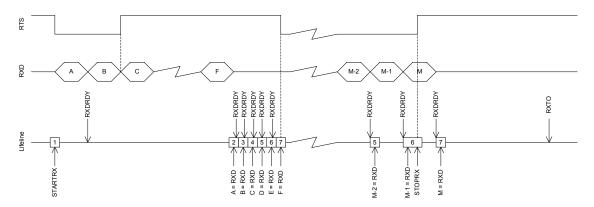


Figure 173: UART reception

As indicated in occurrence 2 in the figure, the RXDRDY event associated with byte B is generated first after byte A has been extracted from RXD.

49.6 Suspending the UART

The UART can be suspended by triggering the SUSPEND task.

SUSPEND will affect both the UART receiver and the UART transmitter, i.e. the transmitter will stop transmitting and the receiver will stop receiving. UART transmission and reception can be resumed, after being suspended, by triggering STARTTX and STARTRX respectively.

Following a SUSPEND task, an ongoing TXD byte transmission will be completed before the UART is suspended.

When the SUSPEND task is triggered, the UART receiver will behave in the same way as it does when the STOPRX task is triggered.

49.7 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.



49.8 Using the UART without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

49.9 Parity configuration

When parity is enabled, the parity will be generated automatically from the even parity of TXD and RXD for transmission and reception respectively.

49.10 Registers

Table 119: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40002000	UART	UART0	Universal asynchronous receiver/		Deprecated
			transmitter		

Table 120: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS_STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_SUSPEND	0x01C	Suspend UART
EVENTS_CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_RXDRDY	0x108	Data received in RXD
EVENTS_TXDRDY	0x11C	Data sent from TXD
EVENTS_ERROR	0x124	Error detected
EVENTS_RXTO	0x144	Receiver timeout
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x480	Error source
ENABLE	0x500	Enable UART
PSEL.RTS	0x508	Pin select for RTS
PSEL.TXD	0x50C	Pin select for TXD
PSEL.CTS	0x510	Pin select for CTS
PSEL.RXD	0x514	Pin select for RXD
RXD	0x518	RXD register
TXD	0x51C	TXD register
BAUDRATE	0x524	Baud rate. Accuracy depends on the HFCLK source selected.
CONFIG	0x56C	Configuration of parity and hardware flow control

49.10.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number		31	30 2	9 2	8 27	7 26	25	24	23 2	22 2	21 2	0 19	9 18	17	16	15 :	14 1	.3 1	2 1	10	9	8	7	6	5	4	3 2	1	0
Id																										В	Α		
Reset 0x00000000		0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Id RW Field	Value Id	Val	ue						Des	crip	tio	1																	

A RW CTS_STARTRX

Shortcut between CTS event and STARTRX task



Bit	numb	er		3	1 30	29	28 2	27 2	26 2	5 2	24 2	23 2	2 2	1 20	0 1	9 1	8 17	16	15	14	13	12	11	10	9	8 7	7 6	5 5	4	3	2	1 0
Id																													В	Α		
Res	et 0x(0000000		0	0	0	0	0	0 () (0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0 0
Id	RW	Field	Value Id	٧	alue						C	Desc	cript	tion	1																	
											S	ee	EVE	NTS	s_ <i>C</i>	TS a	nd	TAS	KS_	STA	RTI	RX										
			Disabled	0								Disa	ble	sho	rtcı	ut																
			Enabled	1							Е	nak	ole s	shor	rtcu	it																
В	RW	NCTS_STOPRX									S	hor	tcu	t be	etwe	een	NC	TS e	ver	it ar	nd S	TO	PRX	tas	k							
											S	ee.	EVE	NTS	S_ <i>N</i>	CTS	an	d <i>T</i> /	SKS	_57	ОР	RX										
			Disabled	0							C	Disa	ble	sho	rtcı	ut																
			Enabled	1							Е	nak	ole s	shor	rtcu	ıt																

49.10.2 INTENSET

Address offset: 0x304

Enable interrupt

	able interrupt			
Bit n	umber		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	2 1
Id			F E D (СВ
Rese	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
Id	RW Field	Value Id	Value Description	
Α	RW CTS		Write '1' to Enable interrupt for CTS event	
			See EVENTS_CTS	
		Set	1 Enable	
		Disabled	0 Read: Disabled	
		Enabled	1 Read: Enabled	
В	RW NCTS		Write '1' to Enable interrupt for NCTS event	
			See EVENTS_NCTS	
		Set	1 Enable	
		Disabled	0 Read: Disabled	
		Enabled	1 Read: Enabled	
С	RW RXDRDY		Write '1' to Enable interrupt for RXDRDY event	
		Set	See EVENTS_RXDRDY 1 Enable	
		Disabled	0 Read: Disabled	
		Enabled	1 Read: Enabled	
D	RW TXDRDY	Lilabica	Write '1' to Enable interrupt for TXDRDY event	
_	NW INDICE		·	
			See EVENTS_TXDRDY	
		Set	1 Enable	
		Disabled	0 Read: Disabled	
_	DW FDDOD	Enabled	1 Read: Enabled	
E	RW ERROR		Write '1' to Enable interrupt for ERROR event	
			See EVENTS_ERROR	
		Set	1 Enable	
		Disabled	0 Read: Disabled	
		Enabled	1 Read: Enabled	
F	RW RXTO		Write '1' to Enable interrupt for RXTO event	
			See EVENTS_RXTO	
		Set	1 Enable	
		Disabled	0 Read: Disabled	
		Enabled	1 Read: Enabled	

49.10.3 INTENCLR

Address offset: 0x308 Disable interrupt



Bit	numbe	er		31	30 2	9 2	8 27	7 26	25	24	23	3 22 2	21 2	0 1	9 1	8 1	7 1	6 1	15 :	14	13 :	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																F									Ε		D				(2 1	3 A
Res	et 0x0	0000000		0	0	0 (0 0	0	0	0	0	0 (0 (0	0 (0) (כ	0	0	0	0	0	0	0	0	0	0	0	0	0) (0 0
Id	RW	Field	Value Id	Val	ue						De	escrip	tio	n																			
Α	RW	CTS									W	rite '1	l' to) Di	sab	e ir	itei	rru	pt f	or	CTS	ev	ent	t									
											Se	ee <i>EVE</i>	NT.	s_0	CTS																		
			Clear	1							Di	isable																					
			Disabled	0							Re	ead: D	isal	ble	d																		
			Enabled	1							Re	ead: E	nab	olec	ł																		
В	RW	NCTS									W	rite '1	l' to	Di	sab	e ir	itei	ru	pt f	or	NCT	S e	eve	nt									
											Se	ee <i>EVE</i>	NT.	'S_1	VCT.	5																	
			Clear	1							Di	isable																					
			Disabled	0							Re	ead: D	isal	ble	d																		
			Enabled	1							Re	ead: E	nab	olec	i																		
С	RW	RXDRDY									W	rite '1	l' to	Di	sab	e ir	itei	rru	pt f	or	RXC	RD	Υe	ever	nt								
											Se	ee <i>EVE</i>	NT.	S_F	RXD	RDY																	
			Clear	1							Di	isable																					
			Disabled	0							Re	ead: D	isal	ble	d																		
			Enabled	1							Re	ead: E	nab	olec	i																		
D	RW	TXDRDY									W	rite '1	L' to	Di	sab	e ir	itei	rru	pt f	or	TXD	RD	Υe	ever	it								
											Se	ee <i>EVE</i>	NT.	·s_1	XD	RDY																	
			Clear	1							Di	isable																					
			Disabled	0							Re	ead: D	isal	ble	d																		
			Enabled	1							Re	ead: E	nab	olec	i																		
Ε	RW	ERROR									W	rite '1	l' to	Di	sab	e ir	itei	rru	pt f	or	ERR	OR	ev	ent									
											Se	ee <i>EVE</i>	NT.	S_E	RR)R																	
			Clear	1							Di	isable																					
			Disabled	0							Re	ead: D	isal	ble	d																		
			Enabled	1							Re	ead: E	nab	olec	i																		
F	RW	RXTO									W	rite '1	l' to	Di	sab	e ir	tei	ru	pt f	or	RXT	0 6	eve	nt									
											Se	ee <i>EVE</i>	NT.	S_F	RXT)																	
			Clear	1							Di	isable																					
			Disabled	0							Re	ead: D	isal	ble	d																		
			Enabled	1							Re	ead: E	nab	olec	ł																		

49.10.4 ERRORSRC

Address offset: 0x480

Error source

Bitı	numbe	er		31	30 :	29	28 2	27 :	26 2	25 2	24 :	23 22	2 21	20	19	18	17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																														D (В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	ue						- 1	Desc	ripti	on																		
Α	RW	OVERRUN									(Over	run	erro	or																	
											,	A sta	rt bi	t is	rece	eive	ed v	vhil	e tł	ne p	revi	ous	dat	a sti	II lie	es ir	n RX	D.				
											((Prev	ious	da	ta is	s los	st.)															
			NotPresent	0							ı	Read	: err	or r	not	pre	sen	t														
			Present	1							1	Read	: err	or p	ores	ent	t															
В	RW	PARITY									-	Parit	y err	or																		
												A cha	aract	er v	with	n ha	nd n	arit	v is	rec	eive	i he	f HV	V na	ritv	che	-ck	ic				
															••••		iu p	uiii	yı			.u, i		• pu	,	Cit	CICI	.5				
											(enab	led.																			
			NotPresent	0							ı	Read	: err	or r	not	pre	sen	t														
			Present	1							-	Read	: err	or p	ores	ent	t															
С	RW	FRAMING									-	Fram	ing	erro	or o	ccu	rred	t														



Bit number	31	30 29 28 27 2	6 25 24	23 22 21 2	0 19 18	3 17 1	6 15 1	14 13 1	2 11	10 9	9 8	7	6	5 4	3	2 1	0
Id															D	СВ	Α
Reset 0x00000000	0	0 0 0 0	0 0	0 0 0 0	0 0	0 0	0 0	0 0	0 0	0 (0 0	0	0	0 0	0	0 0	0
Id RW Field Valu	ie Id Va	alue		Description	1												
				A valid stop	bit is n	ot de	tected	d on the	seri	al da	ta in	put	after	all			
				bits in a cha	aracter	have l	been i	receive	d.								
Noti	Present 0			Read: error	not pre	esent											
Pres	ent 1			Read: error	presen	nt											
D RW BREAK				Break cond	ition												
				The serial o	lata inp	ut is '(o' for l	onger	han t	the le	engt	n of	a da	ta			
				frame. (The	data fi	rame l	ength	is 10 b	its w	ithou	ıt pa	rity	bit, a	and			
				11 bits with	parity	bit.).											
Noti	Present 0			Read: error	not pre	esent											
Pres	ent 1			Read: error	presen	nt											

49.10.5 ENABLE

Address offset: 0x500

Enable UART

Bit nu	umbe	r		33	1 30	29	28	3 2	7 20	6 2	5 2	4 2	2 2	22 2	21 :	20	19	18	17	16	15	14	13	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																																	Α	Α	А А
Rese	t 0x0	000000		0	0	0	0	0	0) (0 0) (0 (0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	9						C)es	crip	tio	n																			
Α	RW	ENABLE										Е	nal	ble	or	disa	able	e U	AR	Г															
			Disabled	0								C	Disa	ble	UA	ART																			
			Enabled	4								Е	nal	ble	UA	RT																			

49.10.6 PSEL.RTS

Address offset: 0x508 Pin select for RTS

Bit r	umbe	r		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	вааа
Rese	t OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

49.10.7 PSEL.TXD

Address offset: 0x50C Pin select for TXD

Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	вааа
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect



49.10.8 PSEL.CTS

Address offset: 0x510 Pin select for CTS

Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ваааа
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

49.10.9 PSEL.RXD

Address offset: 0x514 Pin select for RXD

Bit r	umbe	er		31	30	29	28 2	27 :	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	.0 9	9 8	3 .	7 6	5 5	5 4	3	2	1	0
Id				С																									E	3 A	. A	Α	Α	Α
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	L :	1 1	1 1	l 1	1	1	1	1
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	on																			
Α	RW	PIN		[0.	31]							Pin	nu	mb	er																			
В	RW	PORT		[0.	1]							Por	t n	uml	ber																			
С	RW	CONNECT										Cor	nne	ctio	n																			
			Disconnected	1								Dis	con	nec	ct																			
			Connected	0								Cor	nne	ct																				

49.10.10 RXD

Address offset: 0x518

RXD register

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
ld RW Field	Value Id	Value	Description
A R RXD			RX data received in previous transfers, double buffered

49.10.11 TXD

Address offset: 0x51C

TXD register

Bit	numb	er		31 30	29	28 2	7 26	25	24 :	23 2	2 21	L 20	19	18 1	17 1	16 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4 3	2	1	0
Id																								Α	Α.	Α	A A	A	Α	Α
Res	et 0x0	0000000		0 0	0	0 0	0	0	0	0 (0 0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Value	:				ı	Desc	ript	ion																		
Α	W	TXD												nsfe	erre	d														

49.10.12 BAUDRATE

Address offset: 0x524

Baud rate. Accuracy depends on the HFCLK source selected.



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x04000000	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 &$
Id RW Field Value Id	Value Description
A RW BAUDRATE	Baud rate
Baud1200	0x0004F000 1200 baud (actual rate: 1205)
Baud2400	0x0009D000 2400 baud (actual rate: 2396)
Baud4800	0x0013B000 4800 baud (actual rate: 4808)
Baud9600	0x00275000 9600 baud (actual rate: 9598)
Baud14400	0x003B0000 14400 baud (actual rate: 14414)
Baud19200	0x004EA000 19200 baud (actual rate: 19208)
Baud28800	0x0075F000 28800 baud (actual rate: 28829)
Baud31250	0x00800000 31250 baud
Baud38400	0x009D5000 38400 baud (actual rate: 38462)
Baud56000	0x00E50000 56000 baud (actual rate: 55944)
Baud57600	0x00EBF000 57600 baud (actual rate: 57762)
Baud76800	0x013A9000 76800 baud (actual rate: 76923)
Baud115200	0x01D7E000 115200 baud (actual rate: 115942)
Baud230400	0x03AFB000 230400 baud (actual rate: 231884)
Baud250000	0x04000000 250000 baud
Baud460800	0x075F7000 460800 baud (actual rate: 470588)
Baud921600	0x0EBED000 921600 baud (actual rate: 941176)
Baud1M	0x10000000 1Mega baud
	,

49.10.13 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

Bit n	umbe	er		31	30 2	29 2	28 2	7 2	6 25	5 24	4 23	3 22	2 21	20	19	18	17	16	15	14	13	12	11 :	10 9	9 8	7	6	5	4	3	2	1 0
Id																														В	В	ВА
Rese	t 0x0	0000000		0	0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						D	esci	ripti	on																		
Α	RW	HWFC									Н	ard	war	e flo	w c	con	trol															
			Disabled	0							D	isab	led																			
			Enabled	1							Er	nabl	led																			
В	RW	PARITY									Pa	arity	/																			
			Excluded	0x0)						E	clu	de p	oarii	ty b	it																
			Included	0x7	7						In	clu	de p	arit	y bi	t																

49.11 Electrical specification

49.11.1 UART electrical specification

Symbol	Description	Min.	Тур.	Max.	Units
f _{UART}	Baud rate for UART ³⁹ .			1000	kbps
I _{UART1M}	Run current at max baud rate.		55		μΑ
I _{UART115k}	Run current at 115200 bps.		55		μΑ
I _{UART1k2}	Run current at 1200 bps.		55		μΑ
I _{UART,IDLE}	Idle current for UART		1		μΑ
t _{UART,CTSH}	CTS high time	1			μs
t _{UART,START}	Time from STARTRX/STARTTX task to transmission started		1		μs

High baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.



50 ACL — Access control lists

The Access control lists (ACL) peripheral is designed to assign and enforce access permissions to different regions of the on-chip flash memory map.

Flash memory regions can be assigned individual ACL permission schemes. The following registers are involved:

- PERM register, where the permissions are configured.
- ADDR register, where the word-aligned start address for the flash page is defined.
- SIZE register, where the size of the region the permissions are applied to is determined.

Important: The size of the region in bytes is restricted to a multiple of the flash page size. See the *Memory* on page 20 chapter for more information.

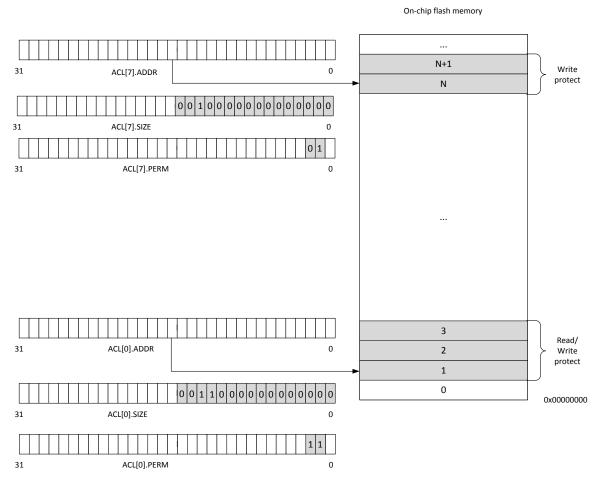


Figure 174: Protected regions of on-chip flash memory

There are four defined ACL permission schemes, with different combinations of read/write permissions:

Table 121: Permission schemes

Read	Write	Protection description
0	0	No protection. Entire region can be executed, read, written or erased.
0	1	Region can be executed and read, but not written or erased.
1	0	Region can be written and erased, but not executed or read.
1	1	Region is locked for all access until next reset

Important: If a permission violation to a protected region is detected by the ACL peripheral, the request is blocked and a Bus Fault exception is triggered.



Access control to a configured region is enforced by the hardware two CPU clock cycles after the ADDR, SIZE, and PERM registers for an ACL instance have been successfully written. The protection is only enforced if a valid start address of the flash page boundary is written into the ADDR register, and the values of the SIZE and PERM registers are not zero.

The ADDR, SIZE, and PERM registers can only be written once. All ACL configuration registers are cleared on reset (by resetting the device from any reset source), which is also the only way of clearing the configuration registers. To ensure that the desired permission schemes are always enforced by the ACL peripheral, the device boot sequence must perform the necessary configuration.

Debugger read access to a read-protected region will be Read-As-Zero (RAZ), while debugger write access to a write-protected region will be Write-Ignored (WI).

50.1 Registers

Table 122: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001E000	ACL	ACL	Access control lists	

Table 123: Register Overview

Register	Offset	Description	
ACL[0].ADDR	0x800	Configure the word-aligned start address of region 0 to protect	
ACL[0].SIZE	0x804	Size of region to protect counting from address ACL[0].ADDR. Write '0' as no effect.	
ACL[0].PERM	0x808	Access permissions for region 0 as defined by start address ACL[0].ADDR and size ACL[0].SIZE	
	0x80C		Reserved
ACL[1].ADDR	0x810	Configure the word-aligned start address of region 1 to protect	
ACL[1].SIZE	0x814	Size of region to protect counting from address ACL[1].ADDR. Write '0' as no effect.	
ACL[1].PERM	0x818	Access permissions for region 1 as defined by start address ACL[1].ADDR and size ACL[1].SIZE	
	0x81C		Reserved
ACL[2].ADDR	0x820	Configure the word-aligned start address of region 2 to protect	
ACL[2].SIZE	0x824	Size of region to protect counting from address ACL[2].ADDR. Write '0' as no effect.	
ACL[2].PERM	0x828	Access permissions for region 2 as defined by start address ACL[2].ADDR and size ACL[2].SIZE	
	0x82C		Reserved
ACL[3].ADDR	0x830	Configure the word-aligned start address of region 3 to protect	
ACL[3].SIZE	0x834	Size of region to protect counting from address ACL[3].ADDR. Write '0' as no effect.	
ACL[3].PERM	0x838	Access permissions for region 3 as defined by start address ACL[3].ADDR and size ACL[3].SIZE	
	0x83C		Reserved
ACL[4].ADDR	0x840	Configure the word-aligned start address of region 4 to protect	
ACL[4].SIZE	0x844	Size of region to protect counting from address ACL[4].ADDR. Write '0' as no effect.	
ACL[4].PERM	0x848	Access permissions for region 4 as defined by start address ACL[4].ADDR and size ACL[4].SIZE	
	0x84C		Reserved
ACL[5].ADDR	0x850	Configure the word-aligned start address of region 5 to protect	
ACL[5].SIZE	0x854	Size of region to protect counting from address ACL[5].ADDR. Write '0' as no effect.	
ACL[5].PERM	0x858	Access permissions for region 5 as defined by start address ACL[5].ADDR and size ACL[5].SIZE	
	0x85C		Reserved
ACL[6].ADDR	0x860	Configure the word-aligned start address of region 6 to protect	
ACL[6].SIZE	0x864	Size of region to protect counting from address ACL[6].ADDR. Write '0' as no effect.	
ACL[6].PERM	0x868	Access permissions for region 6 as defined by start address ACL[6].ADDR and size ACL[6].SIZE	
	0x86C		Reserved
ACL[7].ADDR	0x870	Configure the word-aligned start address of region 7 to protect	
ACL[7].SIZE	0x874	Size of region to protect counting from address ACL[7].ADDR. Write '0' as no effect.	
ACL[7].PERM	0x878	Access permissions for region 7 as defined by start address ACL[7].ADDR and size ACL[7].SIZE	
	0x87C		Reserved

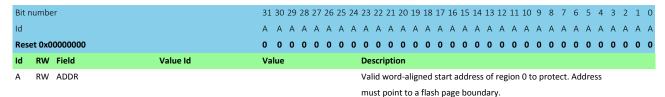
50.1.1 ACL[0].ADDR

Address offset: 0x800



Configure the word-aligned start address of region 0 to protect

This register can only be written once.



50.1.2 ACL[0].SIZE

Address offset: 0x804

Size of region to protect counting from address ACL[0].ADDR. Write '0' as no effect.

This register can only be written once.

Bit r	numbe	er		3	1 30	29	28	8 2	7 2	6 2	5 2	24 2	23 2	22 :	21 2	0 1	19 1	18 1	L7 1	6 1	15 1	4 1	13 :	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				Д	. A	Α	. A	. 4	Δ Δ	\ <i>A</i>	Δ ,	A	Α	Α	Α	Α,	Α.	Α.	Α,	Δ.	Α.	Δ	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et OxO	0000000		0	0	0	0	0	0) (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	alue	:							Des	crip	otio	n																				
Α	RW	SIZE				9	Size	of	flas	h re	egic	n O	in	byt	es.	Mu	st l	oe a	a m	ulti	ple	of	the	fla	sh											
						r	าลต	e si	76																											

50.1.3 ACL[0].PERM

Address offset: 0x808

Access permissions for region 0 as defined by start address ACL[0].ADDR and size ACL[0].SIZE

This register can only be written once.

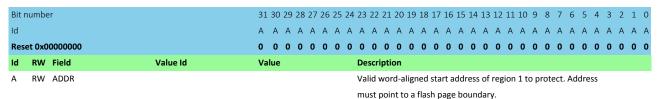
Bit nu	ımbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	1 13	3 1	2 1	1 1	0 9	8	7	6	5	4	3	2	1	0
Id																																	С	В	
Reset	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) () () (0	0	0	0	0	0	0	0	0	0
ld I	RW	Field	Value Id	Va	lue							De	scr	ipti	on																				
В	RW	WRITE										Co	nfig	gure	e w	rite	an	d e	rase	e pe	ern	niss	ion	ıs f	or re	egio	n 0	. Wı	rite	'0'	has	5			
												no	eff	ect																					
			Enable	0								ΑII	ow	wr	ite	and	er	ase	ins	tru	ctio	ns	to	reg	ion	0									
			Disable	1								Blo	ock	wri	te a	and	era	se	ins	tru	ctic	ns	to	reg	ion	0									
C	RW	READ										Со	nfig	gure	e re	ad	per	mis	sio	ns	for	reg	oig	า 0.	Wr	ite '	0' h	ıas ı	10 6	effe	ct.				
			Enable	0								All	ow	rea	ıd iı	nstr	uct	ion	s to	re	gio	n 0)												
			Disable	1								Blo	ock	rea	d ir	nstr	uct	ion	s to	re	gio	n 0													

50.1.4 ACL[1].ADDR

Address offset: 0x810

Configure the word-aligned start address of region 1 to protect

This register can only be written once.



50.1.5 ACL[1].SIZE

Address offset: 0x814

Size of region to protect counting from address ACL[1].ADDR. Write '0' as no effect.



This register can only be written once.

Bit	numbe	er		31	L 30	29	28	27	7 26	25	24	23	22	21	20 :	19 1	8 17	7 16	15	14	13	12	11 1	.0	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A .	А А	Α	Α	Α	Α	Α	A	Δ.	Α	Α	Α	Α	Α	Α	A	۱ ۸	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	alue	:						De	scri	ptic	n																		
Α	RW	SIZE										Siz	e of	flas	sh r	egic	n 1	n b	ytes	. M	ust	be a	ı mı	ılti	ple	of ·	the	fla	sh				
										pag	ge s	ize.																					

50.1.6 ACL[1].PERM

Address offset: 0x818

Access permissions for region 1 as defined by start address ACL[1].ADDR and size ACL[1].SIZE

This register can only be written once.

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 1	19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			СВ
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value Description	
B RW WRITE		Configure writ	ite and erase permissions for region 1. Write '0' has
		no effect.	
	Enable	0 Allow write ar	nd erase instructions to region 1
	Disable	1 Block write an	nd erase instructions to region 1
C RW READ		Configure rea	d permissions for region 1. Write '0' has no effect.
	Enable	0 Allow read ins	structions to region 1
	Disable	1 Block read ins	structions to region 1

50.1.7 ACL[2].ADDR

Address offset: 0x820

Configure the word-aligned start address of region 2 to protect

This register can only be written once.

Bit nu	ımbe	er		31	30	31 30 29 28 27 3 A A A A A											17	16	15	14 1	13 12	2 11	10	9	8	7	6	5	4	3 2	2 1	1 0	
Id			,	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	Α	Α	Α	Α	Α	А А	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	4 A	
Rese	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 () (0 0	
ld	RW	Field	Value Id	Va	lue							Des	crip	otio	1																		ı
A	RW	ADDR										Val	id w	ord/	-alig	ned	sta	rt a	ddre	ess (of re	gior	2 t	o pr	rote	ct.	Add	dres	SS				1
				must point to a flash page boundary.																													

50.1.8 ACL[2].SIZE

Address offset: 0x824

Size of region to protect counting from address ACL[2].ADDR. Write '0' as no effect.

This register can only be written once.

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 1	18 1	17 1	.6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	2 1	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ ,	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	۱ ۸	4 Α	Ą
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0 () (0 ()
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	SIZE										Siz	e of	fla	sh r	egic	n 2	! in l	byte	es. N	∕lus	t be	a m	nulti	ple	of	the	flas	sh					7
												pa	ge s	ize.																				

50.1.9 ACL[2].PERM

Address offset: 0x828

Access permissions for region 2 as defined by start address ACL[2].ADDR and size ACL[2].SIZE



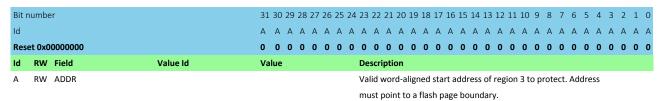
Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		СВ
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
B RW WRITE		Configure write and erase permissions for region 2. Write '0' has
		no effect.
	Enable	0 Allow write and erase instructions to region 2
	Disable	1 Block write and erase instructions to region 2
C RW READ		Configure read permissions for region 2. Write '0' has no effect.
	Enable	0 Allow read instructions to region 2
	Disable	1 Block read instructions to region 2

50.1.10 ACL[3].ADDR

Address offset: 0x830

Configure the word-aligned start address of region 3 to protect

This register can only be written once.

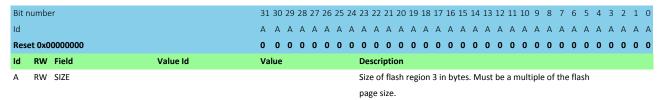


50.1.11 ACL[3].SIZE

Address offset: 0x834

Size of region to protect counting from address ACL[3].ADDR. Write '0' as no effect.

This register can only be written once.



50.1.12 ACL[3].PERM

Address offset: 0x838

Access permissions for region 3 as defined by start address ACL[3].ADDR and size ACL[3].SIZE

	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
		СВ
	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Value Id	Value	Description
		Configure write and erase permissions for region 3. Write '0' has
		no effect.
Enable	0	Allow write and erase instructions to region 3
Disable	1	Block write and erase instructions to region 3
		Configure read permissions for region 3. Write '0' has no effect.
Enable	0	Allow read instructions to region 3
Disable	1	Block read instructions to region 3
	Enable Disable Enable	Value Id Value Enable 0 Disable 0



50.1.13 ACL[4].ADDR

Address offset: 0x840

Configure the word-aligned start address of region 4 to protect

This register can only be written once.

Bitı	numb	er		31	30	29	28	27	26	25	24	23	22	21	20 1	L9 1	.8 1	7 16	5 15	14	13	12	11 :	10	9	8	7	6	5 -	4 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 4	A A	Α	Α	Α	Α	Α	A	Α	Α	Α	Α.	Α.	ДД	A	Α	Α
Res	et Ox(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																		
Α	RW	ADDR										Val	lid v	vord	d-ali	gne	d st	art	addı	ress	of ı	regi	on 4	1 to	pr	ote	ct. /	٩dd	res	S			Τ
												mι	ıst p	oin	t to	a fl	ash	pag	e bo	ound	dary	<i>'</i> .											

50.1.14 ACL[4].SIZE

Address offset: 0x844

Size of region to protect counting from address ACL[4].ADDR. Write '0' as no effect.

This register can only be written once.

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20 1	19 1	8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	A /	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	ΑА	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	SIZE										Siz	e of	flas	h re	egic	n 4	in b	yte	s. N	1ust	be	a n	nult	iple	of	the	fla	sh				
												pag	ge s	ize.																			

50.1.15 ACL[4].PERM

Address offset: 0x848

Access permissions for region 4 as defined by start address ACL[4].ADDR and size ACL[4].SIZE

This register can only be written once.

Bit number		31	30	29 :	28 2	27 2	26 2	5 2	24 2	23 :	22 :	21 2	0 :	19 1	.8 1	l7 1	6 1	5 1	.4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																													(C I	В
Reset 0x00000000		0	0	0	0	0	0 ()	0	0	0	0	0	0	0	0 () (0 (0 () () (0	0	0	0	0	0	0	0	0 (0 0
ld RW Field	Value Id	Va	lue							Des	crip	otio	n																		
B RW WRITE									(Con	ıfigı	ıre	wri	te a	nd	era	se p	eri	niss	sion	s fo	r re	gio	n 4.	Wr	ite '	0' h	ıas			
									r	10 6	effe	ct.																			
	Enable	0							A	Allo	w v	vrit	e a	nd e	ras	e in	str	ucti	ons	to	reg	ion	4								
	Disable	1							E	Bloo	ck v	vrite	a e	nd e	ras	e in	strı	ıcti	ons	to	reg	on 4	4								
C RW READ									C	Con	nfigu	ıre	rea	d pe	erm	issi	ons	fo	r re	gior	ı 4.	Wri	te '	0' h	as r	no e	ffec	t.			
	Enable	0							A	Allo	w r	ead	in	stru	ctic	ns 1	to r	egi	on 4	1											
	Disable	1							E	3lo	ck r	ead	ins	tru	ctio	ns t	o r	egi	on 4	ļ											

50.1.16 ACL[5].ADDR

Address offset: 0x850

Configure the word-aligned start address of region 5 to protect

Bit	numbe	er		31	. 30	29	28	27	7 26	25	5 24	23	22	21	20 1	9 1	8 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 4	4 A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	4 4	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0
Id	RW	Field	Value Id	Va	lue	:						De	scrip	otic	n																		
Α	RW	ADDR										Val	lid w	oro	d-ali	gne	d st	art a	ddr	ess	of	regi	on	5 to	pr	ote	ct.	Add	dres	SS			
														_:		_ £1.	ash i																



50.1.17 ACL[5].SIZE

Address offset: 0x854

Size of region to protect counting from address ACL[5].ADDR. Write '0' as no effect.

This register can only be written once.

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21 :	20 1	9 1	8 17	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	. Α	A
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																		
Α	RW	SIZE										Siz	e of	flas	h re	gio	n 5 i	in b	ytes	. M	ust	be	a m	ulti	ple	of t	the	flas	sh				
												pag	ge si	ize.																			

50.1.18 ACL[5].PERM

Address offset: 0x858

Access permissions for region 5 as defined by start address ACL[5].ADDR and size ACL[5].SIZE

This register can only be written once.

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	С	В	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
В	RW	WRITE										Coi	nfig	ure	wr	ite	and	l er	ase	pe	mi	ssio	ons	for	re	gior	ո 5.	Wr	ite '	0' h	nas				
												no	eff	ect.																					
			Enable	0								Allo	wc	writ	te a	nd	era	se i	nst	ruc	tioi	ns t	o re	egic	on 5	5									
			Disable	1								Blo	ck v	writ	e a	nd (era	se i	nst	uct	ior	ıs t	o re	gic	n 5	,									
С	RW	READ										Coi	nfig	ure	rea	ad p	err	nis	sior	s fo	or r	egi	on !	5. V	Vrit	e '0)' ha	s n	o e	ffec	ct.				
			Enable	0								Allo	ow	read	d in	strı	ucti	ons	to	reg	ior	5													
			Disable	1								Blo	ck ı	read	d in	stru	ıcti	ons	to	reg	ion	5													

50.1.19 ACL[6].ADDR

Address offset: 0x860

Configure the word-aligned start address of region 6 to protect

This register can only be written once.

Bit r	iumbe	er		31	30	29	28	27	7 26	6 2	25 2	24 2	23 2	22 2	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1)
Id				Α	Α	Α	Α	Α	A		Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ.	Α.	٨
Res	et OxC	0000000		0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	Va	lue							ı	Des	crip	otic	n																				
Α	RW	ADDR										١	/ali	d w	oro	d-al	ign	ed :	star	t a	ddr	ess	of	reg	ion	6 t	о р	rote	ct.	Ado	dres	SS				
													~	+ n	oin	+ + ~	- a f	laci	h pa	000	ho	una	dan	,												

50.1.20 ACL[6].SIZE

Address offset: 0x864

Size of region to protect counting from address ACL[6].ADDR. Write '0' as no effect.

Bit r	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20 1	9 1	8 17	7 16	15	14	13	12	11 :	LO	9	8	7	6	5	4	3 2	! :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 4	4 A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A		А А
Res	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
Id	RW	Field	Value Id	Va	lue							Des	scri	otic	n																		
Α	RW	SIZE										Size	e of	flas	sh re	gio	n 6 i	n b	ytes	. M	ust	be a	m	ulti	ple	of 1	the	flas	sh				
												pag	e si	ze.																			



50.1.21 ACL[6].PERM

Address offset: 0x868

Access permissions for region 6 as defined by start address ACL[6].ADDR and size ACL[6].SIZE

This register can only be written once.

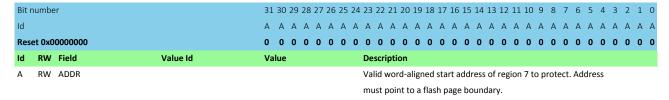
Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		C B
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
B RW WRITE		Configure write and erase permissions for region 6. Write '0' has
		no effect.
	Enable	0 Allow write and erase instructions to region 6
	Disable	1 Block write and erase instructions to region 6
C RW READ		Configure read permissions for region 6. Write '0' has no effect.
	Enable	0 Allow read instructions to region 6
	Disable	1 Block read instructions to region 6

50.1.22 ACL[7].ADDR

Address offset: 0x870

Configure the word-aligned start address of region 7 to protect

This register can only be written once.



50.1.23 ACL[7].SIZE

Address offset: 0x874

Size of region to protect counting from address ACL[7].ADDR. Write '0' as no effect.

This register can only be written once.

Bit r	umbe	er		31	. 30	29	28	3 2	7 2	6 2	25 2	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Δ	Α Α	۱ ۱	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α	Α	Α
Res	t OxO	0000000		0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue	:							Des	cri	ptic	on																				
Α	RW	SIZE	Size of flash region 7 in bytes. Must be										a m	nult	iple	of	the	fla	sh																	
													page size.																							

50.1.24 ACL[7].PERM

Address offset: 0x878

Access permissions for region 7 as defined by start address ACL[7].ADDR and size ACL[7].SIZE

Bit r	iumbe	er		31	L 30	29	28	27	26	25	24	23	22 :	21 2	20 1	19 1	8 1	.7 1	6 1	.5 1	4 1	3 1	2 1:	l 10	9	8	7	6	5	4 3	3 2	1	. 0
Id																															С	В	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0 (0 (0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Value D							Description																						
В	RW	WRITE	/RITE								Configure write and erase permissions for region 7. Write '0' has																						
				r						no effect.																							
			Enable	0						Allo	w v	writ	e ar	nd e	ras	e in	str	ucti	ons	to	regi	on 7	,										
			Disable	1								Block write and erase instructions to region 7																					



Bitı	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16 1	L5 1	L4 1	13 1	2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id																															(C I	В
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																		
С	RW	READ										Coi	nfig	ure	rea	ıd p	ern	niss	ion	s fo	r re	gio	n 7.	Wri	te '	0' h	as n	o e	ffec	t.			
			Enable	0								Allo	ow	rea	d in	strı	ıctio	ons	to i	egi	on	7											
			Disable	1								Blo	ck ı	read	d in	stru	ctic	ons	to r	egi	on :	7											



51 USBD — Universal serial bus device

The USB device controller (USBD) implements a full speed USB device function that meets 2.0 revision of the USB specification.

Listed here are the main features for USBD:

- Fully compliant to Universal Serial Bus Specification Revision 2.0 Full Speed part, including following Engineering Change Notices (ECNs) issued by USB Implementers Forum:
 - Pull-up/pull-down Resistors ECN
 - 5V Short Circuit Withstand Requirement Change ECN
- Implements a USB FS (full speed, 12 Mbps) device
- USB device stack available in the Nordic SDK
- On-chip transceiver
- Software controlled on-chip pull-up on D+
- 2 control (1 IN, 1 OUT), 14 bulk/interrupt (7 IN, 7 OUT) and 2 ISO (1 IN, 1 OUT) endpoints
- Supports double buffering for isochronous endpoint (IN/OUT)
- EasyDMA for all data transfers
- 64 bytes buffer size for each bulk/interrupt endpoint
- Up to 1023 bytes buffer size for ISO endpoints

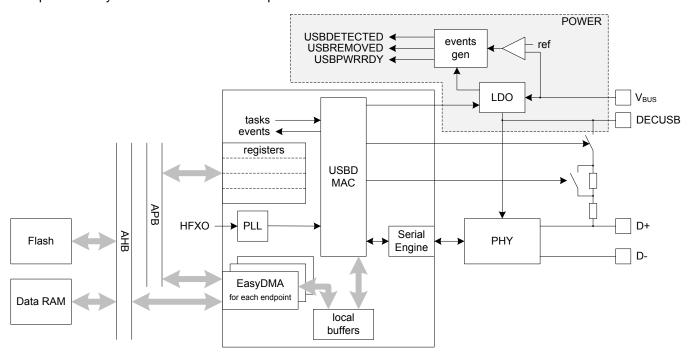


Figure 175: USB block diagram

51.1 USB device states

The behaviour of a USB device can be modelled through a state diagram.

Chapter 9 USB Device Framework in the USB specification revision 2.0 defines a number of states for a USB device, illustrated below.



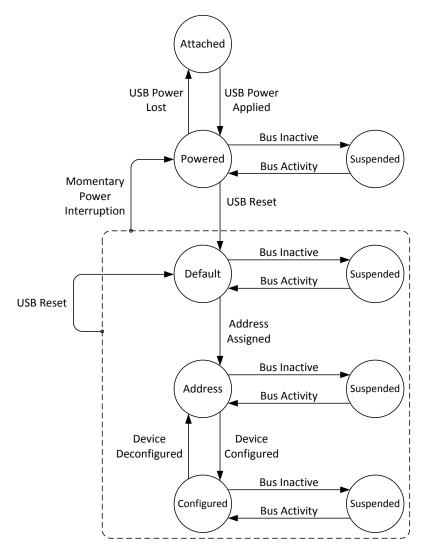


Figure 176: Device state diagram

The device must change state according to host-initiated traffic and USB bus states.

It is up to the software to implement a state machine that matches the above definition.

To detect the presence or absence of USB supply (V_{BUS}), the *POWER* chapter defines two events USBDETECTED and USBREMOVED, they can be used to implement the state machine.

As a general rule when implementing the software, the host behavior shall never be assumed to be predictable, in particular the sequence of commands received during an enumeration. The software shall always react to the current bus conditions or commands sent by the host.

51.2 USB terminology

The USB specification defines bus states, rather than logic levels on the D+ and D- lines.

For a full speed device, the bus state where the D+ line is high and the D- line is low is defined as the J state. The bus state where D+ is low and D- high is called the K state.

An idle bus, where D+ and D- lines are only polarized through the pull-up on D+ and pull-downs on the host side, will be in J state.

Both lines low are called SE0 (single-ended 0), and both lines high SE1 (single-ended 1).



51.3 USB pins

The USBD peripheral features a number of dedicated pins.

For more information about the pinout, please refer to *Pin assignments* on page 13.

The dedicated USB pins can be grouped in two categories: signal and power.

For details on the USB power supply and V_{BUS} detection, refer to the *POWER* chapter.

The signal pins consist of the D+ and D- pins, which are to be connected to the USB host. They are dedicated pins, and not available as standard GPIOs.

The USBD implements the "5V Short Circuit Withstand ECN", which amends the original USB 2.0 Specification. This means that these two pins are not 5 V tolerant.

The signal pins and the pull-up will operate only while V_{BUS} is in its valid voltage range, and USBD is enabled through the *ENABLE* register.

51.4 USBD start-up sequence

The PHY of the USBD is powered separately from the rest of the device (V_{BUS} pin), which has some implications on the USBD power up sequence.

The device is not able to properly signal its presence to the USB host, and handle traffic from the host, unless the PHY's power supply is enabled and stable.

The turning on or off of the PHY's power supply is directly linked to the *ENABLE* register. The device provides events that help synchronizing software to the various steps during the power up sequence.

It is recommended to enable USBD only after V_{BUS} has been detected, and turn on the USB pull-up after a USBPWRRDY event has occurred, and after a USBEVENT has occurred with the READY condition flagged in EVENTCAUSE. This ensures that all resources in USBD are available and the dedicated USB voltage regulator has stabilized.

Below sequence chart illustrates a typical handling of V_{BUS} power up.

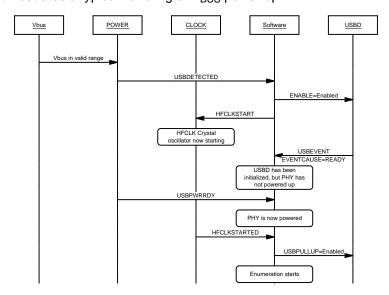


Figure 177: V_{BUS} power up sequence

Upon detection of V_{BUS} removal, signalled by the USBREMOVED event described in the *POWER* chapter, it is recommended to let on-going EasyDMA transfers finish (wait for the relevant ENDEPIN[n], ENDISOIN, ENDEPOUT[n] or ENDISOOUT event, see *EasyDMA* on page 616), then to disable USBD through writing ENABLE = Disabled .



51.5 USB pull-up

The USB pull-up serves two purposes: it indicates to the host that the device is connected to the USB bus, and indicates the device's speed grade.

When no pull-up is connected to the USB bus, the host sees both D+ and D- lines low, as they are pulled down on the host side by 15 kOhm resistors. The device is not seen by the host, and hence defined to be in detached state, even though it could be physically connected to the host. USB spec does not allow to draw any current on V_{BUS} in that situation.

When a full-speed device connects its 1.5 kOhm pull-up to D+, the host sees the corresponding line high. The device is then in attached state. The host may attempt to determine if the device supports higher speeds (which it does not), and will then initiate communication with the device to further identify it; this process is called enumeration.

If the host supports higher speed grades and the device is full-speed, the host may attempt to determine if that device is capable of higher speeds. The USBD peripheral implemented in this device supports only full-speed (12 Mbps), and will ignore the negotiation for higher speeds, in accordance with the USB specification revision 2.0, full speed part.

The *USBPULLUP* register provides means to connect or disconnect the pull-up on D+ under software control. This allows the software to control when USB enumeration takes place. It also allows to emulate a physical disconnect from the USB bus, for instance when re-enumeration is required.

USBPULLUP has to be set to Enabled to allow the USBD to handle USB traffic and generate appropriate events. This forbids the use of an external pull-up.

Note that disconnecting the pull-up through the *USBPULLUP* register while connected to a host will result in both D+ and D- lines to be pulled low by the host's pull-down resistors. However, as mentioned above, this will also inhibit the generation of the USBRESET event.

The pull-up is disabled by default after a chip reset.

The pull-up shall only get connected after USBD has been enabled through the *ENABLE* register. Attempting to access the *USBPULLUP* register prior to that will lead to an ACCESSFAULT event to get generated.

The USB pull-up value is automatically changed depending on bus activity, as specified in the "Resistor ECN" which amends the original USB Specification v2.0. The user does not have access to this function, it is handled in hardware.

While they should never be used in normal traffic activity, the task DPDMDRIVE allows at any time to force the D+ and D- lines to the state specified in the *DPDMVALUE* register. The DPDMNODRIVE task stops driving them, and the PHY returns to normal operation.

51.6 USB reset

The USB specification defines a USB reset, which shall not be confused with a chip reset.

The USB reset results from a single-ended low state (SE0) on the D+ / D- lines for a time T_{DETRST} , as specified in the USB specification chapter 7. Only the host is allowed to drive a USB reset condition on the bus.

The USB reset is a normal USB bus condition, and is used as part of the enumeration sequence, it does not reset the chip.

The UBSD peripheral automatically interprets a SE0 longer than $t_{USB,DETRST}$ as a USB reset. When the device detects a USB reset and generates a USBRESET event, the device USB stack and related parts of the application shall re-initialize themselves, and go back to the **Default** state.

Some of the registers in the USBD peripheral get automatically reset to a known state, in particular all data endpoints will get disabled, and the *USBADDR* will be reset to 0.



After having been connected to the USB bus (i.e. after V_{BUS} gets applied), the device shall not respond to any traffic from the time the pull-up is enabled until it has seen a USB reset condition. This is automatically ensured by the USBD.

After a USB reset, the device shall be fully responsive after at most T_{RSTRCY} (as per USB specification chapter 7). Software shall take into account that it takes $t_{USB,RSTRCY}$ for the hardware to recover from a USB reset condition.

51.7 USB suspend and resume

Normally, the host will maintain activity on the USB at least every millisecond per USB specification.

To signal that the device shall go into low power mode, the host stops activity on the USB bus, which becomes idle, only the device pull-up and host pull-downs act on D+ and D-, and the bus is thus kept at a constant J state. It is up to the device to detect this lack of activity, and enter into a low power mode within a specified time.

The USB host can decide at any moment to suspend USB activity. When this happens, the device is obligated per USB specification to enter a low power mode. The host can decide at any moment to resume USB activity, on its own initiative. If Remote WakeUp has been enabled by the host, the device may also issue a RESUME request to wake up the host.

51.7.1 Entering suspend

The USBD peripheral automatically detects a lack of activity for more than $t_{USB,SUSPEND}$ and will generate the corresponding USBEVENT event, with SUSPEND bit set in the *EVENTCAUSE* register. The software shall ensure that the current drawn from the USB supply line V_{BUS} is within the specified limits before T_{2SUSP} as defined in chapter 7 of the USB specification.

In order to save power, and provided that no other peripheral needs it, the crystal oscillator (HFXO) in CLOCK may be disabled by software during USB suspend, while the USB pull-up is disconnected, or when V_{BUS} is not present. Software must explicitly enable it at any other time. The USBD will not be able to respond to USB traffic unless HFXO is enabled and stable.

51.7.2 Host-initiated resume

If the host resumes bus activity with or without a RESUME condition (in other words: bus activity is defined as any non-J state), the USBD peripheral will generate a USBEVENT event, with RESUME bit set in the *EVENTCAUSE* register, and the device has to be responsive to any incoming request on the USB bus within the time T_{RSMRCY} defined in chapter 7 of the USB specification. It is also allowed to revert to normal power consumption mode.

If the host resumes bus activity simply by restarting sending frames, the USBD peripheral will generate SOF events. Also here the device has to be responsive to any incoming request on the USB bus, and can be in normal power consumption mode.

51.7.3 Device-initiated remote wake-up

Assuming that remote wake-up is supported by the device and has been enabled by the host, if the device meets a wake-up condition while the device is suspended, the device can request the host to resume.

To do so, the software shall first make sure that HFXO gets enabled.

It can then instruct the USBD peripheral to drive a RESUME condition (K state) on the USB bus through the DPDMDRIVE task, and hence attempt to wake up the host. By choosing Resume in DPDMVALUE, the duration of the RESUME state is under hardware control ($T_{USB,DRIVEK}$). By choosing J or K, the duration of that state is under software control (the J or K state is maintained until a DPDMNODRIVE task is issued), and has to meet T_{DRSMUP} from USB specification chapter 7.

The value in the *DPDMVALUE* on page 648 register will only be captured and used when the DPDMDRIVE task is sent.



Note that the device shall ensure that it does not initiate such a remote wake-up request before T_{WTRSM} (as per USB specification chapter 7) after the bus has entered idle state. Using the recommended Resume value in DPDMVALUE, rather than K, takes care of this, and postpones the RESUME state accordingly.

As just explained, the *DPDMVALUE* register contains the value at which the bus shall be forced after a DPDMDRIVE task. If the software needs to read back the actual D+ and D- lines state, it can do so at any time by reading the *BUSSTATE* register.

51.8 EasyDMA

The USBD peripheral includes EasyDMA so that USB buffers are located in Data RAM.

Each endpoint has an associated set of tasks, events and registers.

The *EPIN[n].PTR*, *EPOUT[n].PTR* (n=0..7), *ISOIN.PTR* and *ISOOUT.PTR* registers define the address of the buffer in Data RAM for a specific IN or OUT endpoint.

The *EPIN[n].MAXCNT* and *ISOIN.MAXCNT* registers define the amount of bytes to be sent on USB for next transaction.

The *EPOUT[n].MAXCNT* (n=1..7) and *ISOOUT.MAXCNT* registers define the length of the buffer, in bytes, for next transfer of incoming data. Since the host decides how many bytes are being sent over USB, the MAXCNT value can be copied from the respective *SIZE.EPOUT[n]* (n=1..7) or *SIZE.ISOOUT* register.

The *EPOUT[0].MAXCNT* register defines the length of the control endpoint OUT buffer, in bytes. If the USB host does not misbehave, the *SIZE.EPOUT[0]* register will indicate the same value than MaxPacketSize from the device descriptor or wLength from the SETUP command, whichever is the smallest.

The .AMOUNT registers indicate how many bytes have actually been transferred over EasyDMA during last transfer.

The STARTEPIN[n], STARTEPOUT[n] (n=0..7), STARTISOIN and STARTISOOUT tasks capture the .PTR and .MAXCNT registers values; for IN endpoints, a transaction over USB gets automatically triggered when the EasyDMA transfer is complete; for OUT endpoints, it is up to software to allow the next transaction over USB, see the examples in *Control transfers* on page 617, *Bulk and interrupt transactions* on page 620 and *Isochronous transactions* on page 622.

The STARTED event confirms that the .PTR, .MAXCNT and .CONFIG registers values of the endpoints flagged in the *EPSTATUS* register have been captured; those can then be modified by software for the next transfer.

The ENDEPIN[n], ENDEPOUT[n] (n=0..7), ENDISOIN and ENDISOOUT events indicate that the whole buffer in Data RAM has been consumed. The buffer can be accessed safely by software.

Only a single EasyDMA transfer can take place in USBD at any time. It is up to the software to ensure that no STARTEPIN[n], STARTISOIN, STARTEPOUT[n] or STARTISOOUT task is sent before having received the ENDEPIN[n], ENDISOIN, ENDEPOUT[n] or ENDISOOUT event from an on-going transfer.

EasyDMA and traffic on USB are tightly related. A number of events provide insight of what is happening on the USB bus, and a number of tasks allow to somewhat automate response to traffic.

The EPDATA event indicates that a successful (acknowledged) data transaction has occurred on the data endpoint(s) flagged in the *EPDATASTATUS* register.

In the particular case of the control endpoint 0, OUT transactions are allowed through the EP0RCVOUT task. A successful (acknowledged) data transaction on endpoint 0 is signalled by the EP0DATADONE event. The EP0STATUS task allows a status stage to be initiated, and the EP0STALL task allows stalling further traffic (data or status stage) on the control endpoint.

The EPOSETUP event indicates that a SETUP token has been received on the control endpoint 0. EasyDMA will not copy the SETUP data to Data RAM (it will only transfer data from the data stage), they are available as separate registers in the USBD peripheral: *BMREQUESTTYPE*, *BREQUEST*, *WVALUEL*, *WVALUEH*, *WINDEXL*, *WINDEXH*, *WLENGTHL* and *WLENGTHH*.

At any time, the USBEVENT event may be sent, and the *EVENTCAUSE* register provides details on what happened, for instance if a CRC error is detected during a transaction, or if bus activity stops or resumes.



Enabling endpoints is controlled through the *EPINEN* and *EPOUTEN* registers.

Stalling bulk/interrupt endpoints is controlled through the *EPSTALL* register.

Note that due to USB specification requirements, the effect of the stalling control endpoint 0 may be overridden by hardware, in particular when a new SETUP token is received.

51.9 Control transfers

The USB specification mandates every USB device to implement endpoint 0 IN and OUT as control endpoints.

A control transfer consists of two or three stages:

- Setup stage
- Data stage (optional)
- Status stage

Each control transfer can be of following type:

- Control read
- Control read no data
- Control write
- Control write no data

An EP0SETUP event indicates that the data in the setup stage (i.e. following the SETUP token) is available in the *BREQUEST*, *BMREQUESTTYPE*, *WVALUEL*, *WVALUEH*, *WINDEXL*, *WINDEXH*, *WLENGTHL* and *WLENGTHH* registers.

The data in the data stage(i.e. following the IN or OUT token) is transferred from or to the desired location in Data RAM using EasyDMA.

Note: the control endpoint buffer size in Data RAM can be of any size in bytes, and there is no constraint to keep it 32-bit aligned.

After receiving the SETUP token, the USB controller will NAK any incoming IN or OUT token until software has finished decoding the command, determined the type of transfer, and prepared the next stage (data or status) appropriately.

The software can choose to STALL the command (both data and status stages) through the EP0STALL task, for instance if the command is not supported, or its wValue, wIndex or wLength parameters are wrong. A stalled Control Read transfer is depicted below, but the same mechanism (same tasks) applies to stalling a Control Write transfer (not depicted).

Refer to the chapter 9 of the USB Specification v2.0 and relevant Class specifications for rules on when to STALL a command.



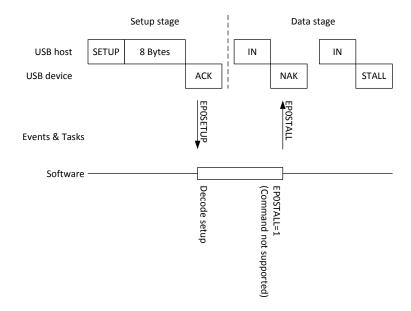


Figure 178: Control read gets STALLed

Important: the USBD peripheral handles the SetAddress transfer by itself. As a consequence, the software shall not process this command, other than updating its state machine (see *Device state diagram*), nor initiate a status stage. If necessary, the address assigned by the host can be read out from the USBADDR register after the command has been processed.

51.9.1 Control Read transfer

This section describes how the software behaves to respond to a Control Read transfer.

As mentioned earlier, the USB controller will NAK any incoming IN token until software has finished decoding the command, determined the type of transfer, and prepared the next stage (data or status) appropriately.

For a control-read, transferring the data from Data RAM memory into USBD will trigger a valid, ACKed IN transaction on USB.

The software has to prepare EasyDMA by pointing to the buffer containing the data to be transferred. If no other EasyDMA transfer is on-going with USBD, software can send the STARTEPINO task, which will initiate the data transfer and transaction on USB.

A STARTED event (with EPIN0 bit set in the *EPSTATUS* register) will get fired as soon as the EPIN[0].PTR and .MAXCNT registers have been captured. Software may then prepare them for next data transaction.

A ENDEPIN[0] event will get fired when the data has been transferred from memory to the USBD peripheral.

Finally, an EP0DATADONE event will get fired when the data has been transmitted over USB and acknowledged by the host.

The software can then either prepare and transmit the next data transaction by repeating the above sequence, or initiate the status stage through the EP0STATUS task.



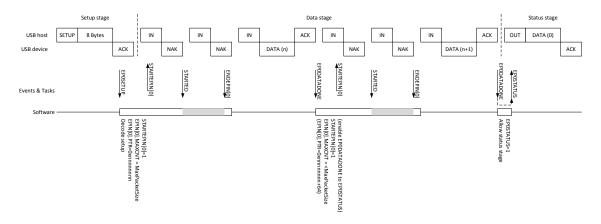


Figure 179: Control read transfer

Note the possibility to enable a shortcut from the EP0DATADONE event to the EP0STATUS task, typically if the data stage is expected to take a single transfer.

If there is no data stage, the software can initiate the status stage through the EP0STATUS task right away, as depicted below.

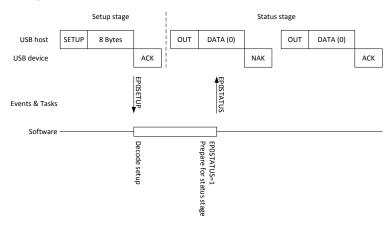


Figure 180: Control read no data transfer

51.9.2 Control Write transfer

This section describes how the software behaves to respond to a Control Write transfer.

The software has to prepare EasyDMA by pointing to the buffer in Data RAM that shall contain the incoming data. If no other EasyDMA transfer is on-going with USBD, software can then send the EP0RCVOUT task, which will make the USBD to accept (ACK) the first OUT+DATA transaction from the host.

An EP0DATADONE event will get fired when a new OUT+DATA has been transmitted over USB, and is about to get acknowledged by the device.

A STARTED event (with EPOUT0 bit set in the *EPSTATUS* register) will get fired as soon as the EPOUT[0].PTR and .MAXCNT registers have been captured, after receiving the first transaction. Software may then prepare them for next data transaction.

A ENDEPOUT[0] event will get fired when the data has been transferred from the USBD peripheral to Data RAM.

The software can then either prepare to receive the next data transaction by repeating the above sequence, or initiate the status stage through the EP0STATUS task. Until then, further incoming OUT + DATA transactions get a NAK response by the device.



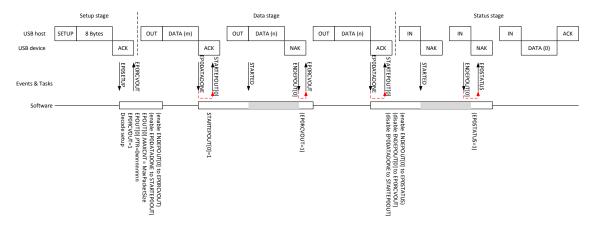


Figure 181: Control write transfer

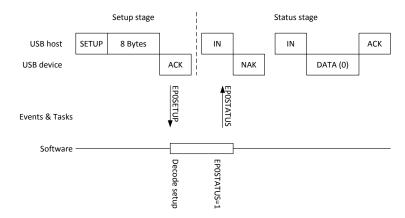


Figure 182: Control write no data transfer

51.10 Bulk and interrupt transactions

The USBD peripheral implements seven pairs of bulk/interrupt endpoints.

The bulk/interrupt endpoints have a fixed USB endpoint number, summarized in the table below.

Table 124: Bulk/interrupt endpoint numbering

Bulk endpoint #	USB IN endpoint	USB OUT endpoint
[1]	0x81	0x01
[2]	0x82	0x02
[3]	0x83	0x03
[4]	0x84	0x04
[5]	0x85	0x05
[6]	0x86	0x06
[7]	0x87	0x07

A bulk/interrupt transaction consists of a single data stage. Two consecutive, successful transactions are distinguished through alternating leading PID: DATA0 follows DATA1, DATA1 follows DATA0, etc.

A repeated transaction is detected by re-using the same PID as previous transaction, i.e DATA0 follows DATA0, or DATA1 follows DATA1.

The USBD controller automatically toggles DATA0/DATA1 PIDs for every bulk/interrupt transaction, and in general software does not need to care about it.

If an incoming data is corrupted (CRC does not match), the USBD controller automatically prevents DATA0/DATA1 from toggling, to request the host to resend the data.

In specific cases, the software may want to force data toggle (usually reset) on a specific IN endpoint, or force the expected toggle on an OUT endpoint, for instance as a consequence of the host issuing a



ClearFeature, SetInterface or selecting an alternate setting. Controlling the data toggle of data IN or OUT endpoint n=1..7 is done through the *DTOGGLE* register.

The maximum size of a bulk/interrupt transaction in USB Full Speed is 64 Bytes, and has to be a multiple of 4 bytes, and be 32-bit aligned in Data RAM. However, the amount of DATA bytes transmitted on the USB data endpoint can be of any size (up to 64 bytes).

When the transaction is done over USB, a EPDATA event is sent, and the hardware will automatically NAK further IN tokens, until software is ready to send more data and has finished configuring EasyDMA, has started it, and the whole buffer content has been moved to the USB controller (signalled by the ENDEPIN[n] event).

Each IN or OUT data endpoint has to be explicitly enabled by software through the *EPINEN* or *EPOUTEN* register, according to the configuration declared by the device and selected by the host through the SetConfig command.

A disabled data endpoint will not respond to any traffic from the host.

An enabled data endpoint will normally respond NAK or ACK (depending on the readiness of the buffers), or STALL if configured so through the *EPSTALL* register (in which case the endpoint is said to be halted).

The halted (or not) state of a given endpoint can be read back from the *HALTED.EPIN[n]* or *HALTED.EPOUT[n]* register. The format of the returned 16 bit value can be copied as is as response to a GetStatusEndpoint request from the host.

Note that enabling or disabling an endpoint will not change its halted state. However, a USB reset will disable and clear the halted state of all data endpoints.

The control endpoint 0 IN and OUT can also get enabled and/or halted through the same mechanisms, but due to USB specification, receiving a SETUP will override its state.

51.10.1 Bulk and interrupt IN transaction

The host issues IN tokens to receive bulk/interrupt data. In order to send data, the software has to enable the endpoint and prepare an EasyDMA transfer on the desired endpoint, as illustrated below.

Bulk/interrupt IN endpoints are enabled or disabled through their respective INn bit (n=1..7) in *EPINEN* register.

It is also possible to stall or un-stall an endpoint through the *EPSTALL* register.

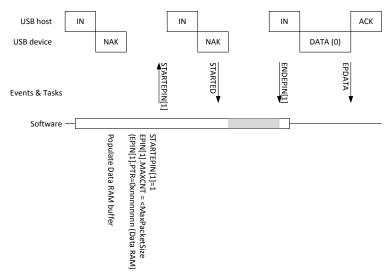


Figure 183: Bulk/interrupt IN transaction

It is possible (and some situations mandate it) to respond to an IN with a zero-length data packet.

Note: on many USB hosts, not responding (DATA+ACK or NAK) to three IN tokens on a interrupt endpoint would have the host disable that endpoint as a consequence. Re-enumerating the device (unplug-replug)



may be required to restore functionality. Make sure the relevant data endpoints are enabled for normal operation as soon as the device gets configured through a SetConfig request.

51.10.2 Bulk and interrupt OUT transaction

When the host wants to transmit bulk/interrupt data, it issues an OUT Token packet followed by a DATA packet on a given endpoint n.

A NAK handshake is returned until the software writes any value to SIZE.EPOUT[n], indicating that the local buffer's content can be overwritten. Upon receiving the next OUT + DATA transaction, an ACK handshake is returned to the host while a EPDATA event is sent (and EPSTATUS register flags set to indicate on which endpoint this happened), and once the EasyDMA is prepared and enabled through writing the EPOUT[n] registers and sending the STARTEPOUT[n] task, the incoming data will be transferred to Data RAM. Until that transfer is finished, the hardware will automatically NAK further incoming OUT+DATA packets. Only when the EasyDMA transfer is done (signalled by the ENDEPOUT[n] event) and the software has written any value to SIZE.EPOUT[n], the endpoint n will accept incoming OUT + DATA again.

It is allowed for the host to send out a zero-length data packet.

Bulk/interrupt OUT endpoints are enabled or disabled through their respective OUTn bit (n=1..7) in the *EPOUTEN* register. It is also possible to stall or un-stall an endpoint through the *EPSTALL* register.

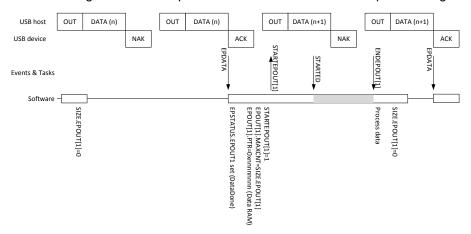


Figure 184: Bulk/interrupt OUT transaction

51.11 Isochronous transactions

The USBD peripheral implements isochronous (iso) endpoints.

The iso endpoints have a fixed USB endpoint number, summarized in the table below.

Table 125: Isochronous endpoint numbering

Iso endpoint #	USB IN endpoint	USB OUT endpoint
[0]	0x88	0x08

A isochronous transaction consists of a single, non-acknowledged data stage. The host sends out a start of frame at a regular interval (1ms), and data follows IN or OUT tokens within each frame.

EasyDMA allows transferring iso data directly from and to Data RAM; EasyDMA transfers must be initiated by software, which can synchronize to the SOF events.

Because the timing of the start of frame is very accurate, the SOF event can be used for instance to synchronize a local timer through the SOF event and PPI. The SOF event gets synchronized to the 16 MHz clock prior to being made available to PPI.

Every Start of Frame increments a free-running counter, which can be read by software through the *FRAMECNTR* register.



Each IN or OUT iso data endpoint has to be explicitly enabled by software through the *EPINEN* or *EPOUTEN* register, according to the configuration declared by the device and selected by the host through the SetConfig command.

A disabled iso IN data endpoint will not respond to any traffic from the host.

A disabled iso OUT data endpoint will ignore any incoming traffic from the host.

The USBD peripheral has an internal 1 kByte buffer associated with iso endpoints. The user can either allocate the full amount to the IN or the OUT endpoint, or split the buffer allocation between the two. This is done through the *ISOSPLIT* register, which provides a number of pre-determined splits.

51.11.1 Isochronous IN transaction

When the host wants to receive isochronous (iso) data, it issues an IN token on the isochronous endpoint.

On the isochronous IN endpoint, after the data has been transferred using the EasyDMA, the USB controller responds to the IN token with the data that had been transferred, using the *ISOIN.MAXCNT* for the size of the packet.

The iso IN data endpoint has to be explicitly enabled by software through the ISOIN0 bit in the *EPINEN* register.

When the iso IN endpoint is enabled, and if no data had been transferred with EasyDMA, the response of the USBD depends on the setting of the RESPONSE field in the *ISOINCONFIG* register. If set to NoResp, no response to an IN token will be provided. If set to ZeroData, the USBD responds with a zero-length data.

Note: the maximum size of an isochronous IN transfer in USB Full Speed is 1023 Bytes, and the data buffer in RAM has to be a multiple of 4 bytes, and be 32-bit aligned in Data RAM. However, the amount of bytes transferred on the USB data endpoint can be of any size (up to 1023 Byte if not shared with an OUT iso endpoint).

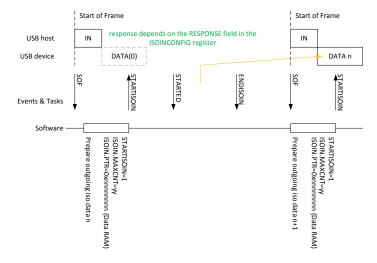


Figure 185: Isochronous IN transfer

51.11.2 Isochronous OUT transaction

When the host wants to send isochronous (iso) data, it issues an OUT token on the isochronous endpoint, followed by data.

The iso OUT data endpoint has to be explicitly enabled by software through the ISOOUT0 bit in the *EPOUTEN* register.

The amount of last received iso OUT data is provided in the SIZE.ISOOUT register.

Software shall interpret the ZERO and SIZE fields as follows:

Table 126: Iso OUT incoming data size

ZERO	SIZE	last received data size
Normal	0	No data received at all



ZERO	SIZE	last received data size
Normal	11023	11023 bytes of data received
ZeroData	(don't care)	Zero-length data packet received

When the EasyDMA is prepared and started, sending a STARTISOOUT task initiates an EasyDMA transfer to Data RAM. Software shall synchronize iso OUT transfers to the SOF events. If OUT data is not consumed and processed until next SOF, it will be overwritten by more recent data.

EasyDMA uses the address in ISOOUT.PTR and size in ISOOUT.MAXCNT for every new transfer.

Note: the maximum size of an isochronous OUT transfer in USB Full Speed is 1023 Bytes, and the data buffer in RAM has to be a multiple of 4 bytes, and be 32-bit aligned in Data RAM. However, the amount of bytes transferred on the USB data endpoint can be of any size (up to 1023 Byte if not shared with an IN iso endpoint).

If the last received iso data packet is corrupted (wrong CRC), the USB controller sends an USBEVENT event (at the same time as SOF) and indicates a CRC error on ISOOUTCRC in the *EVENTCAUSE* register. EasyDMA will transfer the data anyway if it has been set up properly.

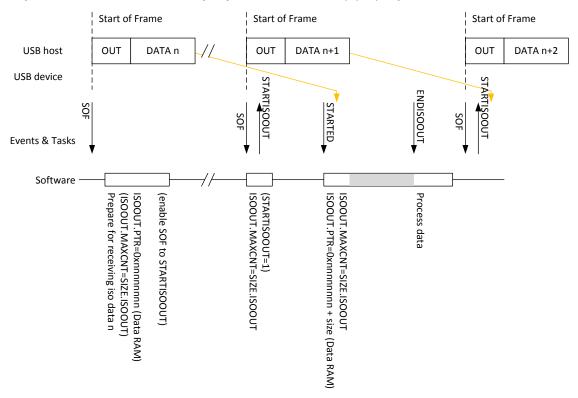


Figure 186: Isochronous OUT transfer

51.12 USB register access limitations

Some of the registers in USBD cannot get accessed in specific conditions.

This is the case while USBD is not enabled (through the *ENABLE* register) and ready (signalled by the READY bit in *EVENTCAUSE* after the USBEVENT event), or when USBD has been placed in low power while the USB bus is suspended.

If any of the register listed below gets accessed (read or write) by software of through the debugger, an ACCESSFAULT event will get fired, and if the associated interrupt has been enabled through the *INTEN* or *INTENSET* register in USBD, an interrupt will be taken.

Following registers are affected by this behaviour:

- firing any task, including through PPI
- BUSSTATE



- HALTED.EPIN[0..7]
- HALTED.EPOUT[0..7]
- USBADDR
- BMREQUESTTYPE
- BREQUEST
- WVALUEL
- WVALUEH
- WINDEXL
- WINDEXH
- WLENGTHL
- WLENGTHH
- SIZE.EPOUT[0..7]
- SIZE.ISOOUT
- USBPULLUP
- DTOGGLE
- EPINEN
- EPOUTEN
- EPSTALL
- ISOSPLIT
- FRAMECNTR

51.13 Registers

Table 127: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40027000	USBD	USBD	Universal serial bus device	

Table 128: Register Overview

Register	Offset	Description
TASKS_STARTEPIN[0]	0x004	Captures the EPIN[0].PTR, EPIN[0].MAXCNT and EPIN[0].CONFIG registers values, and enables
		endpoint IN 0 to respond to traffic from host
TASKS_STARTEPIN[1]	0x008	Captures the EPIN[1].PTR, EPIN[1].MAXCNT and EPIN[1].CONFIG registers values, and enables
		endpoint IN 1 to respond to traffic from host
TASKS_STARTEPIN[2]	0x00C	Captures the EPIN[2].PTR, EPIN[2].MAXCNT and EPIN[2].CONFIG registers values, and enables
		endpoint IN 2 to respond to traffic from host
TASKS_STARTEPIN[3]	0x010	Captures the EPIN[3].PTR, EPIN[3].MAXCNT and EPIN[3].CONFIG registers values, and enables
		endpoint IN 3 to respond to traffic from host
TASKS_STARTEPIN[4]	0x014	Captures the EPIN[4].PTR, EPIN[4].MAXCNT and EPIN[4].CONFIG registers values, and enables
		endpoint IN 4 to respond to traffic from host
TASKS_STARTEPIN[5]	0x018	Captures the EPIN[5].PTR, EPIN[5].MAXCNT and EPIN[5].CONFIG registers values, and enables
		endpoint IN 5 to respond to traffic from host
TASKS_STARTEPIN[6]	0x01C	Captures the EPIN[6].PTR, EPIN[6].MAXCNT and EPIN[6].CONFIG registers values, and enables
		endpoint IN 6 to respond to traffic from host
TASKS_STARTEPIN[7]	0x020	Captures the EPIN[7].PTR, EPIN[7].MAXCNT and EPIN[7].CONFIG registers values, and enables
		endpoint IN 7 to respond to traffic from host
TASKS_STARTISOIN	0x024	Captures the ISOIN.PTR, ISOIN.MAXCNT and ISOIN.CONFIG registers values, and enables sending
		data on iso endpoint
TASKS_STARTEPOUT[0]	0x028	Captures the EPOUT[0].PTR, EPOUT[0].MAXCNT and EPOUT[0].CONFIG registers values, and enables
		endpoint 0 to respond to traffic from host
TASKS_STARTEPOUT[1]	0x02C	Captures the EPOUT[1].PTR, EPOUT[1].MAXCNT and EPOUT[1].CONFIG registers values, and enables
		endpoint 1 to respond to traffic from host
TASKS_STARTEPOUT[2]	0x030	Captures the EPOUT[2].PTR, EPOUT[2].MAXCNT and EPOUT[2].CONFIG registers values, and enables
		endpoint 2 to respond to traffic from host



Register	Offset	Description
TASKS_STARTEPOUT[3]	0x034	Captures the EPOUT[3].PTR, EPOUT[3].MAXCNT and EPOUT[3].CONFIG registers values, and enables
		endpoint 3 to respond to traffic from host
TASKS_STARTEPOUT[4]	0x038	Captures the EPOUT[4].PTR, EPOUT[4].MAXCNT and EPOUT[4].CONFIG registers values, and enables
		endpoint 4 to respond to traffic from host
TASKS_STARTEPOUT[5]	0x03C	Captures the EPOUT[5].PTR, EPOUT[5].MAXCNT and EPOUT[5].CONFIG registers values, and enables
		endpoint 5 to respond to traffic from host
TASKS_STARTEPOUT[6]	0x040	Captures the EPOUT[6].PTR, EPOUT[6].MAXCNT and EPOUT[6].CONFIG registers values, and enables
		endpoint 6 to respond to traffic from host
TASKS_STARTEPOUT[7]	0x044	Captures the EPOUT[7].PTR, EPOUT[7].MAXCNT and EPOUT[7].CONFIG registers values, and enables
		endpoint 7 to respond to traffic from host
TASKS_STARTISOOUT	0x048	Captures the ISOOUT.PTR, ISOOUT.MAXCNT and ISOOUT.CONFIG registers values, and enables
_		receiving of data on iso endpoint
TASKS_EPORCVOUT	0x04C	Allows OUT data stage on control endpoint 0
TASKS_EPOSTATUS	0x050	Allows status stage on control endpoint 0
TASKS EPOSTALL	0x054	STALLs data and status stage on control endpoint 0
TASKS_DPDMDRIVE	0x058	Forces D+ and D-lines to the state defined in the DPDMVALUE register
TASKS_DPDMNODRIVE		Stops forcing D+ and D- lines to any state (USB engine takes control)
EVENTS_USBRESET	0x100	Signals that a USB reset condition has been detected on the USB lines
EVENTS_STARTED	0x104	Confirms that the EPIN[n].PTR, EPIN[n].MAXCNT, EPIN[n].CONFIG, or EPOUT[n].PTR,
EVENTS_STARTED	0.104	
		EPOUT[n].MAXCNT and EPOUT[n].CONFIG registers have been captured on all endpoints reported in the EPSTATUS register
EVENTS ENDEDINIO	0v109	·
EVENTS_ENDEPIN[0]	0x108	The whole EPIN[0] buffer has been consumed. The RAM buffer can be accessed safely by software.
EVENTS_ENDEPIN[1]	0x10C	The whole EPIN[1] buffer has been consumed. The RAM buffer can be accessed safely by software.
EVENTS_ENDEPIN[2]	0x110	The whole EPIN[2] buffer has been consumed. The RAM buffer can be accessed safely by software.
EVENTS_ENDEPIN[3]	0x114	The whole EPIN[3] buffer has been consumed. The RAM buffer can be accessed safely by software.
EVENTS_ENDEPIN[4]	0x118	The whole EPIN[4] buffer has been consumed. The RAM buffer can be accessed safely by software.
EVENTS_ENDEPIN[5]	0x11C	The whole EPIN[5] buffer has been consumed. The RAM buffer can be accessed safely by software.
EVENTS_ENDEPIN[6]	0x120	The whole EPIN[6] buffer has been consumed. The RAM buffer can be accessed safely by software.
EVENTS_ENDEPIN[7]	0x124	The whole EPIN[7] buffer has been consumed. The RAM buffer can be accessed safely by software.
EVENTS_EPODATADONE		An acknowledged data transfer has taken place on the control endpoint
EVENTS_ENDISOIN	0x12C	The whole ISOIN buffer has been consumed. The RAM buffer can be accessed safely by software.
EVENTS_ENDEPOUT[0]	0x130	The whole EPOUT[0] buffer has been consumed. The RAM buffer can be accessed safely by
		software.
EVENTS_ENDEPOUT[1]	0x134	The whole EPOUT[1] buffer has been consumed. The RAM buffer can be accessed safely by
		software.
EVENTS_ENDEPOUT[2]	0x138	The whole EPOUT[2] buffer has been consumed. The RAM buffer can be accessed safely by
		software.
EVENTS_ENDEPOUT[3]	0x13C	The whole EPOUT[3] buffer has been consumed. The RAM buffer can be accessed safely by
		software.
EVENTS_ENDEPOUT[4]	0x140	The whole EPOUT[4] buffer has been consumed. The RAM buffer can be accessed safely by
		software.
EVENTS_ENDEPOUT[5]	0x144	The whole EPOUT[5] buffer has been consumed. The RAM buffer can be accessed safely by
		software.
EVENTS_ENDEPOUT[6]	0x148	The whole EPOUT[6] buffer has been consumed. The RAM buffer can be accessed safely by
		software.
EVENTS_ENDEPOUT[7]	0x14C	The whole EPOUT[7] buffer has been consumed. The RAM buffer can be accessed safely by
		software.
EVENTS_ENDISOOUT	0x150	The whole ISOOUT buffer has been consumed. The RAM buffer can be accessed safely by software.
EVENTS_SOF	0x154	Signals that a SOF (start of frame) condition has been detected on the USB lines
EVENTS_USBEVENT	0x158	An event or an error not covered by specific events has occurred, check EVENTCAUSE register to find
		the cause
EVENTS_EPOSETUP	0x15C	A valid SETUP token has been received (and acknowledged) on the control endpoint
EVENTS_EPDATA	0x160	A data transfer has occurred on a data endpoint, indicated by the EPDATASTATUS register
EVENTS_ACCESSFAULT	0x164	Access to an unavailable USB register has been attempted (software or EasyDMA). This event can
	-	get fired even when USBD is not ENABLEd.
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
HATENSET	UNJUT	Endoic interrupt



Register	Offset	Description
INTENCLR	0x308	Disable interrupt
EVENTCAUSE	0x400	Details on event that caused the USBEVENT event
BUSSTATE	0x404	Provides the logic state of the D+ and D- lines
HALTED.EPIN[0]	0x420	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[1]	0x424	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[2]	0x428	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[3]	0x42C	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[4]	0x430	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[5]	0x434	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[6]	0x438	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[7]	0x43C	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[0]	0x444	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[1]	0x448	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[2]	0x44C	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[3]	0x450	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[4]	0x454	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[5]	0x458	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[6]	0x45C	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[7]	0x460	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
EPSTATUS	0x468	Provides information on which endpoint's EasyDMA registers have been captured
EPDATASTATUS	0x46C	Provides information on which endpoint(s) an acknowledged data transfer has occurred (EPDATA
		event)
USBADDR	0x470	Device USB address
BMREQUESTTYPE	0x480	SETUP data, byte 0, bmRequestType
BREQUEST	0x484	SETUP data, byte 1, bRequest
WVALUEL	0x488	SETUP data, byte 2, LSB of wValue
WVALUEH	0x48C	SETUP data, byte 3, MSB of wValue
WINDEXL	0x490	SETUP data, byte 4, LSB of windex
WINDEXH	0x494	SETUP data, byte 5, MSB of windex
WLENGTHL	0x498	SETUP data, byte 6, LSB of wLength
WLENGTHH	0x49C	SETUP data, byte 7, MSB of wLength
SIZE.EPOUT[0]	0x4A0	Amount of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[1]	0x4A4	Amount of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[2]	0x4A8	Amount of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[3]	0x4AC	Amount of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[4]	0x4B0	Amount of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[5]	0x4B4	Amount of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[6]	0x4B8	Amount of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[7]	0x4BC	Amount of bytes received last in the data stage of this OUT endpoint
SIZE.ISOOUT	0x4C0	Amount of bytes received last on this iso OUT data endpoint
ENABLE	0x500	Enable USB
USBPULLUP	0x504	Control of the USB pull-up
DPDMVALUE	0x508	State at which the DPDMDRIVE task will force D+ and D The DPDMNODRIVE task reverts the
		control of the lines to MAC IP (no forcing).
DTOGGLE	0x50C	Data toggle control and status.
EPINEN	0x510	Endpoint IN enable
EPOUTEN	0x514	Endpoint OUT enable
EPSTALL	0x518	STALL endpoints
ISOSPLIT	0x51C	Controls the split of ISO buffers
FRAMECNTR	0x520	Returns the current value of the start of frame counter
LOWPOWER	0x52C	Controls USBD peripheral low-power mode during USB suspend
ISOINCONFIG	0x530	Controls the response of the ISO IN endpoint to an IN token when no data is ready to be sent
EPIN[0].PTR	0x600	Data pointer
EPIN[0].MAXCNT	0x604	Maximum number of bytes to transfer
EPIN[0].AMOUNT	0x608	Number of bytes transferred in the last transaction
EPIN[1].PTR	0x614	Data pointer
EPIN[1].MAXCNT	0x618	Maximum number of bytes to transfer
EPIN[1].AMOUNT	0x61C	Number of bytes transferred in the last transaction
L. IIV[1].AIVIOUIVI	OVOIC	remote of bytes dufficined in the last datasetion



Register	Offset	Description
EPIN[2].PTR	0x628	Data pointer
EPIN[2].MAXCNT	0x62C	Maximum number of bytes to transfer
EPIN[2].AMOUNT	0x630	Number of bytes transferred in the last transaction
EPIN[3].PTR	0x63C	Data pointer
EPIN[3].MAXCNT	0x640	Maximum number of bytes to transfer
EPIN[3].AMOUNT	0x644	Number of bytes transferred in the last transaction
EPIN[4].PTR	0x650	Data pointer
EPIN[4].MAXCNT	0x654	Maximum number of bytes to transfer
EPIN[4].AMOUNT	0x658	Number of bytes transferred in the last transaction
EPIN[5].PTR	0x664	Data pointer
EPIN[5].MAXCNT	0x668	Maximum number of bytes to transfer
EPIN[5].AMOUNT	0x66C	Number of bytes transferred in the last transaction
EPIN[6].PTR	0x678	Data pointer
EPIN[6].MAXCNT	0x67C	Maximum number of bytes to transfer
EPIN[6].AMOUNT	0x680	Number of bytes transferred in the last transaction
EPIN[7].PTR	0x68C	Data pointer
EPIN[7].MAXCNT	0x690	Maximum number of bytes to transfer
EPIN[7].AMOUNT	0x694	Number of bytes transferred in the last transaction
ISOIN.PTR	0x6A0	Data pointer
ISOIN.MAXCNT	0x6A4	Maximum number of bytes to transfer
ISOIN.AMOUNT	0x6A8	Number of bytes transferred in the last transaction
EPOUT[0].PTR	0x700	Data pointer
EPOUT[0].MAXCNT	0x704	Maximum number of bytes to transfer
EPOUT[0].AMOUNT	0x708	Number of bytes transferred in the last transaction
EPOUT[1].PTR	0x714	Data pointer
EPOUT[1].MAXCNT	0x718	Maximum number of bytes to transfer
EPOUT[1].AMOUNT	0x71C	Number of bytes transferred in the last transaction
EPOUT[2].PTR	0x728	Data pointer
EPOUT[2].MAXCNT	0x72C	Maximum number of bytes to transfer
EPOUT[2].AMOUNT	0x730	Number of bytes transferred in the last transaction
EPOUT[3].PTR	0x73C	Data pointer
EPOUT[3].MAXCNT	0x740	Maximum number of bytes to transfer
EPOUT[3].AMOUNT	0x744	Number of bytes transferred in the last transaction
EPOUT[4].PTR	0x750	Data pointer
EPOUT[4].MAXCNT	0x754	Maximum number of bytes to transfer
EPOUT[4].AMOUNT	0x758	Number of bytes transferred in the last transaction
EPOUT[5].PTR	0x764	Data pointer
EPOUT[5].MAXCNT	0x768	Maximum number of bytes to transfer
EPOUT[5].AMOUNT	0x76C	Number of bytes transferred in the last transaction
EPOUT[6].PTR	0x778	Data pointer
EPOUT[6].MAXCNT	0x77C	Maximum number of bytes to transfer
EPOUT[6].AMOUNT	0x780	Number of bytes transferred in the last transaction
EPOUT[7].PTR	0x78C	Data pointer
EPOUT[7].MAXCNT	0x790	Maximum number of bytes to transfer
EPOUT[7].AMOUNT	0x794	Number of bytes transferred in the last transaction
ISOOUT.PTR	0x7A0	Data pointer
ISOOUT.MAXCNT	0x7A4	Maximum number of bytes to transfer
ISOOUT.AMOUNT	0x7A8	Number of bytes transferred in the last transaction

51.13.1 SHORTS

Address offset: 0x200

Shortcut register



Bit	numbe	er		31 3	0 29	9 28	27	26	25	24 2	23 2	22 2	21 2	0 1	9 18	3 17	16	15	14 :	13 1	.2 13	10	9	8	7	6 5	4	3	2	1	O
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										S	See	EVE	ENTS	S E	POD	AT/	DO	NE a	and	TAS	KS_S	STAF	RTEF	PIN[(01						
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			Enabled	1						Е	nat	ble :	shoi	rtcu	ıt																
В	RW	EPODATADONE_STARTEPO	О							S	Shor	rtcu	ıt be	etw	een	EPC	DA.	TAD	ONE	E ev	ent a	and :	STA	RTE	POL	JT[0]					
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			Disabled	0									sho	_							_				. [-]						
			Enabled	1						Е	Enak	ble :	shoi	rtcu	ıt																
С	RW	EPODATADONE_EPOSTATI	U							S	hor	rtcu	ıt be	tw	een	EPC	DA [.]	TAD	ONE	E ev	ent a	and	EPO:	STA	τυs	task	(
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			Disabled	0									sho																		
			Enabled	1						Е	nat	ble :	sho	rtcu	ıt																

51.13.2 INTEN

Address offset: 0x300

Enable or disable interrupt

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			Disabled	0							D	isa	ble																					
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В	RW	STARTED									E	nak	ble c	or d	lisak	ole	int	err	upt	t fo	r ST	AR	TEC) ev	/ent	t								
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			Disabled	0							D	isa	ble																					
			Enabled	1							E	nat	ble																					
С	RW	ENDEPINO									Е	nat	ble c	or d	lisak	ole	int	err	upt	t fo	r EN	NDE	PIN	1[0]	ev	ent								
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			Enabled	1							Е	nak	ble																					
D	RW	ENDEPIN1									E	nak	ble c	or d	lisak	ole	int	err	upt	t fo	r EN	NDE	PIN	l[1]	ev(ent								
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			Disabled	0							D	isa	ble																					
			Enabled	1							E	nat	ble																					
E	RW	ENDEPIN2									E	nak	ble c	or d	lisak	ole	int	err	upt	t fo	r EN	NDE	PIN	I[2]	ev	ent								
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			Disabled	0							D	isa	ble																					
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Id	RW	Field	Value Id	Value	:				Description
F	RW	ENDEPIN3							Enable or disable interrupt for ENDEPIN[3] event
									See EVENTS_ENDEPIN[3]
			Disabled	0					Disable
			Enabled	1					Enable
G	RW	ENDEPIN4							Enable or disable interrupt for ENDEPIN[4] event
									See EVENTS_ENDEPIN[4]
			Disabled	0					Disable
			Enabled	1					Enable
Н	RW	ENDEPIN5							Enable or disable interrupt for ENDEPIN[5] event
									See EVENTS_ENDEPIN[5]
			Disabled	0					Disable
			Enabled	1					Enable
I	RW	ENDEPIN6							Enable or disable interrupt for ENDEPIN[6] event
									See EVENTS_ENDEPIN[6]
			Disabled	0					Disable
			Enabled	1					Enable
J	RW	ENDEPIN7							Enable or disable interrupt for ENDEPIN[7] event
									See EVENTS_ENDEPIN[7]
			Disabled	0					Disable
			Enabled	1					Enable
K	RW	EPODATADONE							Enable or disable interrupt for EPODATADONE event
									See EVENTS_EPODATADONE
			Disabled	0					Disable
			Enabled	1					Enable
L	RW	ENDISOIN							Enable or disable interrupt for ENDISOIN event
									See EVENTS_ENDISOIN
			Disabled	0					Disable
			Enabled	1					Enable
М	RW	ENDEPOUTO							Enable or disable interrupt for ENDEPOUT[0] event
									See EVENTS_ENDEPOUT[0]
			Disabled	0					Disable
			Enabled	1					Enable
N	RW	ENDEPOUT1							Enable or disable interrupt for ENDEPOUT[1] event
									See EVENTS_ENDEPOUT[1]
			Disabled	0					Disable
			Enabled	1					Enable
0	RW	ENDEPOUT2							Enable or disable interrupt for ENDEPOUT[2] event
									See EVENTS_ENDEPOUT[2]
			Disabled	0					Disable
			Enabled	1					Enable
Р	RW	ENDEPOUT3							Enable or disable interrupt for ENDEPOUT[3] event
									See EVENTS_ENDEPOUT[3]
			Disabled	0					Disable
			Enabled	1					Enable
Q	RW	ENDEPOUT4							Enable or disable interrupt for ENDEPOUT[4] event
									See EVENTS_ENDEPOUT[4]
			Disabled	0					Disable
			Enabled	1					Enable
R	RW	ENDEPOUT5							Enable or disable interrupt for ENDEPOUT[5] event
									See EVENTS_ENDEPOUT[5]



Bit r	numbe	er		31 30	29	28 2	7 26	5 25	24	23	3 22 21	2	0 19	18	3 17	7 1	6 1	L5 1	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 (
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Id	RW	Field	Value Id	Value						De	escript	ion	1																			
			Disabled	0						Di	sable																					
			Enabled	1						En	nable																					
S	RW	ENDEPOUT6								En	nable o	r d	lisab	le i	nte	rru	ıpt	for	EI	ND	EPO	UT	[6]	eve	nt							
										Se	e <i>EVEI</i>	VTS	S_EN	NDE	PO	UT	[6]															
			Disabled	0						Di	sable																					
			Enabled	1						En	nable																					
Т	RW	ENDEPOUT7								En	nable o	r d	lisab	le i	nte	rru	ıpt	for	El	ND	EPO	UT	[7] 6	eve	nt							
										Se	e <i>EVEI</i>	VTS	S_EN	NDE	PO	UT	[7]	1														
			Disabled	0						Di	sable																					
			Enabled	1						En	nable																					
U	RW	ENDISOOUT								En	nable o	r d	isab	le i	nte	rru	ıpt	for	EI	ND	SOC	DU.	Γev	ent	t							
										Se	e <i>EVEI</i>	VTS	S_EN	I DI	soc	שכ	Т															
			Disabled	0						Di	sable																					
			Enabled	1						En	nable																					
V	RW	SOF								En	nable o	r d	lisab	le i	nte	rru	ıpt	for	· S()F	eve	nt										
										Se	e <i>EVEI</i>	VTS	s_sc)F																		
			Disabled	0						Di	sable																					
			Enabled	1						En	nable																					
W	RW	USBEVENT								En	nable o	r d	lisab	le i	nte	rru	ıpt	for	· U	SBE	VEI	NT	eve	nt								
										Se	e <i>EVEI</i>	VTS	s_us	SBE	VEN	VΤ																
			Disabled	0						Di	sable																					
			Enabled	1						En	nable																					
Χ	RW	EPOSETUP								En	nable o	r d	lisab	le i	nte	rru	ıpt	for	El	209	ETL	JP e	ever	nt								
										Se	e <i>EVEI</i>	VTS	S_EF	205	ETU	ΙP																
			Disabled	0						Di	sable																					
			Enabled	1						En	nable																					
Υ	RW	EPDATA								En	nable o	r d	lisab	le i	nte	rru	ıpt	for	EI	PDA	ATA	eve	ent									
										Se	e <i>EVEI</i>	VTS	S EF	DA	TA																	
			Disabled	0							sable		-																			
			Enabled	1						En	nable																					
Z	RW	ACCESSFAULT								En	nable o	r d	lisab	le i	nte	rru	ıpt	for	A	CCI	SSF	AU	ILT 6	eve	nt							
										Se	e <i>EVEI</i>	VTS	s Ac	CCE	SSF	AL	JLT															
			Disabled	0							sable		_																			
			Enabled	1						En	nable																					

51.13.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		3	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14 1	.3 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id								Z	Υ	Χ	W	٧	U	Т	S	R	Q	Р	0 1	N N	1 L	K	J	1	Н	G	F	E I	С	В	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0
Id RW Field	Value Id	٧	alue	•						De	scri	ptic	on																		
A RW USBRESET										W	rite	'1' t	:o E	nab	le i	nte	rru	ot f	or U	SBR	ESE'	Γev	ent								
										Se	e <i>EV</i>	ΈN	TS_	USI	BRE	SET															
	Set	1								En	able	•																			
	Disabled	0								Re	ad:	Disa	able	ed																	
	Enabled	1								Re	ad:	Ena	ble	d																	
B RW STARTED										W	rite	'1' t	o E	nab	le i	nte	rru	ot f	or S	TAR	TED	eve	nt								
										Se	e <i>EV</i>	ΈN	TS_	ST/	RT	ED															



Bit r	numbe	r		31 30	29	28	27 2	26 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								Z	<u> </u>	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0	0	0	0 (0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Valu	9					Description
			Set	1						Enable
			Disabled	0						Read: Disabled
_	DVA	ENDEPINO	Enabled	1						Read: Enabled
С	KVV	ENDEPINO								Write '1' to Enable interrupt for ENDEPIN[0] event
			Set	1						See EVENTS_ENDEPIN[0] Enable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
D	RW	ENDEPIN1								Write '1' to Enable interrupt for ENDEPIN[1] event
										See EVENTS_ENDEPIN[1]
			Set	1						Enable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
E	RW	ENDEPIN2								Write '1' to Enable interrupt for ENDEPIN[2] event
										See EVENTS_ENDEPIN[2]
			Set	1						Enable
			Disabled	0						Read: Disabled
_			Enabled	1						Read: Enabled
F	RW	ENDEPIN3								Write '1' to Enable interrupt for ENDEPIN[3] event
										See EVENTS_ENDEPIN[3]
			Set	1						Enable
			Disabled	0						Read: Disabled
G	RW	ENDEPIN4	Enabled	1						Read: Enabled Write '1' to Enable interrupt for ENDEPIN[4] event
Ū										
			Set	1						See EVENTS_ENDEPIN[4] Enable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Н	RW	ENDEPIN5								Write '1' to Enable interrupt for ENDEPIN[5] event
										See EVENTS_ENDEPIN[5]
			Set	1						Enable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
I	RW	ENDEPIN6								Write '1' to Enable interrupt for ENDEPIN[6] event
										See EVENTS_ENDEPIN[6]
			Set	1						Enable
			Disabled	0						Read: Disabled
	D\A/	ENDEDIN7	Enabled	1						Read: Enabled Write 11 to Enable interrupt for ENDEDIN[7] event
J	KVV	ENDEPIN7								Write '1' to Enable interrupt for ENDEPIN[7] event
			Cot	1						See EVENTS_ENDEPIN[7]
			Set Disabled	0						Enable Read: Disabled
			Enabled Enabled	1						Read: Enabled
K	RW	EPODATADONE		_						Write '1' to Enable interrupt for EPODATADONE event
										See EVENTS_EPODATADONE
			Set	1						Enable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
L	RW	ENDISOIN								Write '1' to Enable interrupt for ENDISOIN event
										See EVENTS_ENDISOIN
			Set	1						Enable



Bitı	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
М	RW ENDEPOUTO		Write '1' to Enable interrupt for ENDEPOUT[0] event
			See EVENTS_ENDEPOUT[0]
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
N	RW ENDEPOUT1		Write '1' to Enable interrupt for ENDEPOUT[1] event
			See EVENTS_ENDEPOUT[1]
		Set	1 Enable
		Disabled	0 Read: Disabled
	DIM ENDEDOUTS	Enabled	1 Read: Enabled
0	RW ENDEPOUT2		Write '1' to Enable interrupt for ENDEPOUT[2] event
			See EVENTS_ENDEPOUT[2]
		Set	1 Enable
		Disabled	0 Read: Disabled
Р	DW ENDEROUTS	Enabled	1 Read: Enabled
Р	RW ENDEPOUT3		Write '1' to Enable interrupt for ENDEPOUT[3] event
			See EVENTS_ENDEPOUT[3]
		Set	1 Enable
		Disabled	0 Read: Disabled
Q	RW ENDEPOUT4	Enabled	1 Read: Enabled Write '1' to Enable interrupt for ENDEPOUT[4] event
Q	NW ENDERGOTT		
		6.1	See EVENTS_ENDEPOUT[4]
		Set Disabled	1 Enable 0 Read: Disabled
		Enabled	1 Read: Enabled
R	RW ENDEPOUT5	Endored	Write '1' to Enable interrupt for ENDEPOUT[5] event
		Set	See EVENTS_ENDEPOUT[5] 1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
S	RW ENDEPOUT6		Write '1' to Enable interrupt for ENDEPOUT[6] event
			See EVENTS_ENDEPOUT[6]
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
Т	RW ENDEPOUT7		Write '1' to Enable interrupt for ENDEPOUT[7] event
			See EVENTS_ENDEPOUT[7]
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
U	RW ENDISOOUT		Write '1' to Enable interrupt for ENDISOOUT event
			See EVENTS_ENDISOOUT
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
V	RW SOF		Write '1' to Enable interrupt for SOF event
			See EVENTS_SOF
		Set	1 Enable
		Disabled	0 Read: Disabled



Bit n	numbe	er		31 30 29 28 27 26 25 24	\$ 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				ΖY	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Enabled	1	Read: Enabled
W	RW	USBEVENT			Write '1' to Enable interrupt for USBEVENT event
					See EVENTS_USBEVENT
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Х	RW	EPOSETUP			Write '1' to Enable interrupt for EPOSETUP event
					See EVENTS_EPOSETUP
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Υ	R\M/	EPDATA	Lilabica	1	Write '1' to Enable interrupt for EPDATA event
	11.44	LIDAIA			
					See EVENTS_EPDATA
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Z	RW	ACCESSFAULT			Write '1' to Enable interrupt for ACCESSFAULT event
					See EVENTS_ACCESSFAULT
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

51.13.4 INTENCLR

Address offset: 0x308

Disable interrupt

•			
Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		Z	Y X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW USBRESET			Write '1' to Disable interrupt for USBRESET event
			See EVENTS_USBRESET
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW STARTED			Write '1' to Disable interrupt for STARTED event
			See EVENTS_STARTED
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW ENDEPINO			Write '1' to Disable interrupt for ENDEPIN[0] event
			See EVENTS_ENDEPIN[0]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW ENDEPIN1			Write '1' to Disable interrupt for ENDEPIN[1] event
			See EVENTS ENDEPIN[1]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW ENDEPIN2			Write '1' to Disable interrupt for ENDEPIN[2] event



Rit r	number			31 30 29 2	8 27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	idilibei			31 30 23 20			X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0000	0000		0 0 0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Fie	ld	Value Id	Value			Description
							See EVENTS_ENDEPIN[2]
			Clear	1			Disable
			Disabled	0			Read: Disabled
			Enabled	1			Read: Enabled
F	RW EN	DEPIN3					Write '1' to Disable interrupt for ENDEPIN[3] event
							See EVENTS_ENDEPIN[3]
			Clear	1			Disable
			Disabled	0			Read: Disabled
			Enabled	1			Read: Enabled
G	RW EN	DEPIN4					Write '1' to Disable interrupt for ENDEPIN[4] event
							See EVENTS_ENDEPIN[4]
			Clear	1			Disable
			Disabled	0			Read: Disabled
			Enabled	1			Read: Enabled
Н	RW EN	DEPIN5					Write '1' to Disable interrupt for ENDEPIN[5] event
							See EVENTS_ENDEPIN[5]
			Clear	1			Disable
			Disabled	0			Read: Disabled
			Enabled	1			Read: Enabled
T	RW EN	DEPIN6					Write '1' to Disable interrupt for ENDEPIN[6] event
							See EVENTS_ENDEPIN[6]
			Clear	1			Disable
			Disabled	0			Read: Disabled
			Enabled	1			Read: Enabled
J	RW EN	DEPIN7					Write '1' to Disable interrupt for ENDEPIN[7] event
							See EVENTS_ENDEPIN[7]
			Clear	1			Disable
			Disabled	0			Read: Disabled
			Enabled	1			Read: Enabled
K	RW EPO	DATADONE					Write '1' to Disable interrupt for EPODATADONE event
							See EVENTS_EPODATADONE
			Clear	1			Disable
			Disabled	0			Read: Disabled
			Enabled	1			Read: Enabled
L	RW EN	DISOIN					Write '1' to Disable interrupt for ENDISOIN event
							See EVENTS_ENDISOIN
			Clear	1			Disable
			Disabled	0			Read: Disabled
			Enabled	1			Read: Enabled
М	RW EN	DEPOUTO					Write '1' to Disable interrupt for ENDEPOUT[0] event
							See EVENTS_ENDEPOUT[0]
			Clear	1			Disable
			Disabled	0			Read: Disabled
			Enabled	1			Read: Enabled
N	RW EN	DEPOUT1					Write '1' to Disable interrupt for ENDEPOUT[1] event
							See EVENTS_ENDEPOUT[1]
			Clear	1			Disable
			Disabled	0			Read: Disabled
			Enabled	1			Read: Enabled
0	RW EN	DEPOUT2					Write '1' to Disable interrupt for ENDEPOUT[2] event

See EVENTS_ENDEPOUT[2]



Bit r	numbe	er		31	30 2	9 2	8 27	26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									Z Y	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Res		0000000		0	0 (0 0	0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Val	ıe					Description
			Clear	1						Disable disabl
			Disabled Enabled	1						Read: Disabled Read: Enabled
Р	R\M/	ENDEPOUT3	спаріец	1						Write '1' to Disable interrupt for ENDEPOUT[3] event
•	11.00	ENDERGOTS								
										See EVENTS_ENDEPOUT[3]
			Clear Disabled	1						Disable Read: Disabled
			Enabled	1						Read: Enabled
Q	RW	ENDEPOUT4	Lindoled	-						Write '1' to Disable interrupt for ENDEPOUT[4] event
-										
			Clear	1						See EVENTS_ENDEPOUT[4] Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
R	RW	ENDEPOUT5								Write '1' to Disable interrupt for ENDEPOUT[5] event
										See EVENTS ENDEPOUT[5]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
S	RW	ENDEPOUT6								Write '1' to Disable interrupt for ENDEPOUT[6] event
										See EVENTS_ENDEPOUT[6]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Т	RW	ENDEPOUT7								Write '1' to Disable interrupt for ENDEPOUT[7] event
										See EVENTS_ENDEPOUT[7]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
U	RW	ENDISOOUT								Write '1' to Disable interrupt for ENDISOOUT event
										See EVENTS_ENDISOOUT
			Clear	1						Disable
			Disabled	0						Read: Disabled
.,	DVA	COL	Enabled	1						Read: Enabled
V	KVV	SOF								Write '1' to Disable interrupt for SOF event
										See EVENTS_SOF
			Clear	1						Disable
			Disabled Enabled	0						Read: Disabled Read: Enabled
W	RW	USBEVENT	Lilabled	1						Write '1' to Disable interrupt for USBEVENT event
			Clear	1						See EVENTS_USBEVENT Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Χ	RW	EPOSETUP								Write '1' to Disable interrupt for EPOSETUP event
										See EVENTS_EPOSETUP
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Υ	RW	EPDATA								Write '1' to Disable interrupt for EPDATA event
										See EVENTS_EPDATA
			Clear	1						Disable



Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		2	Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
Z RW ACCESSFAULT			Write '1' to Disable interrupt for ACCESSFAULT event
			See EVENTS_ACCESSFAULT
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

51.13.5 EVENTCAUSE

Address offset: 0x400

Details on event that caused the USBEVENT event

Dia.	number		21 20 20 27 27 27 27 24 22 22 24 20 10 10 17 17 17 14 12 12 14 10 0 0 0 7 7 7 7 7 1 1 0
	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E C B A
Res	et 0x00000000		$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$
Id	RW Field	Value Id	Value Description
Α	RW ISOOUTCRC		CRC error was detected on isochronous OUT endpoint 8. Write
			'1' to clear.
		NotDetected	0 No error detected
		Detected	1 Error detected
В	RW SUSPEND		Signals that the USB lines have been seen idle long enough for
			the device to enter suspend. Write '1' to clear.
		NotDetected	0 Suspend not detected
		Detected	1 Suspend detected
С	RW RESUME		Signals that a RESUME condition (K state or activity restart) has
			been detected on the USB lines. Write '1' to clear.
		NotDetected	0 Resume not detected
		Detected	1 Resume detected
Ε	RW READY		Wrapper has re-initialized SFRs to the proper values. MAC is
			ready for normal operation. Write '1' to clear.
		NotDetected	0 USBEVENT was not issued due to USBD peripheral ready
		Ready	1 USBD peripheral is ready

51.13.6 BUSSTATE

Address offset: 0x404

Provides the logic state of the D+ and D- lines

Bit	numbe	er		31 3	0 29	9 2	28 2	27 :	26	25	24	23	22	21	. 20	19	18	3 17	7 16	15	14	13	12	11 :	10 9	9 8	7	6	5	4	3	2	1 0
Id																																	ВА
Res	et 0x0	0000000		0	0 0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ie							De	scri	ipti	ion																		
Α	R	DM										Sta	ite	of t	the	D-	line	•															
			Low	0								Lov	N																				
			High	1								Hig	gh																				
В	R	DP										Sta	ite	of t	the	D+	line	9															
			Low	0								Lov	N																				
			High	1								Hig	gh																				

51.13.7 HALTED.EPIN[0]

Address offset: 0x420

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.



Bit	numbe	er		3	1 30	29	28	3 27	7 26	5 25	5 24	23	22	21	20	19	18	17	16	15	14	13 :	L2 1	1 1	0 9	8	7	6	5	4	3	2	1	0
Id																				Α	Α	Α	A A	Δ	Α Α	A	Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id							De	scri	ptic	n																					
Α	R	GETSTATUS								IN	end	lpoi	nt ł	halt	ed:	stat	us.	Ca	n be	e us	ed a	ıs is	as r	esp	ons	e to	а							
												Ge	tSta	itus	() r	equ	est	to	enc	dpo	int.													
			NotHalted							En	dpo	int i	is n	ot h	nalt	ed																		
			Halted	1								En	dpo	int i	is h	alte	d																	

51.13.8 HALTED.EPIN[1]

Address offset: 0x424

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit	numbe	r		31	1 30	29	28	27	26	25	24	23 2	22 2	1 2	0 1	9 1	8 1	7 16	15	14	13	12	11 1	LO !	8	7	6	5	4	3	2	1 0
Id																			Α	Α	Α	Α	Α .	A ,	Α Α	. A	Α	Α	Α	Α	Α	А А
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 Value							0	0	0 (0 (0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value [Des	crip	tio	n																		
Α	R	GETSTATUS									IN e	ndp	oin	ıt ha	lte	d st	atus	. Ca	an b	e u	sed	as is	as	resp	ons	se to	о а					
												Get	Stat	us() red	que	st t	o er	dpo	oint												
			NotHalted	0								End	ioq	nt is	s no	t ha	alte	b														
			Halted	1								End	poir	nt is	hal	tec	ł															

51.13.9 HALTED.EPIN[2]

Address offset: 0x428

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit	numbe	er		3	1 30	29	9 28	8 27	7 26	5 25	5 24	23	22	21	20	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id																				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 А
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id									De	scri	ptio	n																			
Α	R	GETSTATUS		Value								IN	end	poi	nt h	alte	ed s	stat	us.	Cai	n b	e us	sed	as i	s as	re	spo	nse	to	а				
												Ge	tSta	itus	() re	equ	est	to	enc	lpo	int.													
			NotHalted	0								En	dpo	int i	s n	ot h	alte	ed																
			Halted	1								En	dpo	int i	s h	alte	d																	

51.13.10 HALTED.EPIN[3]

Address offset: 0x42C

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit	numb	er		3	1 30	29	9 2	8 2	7 2	6 2	5 2	24 2	23 2	2 2	1 2	0 1	9 1	8 1	7 16	5 1	5 1	1 13	3 12	11	10	9	8	7	6	5	4	3	2 1	L 0
Id																				Δ	. 4	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A
Re	set 0x0	0000000		0	0	0	0	0) (0 (0 (0	0 (0 () (0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 0 Value							1	Desc	rip	tior	١																			
Α	R	GETSTATUS		Value							ı	N er	ndp	oin	t ha	lte	d st	atu	s. C	an	be ι	ısed	as	is as	re	spo	nse	to	а					
												(GetS	tat	us()	rec	que	st t	o er	ndp	oin	t.												
			NotHalted	0)							1	Endp	ooir	nt is	no	t ha	lte	d															
			Halted	1								E	Endp	ooir	nt is	hal	tec	i																

51.13.11 HALTED.EPIN[4]

Address offset: 0x430

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.



Bit	numb	er		3	1 30	29	28	3 27	7 26	5 25	24	23	22 2	21 2	0 1	9 1	8 1	7 16	15	14	13 3	.2 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id																			Α	Α	Α	4 Δ	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Re	et 0x0	0000000		0 0 0 0 0 0 0 Value							0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id								Des	crip	tio	1																		
Α	R	GETSTATUS									IN e	endp	ooin	t ha	lte	d st	atus	. Ca	n b	e us	ed a	s is a	ıs re	espo	nse	to	a					
												Get	Stat	tus()	rec	que	st t	o en	dpc	int.												
			NotHalted	0								End	poi	nt is	no	t ha	lte	t														
			Halted	1								End	poi	nt is	hal	ted																

51.13.12 HALTED.EPIN[5]

Address offset: 0x434

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit	numbe	r		31	1 30	29	28	27	26	25	24	23 2	22 2	1 2	0 1	9 1	8 1	7 16	15	14	13	12	11 1	LO !	8	7	6	5	4	3	2	1 0
Id																			Α	Α	Α	Α	Α .	A ,	Α Α	. A	Α	Α	Α	Α	Α	А А
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 Value							0	0	0 (0 (0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value [Des	crip	tio	n																		
Α	R	GETSTATUS									IN e	ndp	oin	ıt ha	lte	d st	atus	. Ca	an b	e u	sed	as is	as	resp	ons	se to	о а					
												Get	Stat	us() red	que	st t	o er	dpo	oint												
			NotHalted	0								End	ioq	nt is	s no	t ha	alte	b														
			Halted	1								End	poir	nt is	hal	tec	ł															

51.13.13 HALTED.EPIN[6]

Address offset: 0x438

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit	numbe	er		3	1 30	29	9 28	8 2	7 2	6 2	5 2	24 2	23 2	2 2	1 2	0 1	9 1	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Re	et 0x0	0000000		0	0	0	0	0) (0 (0 (0	0 (0 (0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id									Desc	crip	tio	1																					
Α	R	GETSTATUS										ı	IN e	ndp	oin	t ha	alte	ed s	tat	us.	Ca	n b	e u	sed	as i	is as	s re	spo	nse	to	а					
												(GetS	Stat	us()	re	que	est	to e	enc	lpo	int.														
			NotHalted	0								1	Endp	ooir	nt is	no	t h	alte	ed																	
			Halted	1								1	Endp	ooir	nt is	ha	lte	d																		

51.13.14 HALTED.EPIN[7]

Address offset: 0x43C

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit	numbe	er		33	1 30	29	28	27	26	5 25	5 24	23	22	21 2	20 :	19 1	18 1	17 1	.6 1	15 1	L4 1	3 12	2 11	10	9	8	7	6	5	4	3	2	1 0
Id																				Α .	Α.	Δ Δ	. A	Α	Α	Α	Α	Α	Α	Α	Α	A ,	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 0 0 Value							De	scri	ptio	n																			
Α	R	GETSTATUS										IN	end	poir	nt h	alte	ed s	tatı	ıs. (Can	be	use	d as	is a	s re	spc	nse	e to	а				
												Ge	tSta	tus(() re	eque	est '	to e	nd	poi	nt.												
			NotHalted	0								En	dpo	int i	s no	ot h	alte	ed															
			Halted	1								En	dpo	int i	s ha	alte	d																

51.13.15 HALTED.EPOUT[0]

Address offset: 0x444

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.



Bit	numbe	er		3	1 30	29	28	8 27	7 20	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12 :	11 1	0 9	9 8	7	6	5	4	3	2	1	0
Id																				Α	Α	Α	Α	Α /	Δ Α	A A	. Δ	. A	Α	Α	Α	Α	Α	Α
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 0 Value							De	escri	iptic	on																				
Α	R	GETSTATUS										Οl	JT e	ndp	oir	nt h	alte	ed s	tatı	ıs. (Can	be	use	d as	is a	as re	espo	onse	e to	а				
												Ge	etSta	atus	() r	equ	est	to	end	dpo	int.													
			NotHalted	0)							En	dpc	int	is n	ot l	nalt	ed																
			Halted	1								En	dpc	int	is h	alte	ed																	

51.13.16 HALTED.EPOUT[1]

Address offset: 0x448

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit	numbe	er		31	1 30	29	28	27 2	26 2	25 :	24	23 2	2 21	20	19	18	17	16	15	14 1	.3 1	2 11	. 10	9	8	7	6	5	4	3	2	1 0
Id																			Α	Α	Α /	A A	Α	Α	Α	Α	Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id								Des	cripti	ion																			
Α	R	GETSTATUS									OUT	end	poi	nt h	alte	ed s	tatı	ıs. (Can	be u	sed	as i	s as	res	por	ıse	to a	а				
												Get:	Statu	ıs()	requ	ıest	to	end	lpo	int.												
			NotHalted	0								End	ooint	t is	not l	halt	ted															
			Halted	1								End	ooint	t is	halte	ed																

51.13.17 HALTED.EPOUT[2]

Address offset: 0x44C

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit r	iumbe	er		31	1 30	29	28	27	26	25	24	23 2	22 2	1 2	0 19	9 18	8 17	7 16	15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id																			Α	Α	Α	A	4 Δ	. A	Α	Α	Α	Α	Α	A A	Α Α	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Value							Des	crip	tior	1																		
Α	R	GETSTATUS										OUT	en	dpo	int	halt	ted	stat	us.	Can	be	use	d as	is a	s res	spoi	nse	to a	9			
												Get	Stat	us()	rec	que	st to	en	dpc	int.												
			NotHalted	0								End	poir	nt is	not	t ha	ltec	l														
			Halted	1								End	poir	nt is	hal	ted																

51.13.18 HALTED.EPOUT[3]

Address offset: 0x450

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit	numb	er		3	1 30	29	28	3 27	7 26	5 25	5 24	1 23	22	21	20	19	18	17	16	15	14	13	12 1	.1 1	9	8	7	6	5	4	3	2	1	0
Id																				Α	Α	Α	A .	4 Α	A	A	Α	Α	Α	Α	Α	Α	Α	Α
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0								De	escri	iptic	on																			
Α	R	GETSTATUS		Value								Οl	JT e	ndp	oin	nt ha	alte	d s	tatı	ıs. (Can	be	use	d as	is a	s re	spo	nse	to	a				
												Ge	etSta	atus	() r	equ	est	to	end	dpo	int.													
			NotHalted	0								En	dpc	int	is n	ot h	nalt	ed																
			Halted	1								En	dpc	int	is h	alte	ed																	

51.13.19 HALTED.EPOUT[4]

Address offset: 0x454

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.



Bit	numbe	er		3	1 30	29	28	8 27	7 20	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12 :	11 1	0 9	9 8	7	6	5	4	3	2	1	0
Id																				Α	Α	Α	Α	Α /	Δ Α	A A		. A	Α	Α	Α	Α	Α	Α
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 0 Value							De	escri	iptic	on																				
Α	R	GETSTATUS										Οl	JT e	ndp	oir	nt h	alte	ed s	tatı	ıs. (Can	be	use	d as	is a	as re	espo	onse	e to	а				
												Ge	etSta	atus	() r	equ	est	to	end	dpo	int.													
			NotHalted	0)							En	dpc	int	is n	ot l	nalt	ed																
			Halted	1								En	dpc	int	is h	alte	ed																	

51.13.20 HALTED.EPOUT[5]

Address offset: 0x458

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit	numbe	er		31	1 30	29	28	27 2	26 2	25 :	24	23 2	2 21	20	19	18	17	16	15	14 1	.3 1	2 11	. 10	9	8	7	6	5	4	3	2	1 0
Id																			Α	Α	Α /	A A	Α	Α	Α	Α	Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							Des	cripti	ion																		
Α	R	GETSTATUS										OUT	end	poi	nt h	alte	ed s	tatı	ıs. (Can	be u	sed	as i	s as	res	por	ıse	to a	а			
												Get:	Statu	ıs()	requ	ıest	to	end	lpo	int.												
			NotHalted	0								End	ooint	t is	not l	halt	ted															
			Halted	1								End	ooint	t is	halte	ed																

51.13.21 HALTED.EPOUT[6]

Address offset: 0x45C

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit	numbe	er		3	1 30	29	28	3 27	26	5 25	24	23	22	21 2	20 1	9 1	.8 1	7 1	6 1	5 1	4 1	3 12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id																			A	\ <i>A</i>	λ Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α /	4 A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0) C) (0	0	0	0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	V	alue	:						Des	scri	otio	n																		
Α	R	GETSTATUS										ΟÚ	T er	ndp	oint	ha	lted	sta	tus	. Ca	an b	e us	ed a	as is	as	res	oon	se t	to a	ı			
												Get	tSta	tus() re	que	est t	o e	ndp	oin	ıt.												
			NotHalted	0								Enc	ioqb	nt i	s no	t h	alte	d															
			Halted	1								Enc	ioqt	nt i	s ha	lte	b																

51.13.22 HALTED.EPOUT[7]

Address offset: 0x460

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit	numb	er		3	1 30	29	28	8 27	7 26	5 25	5 24	23	22 2	21 2	0 19	9 18	8 17	⁷ 16	15	14	13	12 3	11 1	0 9	8 (7	6	5	4	3	2	1 0
Id																			Α	Α	Α	Α	A A	A 4	Α Α	Α	Α	Α	Α	Α	Α	А А
Re	set 0x(0000000		0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	٧	/alue	9						Des	crip	tio	1																	
Α	R	GETSTATUS										OU'	T en	dpc	int	halt	ted	stat	us.	Car	be	use	d as	is a	is re	spc	nse	to	а			
												Get	Stat	us()	rec	ue:	st to	en	dpc	int.												
			NotHalted	0)							End	lpoi	nt is	not	: ha	ltec	l														
			Halted	1								End	lpoi	nt is	hal	ted																

51.13.23 EPSTATUS

Address offset: 0x468

Provides information on which endpoint's EasyDMA registers have been captured



Bit r	numbe	er		31 3	0 29	28	27 2	26 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									R	Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0	0	0	0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Valu	e					Description
Α	RW	EPIN0								Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
В	RW	EPIN1								Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
С	RW	EPIN2								Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
D	RW	EPIN3								Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
Ε	RW	EPIN4								Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
F	RW	EPIN5								Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
G	RW	EPIN6								Endpoint's EasyDMA registers captured state. Write '1' to clear.
-			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
н	RW	EPIN7	Databone	-						Endpoint's EasyDMA registers captured state. Write '1' to clear.
	11.00	LI IIV/	NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
1	D\A/	EPIN8	Databolie	_						Endpoint's EasyDMA registers captured state. Write '1' to clear.
'	NVV	EFINO	NaData	0						
			NoData							EasyDMA registers have not been captured for this endpoint
	DVA	FROUTO	DataDone	1						EasyDMA registers have been captured for this endpoint
J	KVV	EPOUT0	N. B.	•						Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
.,			DataDone	1						EasyDMA registers have been captured for this endpoint
K	RW	EPOUT1		_						Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
L	RW	EPOUT2								Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
М	RW	EPOUT3								Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
N	RW	EPOUT4								Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
0	RW	EPOUT5								Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
Р	RW	EPOUT6								Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
Q	RW	EPOUT7								Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
R	RW	EPOUT8								Endpoint's EasyDMA registers captured state. Write '1' to clear.
			NoData	0						EasyDMA registers have not been captured for this endpoint
			DataDone	1						EasyDMA registers have been captured for this endpoint
			Databone	_						Lasy Diving registers have been captured for this enuponit



51.13.24 EPDATASTATUS

Address offset: 0x46C

Provides information on which endpoint(s) an acknowledged data transfer has occurred (EPDATA event)

3it r d	numbe	er 		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 N M L K J I H G F E D C B A
	et 0x0	0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
d		Field	Value Id	Value	Description
Δ.		EPIN1			Acknowledged data transfer on this IN endpoint. Write '1' to
					clear.
			NotDone	0	No acknowledged data transfer on this endpoint
			DataDone	1	Acknowledged data transfer on this endpoint has occurred
3	RW	EPIN2			Acknowledged data transfer on this IN endpoint. Write '1' to
					clear.
			NotDone	0	No acknowledged data transfer on this endpoint
			DataDone	1	Acknowledged data transfer on this endpoint has occurred
2	RW	EPIN3			Acknowledged data transfer on this IN endpoint. Write '1' to
					clear.
			NotDone	0	No acknowledged data transfer on this endpoint
			DataDone	1	Acknowledged data transfer on this endpoint has occurred
)	RW	EPIN4			Acknowledged data transfer on this IN endpoint. Write '1' to
					clear.
			NotDone	0	No acknowledged data transfer on this endpoint
			DataDone	1	Acknowledged data transfer on this endpoint has occurred
	RW	EPIN5			Acknowledged data transfer on this IN endpoint. Write '1' to
					clear.
			NotDone	0	No acknowledged data transfer on this endpoint
			DataDone	1	Acknowledged data transfer on this endpoint has occurred
	RW	EPIN6			Acknowledged data transfer on this IN endpoint. Write '1' to
					clear.
			NotDone	0	No acknowledged data transfer on this endpoint
_			DataDone	1	Acknowledged data transfer on this endpoint has occurred
3	RW	EPIN7			Acknowledged data transfer on this IN endpoint. Write '1' to .
					clear.
			NotDone	0	No acknowledged data transfer on this endpoint
	D\A/	FDOUT1	DataDone	1	Acknowledged data transfer on this endpoint has occurred
1	RW	EPOUT1			Acknowledged data transfer on this OUT endpoint. Write '1' to
			NatCtartad	0	clear.
			NotStarted Started	0	No acknowledged data transfer on this endpoint
	D\A/	EPOUT2	Started	1	Acknowledged data transfer on this endpoint has occurred Acknowledged data transfer on this OUT endpoint. Write '1' to
	I VV	EPOOTZ			clear.
			NotStarted	0	No acknowledged data transfer on this endpoint
			Started	1	Acknowledged data transfer on this endpoint has occurred
	RW	EPOUT3	Started	1	Acknowledged data transfer on this OUT endpoint. Write '1' to
		21 0013			clear.
			NotStarted	0	No acknowledged data transfer on this endpoint
			Started	1	Acknowledged data transfer on this endpoint has occurred
(RW	EPOUT4		-	Acknowledged data transfer on this OUT endpoint. Write '1' to
					clear.
			NotStarted	0	No acknowledged data transfer on this endpoint
			Started	1	Acknowledged data transfer on this endpoint has occurred
_	RW	EPOUT5			Acknowledged data transfer on this OUT endpoint. Write '1' to
					clear.
			NotStarted	0	No acknowledged data transfer on this endpoint
			Started	1	Acknowledged data transfer on this endpoint has occurred
					- '
M	RW	EPOUT6			Acknowledged data transfer on this OUT endpoint. Write '1' to



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		N M L K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	NotStarted	0 No acknowledged data transfer on this endpoint
	Started	1 Acknowledged data transfer on this endpoint has occurred
N RW EPOUT7		Acknowledged data transfer on this OUT endpoint. Write '1' to
		clear.
	NotStarted	0 No acknowledged data transfer on this endpoint
	Started	1 Acknowledged data transfer on this endpoint has occurred

51.13.25 USBADDR

Address offset: 0x470 Device USB address

Bi	t nu	ımbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1	0
Id																														Α	Α	Α	Α	Α	Α	Α
Re	eset	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id		RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α		R	ADDR										De	vice	US	Ва	ddı	ress	5																	_

51.13.26 BMREQUESTTYPE

Address offset: 0x480

SETUP data, byte 0, bmRequestType

Bit r	iumbe	er		31 3	30 29	28 27	7 26	25 24	23 22	2 21 2	0 19	18	17	16	15 1	4 13	12	11 1	0 9	8	7	6	5 4	3	2	1 0
Id																					С	В	ВА	А	Α	A A
Res	et 0x0	0000000		0	0 0	0 0	0	0 0	0 0	0 (0	0	0	0	0 0	0	0	0 (0	0	0	0	0 (0	0	0 0
Id	RW	Field	Value Id	Valu	ıe				Desc	riptior	1															
Α	R	RECIPIENT							Data	transf	er ty	/pe														
			Device	0					Devic	e																
			Interface	1					Inter	face																
			Endpoint	2					Endp	oint																
			Other	3					Othe	r																
В	R	TYPE							Data	transf	er ty	рe														
			Standard	0					Stand	dard																
			Class	1					Class																	
			Vendor	2					Vend	or																
С	R	DIRECTION							Data	transf	er di	irect	tion													
			HostToDevice	0					Host-	to-de	vice															
			DeviceToHost	1					Devic	e-to-ł	ost															

51.13.27 BREQUEST

Address offset: 0x484

SETUP data, byte 1, bRequest

Bit	numbe	er		33	1 30	29	9 2	28 2	27	26	25	24	1 2	3 2	2 2	21 :	20	19	18	17	16	15	5 14	1 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1	0
Id																														Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	(0 (0	0	0	0	C) (0	0	0	0	0	0	0	0	0	C) () (0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	V	alue	•							D	esc	rip	otio	n																				
Α	R	BREQUEST											S	EΤL	JP (dat	a, I	byt	e 1,	, bF	Req	ues	st. ۱	∕al	ues	pr	ovid	es f	or:	tan	daı	d					
													re	equ	est	ts c	nly	/, u	ser	mι	ıst	im	olei	me	nt (Clas	s ar	ıd V	en	dor	valı	ues					
			STD_GET_STATUS	0									S	an	daı	rd ı	eq	ues	t G	ET.	_ST	ΑT	US														
			STD_CLEAR_FEATURE	1									S	an	daı	rd ı	eq	ues	t C	LEA	AR_	FE	ΑΤι	JRE													
			STD_SET_FEATURE	3									S	an	daı	rd ı	eq	ues	t S	ET_	FE/	ΑΤΙ	JRE	Ξ													
			STD_CLEAR_FEATURE	1									Si	an	daı	rd ı	eq	ues	t C	LEA	AR_	FE	ΑΤι	JRE													



Bit number		31	30	29	28 2	27 2	26 2	5 24	1 2	3 2:	2 21	1 20) 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
Id																									A	Α	Α	Α	Α	A	A A	Ĺ
Reset 0x00000000		0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	
Id RW Field	Value Id	Va	lue						D	esc	ript	ion																				l
	STD_SET_ADDRESS	5							St	tan	dard	d re	que	st S	ET_	AD	DRI	ESS														
	STD_GET_DESCRIPTOR	6							St	tan	dard	d re	que	st 0	BET.	_DE	SCF	RIPT	OR													
	STD_SET_DESCRIPTOR	7							St	tan	dard	d re	que	st S	ET_	DE	SCR	IPT	OR													
	STD_GET_CONFIGURATIO	8 1							St	tan	dard	d re	que	st 0	BET.	_cc	NF	IGU	IRA	TIO	N											
	STD_SET_CONFIGURATION	١9							St	tan	dard	d re	que	st S	ET_	co	NFI	GU	RAT	IOI	٧											
	STD_GET_INTERFACE	10							St	tan	dard	d re	que	st 0	BET.	_IN	TER	FA	CE													
	STD_SET_INTERFACE	11							St	tan	dard	d re	que	st S	ET_	INT	ΓER	FAC	Œ													
	STD_SYNCH_FRAME	12							St	tan	dard	d re	que	st S	YN	CH_	FRA	٩M	E													

51.13.28 WVALUEL

Address offset: 0x488

SETUP data, byte 2, LSB of wValue

Bit	numb	er		31	30	29	28	27 2	26 2	25 2	24	23 :	22 2	21 2	20 1	19 :	18	17	16	15	14	13	12	11 :	.0	9	8	7	6	5	4	3	2	1 (O
Id																												Α	Α	Α	Α	Α	Α	A	Α
Re	set 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																				
Α	R	WVALUEL										SET	UP	dat	a, b	yte	2,	LSE	3 of	w۱	/alu	ie													7

51.13.29 WVALUEH

Address offset: 0x48C

SETUP data, byte 3, MSB of wValue

00 00 00 00 00 00 00 00 00 00 00 00 00		
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9	9 8 7	6 5 4 3 2 1 0
ld	Α	A A A A A A
Reset 0x000000000 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	0 0 0 0 0 0
Id RW Field Value Id Value Description		
iu kw rieiu value iu value Description		
A R WVALUEH SETUP data, byte 3, MSB of wValue		

51.13.30 WINDEXL

Address offset: 0x490

SETUP data, byte 4, LSB of wIndex

Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 1d Reset 0x000000000 0 0 0 0 0 0 0 0 0 0 0 0 0	R WINDEXL			SETUP data, byte 4, L	SB of windex		
Id A A A A A A A A A A A A A A A A A A A	l RW Field	Value Id	Value	Description			
	eset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	000000000	0 0 0 0 0	0 0 0 0
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1						A A A A	A A A A
	it number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9	8 7 6 5 4	3 2 1 0

51.13.31 WINDEXH

Address offset: 0x494

SETUP data, byte 5, MSB of wIndex

Bit number 31 30 2	9 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000 0 0 0	
id DW Field Velve id Velve	Description
Id RW Field Value Id Value	Description
A R WINDEXH	SETUP data, byte 5. MSB of windex

51.13.32 WLENGTHL

Address offset: 0x498



SETUP data, byte 6, LSB of wLength

Bit r	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description
Α	R	WLENGTHL		SETUP data, byte 6, LSB of wLength

51.13.33 WLENGTHH

Address offset: 0x49C

SETUP data, byte 7, MSB of wLength

Bit n	iumbe	er		31	30 2	9 2	8 27	26	25 2	24 2	3 22	2 21	20	19 1	8 1	.7 16	15	14	13 1	2 11	. 10	9	8	7	6	5 4	1 3	2	1	0
Id																								Α	Α	A A	Α	Α	Α	Α
Rese	et OxC	0000000		0	0	0 (0 0	0	0	0 (0 0	0	0	0	0 (0 0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Va	lue					D	esci	ripti	on																	
Α	R	WLENGTHH								S	ETU	P da	ta. I	bvte	7. [MSB	of v	/Ler	gth											

51.13.34 SIZE.EPOUT[0]

Address offset: 0x4A0

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

Bit r	iumbe	er		31 30	29 2	28 27	7 26	25	24	23 :	22 :	21 2	20 1	9 1	8 17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 ()
Id																									Α	Α	Α	Α	A ,	Δ .	٨
Res	et OxC	0000000		0 0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 ()
Id	RW	Field	Value Id	Value						Des	crip	otio	n																		ı
Α	RW	SIZE								Am	oun	ıt of	byt	es i	ece	ived	llas	t in	the	da	a st	age	of t	his	OU ⁻	г					7
										end	poi	nt																			

51.13.35 SIZE.EPOUT[1]

Address offset: 0x4A4

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

Bit	numbe	er		3:	1 30	29	28	27 2	6 2	25 2	4 2	3 22	21	20	19	18 1	.7 1	16 1	5 1	4 1	3 12	11	10	9	8	7	6	5	4	3	2	1 0
Id																											Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0	0	0	0	0 () (0 (0	0 0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	•					D	escr	ipti	on																		
Α	RW	SIZE									Α	mou	ınt c	of b	ytes	rec	eiv	ed la	ast	in tl	ne d	ata	stag	ge o	of th	nis (וטכ	Γ				
											e	ndpo	oint																			

51.13.36 SIZE.EPOUT[2]

Address offset: 0x4A8

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

Bit	numbe	er		31	L 30	29	28	27 20	5 2	5 24	1 23	3 22	21	20	19	18	17 :	16 :	15 :	L4 1	3 1	2 1:	1 10	9	8	7	6	5	4	3	2 :	1 0
Id																																4 A
Res	et 0x0	0000000		0	0	0	0	0 0	(0 0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	alue						D	escr	ipti	on																		
Α	RW	SIZE									Αı	nou	nt c	of b	ytes	rec	eiv	ed l	last	in t	he c	lata	sta	ge (of tl	his (דטכ	•				
											er	ndpo	oint																			



51.13.37 SIZE.EPOUT[3]

Address offset: 0x4AC

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

Bit r	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													Α	Α	Α	Α	Α	Α	Α
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	:						De	scri	ipti	on																				
Α	RW	SIZE										An	nou	nt c	of b	yte	re	ceiv	/ed	las	t in	the	e da	ata	stag	ge o	f th	is C	TUC	Г					_
												en	dpc	int																					

51.13.38 SIZE.EPOUT[4]

Address offset: 0x4B0

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

Bit r	iumbe	er		31	30	29	28 2	27 2	5 2	5 24	1 2	3 22	21	20	19	18 :	17 :	16 1	5 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	2 1	L 0
Id																											Α	Α	Α	A A	A A	A A
Res	et OxC	0000000		0	0	0	0	0 0	(0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																		
Α	RW	SIZE									Α	mou	nt c	of by	ytes	rec	eiv	ed I	ast	in tl	ne d	lata	sta	ge o	f th	nis C	DUT					
											e	ndpo	oint																			

51.13.39 SIZE.EPOUT[5]

Address offset: 0x4B4

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

Bit r	numbe	er		31 30	29	28 2	27 26	25	24	23 2	22 2	21 2	0 19	18	17	16 1	5 1	4 13	12	11 1	0 9	8	7	6	5	4	3 2	1	0
Id																								Α	Α	A	А А	Α	Α
Res	et OxC	0000000		0 0	0	0	0 0	0	0	0	0	0 (0	0	0	0 (0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value	е					Des	crip	tior	1																
Α	RW	SIZE								Amo	oun	t of	byte	s re	ceiv	ed l	ast i	n th	e da	ta st	age	of t	his (DUT					
										end	poi	nt																	

51.13.40 SIZE.EPOUT[6]

Address offset: 0x4B8

Amount of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.

Bit r	numbe	er		31 30	29 28	3 27 26	5 25	24	23	22	21	20 :	19 1	.8 17	7 16	15	14	13 1	2 1	1 10	9	8	7	6	5 -	4 3	2	1	0
Id																								Α	A .	A A	A	Α	Α
Res	et 0x0	0000000		0 0	0 0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Value					De	scri	ptic	n																	
Α	RW	SIZE							Am	our	nt o	f by	tes	rece	ive	llas	t in	the	data	sta	ge c	of th	nis (DUT					
									end	dpo	int																		

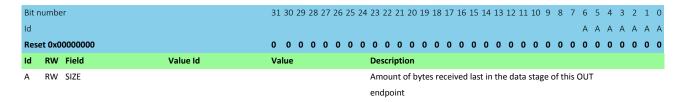
51.13.41 SIZE.EPOUT[7]

Address offset: 0x4BC

Amount of bytes received last in the data stage of this OUT endpoint



Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer.



51.13.42 SIZE.ISOOUT

Address offset: 0x4C0

Amount of bytes received last on this iso OUT data endpoint

Bit r	numbe	er	31 30 29 28 27 26 2 0 0 0 0 0 0 Value Id Value											1 20	0 19	18	3 17	16	15	14	13 3	12 1	.1 10	9	8	7	6	5	4	3 2	1	0
Id																		В						Α	Α	Α	Α	Α	Α.	4 А	. A	Α
Res	et 0x0	0010000		0	0	0	0	0	0	0	0	0 (0	0	0	0	0	1	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	alue						ı	Desc	ript	tion	1																	
Α	R	SIZE													byte	es r	ecei	ived	l las	t or	thi	s isc	OU.	Γda	ita e	nd	ioq	nt				
В	R	ZERO									Z	'ero	-len	gth	dat	ар	ack	et r	ece	ived	ł											
			Normal	0							1	lo z	ero-	-len	gth	dat	ta re	ecei	ved	, us	e va	lue	in SI	ZE								
			ZeroData	1							Z	'ero	-len	gth	dat	a re	ecei	ived	l, igi	nor	e va	lue	in SIZ	Έ								

51.13.43 ENABLE

Address offset: 0x500

Enable USB

E	Bit n	umbe	er		31 30	29	28	27	26	25	24	23 2	22 2	1 20	19	18	17	16	15	14	13 :	12 1	1 10	9	8	7	6	5	4	3	2	1 0
1	d																															Α
F	Reset 0x00000000 0						0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
ı	d	RW	Field	Value Id	Value	•		Description																								
P	A	RW	RW ENABLE												Enable USB																	
				Disabled	0									USB peripheral is disabled																		
				Enabled	1							USB	per	iph	eral	is eı	nab	led														
ı	d	RW	Field	Disabled	Value							Des Ena USB	crip ble l per	tion JSB iph	eral	is di	isab	led														

51.13.44 USBPULLUP

Address offset: 0x504

Control of the USB pull-up

Bit number					31	30 :	29 :	28	27	26	25	24	1 2	3 2	2 2	1 2	0 :	9 :	18	17	16	15	14	13	3 12	2 1	1 10	9	8	7	6	5	4	3	2	1	0	
Id																																						А
Reset 0x00000000 0							0	0	0	0	0	0	0	0) () ()	0	0	0	0	0	0	0	0	0	C	0	0	0	0	0	0	0	0	0	0	O
Id	RV	N	Field	Value Id	Value									Description																								
Α	RV	Ν	CONNECT												Control of the USB pull-up on the D+ line																							
				Disabled	0								Pull-up is disconnected																									
				Enabled		1								Pull-up is connected to D+																								

51.13.45 DPDMVALUE

Address offset: 0x508

State at which the DPDMDRIVE task will force D+ and D-. The DPDMNODRIVE task reverts the control of the lines to MAC IP (no forcing).



Bitı	numbe	er		31	30 2	9 :	28 2	27 :	26 2	25 2	24 :	23 2	22 :	21 :	20 :	19	18	17	16	15	14	13	12	11 1	0 9	9 8	3 7	' 6	5	4	3	2	1	0
Id																														Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () () (0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						- 1	Des	crip	ptio	n																			
Α	RW	STATE									:	Stat	e a	it w	hicl	h th	e D	PD	MD	RIV	⁄Ε t	ask	wil	l for	ce C)+ a	nd	D-						
			Resume	1							- 1	D+ f	ford	ced	low	, D	- fo	rce	d h	igh	(K :	stat	e) f	or a	tim	ing	pre	-se	t in					
											-	har	dwa	are	(50	us	or!	5 m	s, d	lep	end	ling	on	bus	sta	te)								
			J	2							- 1	D+ f	ford	ced	hig	h, C)- f	orce	d l	ow	(J s	tat	e)											
			K	4							- 1	D+ f	ford	ced	low	, D	- fo	rce	d h	igh	(K :	stat	e)											

51.13.46 DTOGGLE

Address offset: 0x50C

Data toggle control and status.

Write this register first with VALUE=Nop to select the endpoint; then read it to get the status from VALUE, or write it again with VALUE=Data0 or Data1.

Bit n	iumbe	er		31	30 :	29	28 2	27	26 2	25 2	24 2	3 22	21	20	19	L8 1	l7 1	6 1	5 1	4 1	3 12	2 11	10	9	8	7	6	5	4 3	3 2	1	0
Id																								С	С	В				Α	Α	Α
Rese	et OxC	0000100		0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 (0 () (0	0	0	0	0	1	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	alue						0	escr	iptio	on																		
Α	RW	EP									S	elec	t bul	k e	ndp	oint	nu	mbe	er													
В	RW	IO									S	elec	ts IN	or	OU	en	dpc	oint														
			Out	0							S	elec	ts O	JT 6	end	oir	nt															
			In	1							S	elec	ts IN	en	dpo	int																
С	RW	VALUE										ata	togg	le v	alue	•																
			Nop	0							Ν	lo ac	tion	on	dat	a to	ggle	e wl	hen	wr	iting	g the	reg	iste	er w	ith	this	5				
											٧	alue																				
			Data0	1							C	ata	togg	le i	DA	TAC	on (en	dpc	oint	set	by E	P ar	nd I	0							
			Data1	2							C	ata	togg	le i	DA	TA1	l on	en	dpc	oint	set	by E	P ar	nd I	0							

51.13.47 EPINEN

Address offset: 0x510 Endpoint IN enable

Bitı	numbe	er		31 30 29 28	27 26 25	5 24	23 2	2 21	20	19 18	3 17	16	15 1	4 13	12	11 1	.0 9	8	7	6	5 4	1 3	2	1 0
Id																		1	Н	G	F E	D	С	ВА
Res	et 0x0	0000001		0 0 0 0	0 0 0	0	0 (0 0	0	0 0	0	0	0 0	0	0	0 (0 0	0	0	0	0 (0	0	0 1
Id	RW	Field	Value Id	Value			Desc	cripti	ion															
Α	RW	INO					Enab	ble IN	l end	dpoin	t 0													
			Disable	0			Disa	ble e	ndp	oint I	N 0	(no	respo	onse	to II	N to	kens)						
			Enable	1			Enab	ble er	ndpc	oint II	V 0 ((resp	onse	e to I	N to	ken	s)							
В	RW	IN1					Enab	ble IN	l end	dpoin	t 1													
			Disable	0			Disa	ble e	ndp	oint I	N 1	(no	respo	onse	to II	N to	kens)						
			Enable	1			Enab	ble er	ndpc	oint II	N 1 ((resp	onse	e to I	N to	ken:	s)							
С	RW	IN2					Enal	ble IN	l end	dpoin	t 2													
			Disable	0			Disa	ble e	ndp	oint I	N 2	(no	respo	onse	to II	N to	kens)						
			Enable	1			Enak	ole er	ndpc	oint II	N 2 ((resp	onse	e to I	N to	ken	s)							
D	RW	IN3					Enab	ble IN	l end	dpoin	t 3													
			Disable	0			Disa	ble e	ndp	oint I	N 3	(no	respo	onse	to II	N to	kens)						
			Enable	1			Enab	ble er	ndpc	oint II	N 3 ((resp	onse	e to I	N to	ken	s)							
Ε	RW	IN4					Enab	ble IN	l end	dpoin	t 4													
			Disable	0			Disa	ble e	ndp	oint I	N 4	(no	respo	onse	to II	N to	kens)						
			Enable	1			Enak	ole er	ndpc	oint II	N 4 ((resp	onse	e to I	N to	ken	s)							
F	RW	IN5					Enab	ble IN	l end	dpoin	t 5													
			Disable	0			Disa	ble e	ndp	oint I	N 5	(no	respo	onse	to II	N to	kens)						



Bit number	31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		IHGFEDCBA
Reset 0x00000001	0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field Value Id	Value	Description
Enable	1	Enable endpoint IN 5 (response to IN tokens)
G RW IN6		Enable IN endpoint 6
Disable	0	Disable endpoint IN 6 (no response to IN tokens)
Enable	1	Enable endpoint IN 6 (response to IN tokens)
H RW IN7		Enable IN endpoint 7
Disable	0	Disable endpoint IN 7 (no response to IN tokens)
Enable	1	Enable endpoint IN 7 (response to IN tokens)
I RW ISOIN		Enable iso IN endpoint
Disable	0	Disable iso IN endpoint 8
Enable	1	Enable iso IN endpoint 8

51.13.48 EPOUTEN

Address offset: 0x514 Endpoint OUT enable

Bit nur	mbe	r		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
Id					I H G F E D C B /
Reset	0x0	0000001		0 0 0 0 0 0 0 0	000000000000000000000000000000000000000
ld R	RW	Field	Value Id	Value	Description
A R	RW	OUT0			Enable OUT endpoint 0
			Disable	0	Disable endpoint OUT 0 (no response to OUT tokens)
			Enable	1	Enable endpoint OUT 0 (response to OUT tokens)
B R	RW	OUT1			Enable OUT endpoint 1
			Disable	0	Disable endpoint OUT 1 (no response to OUT tokens)
			Enable	1	Enable endpoint OUT 1 (response to OUT tokens)
C R	RW	OUT2			Enable OUT endpoint 2
			Disable	0	Disable endpoint OUT 2 (no response to OUT tokens)
			Enable	1	Enable endpoint OUT 2 (response to OUT tokens)
D R	RW	OUT3			Enable OUT endpoint 3
			Disable	0	Disable endpoint OUT 3 (no response to OUT tokens)
			Enable	1	Enable endpoint OUT 3 (response to OUT tokens)
E R	RW	OUT4			Enable OUT endpoint 4
			Disable	0	Disable endpoint OUT 4 (no response to OUT tokens)
			Enable	1	Enable endpoint OUT 4 (response to OUT tokens)
F R	RW	OUT5			Enable OUT endpoint 5
			Disable	0	Disable endpoint OUT 5 (no response to OUT tokens)
			Enable	1	Enable endpoint OUT 5 (response to OUT tokens)
G R	RW	OUT6			Enable OUT endpoint 6
			Disable	0	Disable endpoint OUT 6 (no response to OUT tokens)
			Enable	1	Enable endpoint OUT 6 (response to OUT tokens)
H R	RW	OUT7			Enable OUT endpoint 7
			Disable	0	Disable endpoint OUT 7 (no response to OUT tokens)
			Enable	1	Enable endpoint OUT 7 (response to OUT tokens)
I R	RW	ISOOUT			Enable iso OUT endpoint 8
			Disable	0	Disable iso OUT endpoint 8
			Enable	1	Enable iso OUT endpoint 8

51.13.49 EPSTALL

Address offset: 0x518 STALL endpoints



Bit	numbe	er		31	30	29	28	27	26 2	5 2	24 2	23 2	22 2	21 2	0 1	9 1	3 17	16	15	14	13	12	11 1	9	8	7	6	5	4	3 2	1	0
Id																									С	В				Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0	0 (0 0) (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tior																		
Α	W	EP									5	Sele	ct e	endp	oir	it ni	ımb	er														
В	W	10									S	Sele	cts	IN c	r O	UT	end	poi	nt													
			Out	0							5	Sele	cts	OU ⁻	Γer	ndp	oint															
			In	1							5	Sele	cts	IN e	nd	poir	it															
С	W	STALL									5	Stal	l sel	ecte	ed e	end	ooin	t														
			UnStall	0								Don	't st	talls	ele	cte	d en	dpo	oint													
			Stall	1							5	Stal	l sel	ecte	ed e	end	oin	t														

51.13.50 ISOSPLIT

Address offset: 0x51C

Controls the split of ISO buffers

Bit	num	ber			3	1 30	29	28	3 27	7 26	6 25	5 24	1 2	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id																					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	А А
Res	et 0	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RV	W	Field	Value Id	٧	alu	9						D	esci	ripti	on																			
Α	RV	N :	SPLIT										C	onti	ols	the	spl	it o	f IS	O b	uffe	ers													
				OneDir	0	x00	00						F	ull b	uffe	er d	edio	ate	d t	o ei	the	r is	o IN	l or	ΟU	IT									
				HalfIN	0	x00	80						Lo	owe	r ha	lf fo	or II	۱, u	ppe	er h	alf	for	OU	Т											

51.13.51 FRAMECNTR

Address offset: 0x520

Returns the current value of the start of frame counter

Bit r	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description
Α	R	FRAMECNTR		Returns the current value of the start of frame counter

51.13.52 LOWPOWER

Address offset: 0x52C

Controls USBD peripheral low-power mode during USB suspend

Bit r	umbe	er		31	1 30	29	2	8 2	7 2	26 2	5 2	24	23	22	21	20	19	18	3 17	7 1	5 1	5 1	4 1	3 1	.2 1	11 1	10	9	8	7	6	5	4	3	2	1 0
Id																																				Α
Res	t 0x0	0000000		0	0	0	C	0)	0 (0	0	0	0	0	0	0	0	0	0	C) () ()	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue								Des	cri	pti	on																				
Α	RW	LOWPOWER											Cor	ntro	ols I	USE	BD	per	iph	era	ıl lo	w-	рον	ver	mo	ode	du	rin	g US	B s	usp	oer	nd			
			ForceNormal	0									Sof	twa	are	mu	ıst	wri	te 1	this	va	lue	to	exi	t lo	w p	ow	er	mod	de :	and	ı				
													bef	ore	e pe	erfo	rm	ing	a r	em	ote	e w	ake	-up)											
			LowPower	1								:	Sof	twa	are	mu	ıst	wri	te 1	this	va	lue	to	ent	er	low	ро	we	r m	od	e af	ter				
													DM	A a	and	sof	ftw	are	ha	ive	fini	ish	ed i	nte	rac	tin	g w	ith	the	US	В					
													per	iph	era	al																				

51.13.53 ISOINCONFIG

Address offset: 0x530

Controls the response of the ISO IN endpoint to an IN token when no data is ready to be sent



Bi	t nu	ımbe	r		3	1 30	29	28	8 27	7 2	6 2	5 2	4 2	3 22	2 21	20	19	18	17	16	15	14	13	12 :	11 1	9	8	7	6	5	4	3	2	1 0
Id																																		Α
R	eset	0x0	0000000		0	0	0	0	0) (0	0) (0 0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id		RW	Field	Value Id	V	alue)						C	esc	ripti	on																		
Α		RW	RESPONSE										C	onti	ols	the	res	por	ise	of t	he	ISO	IN	end	poin	t to	an l	Νt	oke	n				
													٧	vher	no	dat	ta is	rea	dy	to b	oe s	ent												
				NoResp	0								Е	ndp	oint	do	es n	ot ı	resp	on	d in	th	at c	ase										
				ZeroData	1								Е	ndp	oint	res	spor	nds	wit	h a	zer	o-le	engt	h d	ata p	ack	et i	th	at c	ase				

51.13.54 EPIN[0].PTR

Address offset: 0x600

Data pointer

Bit numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20 1	19 1	8 1	7 1	6 1	5 1	4 1	3 12	2 11	. 10	9	8	7	6	5	4	3 2	2 1	. 0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α ,	4 4	A A	A <i>A</i>	A /	A	. A	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	A
Reset 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0 () (0	0	0	0	0	0	0	0	0	0 (0	0
Id RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
A RW	PTR										Dat	ар	oin	ter.	Acc	ept	s ar	ıv a	ddr	ess	in [Data	RA	М.								

51.13.55 EPIN[0].MAXCNT

Address offset: 0x604

Maximum number of bytes to transfer

Bi	t number	31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A
Re	eset 0x00000000	0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field Value Id	Value	Description
Α	RW MAXCNT	[640]	Maximum number of bytes to transfer

51.13.56 EPIN[0].AMOUNT

Address offset: 0x608

Number of bytes transferred in the last transaction

Bit	numbe	er		31	30	29 :	28 2	27 2	6 2	5 2	4 2	23 2	22 2	21 2	20 :	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													Α	Α	Α	Α	Α	Α	А
Res	et 0x0	0000000		0	0	0	0	0 (0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																				
Α	R	AMOUNT									١	Nun	nbe	r o	f by	/tes	tra	ans	feri	ed	in t	the	las	t tr	ansa	acti	on								

51.13.57 EPIN[1].PTR

Address offset: 0x614

Data pointer

ı	d	RW	Field	Value Id	Val										ptic																			
F	Rese	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0
1	d				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Δ,	Δ Δ	Α	Α	Α	Α	Α	Α	A	A A	Α
E	3it nı	ımbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14 1	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	2 1	0

A RW PTR Data pointer. Accepts any address in Data RAM.

51.13.58 EPIN[1].MAXCNT

Address offset: 0x618

Maximum number of bytes to transfer



Bit nui	mbe	r		31 30	29 2	28 27	7 26	25 2	24 2	23 22	2 21	20	19 3	18 1	L7 1	6 15	5 14	- 13	12	11:	10 !	9	8	7	6	5	4	3 :	2 1	0
Id																									Α	Α	Α	A A	٩А	Α
Reset	0x0	0000000		0 0	0	0 0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 0	0
Id F	ĸw	Field	Value Id	Value					L	Desc	rıptı	on																		
				[64.6]											٠.				,											
A F	RW	MAXCNT		[640]					ľ	vlaxı	mur	n nı	ımb	er o	t by	tes 1	to t	rans	ster											

51.13.59 EPIN[1].AMOUNT

Address offset: 0x61C

Number of bytes transferred in the last transaction

Bit r	numbe	er		31 30 29 28 27	7 26 25 24	23 22	21 20	19 1	.8 17	16 1	5 14	13 12	11 1	.0 9	8	7	6	5 -	4 3	3 2	1	0
Id																	Α	A	A A	A A	Α	Α
Res	et 0x0	0000000		0 0 0 0 0	0 0 0	0 0	0 0	0 (0 0	0 0	0	0 0	0	0 0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Value		Descri	ption															
Α	R	AMOUNT				Numb	er of b	ytes	transf	ferre	d in t	he las	t trar	ısact	ion							_

51.13.60 EPIN[2].PTR

Address offset: 0x628

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Data pointer. Accepts any address in Data RAM.

51.13.61 EPIN[2].MAXCNT

Address offset: 0x62C

Maximum number of bytes to transfer

Bit	numb	er		31 30 29 28 27 20	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A A A A A A
Res	et 0x0	0000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	MAXCNT		[640]	Maximum number of bytes to transfer

51.13.62 EPIN[2].AMOUNT

Address offset: 0x630

Number of bytes transferred in the last transaction

Bit nur	nber			31	30	29	28 2	7 26	25	24	23	22 2	21 2	20 1	9 18	3 17	16	15	14 1	3 12	11	10	9	8	7	6 5	5 4	3	2	1 (
Id																										A A	4 Α	A	Α	A A
Reset (0x0000	00000		0	0	0	0 (0	0	0	0	0 (0	0 0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0 (
ld R	RW Fi	eld	Value Id	Va	lue						Des	crip	tio	n																
A R	R Al	MOUNT									Nui	nbe	r of	byt	es t	rans	feri	ed i	n th	e las	t tra	ansa	ctic	n						

51.13.63 EPIN[3].PTR

Address offset: 0x63C

Data pointer

Bit number	31 30 2	29 28 27 26 25 24	23 22 21 20 19 18	17 16 15 14 13 12 11 10	0 9 8 7 6 5 4 3 2 1 0
Id	A A A	AAAAAA	A A A A A	A A A A A A A	
Reset 0x00000000	0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0 0 0	00000000000
Id RW Field Value	Id Value		Description		

A RW PTR Data pointer. Accepts any address in Data RAM.



51.13.64 EPIN[3].MAXCNT

Address offset: 0x640

Maximum number of bytes to transfer

Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
A RW MAXCNT		[640]	Maximum number of bytes to transfer

51.13.65 EPIN[3].AMOUNT

Address offset: 0x644

Number of bytes transferred in the last transaction

Bit r	iumbe	er		31	30 2	29 2	28 27	7 26	25	24	23	22	21 2	20 :	19 1	8 1	7 1	6 15	14	1 13	12	11	10 !	9	8	7	6	5	4	3 :	2 1	L 0
Id																											Α	Α	Α	A A	Δ Δ	A A
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Va	lue						De	scri	ptio	n																		
Α	R	AMOUNT									Nu	mb	er o	f by	tes	trar	sfe	rred	l in	the	last	tra	nsac	tic	on							

51.13.66 EPIN[4].PTR

Address offset: 0x650

Data pointer

Bi	it nı	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id	ı				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	А А
R	ese	t OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	ı	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α		RW	PTR										Dat	ta p	oin	ter.	Ac	сер	ts a	ny	ado	ires	s ir	ı Da	ita I	RAN	Λ.								

51.13.67 EPIN[4].MAXCNT

Address offset: 0x654

Maximum number of bytes to transfer

Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW MAXCNT		[640]	Maximum number of bytes to transfer

51.13.68 EPIN[4].AMOUNT

Address offset: 0x658

Number of bytes transferred in the last transaction

Bi	numb	er		31 30	29 2	8 27	26	25 2	4 2	3 22	21	20 1	19 18	3 17	16	15	14 1	3 12	11	10	9 8	3 7	6	5	4	3 2	1	0
Id																							Α	Α	A	4 A	Α	Α
Re	set 0x	00000000		0 0	0 (0 0	0	0 (0	0	0	0	0 0	0	0	0	0 (0	0	0	0 (0	0	0	0	0 0	0	0
Id	RW	/ Field	Value Id	Value					D	escri	ptio	n																
Δ	R	AMOUNT							N	umh	er o	f hv	toc t	rans	forr	i ha	n th	عدا م	t tra	nca	-tio	,						

51.13.69 EPIN[5].PTR

Address offset: 0x664

Data pointer



Bit r	numbe	er		31	. 30	29	28	27	7 26	5 25	24	23	22	21	20	19	18	17	16	15 :	14	13 1	12 1	.1 10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α .	4 A	Α	Α	Α	Α	Α	Α	A	4 Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																		
Α	RW	PTR										Da	ta p	oin	ter.	. Ac	сер	ts a	ny	add	res	s in	Da	ta R	١M.								

51.13.70 EPIN[5].MAXCNT

Address offset: 0x668

Maximum number of bytes to transfer

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			АААААА
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW MAXCNT		[640]	Maximum number of bytes to transfer

51.13.71 EPIN[5].AMOUNT

Address offset: 0x66C

Number of bytes transferred in the last transaction

Bit nu	ımbe	er		31 30 29 28 27 2	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A A A A A A
Reset	0x0	0000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld I	RW	Field	Value Id	Value	Description
A I	R	AMOUNT			Number of bytes transferred in the last transaction

51.13.72 EPIN[6].PTR

Address offset: 0x678

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW PTR		Data pointer. Accepts any address in Data RAM.

51.13.73 EPIN[6].MAXCNT

Address offset: 0x67C

Maximum number of bytes to transfer

Bit r	number	31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A
Res	et 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field Value Id	Value	Description
Α	RW MAXCNT	[640]	Maximum number of bytes to transfer

51.13.74 EPIN[6].AMOUNT

Address offset: 0x680

Number of bytes transferred in the last transaction

Bit	number			31	1 30	29	28	27 2	26 2	25 2	24 2	3 2	2 2	21 2	0 1	L9 1	.8 1	7 1	6 1	15 1	.4 1	13 1	12 1	11 :	10 9	9	8 7	7	6	5	4	3 2		1 0
Id																													Α	Α.	Α	A A		А А
Res	et 0x00	000000		0	0	0	0	0	0	0 (0	0 (0	0 (0	0 (0 (0 (0 (0	0	0	0	0	0 (0	0 (0	0	0	0	0 0	(0 0
Id	RW	Field	Value Id	Va	alue	9					0	esc	crip	tio	n																			
	D	ANACHINIT												4	·		.			:.		1.					_							

A R AMOUNT Number of bytes transferred in the last transaction



51.13.75 EPIN[7].PTR

Address offset: 0x68C

Data pointer

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16 1	15 1	L4 1	3 1	.2 1	.1 1	9	8	7	6	5	4	3	2	1 (Ò
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Δ,	Δ.	4 <i>A</i>	Α	Α	Α	Α	Α	Α	Α	Α	A	4
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (כ
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	PTR										Da	ta p	oin	ter.	. Ac	сер	ts a	ny a	add	res	in	Da	ta R	١M.									_

51.13.76 EPIN[7].MAXCNT

Address offset: 0x690

Maximum number of bytes to transfer

Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW MAXCNT		[640]	Maximum number of bytes to transfer

51.13.77 EPIN[7].AMOUNT

Address offset: 0x694

Number of bytes transferred in the last transaction

Bi	t num	ber		31 30	29	28 2	27 26	5 25	24	23	22 2	21 2	20 1	9 1	8 17	7 16	15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	. 1	0
Id																									Α	Α	Α	А А	A	. A
R	eset O	k00000000		0 0	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 0	0	0
Id	RV	V Field	Value Id	Value						De	scrip	otio	n																	
Α	R	AMOUNT								Nu	mbe	er o	f by	tes 1	ran	sfer	red	in t	he I	ast t	rans	acti	on							

51.13.78 ISOIN.PTR

Address offset: 0x6A0

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW PTR		Data pointer, Accepts any address in Data RAM.

51.13.79 ISOIN.MAXCNT

Address offset: 0x6A4

Maximum number of bytes to transfer

A RW MAXCNT		[10231]	Maximum number of bytes to transfer
Id RW Field	Value Id	Value	Description
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id			A A A A A A A A A
Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

51.13.80 ISOIN.AMOUNT

Address offset: 0x6A8

Number of bytes transferred in the last transaction



Bit r	numbe	er		31	30	29	28	8 27	' 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 :	2 :	1 0
Id																										Α	Α	Α	Α	Α	Α	A A	A A	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	Va	lue	•						De	scri	ptic	on																			
Α	R	AMOUNT										Nu	mb	er c	of b	yte	s tr	ans	feri	red	in t	he	last	tra	nsa	ctio	on							

51.13.81 EPOUT[0].PTR

Address offset: 0x700

Data pointer

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19 1	L8 1	L7 1	16 1	L5 1	L4 1	L3 1	.2 1	1 1	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A ,	Α,	Α.	Α.	Α.	Α.	Δ.	Δ	. A	Α	Α	Α	Α	Α	Α	A	А А
Rese	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	otic	n																		
Α	RW	PTR										Dat	ар	oin	ter.	Acc	ept	s aı	ny a	add	res	s in	Da	ta R	۱M								

51.13.82 EPOUT[0].MAXCNT

Address offset: 0x704

Maximum number of bytes to transfer

Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW MAXCNT		[640]	Maximum number of bytes to transfer

51.13.83 EPOUT[0].AMOUNT

Address offset: 0x708

Number of bytes transferred in the last transaction

Bit r	iumbe	er		31	30	29 2	28 2	7 26	5 25	24	23	22	21 2	20 1	19 1	18 1	L7 1	16 1	L5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id																											Α	Α.	Α.	А А	Α	A
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Val	lue						De	scri	ptio	n																		
Α	R	AMOUNT									Nu	mb	er o	f by	/tes	tra	nsfe	erre	ed ir	the	las	t tra	ansa	ctio	on							

51.13.84 EPOUT[1].PTR

Address offset: 0x714

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Data pointer. Accepts any address in Data RAM.

51.13.85 EPOUT[1].MAXCNT

Address offset: 0x718

Maximum number of bytes to transfer

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ААААА
Reset 0x00000000		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
ld RW Field	Value Id	Value	Description
A RW MAXCNT		[640]	Maximum number of bytes to transfer



51.13.86 EPOUT[1].AMOUNT

Address offset: 0x71C

Number of bytes transferred in the last transaction

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 :	18 :	17 1	16 1	.5 1	4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0	ı
Id																												Α	Α	Α	Α	A	А А	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0 (0 (0	0	0	0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	Va	lue							De	scri	otic	n																			ĺ
Α	R	AMOUNT										Nu	mbe	er o	f by	tes	tra	nsf	erre	d ii	n th	e la	ıst t	rans	acti	on								١

51.13.87 EPOUT[2].PTR

Address offset: 0x728

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
bit ilumber		31 30 29 26 27 20 23 24 23 22 21 20 19 16 17 10 13 14 13 12 11 10 9 6 7 0 3 4 3 2 1 10
Id		
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Data pointer. Accepts any address in Data RAM.

51.13.88 EPOUT[2].MAXCNT

Address offset: 0x72C

Maximum number of bytes to transfer

Bit	number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ААААА
Res	set 0x00000000	0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field Value Id	Value	Description
Α	RW MAXCNT	[640]	Maximum number of bytes to transfer

51.13.89 EPOUT[2].AMOUNT

Address offset: 0x730

Number of bytes transferred in the last transaction

Bit nur	mber		31	30 2	9 28	27	26 2	25 2	4 2	3 22	21	20	19	18 :	17 1	.6 1	5 1	4 13	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id																									A	4 Δ	A	Α	Α	Α
Reset (0x00000000		0	0 (0	0	0	0 (0 (0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	0	0	0	0
ld R	W Field	Value Id	Val	ue					D	escr	ipti	on																		
A R	AMOUNT								N	uml	oer (of b	vtes	tra	nsfe	erre	d ir	the	las	t tra	nsa	ctic	on							

51.13.90 EPOUT[3].PTR

Address offset: 0x73C

Data pointer

Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 :	10	9	8	7	6	5	4	3	2 :	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α.	Α	Α	Α	Α	Α /	Δ Α	A A
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0
ld RW Field	Value Id	Va	lue							De	scri	ptic	on																			
A RW PTR										Da	ta p	oin	ter	. Ac	сер	ts a	ny	ado	lres	s in	Da	ta F	RAN	1.								

51.13.91 EPOUT[3].MAXCNT

Address offset: 0x740

Maximum number of bytes to transfer



Bit nui	mbe	r		31 30	29 2	28 27	7 26	25 2	24 2	23 22	2 21	20	19 3	18 1	L7 1	6 15	5 14	- 13	12	11:	10 !	9	8	7	6	5	4	3 :	2 1	0
Id																									Α	Α	Α	A A	٩А	Α
Reset	0x0	0000000		0 0	0	0 0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 0	0
Id F	ĸw	Field	Value Id	Value					L	Desc	rıptı	on																		
				[64.6]											٠.				,											
A F	RW	MAXCNT		[640]					ľ	vlaxı	mur	n nı	ımb	er o	t by	tes 1	to t	rans	ster											

51.13.92 EPOUT[3].AMOUNT

Address offset: 0x744

Number of bytes transferred in the last transaction

Bit r	numbe	er		31	30	29	28	27 2	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0	ĺ
Id																													Α	Α	Α	Α	A A	4 Α	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	
Id	RW	Field	Value Id	Va	lue							Des	cri	otic	n																				l
Α	R	AMOUNT										Nui	nbe	er o	f b	/tes	tra	ansi	feri	red	in t	he	las	t tr	ansa	acti	on								١

51.13.93 EPOUT[4].PTR

Address offset: 0x750

Data pointer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW PTR	Data pointer. Accepts any address in Data RAM.

51.13.94 EPOUT[4].MAXCNT

Address offset: 0x754

Maximum number of bytes to transfer

Bit r	numbe	r		31	30	29	28 2	7 26	25	24	23	22 2	21 2	20 1	9 18	3 17	16	15	14 1	13 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id																										Α	Α	Α	A A	Α	Α
Res	et 0x0(000000		0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	tio	n																	
Α	RW	MAXCNT		[64	10]						Ma	xim	um	nun	nbei	of	byte	es to	tra	nsfe	r										

51.13.95 EPOUT[4].AMOUNT

Address offset: 0x758

Number of bytes transferred in the last transaction

Bit n	umbe	er		31 30 2	29 2	28 27	26	25 2	24 2	23 2	2 2	1 20	19	18	17	16	15 1	L4 1	.3 1	2 1:	l 10	9	8	7	6	5	4	3	2 1	. 0
Id																									Α	Α	Α	Α .	A A	A A
Rese	t 0x0	0000000		0 0	0 (0 0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0 (
Id	RW	Field	Value Id	Value						Desc	crip	tion																		
Α	R	AMOUNT							١	lum	nber	of	byte	s tr	ansi	err	ed i	n th	e la	st tr	ans	acti	on							

51.13.96 EPOUT[5].PTR

Address offset: 0x764

Data pointer

Bit number		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 :	16 1	15 :	14 1	13 1	12 1	1 10	9	8	7	6	5	4	3	2 1	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A.	Α	Α.	Α.	Α ,	Δ Δ	A	Α	Α	Α	Α	Α	Α ,	4 4	A A
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 0
Id RW Field	Value Id	Va	lue							De	scri	ptic	on																		

A RW PTR Data pointer. Accepts any address in Data RAM.



51.13.97 EPOUT[5].MAXCNT

Address offset: 0x768

Maximum number of bytes to transfer

Bit num	ber		31	30 29	9 28	27 26	5 25	24	23 2	2 21	20	19 3	18 1	7 1	5 15	14	13 1	2 11	10	9	8	7	6	5	4 3	2	1	0
Id																							Α	Α.	А А	Α	Α	Α
Reset 0	x00000000		0	0 0	0	0 0	0	0	0 (0 0	0	0	0 (0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0
Id R	N Field	Value Id	Val	ue					Desc	cripti	ion																	
A R\	N MAXCNT		[64	0]					Max	imur	m nı	umb	er o	f by	es t	o tra	ansfe	er										

51.13.98 EPOUT[5].AMOUNT

Address offset: 0x76C

Number of bytes transferred in the last transaction

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9	9 8 7 6 5 4	3 2 1 0
Id					ААА	A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0000000	0 0 0 0 0	0 0 0 0
Id RW Field	Value Id	Value	Description			
A R AMOUNT			Number of bytes tran	nsferred in the last transac	ction	

51.13.99 EPOUT[6].PTR

Address offset: 0x778

Data pointer

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 1	16 1	L5 1	L4 1	L3 1	.2 1	.1 1	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α.	A ,	Δ,	4 Δ	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	PTR										Dat	ta p	oin	ter.	Aco	cept	ts a	ny a	add	res	s in	Da	ta R	١M.								

51.13.100 EPOUT[6].MAXCNT

Address offset: 0x77C

Maximum number of bytes to transfer

Bit number		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW MAXCNT		[640]	Maximum number of bytes to transfer

51.13.101 EPOUT[6].AMOUNT

Address offset: 0x780

Number of bytes transferred in the last transaction

Bit	numb	er		31	30 2	29 2	28 2	7 26	25	24	23	22	21 2	20 1	9 1	8 17	16	15	14 :	.3 1	2 11	. 10	9	8	7	6	5 4	3	2	1)
Id																										Α.	А А	A	Α	Α.	A
Re	set Ox	00000000		0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0	0)
Id	RW	Field	Value Id	Va	lue						Des	crip	otio	n																	
Δ	R	AMOUNT									Niii	mhe	r of	f hv	tes t	ran	sfer	red	in th	e la	st tr	ans	actio	าท							7

51.13.102 EPOUT[7].PTR

Address offset: 0x78C

Data pointer



Bit r	numbe	er		31	. 30	29	28	27	7 26	5 25	24	23	22	21	20	19	18	17	16	15 :	14	13 1	12 1	.1 10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α .	4 A	Α	Α	Α	Α	Α	Α	A	4 Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	PTR										Da	ta p	oin	ter.	. Ac	сер	ts a	ny	add	res	s in	Da	ta R	١M.								

51.13.103 EPOUT[7].MAXCNT

Address offset: 0x790

Maximum number of bytes to transfer

Bit	numb	er		31 30 2	9 28	27 2	6 25	24	23 2:	2 21	20	19 1	8 17	16	15 :	14 1	3 12	11 :	10 9	8	7	6	5	4 :	3 2	1	0
Id																						Α	Α.	A A	4 A	Α	Α
Re	set Ox	00000000		0 0 (0 0	0 (0 0	0	0 0	0	0	0 (0 0	0	0	0 0	0	0	0 0	0	0	0	0	0 (0 0	0	0
Id	RW	Field	Value Id	Value					Desc	ripti	on																
Α	RW	MAXCNT		[640]					Maxi	mun	n nu	mbe	r of	byte	es to	tran	sfer										

51.13.104 EPOUT[7].AMOUNT

Address offset: 0x794

Number of bytes transferred in the last transaction

Bit r	numbe	er		31 3	0 29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	7 16	15	14	13	12	11 :	LO	9	8 7	7 (5 5	4	3	2	1 ()
Id																										,	Δ Δ	A	Α	Α	Α ,	4
Res	et 0x0	0000000		0 (0 0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0 ()
Id	RW	Field	Value Id	Valu	e						Des	crip	tio	n																		ı
A R AMOUNT										Nur	nbe	r of	f by	tes 1	tran	sfei	red	in t	he	last	trai	nsa	ctio	n							7	

51.13.105 ISOOUT.PTR

Address offset: 0x7A0

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW PTR		Data pointer. Accepts any address in Data RAM.

51.13.106 ISOOUT.MAXCNT

Address offset: 0x7A4

Maximum number of bytes to transfer

Bit number		31 30 29 28 27 26	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW MAXCNT			Maximum number of bytes to transfer

51.13.107 ISOOUT.AMOUNT

Address offset: 0x7A8

Number of bytes transferred in the last transaction

Rit	numbe	or .		31 30	29	28.2	7 26	5 25	24	23 :	22.2	1 2	0 19	18	17	16	15	14 1	3 1:	2 11	10	9	8	7	6	5	4	3 2	1	0
ld.				51 50									0 1.	, 10																. A
Iu																														
Res	et 0x0	0000000		0 0	0	0 (0	0	0	0	0 (0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value	:					Des	crip	tior	1																	
Α	R							Nun	nbe	r of	byt	es ti	rans	feri	ed i	n th	e la:	st tr	ansa	actio	on									



51.14 Electrical specification

51.14.1 USB Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{USB,ACTIVE,VBUS}	Current from V _{BUS} supply, USB active, excluding current through				mA
	pull-up and I _{USB,QUIES}				
I _{USB,SUSPEND,VBUS}	Current from V _{BUS} supply, USB suspended, excluding current				μΑ
	through pull-up				
I _{USB,DISABLED,VBUS}	Current from V _{BUS} supply, USB disabled				μΑ
I _{USB,ACTIVE,VDD}	Current from V _{DD} supply, USB active, including 48 MHz clock,				mA
	excluding DMA accesses				
I _{USB,SUSPEND,VDD}	Current from V _{DD} supply, USB suspended				μΑ
I _{USB,DISABLED,VDD}	Current from V_{DD} supply, USB disabled, V_{BUS} supply connected				μΑ
R _{USB,PU,ACTIVE}	Value of pull-up on D+, bus active (upstream device	1425	2300	3090	Ω
	transmitting)				
R _{USB,PU,IDLE}	Value of pull-up on D+, bus idle	900	1200	1575	Ω
t _{USB,DETRST}	Minimum duration of an SEO state to be detected as a USB reset				μs
	condition				
f _{USB,CLK}	Frequency of local clock, USB active		48		MHz
f _{USB,TOL}	Accuracy of local clock, USB active ⁴⁰			±1000	ppm
T _{USB,JITTER}	Jitter on USB local clock, USB active			±1	ns
t _{USB,RSMREC}	Hardware Resume Recovery Time (includes local clock startup				ms
	time) ⁴¹				
t _{USB,SUSPEND}	Time of bus inactivity detected as USB suspend				ms
t _{USB,RSTREC}	Hardware Reset Recovery Time (includes local clock startup				ms
	time) ⁴²				
t _{USB,DRIVEK}	Duration of driving resume upstream (using the automated				ms
	Resume function in the DPDMVALUE register)				
t _{USB,FDRATE}	Full-speed data rate				Mb/s
t _{SOF,EVENT}	Time from USB start of frame to EVENTS_SOF sent				μs
t _{EN2RDY}	Time from ENABLE=Enabled to READY event sent				μs

The local clock can be stopped during USB suspend
 This is a contributor to the T_{RSMRCY} time as defined in USB specification chapter 7
 This is a contributor to the T_{RSTRCY} time as defined in USB specification chapter 7



52 QSPI — Quad serial peripheral interface

The QSPI peripheral provides support for communicating with an external flash memory device using SPI.

Listed here are the main features for the QSPI peripheral:

- · Single/dual/quad SPI input/output
- 2-32 MHz configurable clock frequency
- Single-word read/write access from/to external flash
- · EasyDMA for block read and write transfers
- · Execute in place (XIP) for executing program directly from external flash
- XIP execution speed: Up to 8 million instruction fetches per second for 16 bit instructions, up to 4 million instruction fetches per second for 32 bit instructions.

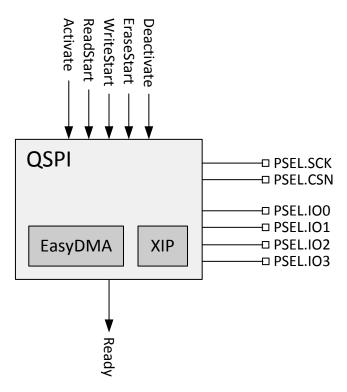


Figure 187: Block diagram

52.1 Configuring peripheral

Before any data can be transferred to or from the external flash memory, the peripheral needs to be configured.

- Select input/output pins in PSEL.SCK on page 674, PSEL.CSN on page 675, PSEL.IO0 on page 675, PSEL.IO1 on page 675, PSEL.IO2 on page 675, and PSEL.IO3 on page 676. See Reference circuitry on page 688 for the recommended pins.
- 2. To ensure stable operation, set the GPIO drive strength to "high drive". See the GPIO General purpose input/output on page 154 chapter for details on how to configure GPIO drive strength.
- **3.** Configure the interface towards the external flash memory using *IFCONFIG0* on page 676, *IFCONFIG1* on page 677, and *ADDRCONF* on page 678.
- 4. Enable the QSPI peripheral and acquire I/O pins using *ENABLE* on page 673.
- **5.** Activate the external flash memory interface using the ACTIVATE task. The READY event will be generated when the interface has been activated and the external flash memory is ready for access.



Important: If the *IFCONFIGO* on page 676 register is configured to use the quad mode, the external flash device also needs to be set in the quad mode before any data transfers can take place.

This can be done by sending custom instructions to the external flash device, as described in *Sending custom instructions* on page 665.

52.2 Write operation

A write operation to the external flash is configured using the *WRITE.DST* on page 673, *WRITE.SRC* on page 674, and *WRITE.CNT* on page 674 registers and started using the WRITESTART task.

The READY event is generated when the transfer is complete.

The QSPI peripheral automatically takes care of splitting DMA transfers into page writes.

52.3 Read operation

A read operation from the external flash is configured using the *READ.SRC* on page 673, *READ.DST* on page 673, and *READ.CNT* on page 673registers and started using the READSTART task.

The READY event is generated when the transfer is complete.

52.4 Erase operation

Erase of pages/blocks of the external flash is configured using the *ERASE.PTR* on page 674and *ERASE.LEN* on page 674registers and started using the ERASESTART task.

The READY event is generated when the erase operation has been started.

Note that in this case the READY event will not indicate that the erase operation of the flash has been completed, but it only signals that the erase operation has been started. The actual status of the erase operation can normally be read from the external flash using a custom instruction, see *Sending custom instructions* on page 665.

52.5 Execute in place

Execute in place (XIP) allows the CPU to execute program code directly from the external flash.

After the external flash has been configured, the CPU can execute code from the external flash by accessing the XIP memory region. See the figure below and *Memory map* on page 21 for details.

When accessing the XIP memory region, the start address of this XIP memory region will map to the address XIPOFFSET on page 676 of the external flash.



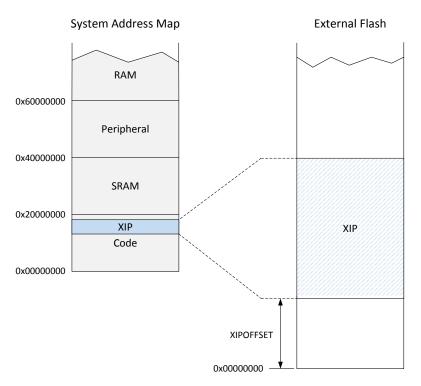


Figure 188: XIP memory map

52.6 Sending custom instructions

Custom instructions can be sent to the external flash using the *CINSTRCONF* on page 678, *CINSTRDAT0* on page 679, and *CINSTRDAT1* on page 679 registers. It is possible to send an instruction consisting of a one-byte opcode and up to 8 bytes of additional data and to read its response.

A custom instruction is prepared by first writing the data to be sent to *CINSTRDAT0* on page 679 and *CINSTRDAT1* on page 679 before writing the opcode and other configurations to the *CINSTRCONF* on page 678 register.

The custom instruction is sent when the *CINSTRCONF* on page 678 register is written and it is always sent on a single data line SPI interface.

The READY event will be generated when the custom instruction has been sent.

After a custom instruction has been sent, the *CINSTRDAT0* on page 679 and *CINSTRDAT1* on page 679 will contain the response bytes from the custom instruction.

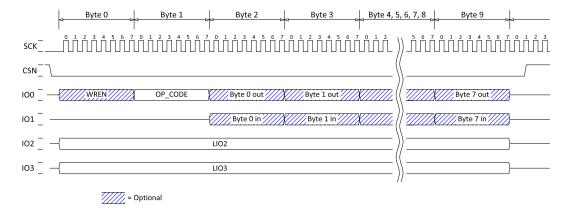


Figure 189: Sending custom instruction



52.6.1 Long frame mode

The LFEN and LFSTOP fields in the *CINSTRCONF* on page 678 control the operation of the custom instruction long frame mode. The long frame mode is a mechanism that permits arbitrary byte length custom instructions. While in long frame mode a long custom instruction sequence is split in multiple writes to the *CINSTRDAT0* on page 679 and *CINSTRDAT1* on page 679 registers.

To enable the long frame mode every write to the *CINSTRCONF* on page 678 register must have the LFEN field set to 1. The contents of the OPCODE field will be transmitted after the first write to *CINSTRCONF* on page 678 and will be omitted in every subsequent write to this register. For subsequent writes the number of data bytes as specified in the LENGTH field are transferred (that is the value of LENGTH - 1 data bytes). The values of the LIO2 and LIO3 fields are set in the first write to *CINSTRCONF* on page 678 and will apply for the entire custom instruction transmission until the long frame is finalized.

To finalize a long frame transmission, the LFSTOP field in *CINSTRCONF* on page 678 must be set to 1 in the last write to this register.

52.7 Deep power-down mode

The external flash memory can be put in deep power-down mode (DPM) to minimize its current consumption when there is no need to access the memory.

DPM is enabled in the *IFCONFIGO* on page 676 register and configured in the *DPMDUR* on page 678 register. The DPM status of the external memory can be read in the *STATUS* on page 677 register. The DPMDUR register has to be configured according to the external flash specification to get the information in the STATUS register and the timing of the READY event correct.

Entering/exiting DPM is controlled using the IFCONFIG1 on page 677 register.

52.8 Instruction set

The table below shows the instruction set being used by the QSPI peripheral when communicating with an external flash device.

Table 129: Instruction set

		5 · · ·
Instruction	Opcode	Description
WREN	0x06	Write enable
RDSR	0x05	Read status register
WRSR	0x01	Write status register
FASTREAD	0x0B	Read bytes at higher speed
READ2O	0x3B	Dual-read output
READ2IO	0xBB	Dual-read input/output
READ4O	0x6B	Quad-read output
READ4IO	0xEB	Quad-read input/output
PP	0x02	Page program
PP2O	0xA2	Dual-page program output
PP4O	0x32	Quad-page program output
PP4IO	0x38	Quad-page program input/output
SE	0x20	Sector erase
BE	0xD8	Block erase
CE	0xC7	Chip erase
DP	0xB9	Enter deep power-down mode
DPE	0xAB	Exit deep power-down mode
EN4B	Specified in the ADDRCONF on page	678 register Enable 32 bit address mode



52.9 Interface description

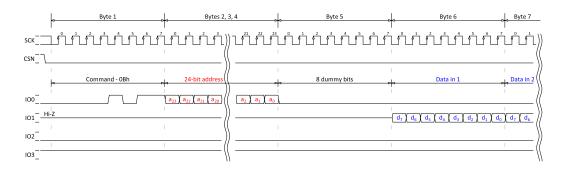


Figure 190: 24-bit FASTREAD, SPIMODE = MODE0

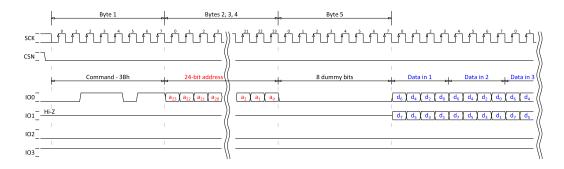


Figure 191: 24-bit READ2O (dual-read output), SPIMODE = MODE0

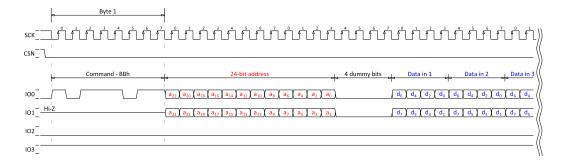


Figure 192: 24-bit READ2IO (dual read input/output), SPIMODE = MODE0

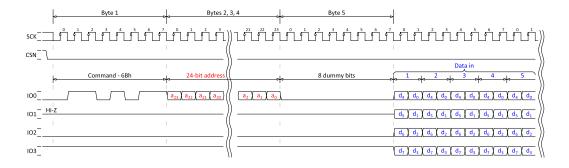


Figure 193: 24-bit READ4O (quad-read output), SPIMODE = MODE0



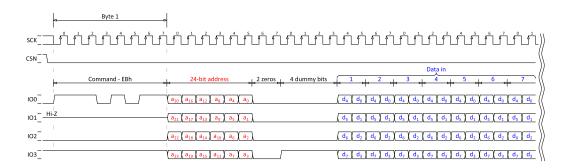


Figure 194: 24-bit READ4IO (quad-read input/output), SPIMODE = MODE0

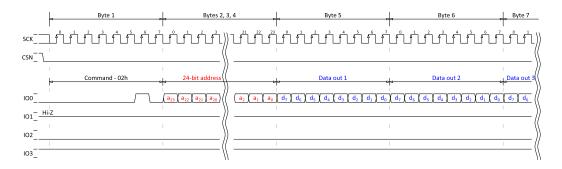


Figure 195: 24-bit PP (page program), SPIMODE = MODE0

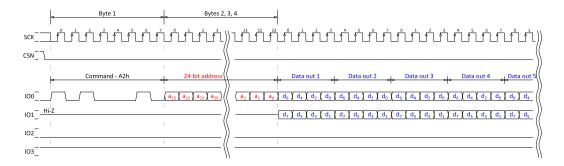


Figure 196: 24-bit PP2O (dual-page program output), SPIMODE = MODE0

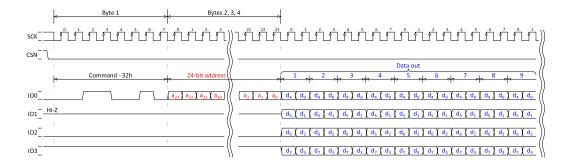


Figure 197: 24-bit PP4O (quad page program output), SPIMODE = MODE0



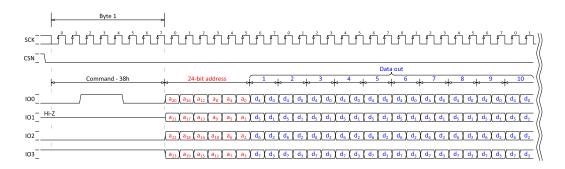


Figure 198: 24-bit PP4IO (quad page program input/output), SPIMODE = MODE0

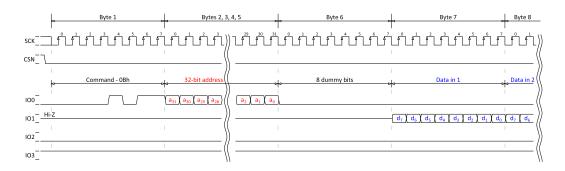


Figure 199: 32-bit FASTREAD, SPIMODE = MODE0

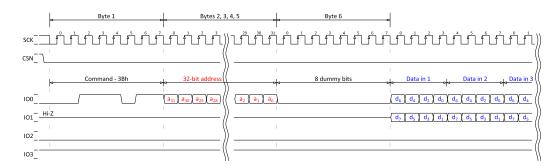


Figure 200: 32-bit READ2O (dual-read output), SPIMODE = MODE0

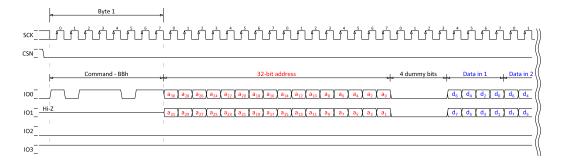


Figure 201: 32-bit READ2IO (dual read input/output), SPIMODE = MODE0



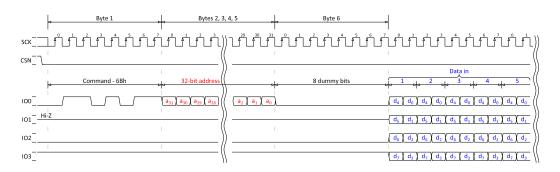


Figure 202: 32-bit READ4O (quad-read output), SPIMODE = MODE0

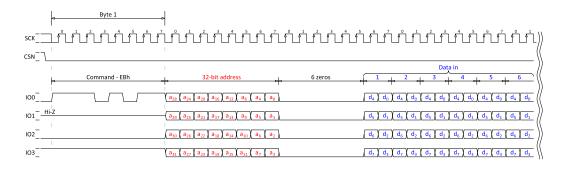


Figure 203: 32-bit READ4IO (quad-read input/output), SPIMODE = MODE0

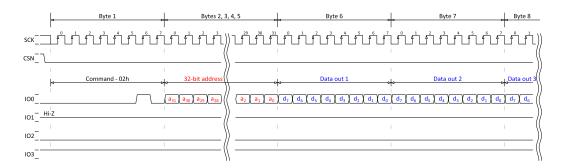


Figure 204: 32-bit PP (page program), SPIMODE = MODE0

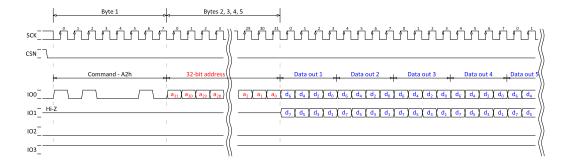


Figure 205: 32-bit PP2O (dual-page program output), SPIMODE = MODE0



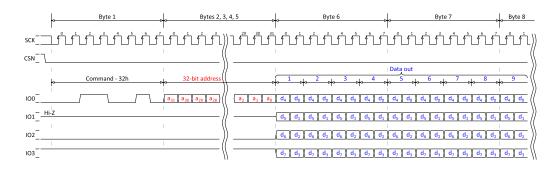


Figure 206: 32-bit PP4O (quad-page program output), SPIMODE = MODE0



Figure 207: 32-bit PP4IO (quad page program input/output), SPIMODE = MODE0

52.10 Registers

Table 130: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40029000	OSPI	OSPI	External memory interface		

Table 131: Register Overview

Register	Offset	Description
TASKS_ACTIVATE	0x000	Activate QSPI interface
TASKS_READSTART	0x004	Start transfer from external flash memory to internal RAM
TASKS_WRITESTART	0x008	Start transfer from internal RAM to external flash memory
TASKS_ERASESTART	0x00C	Start external flash memory erase operation
TASKS_DEACTIVATE	0x010	Deactivate QSPI interface
EVENTS_READY	0x100	QSPI peripheral is ready. This event will be generated as a response to any QSPI task.
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable QSPI peripheral and acquire the pins selected in PSELn registers
READ.SRC	0x504	Flash memory source address
READ.DST	0x508	RAM destination address
READ.CNT	0x50C	Read transfer length
WRITE.DST	0x510	Flash destination address
WRITE.SRC	0x514	RAM source address
WRITE.CNT	0x518	Write transfer length
ERASE.PTR	0x51C	Start address of flash block to be erased
ERASE.LEN	0x520	Size of block to be erased.
PSEL.SCK	0x524	Pin select for serial clock SCK
PSEL.CSN	0x528	Pin select for chip select signal CSN.
PSEL.IO0	0x530	Pin select for serial data MOSI/IOO.
PSEL.IO1	0x534	Pin select for serial data MISO/IO1.



Register	Offset	Description
PSEL.IO2	0x538	Pin select for serial data IO2.
PSEL.IO3	0x53C	Pin select for serial data IO3.
XIPOFFSET	0x540	Address offset into the external memory for Execute in Place operation.
IFCONFIG0	0x544	Interface configuration.
IFCONFIG1	0x600	Interface configuration.
STATUS	0x604	Status register.
DPMDUR	0x614	Set the duration required to enter/exit deep power-down mode (DPM).
ADDRCONF	0x624	Extended address configuration.
CINSTRCONF	0x634	Custom instruction configuration register.
CINSTRDATO	0x638	Custom instruction data register 0.
CINSTRDAT1	0x63C	Custom instruction data register 1.
IFTIMING	0x640	SPI interface timing.

52.10.1 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit	numb	er		31	. 30	29	28	27 2	26 2	25 2	24 2	3 2	2 2	1 2	0 19	18	17	16	15	14 1	3 12	11	10	9	8 7	' 6	5	4	3	2	1 0
Id																															Α
Res	et 0x	0000000		0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0 0	0	0	0	0 (0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						0	esc	cript	tion	1																
Α	RW	READY								nak	ole c	or d	isab	le ii	nter	rup	t fo	RE	٩DY	evei	nt										
											S	ee	EVE	NTS	S_RE	AD	Υ														
			Disabled	0								Disa	ble																		
			Enabled	1							Е	nak	ole																		

52.10.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit numbe	er		31	30 2	9 :	28	27	26	5 25	24	4 23	3 22	2 21	20	19	18	17	7 16	5 1	5 14	4 1	3 1	2 1	1 1	0 9	9 8	8 7	7	6 !	5	4	3	2 :	1 0
Id																																		Α
Reset 0x0	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) () () (0) (0 (כ	0 (0	0	0 (0 (0 0
ld RW	Field	Value Id								D	esci	ripti	on																					
A RW	READY									W	rite	'1'	to E	na	ble	int	err	upt	fo	r Ri	ΕΑΕ)Y e	ver	nt										
											Se	e E	VEN	ITS_	RE	AD	Υ																	
		Set	1								Er	nab	le																					
		Disabled	0								R	ead	: Dis	abl	ed																			
		Enabled	1								R	ead	: En	able	ed																			
		Set Disabled	1	lue							Se Er Re	rite ee <i>E</i> nabl	: '1' <i>VEN</i> le : Dis	to E	na <i>RE</i> ed			err	upt	: foi	r RI	ΞΑΓ)Y e	ver	nt									

52.10.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bitı	numbe	er		31	L 30	29	28	8 27	26	25	24	23	3 2:	2 2:	1 20	19	18	3 17	7 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							D	esc	ript	tion																				
Α	RW	READY										W	/rite	e '1'	' to	Disa	able	e in	terr	upt	for	RE	AD۱	ev ev	ent										_
												Se	ee E	VE	NTS	RE	AD	Y																	
			Clear	1								Di	isak	ole																					
			Disabled	0								Re	ead	: Di	isab	led																			
			Enabled	1 Re						ead	: Er	nabl	ed																						



52.10.4 ENABLE

Address offset: 0x500

Enable QSPI peripheral and acquire the pins selected in PSELn registers

Bitı	numbe	r		31 30	29	28	27	26	25 2	24 2	23 2	22 2	1 20) 19	18	17	16	15 :	14 1	3 12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Value	9					ı	Des	crip	tion																		
Α	RW	ENABLE								1	Enal	ble (or d	isab	le C	SPI															
			Disabled	0						[Disa	ble	QSF	l l																	
			Enabled	1						1	Enal	ble (QSP	ı																	

52.10.5 READ.SRC

Address offset: 0x504

Flash memory source address

Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 1	16	15 1	14 1	13 1	.2 1	11 1	0 9	9 (3 7	' E	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ.	A A	A 4	۱ ۸	Δ Δ		. Α	. A	Α	Α	Α	Α
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0	0	o
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	n																			
Α	RW	SRC										Wo	rd-	alig	nec	l fla	sh ı	mer	nor	ry so	our	ce a	dd	ress										

52.10.6 READ.DST

Address offset: 0x508 RAM destination address

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19 1	l8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	ı
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	۸ 4	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А	ı
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	ı
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			l
Α	RW	DST										Wc	ord-	alig	ned	RA	M d	est	inati	ion	add	res	5.											1

52.10.7 READ.CNT

Address offset: 0x50C Read transfer length

Bit r	umber		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW CNT			Read transfer length in number of bytes. The length must be a
				multiple of 4 bytes.

52.10.8 WRITE.DST

Address offset: 0x510 Flash destination address

Bit number		31	30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	8 17	7 16	15	14	13	12	11 3	.0	9 8	3 7	6	5	4	3	2	1 ()
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 A	A	Α	Α	Α	Α	Α	Δ.	A A	A /	A	A	Α	Α	A	A A	
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0 (
Id RW Field	Value Id	Va	lue							Des	crip	otio	n																		ı

A RW DST Word-aligned flash destination address.



52.10.9 WRITE.SRC

Address offset: 0x514 RAM source address

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13 :	L2 :	11 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	Α Δ	. A	Α	Α	Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	cri	ptic	on																		
Α	RW	SRC										Wc	rd-	alig	nec	l RA	M	sou	rce	ado	dre	ss.											

52.10.10 WRITE.CNT

Address offset: 0x518 Write transfer length

Bit r	numbe	er		31	. 30	29	28 :	27 2	6 2	25 2	4 2	3 22	21	20	19	18	17	16	15	14 1	.3 1	2 1	1 10) 9	8	7	6	5	4	3	2	1	0
Id														Α	Α	Α	Α	Α	Α	Α.	4 4	A A	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et OxC	0000000		0	0	0	0	0 () (0 (0 (0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	llue						D	escr	ipti	on																			
Α	RW	CNT									٧	/rite	tra	nsfe	er le	engt	th ir	n nu	ımb	er c	f by	/tes	. Th	e le	ngt	h m	ust	be	а				
											n	nulti	ole d	of 4	byt	es.																	

52.10.11 ERASE.PTR

Address offset: 0x51C

Start address of flash block to be erased

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Word-aligned start address of block to be erased.

52.10.12 ERASE.LEN

Address offset: 0x520

Size of block to be erased.

Dit access have		21 20 20 20 27 26 25 24	22 22 24 20 40 40 47 46 45 44 42 42 44 40 0 0 7 6 5 4 2 2 4 0
Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A
Reset 0x00000000		0 0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
A RW LEN			LEN
4	4KB	0	Erase 4 kB block (flash command 0x20)
6	64KB	1	Erase 64 kB block (flash command 0xD8)
A	All	2	Erase all (flash command 0xC7)

52.10.13 PSEL.SCK

Address offset: 0x524

Pin select for serial clock SCK

Bit r	numbe	er		31 30	29	28 2	7 26	25	24	23 2	22 2	1 20	19	18 1	7 1	6 15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	! 1	0
Id				С																					В	Α	A A	A A	Α
Res	et OxF	FFFFFF		1 1	1	1 1	l 1	1	1	1	1 1	l 1	1	1 1	L :	l 1	1	1	1 1	l 1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Value					ı	Des	crip	tion																	
Α	RW	PIN		[031]				ı	Pin ı	num	ber																	
В	RW	PORT		[01]					ı	Port	nuı	nbe	r																
С	RW	CONNECT							(Con	nec	ion																	



Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 3	17 16 15 14	13 12 11 10 9	8 7	' 6	5 4	4 3	2 1 0
Id		С						В	А А	A A A
Reset 0xFFFFFFF		1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1	1 1 1 1	l 1 1	. 1	1	1 1	1 1 1
Id RW Field	Value Id	Value	Description							
ld RW Field	Value Id Disconnected	Value 1	Description Disconnect							

52.10.14 PSEL.CSN

Address offset: 0x528

Pin select for chip select signal CSN.

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	вааа
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

52.10.15 PSEL.IO0

Address offset: 0x530

Pin select for serial data MOSI/IO0.

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	вааа
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

52.10.16 PSEL.IO1

Address offset: 0x534

Pin select for serial data MISO/IO1.

Bit r	umbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	вааа
Rese	t OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	PORT		[01]	Port number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

52.10.17 PSEL.IO2

Address offset: 0x538

Pin select for serial data IO2.



Bit r	iumbe	er		31	30 2	29 2	28 2	7 2	6 2	5 2	4 2	23 2	2 2	1 2	0 19	9 18	3 17	16	15	14 :	13 1	12 1	.1 10	9	8	7	6	5	4	3	2 1	١ 0
Id				С																								В	Α	A	4 Α	A A
Res	et OxF	FFFFFF		1	1	1	1 :	1 :	L 1	1 1	1	1	1 :	1 1	l 1	. 1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1 1	. 1
Id	RW	Field	Value Id	Va	lue							Des	crip	tior	1																	
Α	RW	PIN		[0.	.31]						F	Pin r	nun	nbei	r																	
В	RW	PORT		[0.	.1]						F	ort	nu	mbe	er																	
С	RW	CONNECT									(Con	nec	tion	1																	
			Disconnected	1							[Disc	onn	ect																		
			Connected	0							(Con	nec	t																		

52.10.18 PSEL.IO3

Address offset: 0x53C

Pin select for serial data IO3.

Bit r	iumbe	er		31	. 30	29	28 2	27 2	26 2	25 2	24 2	23 2	2 2	1 20	2 19	9 18	17	16	15	14	13 1	2 1	.1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id				С																								В	Α	A A	A A	A A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1 :	1	1	1 1	l 1	. 1	1	1	1	1	1	1 :	1 :	1 1	1	1	1	1	1	1	1 :	l 1	. 1
Id	RW	Field	Value Id	Va	lue							Des	cript	tion	ı																	
Α	RW	PIN		[0	31]						F	Pin r	num	ber																		
В	RW	PORT		[0	1]						F	ort	nur	nbe	er																	
С	RW	CONNECT									(Con	nect	tion																		
			Disconnected	1							[Disc	onn	ect																		
			Connected	0							(Con	nect	t																		

52.10.19 XIPOFFSET

Address offset: 0x540

Address offset into the external memory for Execute in Place operation.

Bitı	numbe	r		33	1 30	0 29	9 2	28 :	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	. 10	9	8	7	6	5	4	3	2	1)
Id				Α	Д	. Α	۱ ۸	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	4
Res	et 0x0	0000000		0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	V	alu	e							De	scri	ptic	on																				
Α	RW	XIPOFFSET											Ad	dre	ss o	ffse	et ir	to 1	the	ex	ter	nal	me	mc	ry	for	Exe	cut	e in	Pla	ice					
													ор												_											

52.10.20 IFCONFIG0

Address offset: 0x544 Interface configuration.

Bitı	numbe	er		31	30 2	29	28	27	20	5 25	5 2	24 2	23 2	22	21	20	19	18	3 1	7 1	6 1	5 :	L4 1	13 1	L2	11	10	9	8	7	6	5	4	3	2	1	0
Id																									G					D	С	В	В	В	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	(0	0	0	0	0	0	0	C	C) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue								Des	cri	pti	on																					
Α	RW	READOC										(Con	fig	ure	nı.	ıml	oer	of	dat	a I	ine	s aı	nd c	орс	ode	e us	sed	for	rea	adir	ng.					Π
			FASTREAD	0								9	Sing	gle	da	ta li	ine	SP	l. F	AST	_R	EΑ	D (орс	ode	e 0x	ίОВ).									
			READ2O	1								[Dua	ıl d	ata	lin	e S	PI.	RE	AD:	20	(o	осо	de (0x3	В).											
			READ2IO	2								[Dua	ıl d	ata	lin	e S	PI.	RE	AD:	210) (c	рсс	de	0x	вв)											
			READ4O	3								(Qua	d	dat	a li	ne	SPI	. R	Α	40) (c	рс	ode	0x	6B)											
			READ4IO	4								(Qua	d	dat	a li	ne	SPI	. R	Α)41	O (opc	ode	0)	ŒΒ).										
В	RW	WRITEOC										(Con	fig	ure	nı	ıml	oer	of	dat	a I	ine	s aı	nd c	ppc	ode	e us	sed	for	wr	itin	g.					
			PP	0								9	Sing	gle	da	ta li	ine	SP	I. P	P (d	opo	od	e 0	x02).												
			PP2O	1								[Dua	ıl d	ata	lin	e S	PI.	PP	20	(o)	occ	de	0xA	(2).												
			PP4O	2								(Qua	d	dat	a li	ne	SPI	. PI	40) (c	рс	ode	0x	32)												
			PP4IO	3								(Qua	d	dat	a li	ne	SPI	. PI	410) C	оро	od	e 0x	(38).											
С	RW	ADDRMODE										1	Add	lre	ssir	ng r	no	de.																			



Bit r	numbe	er		31	30	29 :	28 2	7 2	26 2	25 2	24 2	3 22	2 21	1 20	19	18	17 1	6 1	5 1	4 13	3 12	11	10	9	8 7	6	5	4	3	2 :	1 0
Id																					G				D	С	В	В	В	Α /	А А
Rese	et 0x0	0000000		0	0	0	0 (0	0 (0	0 0	0	0	0	0	0	0) () (0	0	0	0	0	0 0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						D	esc	ript	ion																	
			24BIT	0							2	4-bi	it ac	ddre	ssin	g.															
			32BIT	1							3	2-bi	it ac	ddre	ssin	g.															
D	RW	DPMENABLE									Е	nab	le d	leep	pov	ver-	dov	n r	nod	e (D	PM	fea	ture	e.							
			Disable	0							D	isak	ble (DPIV	l fea	tur	2.														
			Enable	1							E	nab	le D	PM	fea	ture															
G	RW	PPSIZE									P	age	size	e for	cor	nma	nds	PP	, PF	20,	PP4	O ar	nd F	P4I	Ο.						
			256Bytes	0							2	56 k	byte	es.																	
			512Bytes	1							5	12 k	byte	es.																	

52.10.21 IFCONFIG1

Address offset: 0x600 Interface configuration.

																													ä
Bit r	numbe	er		31	30 2	9 28	27	26 2	5 24	1 23 :	22 23	1 20	19	18	17 1	16 1	.5 1	1 13	12	11 1	0 9	8	7	6	5 4	1 3	2	1 ()
Id				G	G G	G G		Е	D														Α	Α	A A	A A	Α	A A	Ĺ
Res	et 0x0	0040480		0	0 0	0 0	0	0 0	0	0	0 0	0	0	1	0 (0 (0 0	0	0	0 1	. 0	0	1	0	0 (0	0	0 (,
Id	RW	Field	Value Id	Val	ue					Des	script	tion																	
Α	RW	SCKDELAY		[0	255]					Mir	nimuı	m an	nour	nt o	f tin	ne t	hat	the	CSN	pin ı	nust	sta	y hi	gh					
										bef	fore it	t can	ı go l	low	aga	in. '	Valu	ie is	spe	cified	l in r	um	ber	of 1	.6				
										МН	Iz per	riods	62	.5 n	ıs).														
D	RW	DPMEN								Ent	ter/ex	kit de	еер і	pov	ver-	dow	vn m	ode	(DF	M) f	or ex	teri	nal f	flash	ı				
										mei	mory	<i>'</i> .																	
			Exit	0						Exit	t DPN	Λ.																	
			Enter	1						Ent	ter DF	PM.																	
Ε	RW	SPIMODE								Sele	ect SI	PI mo	ode.																
			MODE0	0						Мо	ode 0:	Dat	a ar	e ca	ptu	red	on	the c	locl	risii	ng ed	lge :	and	dat	a				
										is o	outpu	t on	a fal	lling	g ed	ge.	Base	e lev	el o	fclo	k is	0 (C	POL	=0,					
										CPF	HA=0).																	
			MODE3	1						Мо	ode 3:	Dat	a ar	e ca	ptu	red	on	the c	locl	(falli	ng e	dge	and	d da	ta				
										is o	outpu	t on	a ris	sing	edg	ge. E	Base	leve	el of	cloc	c is 1	(CF	OL:	=1,					
										CPF	HA=1).																	
G	RW	SCKFREQ		[0	15]					SCK	K freq	uen	cy is	giv	en a	is 32	2 M	Hz/	(SCI	KFRE	Q + :	L).							

52.10.22 STATUS

Address offset: 0x604

Status register.

Bit r	numb	er		31	1 30	29	28	27	26 2	25 2	24	23 2	22 2	21 2	0 1	9 1	8 1	7 1	6 1	5 1	4 1	3 1	2 11	10	9	8	7	6	5	4 3	2	1	0
Id				F	F	F	F	F	F	F	F																			[С		
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0 0) (0 () () () () () () (0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	alue							Des	crip	otion	1																		
С	R	DPM										Dee	рр	owe	r-d	ow	n m	ode	e (D	PΝ	1) st	atu	s of	ext	erna	al fl	ash						
			Disabled	0								Exte	erna	al fla	sh	is n	ot i	n D	PM														
			Enabled	1								Exte	erna	al fla	sh	is in	DF	M.															
D	R	READY										Rea	dy s	statı	JS.																		
			READY	1								QSP	PI pe	eriph	ner	al is	rea	ady.	. It i	is a	llow	ed	to t	rigg	er n	ew	tas	ks,					
											,	writ	ting	cus	ton	n in:	stru	ıcti	ons	or	ent	er/e	exit	DPN	Λ.								
			BUSY	0								QSP	PI pe	eriph	ner	al is	bu	sy.	lt is	no	t al	low	ed t	o tr	igge	er a	ny r	iew					
											1	task	κs, ν	vritii	ng	cust	om	ins	tru	ctio	ons	or e	ente	r/ex	cit D	PM							
F	R	SREG									,	Valu	ue c	of ex	ter	nal	flas	h d	evi	ce S	Stat	us F	Regi	ster	. W	hen	the	9					
												exte	erna	al fla	sh	has	tw	o b	ytes	st	atus	re	giste	er th	is f	ield	inc	lude	es				
											1	the	val	ue o	f th	ne lo	w	byte	≥.														



52.10.23 DPMDUR

Address offset: 0x614

Set the duration required to enter/exit deep power-down mode (DPM).

Bit r	numbe	r		31	30	29	28	27	26 2	25 2	4 2	3 22	21	20	19 1	18 :	17 1	.6 1	5 1	4 13	12	11 1	.0 9	8	7	6	5	4	3	2 1	. 0
Id				В	В	В	В	В	В	ВЕ	3 E	В	В	В	В	В	В	В.	A A	А	Α	Α /	Δ Α	A	Α	Α	Α	Α	A	4 Α	A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1 1	1 1	. 1	1	1	1	1	1 :	1	1 1	l 1	1	1	1 1	. 1	1	1	1	1	1 :	1 1	. 1
Id	RW	Field	Value Id	Va	lue						D	escri	ptic	on																	
Α	RW	ENTER		[0.	.0xF	FFFF	F]				D	urati	on i	nee	ded	by	exte	ern	al fl	ash t	o en	ter	DPN	1. D	ırat	ion	is				
											gi	ven	as E	NTE	ER *	25	6 * (62.	5 ns												
В	RW	EXIT		[0.	.0xF	FFFF	F]				D	urati	on i	nee	ded	by	exte	ern	al fl	ash t	о ех	it DI	PM.	Dur	atio	n is	giv	en			
											as	s EXI	Г*2	256	* 6	2.5	ns.														

52.10.24 ADDRCONF

Address offset: 0x624

Extended address configuration.

Bit r	numbe	er		31	1 30	29	28	27 2	26 2	5 2	4 2	3 22	2 21	20	19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4 3	2	1	0
Id								F	E C) [) (C C	С	С	С	С	С	С	В	В	В	B E	В	В	В	Α	Α	Α	A A	A	Α	Α
Res	et OxO	00000B7		0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	1	0	1	1 (1	1	1
Id	RW	Field	Value Id	Va	alue						D	esc	ripti	on																		
Α	RW	OPCODE		[0	xFF.	.0]					С	рсо	de t	hat	ent	ers	the	32	-bit	ad	dres	sing	g mo	de.								
В	RW	BYTE0		[0	xFF.	.0]					В	yte	0 fo	llow	/ing	ор	cod	e.														
С	RW	BYTE1		[0	xFF.	.0]					В	yte	1 fo	llow	/ing	byt	te 0															
D	RW	MODE									E	xter	nded	lad	dres	ssin	g m	od	e.													
			NoInstr	0							D	o n	ot se	end	any	ins	tru	ctio	n.													
			Opcode	1							S	end	орс	ode	١.																	
			OpByte0	2							S	end	орс	ode	, by	teO).															
			All	3							S	end	орс	ode	, by	teO), by	/te1	L.													
E	RW	WIPWAIT									٧	√ait	for	writ	e co	mp	olet	e b	efoi	re s	end	ng (com	mar	ıd.							
			Disable	0							N	lo w	ait.																			
			Enable	1							٧	√ait																				
F	RW	WREN									S	end	WR	EN ((wri	te e	ena	ble	opo	code	e Ox	06)	befo	re i	nstr	ucti	ion.					
			Disable	0							D	o n	ot se	end	WR	EN.																
			Enable	1							S	end	WR	EN.																		

52.10.25 CINSTRCONF

Address offset: 0x634

Custom instruction configuration register.

A new custom instruction is sent every time this register is written. The READY event will be generated when the custom instruction has been sent.

Bitı	numbe	er		3	1 30	29	28	27	26	25 :	24 :	23 2	2 2	1 20	19	18	17	16	15	14 1	3 12	2 11	10	9	8	7	6	5 4	3	2	1	0
Id																	Н	G	F	ЕΙ) C	В	В	В	В.	A	A	Δ Δ	A	Α	Α	Α
Res	et 0x0	0002000		0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 :	1 0	0	0	0	0	0	0	0 0	0	0	0	0
Id	RW	Field	Value Id	٧	'alue						ı	Desc	ript	ion																		
Α	RW	OPCODE		[(025	5]					(Орс	ode	of C	ust	om	inst	ruc	tion													
В	RW	LENGTH									ı	Leng	th c	of cu	isto	m ir	istri	ıcti	on i	n nı	ımb	er of	byt	es.								
			1B	1							:	Send	d op	cod	e or	ıly.																
			2B	2							:	Send	d op	cod	e, C	INS	ΓRD	ATC	BY.	TE0												
			3B	3							:	Send	d op	cod	e, C	INS	ΓRD	ATC	BY.	TE0	-> C	INST	RD	4T0	.BY	E1						
			4B	4							:	Send	d op	cod	e, C	INS	ΓRD	ATC	.BY	TE0	-> C	INST	RD	ATO	.BY	E2						
			5B	5							:	Send	d ор	cod	e, C	INS	ΓRD	ATC	BY.	TE0	-> C	INST	RD	ATO	.BY	E3						
			6B	6							:	Send	d op	cod	e, C	INS	ΓRD	ATC	BY.	TE0	-> C	INST	RD	4T1	.BY	E4						



Bitı	number		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				H G F E D C B B B A A A A A A A
Res	et 0x00002000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		7B	7	Send opcode, CINSTRDATO.BYTEO -> CINSTRDAT1.BYTE5.
		8B	8	Send opcode, CINSTRDATO.BYTEO -> CINSTRDAT1.BYTE6.
		9B	9	Send opcode, CINSTRDATO.BYTEO -> CINSTRDAT1.BYTE7.
С	RW LIO2		[01]	Level of the IO2 pin (if connected) during transmission of
				custom instruction.
D	RW LIO3		[01]	Level of the IO3 pin (if connected) during transmission of
				custom instruction.
Ε	RW WIPWAI	ī		Wait for write complete before sending command.
		Disable	0	No wait.
		Enable	1	Wait.
F	RW WREN			Send WREN (write enable opcode 0x06) before instruction.
		Disable	0	Do not send WREN.
		Enable	1	Send WREN.
G	RW LFEN			Enable long frame mode. When enabled, a custom instruction
				transaction has to be ended by writing the LFSTOP field.
		Disable	0	Long frame mode disabled
		Enable	1	Long frame mode enabled
Н	RW LFSTOP			Stop (finalize) long frame transaction
		Stop	1	Stop

52.10.26 CINSTRDAT0

Address offset: 0x638

Custom instruction data register 0.

Bit	numbe	r		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 18	3 17	16	15	14 :	13 1	2 11	10	9	8	7	6	5	4	3	2 1	1 0
Id				D	D	D	D	D	D	D	D	С	С	C (C C	. c	С	С	В	В	ВЕ	В	В	В	В	Α	Α	Α	Α	Α .	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	llue							Des	scrip	tio	n																	
Α	RW	BYTE0		[0.	0xF	F]						Dat	ta by	rte ()																	
В	RW	BYTE1		[0.	0xF	F]						Dat	ta by	te 1	1																	
С	RW	BYTE2		[0	0xF	F]						Dat	ta by	rte 2	2																	
D	RW	BYTE3		[0.	0xF	F]						Dat	ta by	rte 3	3																	

52.10.27 CINSTRDAT1

Address offset: 0x63C

Custom instruction data register 1.

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 1	8 17	7 16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				D	D	D	D	D	D	D	D	С	С	C (0	0	C C	С	В	В	В	В	В	В	В	В	Α	Α	Α	A A	A A	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	1																		
Α	RW	BYTE4		[0.	0xF	F]						Dat	a by	rte 4	1																		
В	RW	BYTE5		[0.	0xF	F]						Dat	a by	te !	5																		
С	RW	BYTE6		[0.	.0xF	F]						Dat	a by	rte 6	5																		
D	RW	BYTE7		[0.	0xF	F]						Dat	a by	te 7	7																		

52.10.28 IFTIMING

Address offset: 0x640 SPI interface timing.



Bit r	numbe	r		31 30 2	29 28 :	27 26	25	24 2	23 2:	2 21	20	19	18	17 1	6 15	5 14	13 1	2 13	1 10	9	8	7 6	5	4	3	2	1 0
Id																			С	С	С						
Res	et 0x0	0000200		0 0	0 0	0 0	0	0	0 0	0	0	0	0	0 (0	0	0	0 0	0	1	0 (0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value				ı	Desc	ript	ion																
С	RW	RXDELAY		[70]				1	Timir	ng re	elat	ed to	sa c	mpli	ng c	of the	e inp	ut se	erial	dat	a. Th	e va	lue				
								(of RX	(DEL	.AY	spec	ifie	s the	nuı	mbe	r of	54 N	1Hz c	ycle	s (1	5.62	5 ns	5)			
								(delay	y fro	m t	he t	he r	ising	edg	ge of	the	SPI	Clocl	(S0	CK) u	ntil	the				
								i	nput	t ser	ial (data	is s	amp	led.	As e	n ex	amp	le, it	set	to C	the	inp	ut			
								9	seria	l da	ta is	san	nple	d or	the	risi	ng e	dge (of SC	K.							

52.11 Electrical specification

52.11.1 Current consumption

Symbol	Description	Mi	n.	Тур.	Max.	Units
I _{QSPI,IDLE}	Idle current (enabled, but not activated).					μΑ
I _{QSPI,ACTIVE}	Idle current (activated, but not transferring data).					μΑ
I _{QSPI,DATA}	Run current (activated and transferring data to/from external					μΑ
	Flash at 32 MHz clock frequency).					

52.11.2 Timing specification

Symbol	Description	Mi	n.	Тур.	Max.	Units
F _{QSPI,CLK}	SCK frequency				32	MHz
DC _{QSPI,CLK}	SCK duty cycle					%
F _{QSPI,XIP,16}	XIP fetch frequency for 16 bit instructions.				8	MHz
F _{QSPI,XIP,32}	XIP fetch frequency for 32 bit instructions.				4	MHz
t _{IO,OUT,VALID}	Time from SCK falling until new data valid.					ns
t _{IO,OUT,INVALID}	Time from SCK falling until previous data invalid.					ns



53 CRYPTOCELL — ARM TrustZone CryptoCell 310

ARM® TrustZone® CryptoCell 310 (CRYPTOCELL) is a security subsystem which provides root of trust (RoT) and cryptographic services for a device. CRYPTOCELL services are available to the application through a software library API.

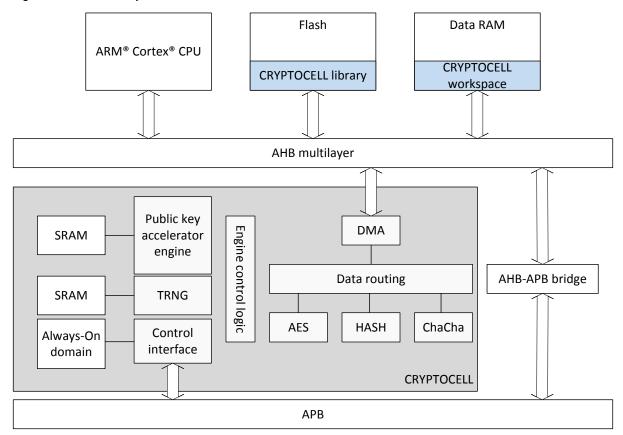


Figure 208: Block diagram for CRYPTOCELL

The following cryptographic features are provided:

- FIPS-140-2 certified true random number generator (TRNG)
- RSA asymmetric encryption
 - Up to 2048 bit key size
 - PKCS#1 v2.1/v1.5
 - · Optional CRT support
- Elliptic curve cryptography (ECC)
 - NIST FIPS 186-4 recommended curves using pseudo-random parameters, up to 521 bits:
 - Prime field: P-192, P-224, P-256, P-384, P-521
 - SEC 2 recommended curves using pseudo-random parameters, up to 521 bits:
 - Prime field: P-160, P-192, P-224, P-256, P-384, P-521
 - Koblitz curves using fixed parameters, up to 256 bits:
 - Prime field: P-160, P-192, P-224, P-256
 - Edwards/Montgomery curves:
 - Ed25519, Curve25519
 - ECDH/ECDSA support
- Secure remote password protocol (SRP)



- Up to 3072 bit operations
- · Hashing functions
 - SHA-1, SHA-2 up to 256 bit size
 - Keyed-hash message authentication code (HMAC)
- AES symmetric encryption
 - General purpose AES engine (encrypt/decrypt, sign/verify)
 - 128 bit key size
 - Supported encryption modes: ECB, CBC, CMAC/CBC-MAC, CTR, CCM/CCM*
- ChaCha20/Poly1305 symmetric encryption
 - · Supported key size: 128 and 256 bits
 - Authenticated encryption with associated data (AEAD) mode

53.1 Standards

ARM® TrustZone® CryptoCell 310 (CRYPTOCELL) supports a number of cryptography standards.

Table 132: CRYPTOCELL cryptography standards

NIST 800-908 ⁴³ Recommendation for the entropy sources used for random bit generation AIS-31 Functionality classes and evaluation methodology for physical random number generators NIST 800-90A Recommendation for random number generation using deterministic random bit generators Stream cipher Chacha "ChaCha, a variant of Salsa20", Daniel J. Bernstein, January 28th 2008 MAC Poly1305 "The Poly1305-AES message-authentication code", Daniel J. Bernstein "Cryptography in NaCl", Daniel J. Bernstein Key agreement SRP "The Secure Remote Password Protocol", Thomas Wu AES FIPS-197 Advanced Encryption Standard NIST SP 800-38A Recommendation for block cipher modes of operation - methods and techniques NIST SP 800-38B Recommendation for block cipher modes of operation: The CMAC mode for authentication NIST SP 800-38C Recommendation for block cipher modes of operation: The CCM mode for authentication and confidentiality ISO/IEC 9797-1 AES CBC-MAC per ISO/IEC 9797-1 MAC algorithm 1 IEEE 802.15.4-2011 Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation Hash FIPS 180-3 Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) RFC2104 HMAC: Keyed-hashing for message authentication RSA PKCS#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS x9.42 Agreement of symmetric keys using discrete logarithm cryptography PKCS#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography IEEE 1363 Standard specifications for public key cryptography	Algorithm family	Identification code	Document name
PRNG NIST 800-90A Recommendation for random number generation using deterministic random bit generators Stream cipher Chacha "ChaCha, a variant of Salsa20", Daniel J. Bernstein, January 28th 2008 MAC Poly1305 "The Poly1305-AES message-authentication code", Daniel J. Bernstein "Cryptography in NaCl", Daniel J. Bernstein Key agreement SRP "The Secure Remote Password Protocol", Thomas Wu AES FIPS-197 Advanced Encryption Standard NIST \$P 800-38A Recommendation for block cipher modes of operation - methods and techniques NIST \$P 800-38B Recommendation for block cipher modes of operation: The CMAC mode for authentication NIST \$P 800-38C Recommendation for block cipher modes of operation: The CCM mode for authentication and confidentiality ISO/IEC 9797-1 AES CBC-MAC per ISO/IEC 9797-1 AMC algorithm 1 IEEE 802.15.4-2011 Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation Hash FIPS 180-3 Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) RFC2104 HMAC: Keyed-hashing for message authentication RSA PKC\$#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS x9.42 Agreement of symmetric keys using discrete logarithm cryptography PKC\$#3 Diffie-Hellman key agreement standard ECC ANS x9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography	TRNG	NIST 800-90B ⁴³	Recommendation for the entropy sources used for random bit generation
Stream cipher Chacha Chacha Chacha, a variant of Salsa20", Daniel J. Bernstein, January 28th 2008 MAC Poly1305 "The Poly1305-AES message-authentication code", Daniel J. Bernstein "Cryptography in NaCl", Daniel J. Bernstein Key agreement SRP The Secure Remote Password Protocol", Thomas Wu AES FIPS-197 Advanced Encryption Standard NIST SP 800-38A Recommendation for block cipher modes of operation - methods and techniques NIST SP 800-38B Recommendation for block cipher modes of operation: The CMAC mode for authentication NIST SP 800-38C Recommendation for block cipher modes of operation: The CCM mode for authentication and confidentiality ISO/IEC 9797-1 AES CBC-MAC per ISO/IEC 9797-1 MAC algorithm 1 IEEE 802.15.4-2011 Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation Hash FIPS 180-3 Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) RFC2104 HMAC: Keyed-hashing for message authentication RSA PKCS#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS X9.42 Agreement of symmetric keys using discrete logarithm cryptography PKCS#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography		AIS-31	Functionality classes and evaluation methodology for physical random number generators
MAC Poly1305 "The Poly1305-AES message-authentication code", Daniel J. Bernstein "Cryptography in NaCl", Daniel J. Bernstein Key agreement SRP "The Secure Remote Password Protocol", Thomas Wu AES FIPS-197 Advanced Encryption Standard NIST SP 800-38A Recommendation for block cipher modes of operation - methods and techniques NIST SP 800-38B Recommendation for block cipher modes of operation: The CMAC mode for authentication NIST SP 800-38C Recommendation for block cipher modes of operation: The CCM mode for authentication and confidentiality ISO/IEC 9797-1 AES CBC-MAC per ISO/IEC 9797-1 MAC algorithm 1 IEEE 802.15.4-2011 Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation Hash FIPS 180-3 Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) RFC2104 HMAC: Keyed-hashing for message authentication RSA PKCS#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS X9.42 Agreement of symmetric keys using discrete logarithm cryptography PKCS#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography	PRNG	NIST 800-90A	Recommendation for random number generation using deterministic random bit generators
"Cryptography in NaCl", Daniel J. Bernstein Key agreement SRP "The Secure Remote Password Protocol", Thomas Wu AES FIPS-197 Advanced Encryption Standard NIST SP 800-38A Recommendation for block cipher modes of operation - methods and techniques NIST SP 800-38B Recommendation for block cipher modes of operation: The CMAC mode for authentication NIST SP 800-38C Recommendation for block cipher modes of operation: The CCM mode for authentication and confidentiality ISO/IEC 9797-1 AES CBC-MAC per ISO/IEC 9797-1 MAC algorithm 1 IEEE 802.15.4-2011 Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation Hash FIPS 180-3 Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) RFC2104 HMAC: Keyed-hashing for message authentication RSA PKCS#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS X9.42 Agreement of symmetric keys using discrete logarithm cryptography PKCS#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography	Stream cipher	Chacha	"ChaCha, a variant of Salsa20", Daniel J. Bernstein, January 28th 2008
Key agreement SRP "The Secure Remote Password Protocol", Thomas Wu AES FIPS-197 Advanced Encryption Standard NIST SP 800-38A Recommendation for block cipher modes of operation - methods and techniques NIST SP 800-38B Recommendation for block cipher modes of operation: The CMAC mode for authentication NIST SP 800-38C Recommendation for block cipher modes of operation: The CCM mode for authentication and confidentiality ISO/IEC 9797-1 AES CBC-MAC per ISO/IEC 9797-1 MAC algorithm 1 IEEE 802.15.4-2011 Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation Hash FIPS 180-3 Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) RFC2104 HMAC: Keyed-hashing for message authentication RSA PKCS#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS X9.42 Agreement of symmetric keys using discrete logarithm cryptography PKCS#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography	MAC	Poly1305	"The Poly1305-AES message-authentication code", Daniel J. Bernstein
AES FIPS-197 Advanced Encryption Standard NIST SP 800-38A Recommendation for block cipher modes of operation - methods and techniques NIST SP 800-38B Recommendation for block cipher modes of operation: The CMAC mode for authentication NIST SP 800-38C Recommendation for block cipher modes of operation: The CCM mode for authentication and confidentiality ISO/IEC 9797-1 AES CBC-MAC per ISO/IEC 9797-1 MAC algorithm 1 IEEE 802.15.4-2011 Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation FIPS 180-3 Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) RFC2104 HMAC: Keyed-hashing for message authentication RSA PKCS#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS X9.42 Agreement of symmetric keys using discrete logarithm cryptography PKCS#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography			"Cryptography in NaCl", Daniel J. Bernstein
NIST SP 800-38A Recommendation for block cipher modes of operation - methods and techniques NIST SP 800-38B Recommendation for block cipher modes of operation: The CMAC mode for authentication NIST SP 800-38C Recommendation for block cipher modes of operation: The CCM mode for authentication and confidentiality ISO/IEC 9797-1 AES CBC-MAC per ISO/IEC 9797-1 MAC algorithm 1 IEEE 802.15.4-2011 Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation FIPS 180-3 Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) RFC2104 HMAC: Keyed-hashing for message authentication RSA PKCS#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS X9.42 Agreement of symmetric keys using discrete logarithm cryptography PKCS#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography	Key agreement	SRP	"The Secure Remote Password Protocol", Thomas Wu
NIST SP 800-38B Recommendation for block cipher modes of operation: The CMAC mode for authentication NIST SP 800-38C Recommendation for block cipher modes of operation: The CCM mode for authentication and confidentiality ISO/IEC 9797-1 AES CBC-MAC per ISO/IEC 9797-1 MAC algorithm 1 IEEE 802.15.4-2011 Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation Hash FIPS 180-3 Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) RFC2104 HMAC: Keyed-hashing for message authentication RSA PKCS#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS X9.42 Agreement of symmetric keys using discrete logarithm cryptography PKCS#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography	AES	FIPS-197	Advanced Encryption Standard
NIST SP 800-38C Recommendation for block cipher modes of operation: The CCM mode for authentication and confidentiality ISO/IEC 9797-1 AES CBC-MAC per ISO/IEC 9797-1 MAC algorithm 1 IEEE 802.15.4-2011 Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation FIPS 180-3 Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) RFC2104 HMAC: Keyed-hashing or message authentication RSA PKCS#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS X9.42 Agreement of symmetric keys using discrete logarithm cryptography PKCS#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography		NIST SP 800-38A	Recommendation for block cipher modes of operation - methods and techniques
ISO/IEC 9797-1 IEEE 802.15.4-2011 Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation Hash FIPS 180-3 Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) RFC2104 HMAC: Keyed-hashing for message authentication RSA PKCS#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS X9.42 PKCS#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography		NIST SP 800-38B	Recommendation for block cipher modes of operation: The CMAC mode for authentication
IEEE 802.15.4-2011 Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation Hash FIPS 180-3 Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) RFC2104 HMAC: Keyed-hashing for message authentication RSA PKC5#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS X9.42 Agreement of symmetric keys using discrete logarithm cryptography PKC5#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography		NIST SP 800-38C	Recommendation for block cipher modes of operation: The CCM mode for authentication and confidentiality
Hash FIPS 180-3 Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512) RFC2104 HMAC: Keyed-hashing for message authentication RSA PKC\$#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS X9.42 Agreement of symmetric keys using discrete logarithm cryptography PKC\$#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography		ISO/IEC 9797-1	AES CBC-MAC per ISO/IEC 9797-1 MAC algorithm 1
RSA PKC\$104 HMAC: Keyed-hashing for message authentication RSA PKC\$#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS X9.42 Agreement of symmetric keys using discrete logarithm cryptography PKC\$#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography		IEEE 802.15.4-2011	Low-Rate Wireless Personal Area Networks, Annex B.4: Specification of generic CCM* mode of operation
RSA PKCS#1 RSA cryptography standard v1.5/v2.1 Diffie-Hellman ANS X9.42 Agreement of symmetric keys using discrete logarithm cryptography PKCS#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography	Hash	FIPS 180-3	Secure Hash Standard (SHA1, SHA-224, SHA-256, SHA-512)
Diffie-Hellman ANS X9.42 PKCS#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography		RFC2104	HMAC: Keyed-hashing for message authentication
PKCS#3 Diffie-Hellman key agreement standard ECC ANS X9.63 Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography	RSA	PKCS#1	RSA cryptography standard v1.5/v2.1
Public Key cryptography for the financial services industry, key agreement and key transport using Elliptic Curve Cryptography	Diffie-Hellman	ANS X9.42	Agreement of symmetric keys using discrete logarithm cryptography
Cryptography		PKCS#3	Diffie-Hellman key agreement standard
IEEE 1363 Standard specifications for public key cryptography	ECC	ANS X9.63	, ,, , , , , , , , , , , , , , , , , , ,
		IEEE 1363	Standard specifications for public key cryptography
ANS X9.62 Public key cryptography for the financial services industry, the Elliptic Curve Digital Signature Algorithm (ECDSA)		ANS X9.62	Public key cryptography for the financial services industry, the Elliptic Curve Digital Signature Algorithm (ECDSA)
Ed25519 Edwards-curve, "High-speed high-security signatures", Daniel J. Bernstein, Niels Duif, Tanja Lange, Peter Schwabe, and Bo-Yin Yang		Ed25519	
Curve25519 Montgomery curve, "Curve25519: new Diffie-Hellman speed records", Daniel J. Bernstein		Curve25519	, ,
FIPS 186-4 Digital Signature Standard (DSS)			
NIST SP 800-56A rev. 2 Recommendation for Pair-Wise Key Establishment Schemes Using Discrete Logarithm Cryptography			
General FIPS 140-2 Security requirements for cryptographic modules	General		, , , , , , , , , , , , , , , , , , , ,

53.2 Control interface

To reduce power consumption, the CRYPTOCELL subsystem is disabled by default, and must be enabled prior to use. Device specific secrets are retained even when CRYPTOCELL is disabled.

53.2.1 Registers

Table 133: Instances

Base address	Peripheral	Instance	Description	Configuration
0x5002A000	CRYPTOCELL	CRYPTOCELL	CryptoCell subsystem control interface	

⁴³ This standard is still marked as draft.



Table 134: Register Overview

Register	Offset	Description
ENABLE	0x500	Control power and clock for CRYPTOCELL subsystem

ENABLE

Address offset: 0x500

Control power and clock for CRYPTOCELL subsystem

Bit r	numbe	r		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	.0 9	9	8 7	' (5 5	5 .	4 3	3 2	2 :	1 0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 () () (0	0 () (0 (0 0
Id	RW	Field	Value Id	Va	alue							Des	scri	ipti	on																			
Α	RW	ENABLE										Ena	able	e or	dis	abl	e th	e C	RYI	PTC	CEI	L s	ubs	/ste	m									
			Disabled	0								CR۱	YPT	oc	ELL	sub	sys	ten	n di	sak	led													
			Enabled	1								CR۱	YPT	oc	ELL	sub	sys	ten	n er	nab	led													
												Wh	ien	en	able	ed t	he (CRY	PTO	OCE	LL:	sub	syst	em	can	be	init	iali	zed	l an	nd			
												con	ntro	olle	d th	rou	gh	the	Cry	/pt	Се	II fii	mv	are	AP	1								

53.2.2 Electrical specification

ARM TrustZone CryptoCell 310 Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{CC310,DISABLED}	CRYPTOCELL subsystem disabled. Regulator = DC/DC, VDD = 3 V.		1.5		μΑ
I _{CC310,IDLE}	CRYPTOCELL subsystem enabled. Regulator = DC/DC, VDD = 3 V.		0.8		mA



54 Mechanical specifications

The mechanical specifications for the packages show the dimensions in millimeters.

54.1 AQFN73 7 x 7 mm package

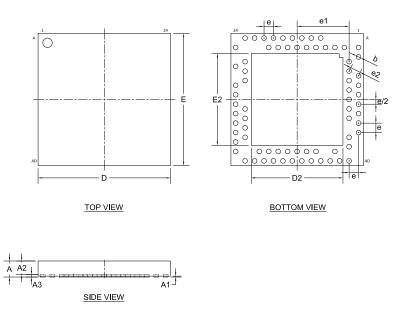


Figure 209: AQFN73 7 x 7 mm package

Table 135: AQFN73 dimensions in millimeters

Package	Α	A1	A2	А3	b	D, E	D2, E2	e	e1	e2	
		0.02			0.20		4.75				Min.
AQFN73 (7x7)		0.05	0.675	0.13	0.25	7.00	4.85	0.5	2.75	0.559	Nom.
	0.85	0.08			0.30		4.95				Max.



55 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

55.1 Package marking

The nRF52840 SoC package is marked as shown in the figure below.

N	5	2	8	4	0
<p< td=""><td>P></td><td><v< td=""><td>V></td><td><h></h></td><td><p></p></td></v<></td></p<>	P>	<v< td=""><td>V></td><td><h></h></td><td><p></p></td></v<>	V>	<h></h>	<p></p>
<y< td=""><td>Y></td><td><w< td=""><td>W></td><td><l< td=""><td>L></td></l<></td></w<></td></y<>	Y>	<w< td=""><td>W></td><td><l< td=""><td>L></td></l<></td></w<>	W>	<l< td=""><td>L></td></l<>	L>

Figure 210: Package marking

55.2 Box labels

Here are the box labels used for the nRF52840.



Figure 211: Inner box label



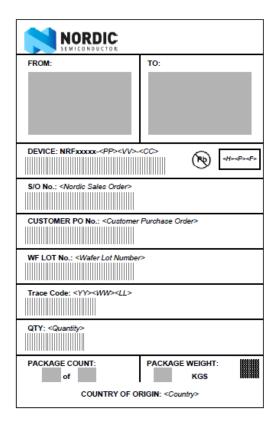


Figure 212: Outer box label

55.3 Order code

Here are the nRF52840 order codes and definitions.

Figure 213: Order code

Table 136: Abbreviations

Definition and implemented codes		
nRF52 series product		
Part code		
Package variant code		
Function variant code		
Build code		
H - Hardware version code		
P - Production configuration code (production site, etc.)		
F - Firmware version code (only visible on shipping container label) Tracking code		
YY - Year code		
WW - Assembly week number		
LL - Wafer lot code Container code		

55.4 Code ranges and values

Defined here are the nRF52840 code ranges and values.

Table 137: Package variant codes

<pp></pp>	Package	Size (mm)	Pin/Ball count	Pitch (mm)	
OI	AOFN	7 x 7	73	0.5	



Table 138: Function variant codes

<vv></vv>	Flash (kB)	RAM (kB)
AA	1024	256

Table 139: Hardware version codes

<h></h>	Description
[A Z]	Hardware version/revision identifier (incremental)

Table 140: Production configuration codes

<p></p>	Description
[09]	Production device identifier (incremental)
[A Z]	Engineering device identifier (incremental)

Table 141: Production version codes

<f></f>	Description
[A N, P Z]	Version of preprogrammed firmware
[0]	Delivered without preprogrammed firmware

Table 142: Year codes

<yy></yy>	Description
[1699]	Production year: 2016 to 2099

Table 143: Week codes

<ww></ww>	Description
[152]	Week of production

Table 144: Lot codes

<ll></ll>	Description	
[AA ZZ]	Wafer production lot identifier	

Table 145: Container codes

<cc></cc>	Description
R7	7" Reel
R	13" Reel
T	Tray

55.5 Product options

Defined here are the nRF52840 product options.

Table 146: nRF52840 order codes

Order code	MOQ ⁴⁴	Comment
nRF52840-QIAA-R7	800	Availability to be announced.
nRF52840-QIAA-R	3000	
nRF52840-QIAA-T	260	

Table 147: Development tools order code

Order code	Description
nRE52840-PREVIEW-DK	nRE52840 Preview Development Kit



56 Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from www.nordicsemi.com.

In this section there are 6 reference circuits to show the components and component values to support onchip features in a design.

Important: This is not a complete list of configurations, but all required circuitry is shown for further configurations.

Some general guidance is summarized here:

- External supply from VDD is only available when power is supplied to VDDH. External supply is annotated with the VEXT net name.
- When supplying power from a USB source only, VBUS must be connected to VDDH if USB is to be used.
- Components required for DC/DC function are only needed if DC/DC mode is enabled for that regulator.
- · NFC can be used in any configuration.
- USB can be used in any configuration as long as VBUS is supplied by the USB host.

Table 148: Circuit configurations

Config no.	Supply configuration		Features tha	t can be enab	oled for each o	onfiguratio	n example
	VDDH	VDD	EXTSUPPLY	DCDCEN0	DCDCEN1	USB	NFC
Config. 1	USB (VDDH = VBUS)	N/A	Yes	No	No	Yes	No
Config. 2	Battery/Ext. regulator	N/A	Yes	No	No	Yes	No
Config. 3	N/A	Battery/Ext. regulator	No	No	No	Yes	No
Config. 4	Battery/Ext. regulator	N/A	Yes	Yes	Yes	Yes	No
Config. 5	N/A	Battery/Ext. regulator	No	No	Yes	Yes	Yes
Config. 6	N/A	Battery/Ext. regulator	No	No	No	No	No

56.1 Circuit configuration no. 1

Table 149: Configuration summary for circuit configuration no. 1

Config no. Supply configuration		Enabled features					
	VDDH	VDD	EXTSUPPLY	DCDCEN0	DCDCEN1	USB	NFC
Config. 1	USB (VDDH = VBUS)	N/A	Yes	No	No	Yes	No



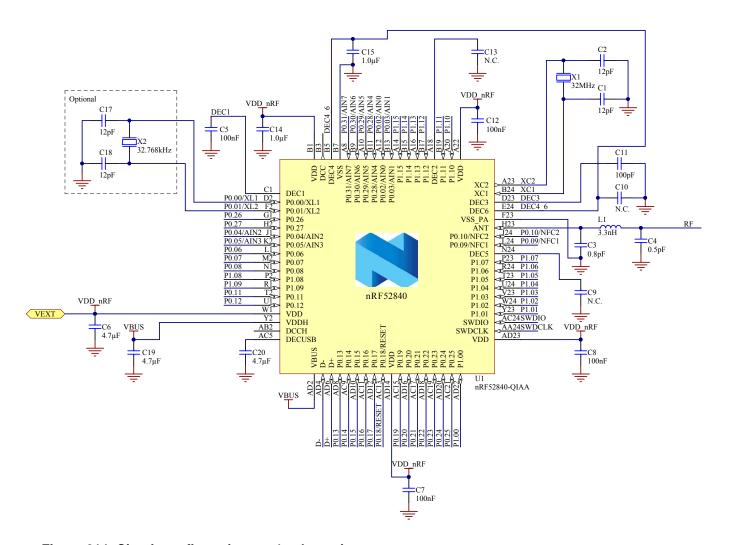


Figure 214: Circuit configuration no. 1 schematic

Important: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52840 on www.nordicsemi.com.

Table 150: Bill of material for circuit configuration no. 1

Designator	Value	Description	Footprint
C1, C2, C17, C18	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4	0.5 pF	Capacitor, NPO, ±10%	0402
C5, C7, C8, C12	100 nF	Capacitor, X7R, ±10%	0402
C6, C20	4.7 μF	Capacitor, X7R, ±10%	0603
C9, C10, C13	N.C.	Not mounted	0402
C11	100 pF	Capacitor, NPO, ±5%	0402
C14, C15	1.0 μF	Capacitor, X7R, ±10%	0603
C19	4.7 μF	Capacitor, X7S, ±10%	0603
L1	3.3 nH	High frequency chip inductor ±5%	0402
U1	nRF52840-QIAA	Multi-protocol Bluetooth low energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary	AQFN-73
		system-on-chip	
X1	32 MHz	Crystal SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	Crystal SMD 3215, 32.768 kHz, Cl=9 pF, Total Tol: ±50 ppm	XTAL_3215

56.2 Circuit configuration no. 2

Table 151: Configuration summary for circuit configuration no. 2

Config no.	onfig no. Supply configuration		Enabled features				
	VDDH	VDD	EXTSUPPLY	DCDCEN0	DCDCEN1	USB	NFC
Config. 2	Battery/Ext. regulator	N/A	Yes	No	No	Yes	No



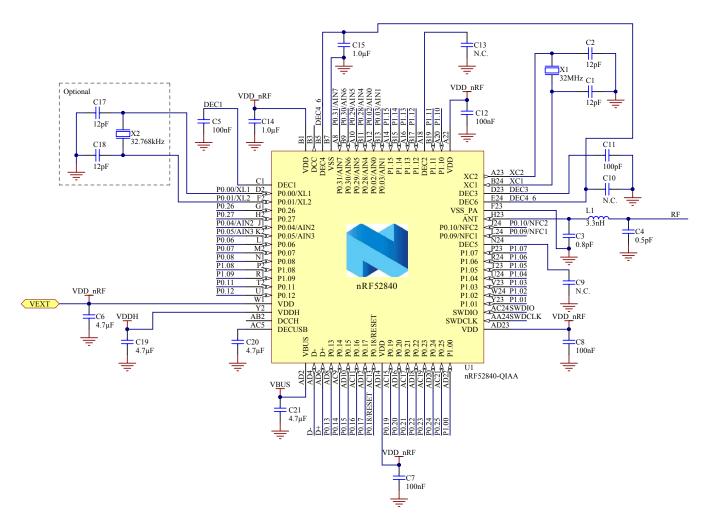


Figure 215: Circuit configuration no. 2 schematic

Important: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52840 on www.nordicsemi.com.

Table 152: Bill of material for circuit configuration no. 2

Designator	Value	Description	Footprint
C1, C2, C17, C18	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4	0.5 pF	Capacitor, NPO, ±10%	0402
C5, C7, C8, C12	100 nF	Capacitor, X7R, ±10%	0402
C6, C20	4.7 μF	Capacitor, X7R, ±10%	0603
C9, C10, C13	N.C.	Not mounted	0402
C11	100 pF	Capacitor, NPO, ±5%	0402
C14, C15	1.0 µF	Capacitor, X7R, ±10%	0603
C19, C21	4.7 μF	Capacitor, X7S, ±10%	0603
L1	3.3 nH	High frequency chip inductor ±5%	0402
U1	nRF52840-QIAA	Multi-protocol Bluetooth low energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary system-on-chip	AQFN-73
X1	32 MHz	Crystal SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	Crystal SMD 3215, 32.768 kHz, Cl=9 pF, Total Tol: ±50 ppm	XTAL_3215

56.3 Circuit configuration no. 3

Table 153: Configuration summary for circuit configuration no. 3

Config no. Supply configuration		Enabled feat	Enabled features				
	VDDH	VDD	EXTSUPPLY	DCDCEN0	DCDCEN1	USB	NFC
Config. 3	N/A	Battery/Ext. regulator	No	No	No	Yes	No



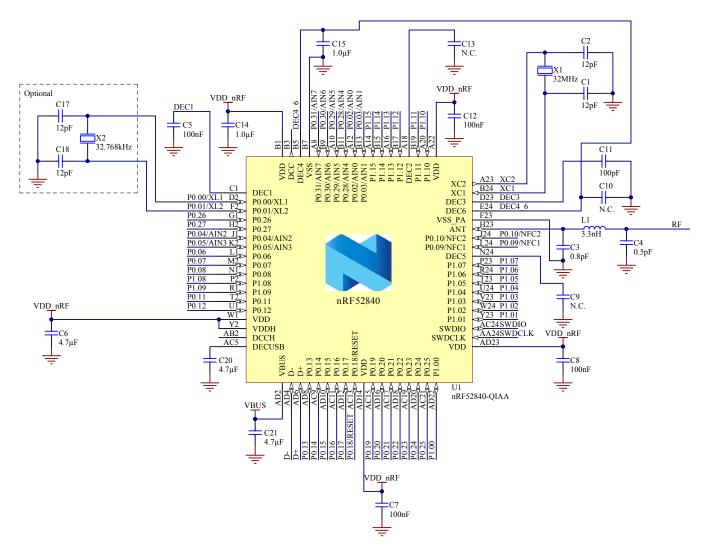


Figure 216: Circuit configuration no. 3 schematic

Important: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52840 on *www.nordicsemi.com*.

Table 154: Bill of material for circuit configuration no. 3

Designator	Value	Description	Footprint
C1, C2, C17, C18	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4	0.5 pF	Capacitor, NPO, ±10%	0402
C5, C7, C8, C12	100 nF	Capacitor, X7R, ±10%	0402
C6, C20	4.7 μF	Capacitor, X7R, ±10%	0603
C9, C10, C13	N.C.	Not mounted	0402
C11	100 pF	Capacitor, NPO, ±5%	0402
C14, C15	1.0 μF	Capacitor, X7R, ±10%	0603
C21	4.7 μF	Capacitor, X7S, ±10%	0603
L1	3.3 nH	High frequency chip inductor ±5%	0402
U1	nRF52840-QIAA	Multi-protocol Bluetooth low energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary system-on-chip	AQFN-73
X1	32 MHz	Crystal SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	Crystal SMD 3215, 32.768 kHz, Cl=9 pF, Total Tol: ±50 ppm	XTAL_3215



56.4 Circuit configuration no. 4

Table 155: Configuration summary for circuit configuration no. 4

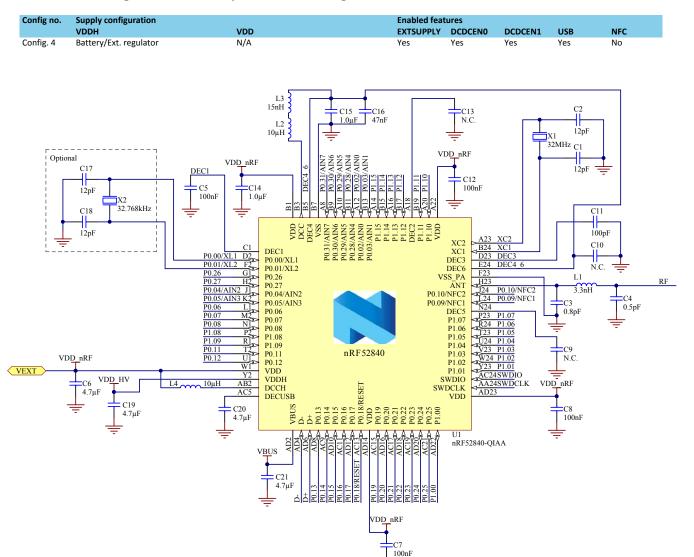


Figure 217: Circuit configuration no. 4 schematic

Important: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52840 on *www.nordicsemi.com*.

Table 156: Bill of material for circuit configuration no. 4

Designator	Value	Description	Footprint
C1, C2, C17, C18	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4	0.5 pF	Capacitor, NPO, ±10%	0402
C5, C7, C8, C12	100 nF	Capacitor, X7R, ±10%	0402
C6, C20	4.7 μF	Capacitor, X7R, ±10%	0603
C9, C10, C13	N.C.	Not mounted	0402
C11	100 pF	Capacitor, NPO, ±5%	0402
C14, C15	1.0 μF	Capacitor, X7R, ±10%	0603
C16	47 nF	Capacitor, X7R, ±10%	0402
C19, C21	4.7 μF	Capacitor, X7S, ±10%	0603
L1	3.3 nH	High frequency chip inductor ±5%	0402
L2	10 μΗ	Chip inductor, IDC min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
L4	10 μΗ	Chip inductor, IDC min = 80 mA, ±10%	0603



Designator	Value	Description	Footprint
U1	nRF52840-QIAA	Multi-protocol Bluetooth low energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary	AQFN-73
		system-on-chip	
X1	32 MHz	Crystal SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	Crystal SMD 3215, 32.768 kHz, Cl=9 pF, Total Tol: ±50 ppm	XTAL_3215

56.5 Circuit configuration no. 5

Table 157: Configuration summary for circuit configuration no. 5

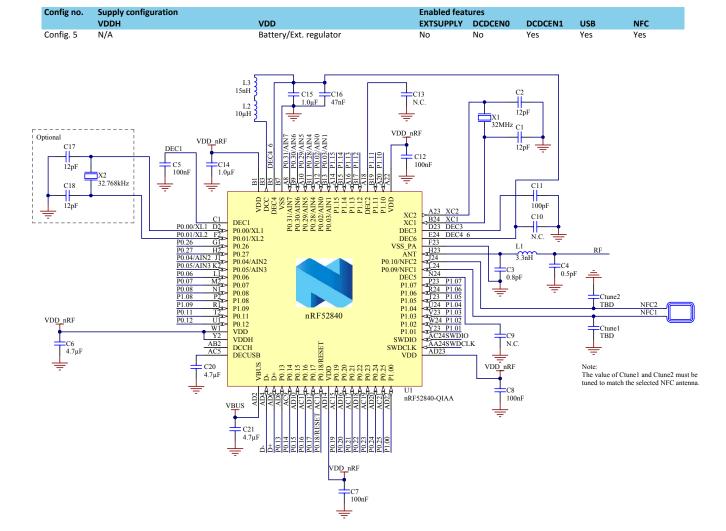


Figure 218: Circuit configuration no. 5 schematic

Important: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52840 on *www.nordicsemi.com*.

Table 158: Bill of material for circuit configuration no. 5

Designator	Value	Description	Footprint
•			
C1, C2, C17, C18	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4	0.5 pF	Capacitor, NPO, ±10%	0402
C5, C7, C8, C12	100 nF	Capacitor, X7R, ±10%	0402
C6, C20	4.7 μF	Capacitor, X7R, ±10%	0603
C9, C10, C13	N.C.	Not mounted	0402
C11	100 pF	Capacitor, NPO, ±5%	0402
C14, C15	1.0 μF	Capacitor, X7R, ±10%	0603
C16	47 nF	Capacitor, X7S, ±10%	0402
C21	4.7 μF	Capacitor, X7S, ±10%	0603
C _{tune1} , C _{tune2}	TBD	Capacitor, NPO, ±5%	0402
L1	3.3 nH	High frequency chip inductor ±5%	0402



Designator	Value	Description	Footprint
L2	10 μΗ	Chip inductor, IDC min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52840-QIAA	Multi-protocol Bluetooth low energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary system-on-chip	AQFN-73
X1	32 MHz	Crystal SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	Crystal SMD 3215, 32.768 kHz, Cl=9 pF, Total Tol: ±50 ppm	XTAL_3215

56.6 Circuit configuration no. 6

Table 159: Configuration summary for circuit configuration no. 6

Config no.	Supply configuration		Enabled features	Enabled features			
	VDDH	VDD	EXTSUPPLY DCD	CENO DCDCEN1	USB	NFC	
Config 6	N/A	Battery/Ext_regulator	No No	No	Nο	No	

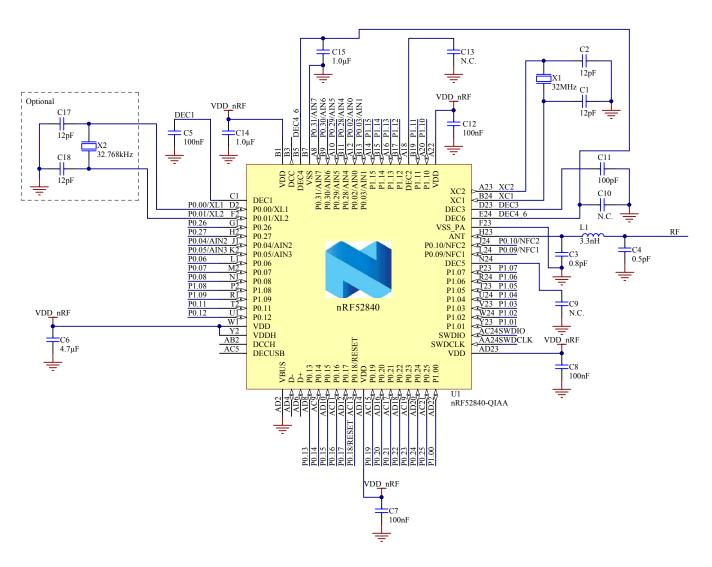


Figure 219: Circuit configuration no. 6 schematic

Important: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52840 on www.nordicsemi.com.

Table 160: Bill of material for circuit configuration no. 6

Designator	Value	Description	Footprint
C1, C2, C17, C18	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4	0.5 pF	Capacitor, NPO, ±10%	0402
C5, C7, C8, C12	100 nF	Capacitor, X7R, ±10%	0402



Designator	Value	Description	Footprint
C6	4.7 μF	Capacitor, X7R, ±10%	0603
C9, C10, C13	N.C.	Not mounted	0402
C11	100 pF	Capacitor, NPO, ±5%	0402
C14, C15	1.0 μF	Capacitor, X7R, ±10%	0603
L1	3.3 nH	High frequency chip inductor ±5%	0402
U1	nRF52840-QIAA	Multi-protocol Bluetooth low energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary system-on-chip	AQFN-73
X1	32 MHz	Crystal SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	Crystal SMD 3215, 32.768 kHz, Cl=9 pF, Total Tol: ±50 ppm	XTAL_3215

56.7 PCB guidelines

A well designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss in performance or functionality.

A qualified RF layout for the IC and its surrounding components, including matching networks, can be downloaded from *www.nordicsemi.com*.

To ensure optimal performance it is essential that you follow the schematics- and layout references closely. Especially in the case of the antenna matching circuitry (components between device pin ANT and the antenna), any changes to the layout can change the behavior, resulting in degradation of RF performance or a need to change component values. All the reference circuits are designed for use with a 50 ohm single-ended antenna.

A PCB with a minimum of two layers, including a ground plane, is recommended for optimal RF performance. On PCBs with more than two layers, put a keep-out area on the inner layers directly below the antenna matching circuitry (components between device pin ANT and the antenna) to reduce the stray capacitances that influence RF performance.

A matching network is needed between the RF pin ANT and the antenna, to match the antenna impedance (normally 50 ohm) to the optimum RF load impedance for the chip. For optimum performance, the impedance for the matching network should be set as described in the recommended AQFN73 package reference circuitry from *Circuit configuration no. 1* on page 688.

The DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. See the schematics for recommended decoupling capacitor values. The supply voltage for the chip should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. A minimum of one via hole should be used for each VSS pin.

Fast switching digital signals should not be routed close to the crystal or the power supply lines. Capacitive loading of fast switching digital output lines should be minimized in order to avoid radio interference.

56.8 PCB layout example

The PCB layout shown below is a reference layout for the AQFN package with internal LDO setup and VBUS supply.

Important: Pay attention to how the capacitor C3 is grounded. It is not directly connected to the ground plane, but grounded via VSS_PA pin F23. This is done to create additional filtering of harmonic components.

For all available reference layouts, see the Reference Layout section on the Downloads tab for nRF52840 on www.nordicsemi.com.



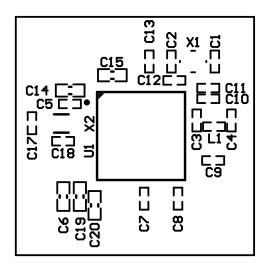


Figure 220: Top silk layer

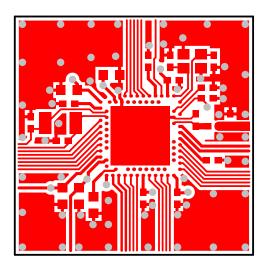


Figure 221: Top layer

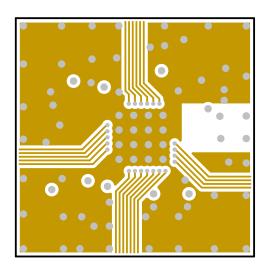


Figure 222: Mid layer 1



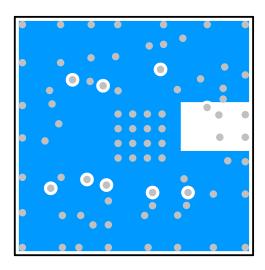


Figure 223: Mid layer 2

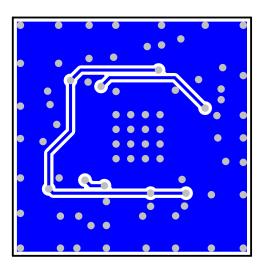


Figure 224: Bottom layer

Important: No components in bottom layer.



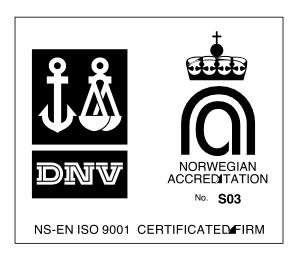
57 Liability disclaimer

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Nordic Semiconductor products meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substances (RoHS) and the requirements of the REACH regulation (EC 1907/2006) on Registration, Evaluation, Authorization and Restriction of Chemicals.

The SVHC (Substances of Very High Concern) candidate list is continually being updated. Complete hazardous substance reports, material composition reports and latest version of Nordic's REACH statement can be found on our website.



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