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3.51 RADIO: Low sensitivity in long range mode
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3.53 I2S: NRF_I2S->PSEL CONNECT fields are not readable
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3.58 NFC: Invalid value in FICR for double-size NFCID1
3.59 PWM: False SEQEND[0] and SEQEND[1] events
3.60 NVMC: Erase or write operations from the external debugger fail when CPU is not halted
nRF52840 Engineering A Errata

This Errata document contains anomalies for the nRF52840 chip, revision Engineering A (QIAA-AA0).
## Change log

See the following list for an overview of changes from previous versions of this document.

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<th>Version</th>
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<td>- Added: No. 78. “High current consumption when using timer STOP task only”</td>
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<td>- Added: No. 158. “High power consumption in DISABLED state”</td>
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<td>v1.3</td>
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<td>- Added: No. 166. “ISO double buffering not functional”</td>
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<td>- Added: No. 170. “NRF_J2S-&gt;PSEL CONNECT fields are not readable”</td>
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<td>- Added: No. 173. “Writes to LATCH register take several CPU cycles to take effect”</td>
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<td>- Added: No. 176. “Flash erase through CTRL-AP fails due to watchdog time-out”</td>
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<td>- Added: No. 179. “COMPARE event is generated twice from a single RTC compare match”</td>
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<td>- Added: No. 184. “Erase or write operations from the external debugger fail when CPU is not halted”</td>
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<td>- Added: No. 156. “Some CLR tasks give unintentional behavior”</td>
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<td>- Added: No. 160. “VDDHDIV5 not functional”</td>
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<td>- Added: No. 164. “Low sensitivity in long range mode”</td>
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<td>• Updated: No. 115. “RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode”</td>
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<td>• Revoked (invalid): No. 129. “Reading EPSTALL register causes undefined behavior”</td>
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<td>• Revoked (invalid): No. 130. “Writing to certain read-only registers causes undefined behavior”</td>
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<td>• Updated: No. 136. “Bits in RESETREAS are set when they should not be”</td>
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<td>• Added: No. 144. “Not optimal NFC performance “</td>
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<td>• Added: No. 145. “SPIM3 not functional”</td>
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<td>• Added: No. 147. “LFRC ULP mode not calibrated in production”</td>
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<td>• Added: No. 150. “EVENT_STARTED does not fire”</td>
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<td>• Added: No. 151. “Access to protected memory through Cache”</td>
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<tr>
<td>Version</td>
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<td>Change</td>
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| nRF52840 Engineering A v1.0 | 06.12.2016 | • Added: No. 15. “RAM[x].POWerset/CLR read as zero”  
• Added: No. 20. “Register values are invalid”  
• Added: No. 36. “Some registers are not reset when expected”  
• Added: No. 51. “Aligned stereo slave mode does not work”  
• Added: No. 54. “Wrong LRCK polarity in Aligned mode”  
• Added: No. 55. “RXPTRUPD and TXPTRUPD events asserted after STOP”  
• Added: No. 58. “An additional byte is clocked out when RXD.MAXCNT = 1”  
• Added: No. 66. “Linearity specification not met with default settings”  
• Added: No. 68. “EVENTS_HFCLKSTARTED can be generated before HFCLK is stable”  
• Added: No. 81. “PIN_CNFF is not retained when in debug interface mode”  
• Added: No. 83. “STOPPED event occurs twice if the STOP task is triggered during a transaction”  
• Added: No. 87. “Unexpected wake from System ON Idle when using FPU”  
• Added: No. 89. “Static 400 µA current while using GPIOTE”  
• Added: No. 94. “BUSSTATE register is not functional”  
• Added: No. 96. “DMA buffers can only be located in the first 64 kB of data RAM”  
• Added: No. 98. “Not able to communicate with the peer”  
• Added: No. 101. “Sleep current increases after soft reset”  
• Added: No. 103. “Reset value of CCM.MAXPACKETSIZE causes encryption, decryption, and MIC failures”  
• Added: No. 104. “EPDATA event is not always generated”  
• Added: No. 110. “Packet loss or degraded sensitivity”  
• Added: No. 111. “Retention in OFF mode is not controlled by RAM[n].POWER->SxRETENTION, but by RAM[n].POWER->SxPOWER”  
• Added: No. 112. “False SFD field matches in IEEE 802.15.4 mode RX”  
• Added: No. 113. “Single-ended mode with external reference is not functional”  
• Added: No. 115. “RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode”  
• Added: No. 116. “HFCLK not stopped when entering into SENSE_FIELD state”  
• Added: No. 117. “Reading address 0x40029618 blocks the device”  
• Added: No. 118. “Reading halfwords or bytes from the XIP region is not supported”  
• Added: No. 119. “Wake up from System OFF on VBUS detect is not functional”  
• Added: No. 121. “Second read and long read commands fail”  
• Added: No. 122. “QSPI uses current after being disabled”  
• Added: No. 127. “Two stop bit setting is not functional”  
• Added: No. 128. “RATIO register is not functional”  
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<td>• Added: No. 131. “EasyDMA transfer size is limited to 255 bytes”</td>
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<td>• Added: No. 133. “NRF_RADIO-&gt;EVENTS_BCMATCH event might trigger twice”</td>
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<td>• Added: No. 134. “ISOINCONFIG register is not functional”</td>
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<td>• Added: No. 135. “SIZE.ISOOUT register does not report empty incoming packets”</td>
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<td>• Added: No. 140. “REG0 External circuitry supply in LDO mode is not functional in System ON IDLE”</td>
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<td>• Added: No. 142. “Sensitivity not according to specification”</td>
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## New and inherited anomalies

The following anomalies are present in revision Engineering A of the nRF52840 chip.

<table>
<thead>
<tr>
<th>ID</th>
<th>Module</th>
<th>Description</th>
<th>New in Engineering A</th>
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<tr>
<td>15</td>
<td>POWER</td>
<td>RAM[x].POWERS/CLR read as zero</td>
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<td>Register values are invalid</td>
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<td>36</td>
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<td>Some registers are not reset when expected</td>
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<tr>
<td>54</td>
<td>I2S</td>
<td>Wrong LRCK polarity in Aligned mode</td>
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<td>55</td>
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<td>RXPTRUPD and TXPTRUPD events asserted after STOP</td>
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<td>SPI</td>
<td>An additional byte is clocked out when RXD.MAXCNT = 1</td>
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<td>66</td>
<td>TEMP</td>
<td>Linearity specification not met with default settings</td>
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<td>68</td>
<td>CLOCK</td>
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<td>NVMC</td>
<td>Access to protected memory through Cache</td>
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<td>153</td>
<td>RADIO</td>
<td>RSSI parameter adjustment</td>
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<td>155</td>
<td>GPIOTE</td>
<td>IN event may occur more than once on input edge</td>
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<td>SAADC</td>
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### Table 1: New and inherited anomalies

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<th>Module</th>
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<td>NFCT</td>
<td>Invalid value in FICR for double-size NFCID1</td>
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<td>PWM</td>
<td>False SEQEND[0] and SEQEND[1] events</td>
<td>X</td>
</tr>
<tr>
<td>184</td>
<td>NVMC</td>
<td>Erase or write operations from the external debugger fail when CPU is not halted</td>
<td>X</td>
</tr>
</tbody>
</table>

#### 3.1 [15] POWER: RAM[x].POWERSET/CLR read as zero

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**

RAM[x].POWERSET and RAM[x].POWERCLR read as zero, even though the RAM is on.

**Conditions**

Always.

**Consequences**

Not possible to read the RAM state using RAM[x].POWERSET and RAM[x].POWERCLR registers. Write works as it should.

**Workaround**

Use RAM[x].POWER to read the state of the RAM.

#### 3.2 [20] RTC: Register values are invalid

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**

RTC registers will not contain the correct/expected value if read.

**Conditions**

The RTC has been idle.

**Consequences**

RTC configuration cannot be determined by reading RTC registers.
### Workaround

Execute the below code before you use RTC.

```c
NRF_CLOCK->EVENTS_LFCLKSTARTED = 0;
NRF_CLOCK->TASKS_LFCLKSTART = 1;
while (NRF_CLOCK->EVENTS_LFCLKSTARTED == 0) {};
NRF_RTC0->TASKS_STOP = 0;
```

### 3.3 [36] CLOCK: Some registers are not reset when expected

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

#### Symptoms

After watchdog timeout reset, CPU lockup reset, soft reset, or pin reset, the following CLOCK peripheral registers are not reset:
- CLOCK->EVENTS_DONE
- CLOCK->EVENTS_CTTO
- CLOCK->CTIV

#### Conditions

After watchdog timeout reset, CPU Lockup reset, soft reset, and pin reset.

#### Consequences

Register reset values might be incorrect. It may cause undesired interrupts in case of enabling interrupts without clearing the DONE or CTTO events.

#### Workaround

Clear affected registers after reset. This workaround has already been added into system_nrf52.c file. This workaround has already been added into system_nrf52840.c file present in MDK 8.11.0 or later.

### 3.4 [54] I2S: Wrong LRCK polarity in Aligned mode

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

#### Symptoms

In Aligned mode, left and right samples are swapped.

#### Conditions

CONFIG.FORMAT = ALIGNED

#### Consequences

Left and right audio channels are swapped.
3.5 [55] I2S: RXPTRUPD and TXPTRUPD events asserted after STOP

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
The RXPTRUPD event is generated when the STOP task is triggered, even though reception (RX) is disabled. Similarly, the TXPTRUPD event is generated when the STOP task is triggered, even though transmission (TX) is disabled.

Conditions
A previous transfer has been performed with RX/TX enabled, respectively.

Consequences
The indication that RXTXD.MAXCNT words were received/transmitted is false.

Workaround
Ignore the RXPTRUPD and TXPTRUPD events after triggering the STOP task. Clear these events before starting the next transfer.

3.6 [58] SPIM: An additional byte is clocked out when RXD.MAXCNT = 1

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
SPIM clocks out additional byte.

Conditions
RXD.MAXCNT = 1
TXD.MAXCNT <= 1

Consequences
Additional byte is redundant.
New and inherited anomalies

Workaround

Use the SPI module (deprecated but still available) or use the following workaround with SPIM:

```c
/**  
 * @brief Work-around for transmitting 1 byte with SPIM.  
 *  
 * @param spim: The SPIM instance that is in use.  
 * @param ppi_channel: An unused PPI channel that will be used by the workaround.  
 * @param gpiote_channel: An unused GPIOTE channel that will be used by the workaround.  
 *  
 * @warning Must not be used when transmitting multiple bytes.  
 * @warning After this workaround is used, the user must reset the PPI channel and the  
 * GPIOTE channel before attempting to transmit multiple bytes.  
 */  
void setup_workaround_for_ftpan_58(NRF_SPIM_Type * spim, uint32_t ppi_channel, uint32_t  
  gpiote_channel)
{
  // Create an event when SCK toggles.
  NRF_GPIOTE->CONFIG[gpiote_channel] = (  
    GPIOTE_CONFIG_MODE_Event <<  
    GPIOTE_CONFIG_MODE_Pos
  ) | (  
    spim->PSEL.SCK <<  
    GPIOTE_CONFIG_PSEL_Pos
  ) | (  
    GPIOTE_CONFIG_POLARITY_Toggle <<  
    GPIOTE_CONFIG_POLARITY_Pos
  );

  // Stop the spim instance when SCK toggles.
  NRF_PPI->CH[ppi_channel].EEP = (uint32_t)&NRF_GPIOTE->EVENTS_IN[gpiote_channel];
  NRF_PPI->CH[ppi_channel].TEP = (uint32_t)&spim->TASKS_STOP;
  NRF_PPI->CHENSET = 1U << ppi_channel;

  // The spim instance cannot be stopped mid-byte, so it will finish  
  // transmitting the first byte and then stop. Effectively ensuring  
  // that only 1 byte is transmitted.
}
```

3.7 [66] TEMP: Linearity specification not met with default settings

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

TEMP module provides non-linear temperature readings over the specified temperature range.

Conditions

Always
**Consequences**
TEMP module returns out of spec temperature readings.

**Workaround**
Execute the following code after reset:

```
NRF_TEMP->A0 = NRF_FICR->TEMP.A0;
NRF_TEMP->A1 = NRF_FICR->TEMP.A1;
NRF_TEMP->A2 = NRF_FICR->TEMP.A2;
NRF_TEMP->A3 = NRF_FICR->TEMP.A3;
NRF_TEMP->A4 = NRF_FICR->TEMP.A4;
NRF_TEMP->A5 = NRF_FICR->TEMP.A5;
NRF_TEMP->B0 = NRF_FICR->TEMP.B0;
NRF_TEMP->B1 = NRF_FICR->TEMP.B1;
NRF_TEMP->B2 = NRF_FICR->TEMP.B2;
NRF_TEMP->B3 = NRF_FICR->TEMP.B3;
NRF_TEMP->B4 = NRF_FICR->TEMP.B4;
NRF_TEMP->B5 = NRF_FICR->TEMP.B5;
NRF_TEMP->T0 = NRF_FICR->TEMP.T0;
NRF_TEMP->T1 = NRF_FICR->TEMP.T1;
NRF_TEMP->T2 = NRF_FICR->TEMP.T2;
NRF_TEMP->T3 = NRF_FICR->TEMP.T3;
NRF_TEMP->T4 = NRF_FICR->TEMP.T4;
```

This code is already present in the latest `system_nrf52.c` file and in the `system_nrf52840.c` file released in MDK 8.12.0.

### 3.8 [68] CLOCK: EVENTS_HFCLKSTARTED can be generated before HFCLK is stable

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
EVENTS_HFCLKSTARTED may come before HFXO is started.

**Conditions**
When using a 32 MHz crystal with start-up longer than 400 µs.

**Consequences**
Performance of radio and peripheral requiring HFXO will be degraded until the crystal is stable.

**Workaround**
32 MHz crystal oscillator startup time must be verified by the user. If the worst-case startup time is shorter than 400 µs, no workaround is required. If the startup time can be longer than 400 µs, the software must ensure, using a timer, that the crystal has had enough time to start up before using peripherals that
require the HFXO. The Radio requires the HFXO to be stable before use. The ADC, TIMERS, and TEMP sensor for example can use the HFXO as a reference for improved accuracy.

3.9 [78] TIMER: High current consumption when using timer STOP task only
This anomaly applies to IC Rev. Engineering A, build codes Q1AA-AA0.

**Symptoms**
Increased current consumption when the timer has been running and the STOP task is used to stop it.

**Conditions**
The timer has been running (after triggering a START task) and then it is stopped using a STOP task only.

**Consequences**
Increased current consumption.

**Workaround**
Use the SHUTDOWN task after the STOP task or instead of the STOP task.

3.10 [81] GPIO: PIN_CNF is not retained when in debug interface mode
This anomaly applies to IC Rev. Engineering A, build codes Q1AA-AA0.

**Symptoms**
GPIO pin configuration is reset on wakeup from System OFF.

**Conditions**
The system is in debug interface mode.

**Consequences**
GPIO state unreliable until PIN_CNF is reconfigured.

3.11 [83] TWIS: STOPPED event occurs twice if the STOP task is triggered during a transaction
This anomaly applies to IC Rev. Engineering A, build codes Q1AA-AA0.

**Symptoms**
STOPPED event is set after clearing it.
New and inherited anomalies

3.12 [87] CPU: Unexpected wake from System ON Idle when using FPU
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
The CPU is unexpectedly awoken from System ON Idle.

Conditions
The FPU has been used.

Consequences
The CPU is awoken from System ON Idle.

Workaround
The FPU can generate pending interrupts just like other peripherals, but unlike other peripherals there are no INTENSET, INTENCLR registers for enabling or disabling interrupts at the peripheral level. In order to prevent unexpected wake-up from System ON Idle, add this code before entering sleep:

```c
#if (__FPU_USED == 1)
  __set_FPSCR(_get_FPSCR() & ~(0x0000009F));
  (void)__get_FPSCR();
  NVIC_ClearPendingIRQ(FPU_IRQn);
#endif
__WFE();
```

3.13 [89] TWI: Static 400 µA current while using GPIOTE
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
Static current consumption between 400 µA to 450 µA when using TWI in combination with GPIOTE.
New and inherited anomalies

Conditions
- GPIOTE is configured in event mode
- TWI utilizes EasyDMA

Consequences
Current consumption higher than specified

Workaround
Turn the TWI off and back on after it has been disabled. To do so: If TWI0 is used,

```c
*(volatile uint32_t *)0x40003FFC = 0;
*(volatile uint32_t *)0x40003FFC;
*(volatile uint32_t *)0x40003FFC = 1;
```

If TWI1 is used,

```c
*(volatile uint32_t *)0x40004FFC = 0;
*(volatile uint32_t *)0x40004FFC;
*(volatile uint32_t *)0x40004FFC = 1;
```

Write 0 followed by a 1 to the POWER register (address 0xFFC) of the TWI that needs to be disabled. Reconfiguration of TWI is required before next usage.

3.14 [94] USBD: BUSSTATE register is not functional
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
BUSSTATE register is not functional.

Conditions
Always.

Consequences
Reading BUSSTATE will not show the state of the bus as documented. No impact on USB 2.0 compliance.

Workaround
None.

3.15 [96] I2S: DMA buffers can only be located in the first 64 kB of data RAM
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.
New and inherited anomalies

Symptoms
The I2S will not read and write the RAM location specified by the data pointer.

Conditions
DMA buffers are located entirely or in part above address 0x2000 FFFF.

Consequences
Data or memory corruption

Workaround
Set DMA buffers to use memory range 0x2000 0000 to 0x2000 FFFF.

3.16 [97] GPIOTE: High current consumption in System ON Idle mode
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
High current consumption (<20 µA) in System ON Idle mode.

Conditions
GPIOTE used with one or more channels in input mode.

Consequences
Higher current consumption.

Workaround
Use Port event to detect transitions on inputs instead of GPIOTE input mode.

3.17 [98] NFCT: Not able to communicate with the peer
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
The NFCT is not able to receive or transmit messages to the peer.

Conditions
Always

Consequences
The NFCT cannot communicate with the peer.
Workaround

Write 0x00038148 to 0x4000568C before the NFC peripheral is enabled:

```
*(volatile uint32_t *)0x4000568Cu1 = 0x00038148ul;
```

The workaround is included in the system_nrf52840.c file present in MDK 8.11.0 or later.

3.18 [103] CCM: Reset value of CCM.MAXPACKETSIZE causes encryption, decryption, and MIC failures

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Failing encryption, decryption, and MIC on extended length packets.

Conditions

Always for extended length packets.

Consequences

Failing encryption, decryption, and MIC on extended length packets.

Workaround

Set CCM.MAXPACKETSIZE to 0xFB.

This workaround has already been added into the system_nrf52840.c file present in MDK 8.11.1 or later.

3.19 [104] USBD: EPDATA event is not always generated

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The EPDATA event might not be generated, and the related update of EPDATASTATUS does not occur.

Conditions

Sometimes.

Consequences

It is not possible to develop a custom USB stack.

Workaround

Use the USB stack provided in Nordic's SDK.
3.20 [110] RADIO: Packet loss or degraded sensitivity

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
In BLE Long Range or 802.15.4 modes, subsequent packets after the first packet might not be received. In BLE and proprietary modes, the sensitivity might be degraded.

**Conditions**
Always.

**Consequences**
Might lose packets in BLE LR or 802.15.4 mode. Might lose some sensitivity in BLE and proprietary mode.

**Workaround**
Always disable the radio after having received a packet (using TASK_DISABLE). The workaround is included in the S132 and S140 SoftDevice.

3.21 [111] RAM: Retention in OFF mode is not controlled by RAM[n].POWER->SxRETENTION, but by RAM[n].POWER->SxPOWER

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
Current consumption in OFF mode is higher than expected. RAM contents are retained in OFF mode when they should not be.

**Conditions**
Always.

**Consequences**
Cannot independently control RAM retention in OFF mode and power in ON mode.

**Workaround**
Use RAM[n].POWER->SxPOWER to control the retention in OFF mode and power in ON mode. Exercise caution when using this workaround, because the firmware requires a certain amount of RAM to be powered when waking from OFF mode (such as the RAM where the call stack is located), and RAM[n].POWER registers are retained registers.
3.22 [112] RADIO: False SFD field matches in IEEE 802.15.4 mode RX

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
False FRAMESTART, ADDRESS, PAYLOAD, and END events are triggered and a corrupted packet with a failing CRC is received.

**Conditions**
The SFD octet of the packet on air does not match the value configured in the SFD register.

**Consequences**
Packet with CRC error is received, when it should have been discarded based on SFD field.

**Workaround**
Check for CRC failure after the END event triggers.

3.23 [113] COMP: Single-ended mode with external reference is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
COMP output is not correct.

**Conditions**
COMP is used in single-ended mode with external reference.

**Consequences**
COMP cannot be used in this mode.

**Workaround**
None.

3.24 [115] RAM: RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.
New and inherited anomalies

**Symptoms**
RAM not correctly retained.

**Conditions**
System ON Idle mode or System OFF is used with parts or all RAM retained.

**Consequences**
RAM not correctly retained.

**Workaround**
Apply the following code after any reset:

```c
*(volatile uint32_t *)0x40000EE4 = ( (*(volatile uint32_t *)0x40000EE4 & 0x00000070) | // Keep bit 6:4
    (*(uint32_t *)0x10000258 & 0x0000000F) ); // Replace bit 3:0
```

This workaround has already been added into system_nrf52840.c file present in MDK 8.11.0 or later. This workaround increases the I_RAM current per 4 KB section from 20 nA to 30 nA.

### 3.25 [116] NFCT: HFCLK not stopped when entering into SENSE_FIELD state

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
Higher current consumption than specified in SENSE_FIELD state.

**Conditions**
The NFCT is going from ACTIVATED state to SENSE_FIELD state.

**Consequences**
Higher current consumption in SENSE_FIELD state.

**Workaround**
- Do not use the FIELDLOST_SENSE shortcut in NFCT.
- Do not use a PPI channel to short FIELDLOST event and SENSE task in NFCT.
- When the FIELDLOST event is triggered in NFCT, write 0x01 to address 0x40005010. Then trigger the SENSE task in NFCT to go into SENSE_FIELD state.
3.26 [117] System: Reading address 0x40029618 blocks the device
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
The debugger interface is lost. The device halts or seems to stop executing.

Conditions
Reading address 0x40029618ul, either directly from firmware or with the debugger (for example, using a memory window in the IDE).

Consequences
Crash. Need to power cycle the device and restart the debugging session.

Workaround
Do not read address 0x40029618ul.

3.27 [118] QSPI: Reading halfwords or bytes from the XIP region is not supported
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
The CPU is interrupted with a bus fault.

Conditions
The CPU reads a halfword or a byte from the XIP region. The following instructions could cause a byte or halfword load:

- LDRB
- LDRBT
- LDREXB
- LDRSB
- LDRSBT
- LDRH
- LDRHT
- LDREXH
- LDRSH
- LDRSHT
- TBB
- TBH
**Consequences**

Cannot run code from external memory.

**Workaround**

Link the firmware such that the run-time location of the read-only data section is in internal flash or RAM. Also, do not write assembly or C code that reads byte or halfword sized data from external flash.

**ARM® Compiler armcc**

To prevent the generation of TBB and TBH instructions, use the compiler command line option `--execute_only`. This option will also prevent the generation of instructions that read literals from code sections.

**GNU ARM Embedded Toolchain**

Using version Q3 2016 or later, you can prevent the generation of TBB and TBH instructions by using the compiler option `--mpure-code`. This option will also prevent the generation of instructions that read literals from the .text section.

3.28 [119] POWER: Wake up from System OFF on $V_{BUS}$
detect is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**

In System OFF mode, the device will not wake up when $V_{BUS}$ supply is connected.

**Conditions**

Always.

**Consequences**

The device remains in System OFF mode.

**Workaround**

External circuitry can be used to translate $V_{BUS}$ voltage levels to GPIO voltage levels that can be used to trigger a GPIO DETECT signal (configured using the GPIOTE peripheral) to wake from System OFF.

3.29 [121] QSPI: Second read and long read commands fail

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**

- QSPI read command never gets sent.
- QSPI read command of more than 0x20 characters fails.
3.30 [122] QSPI: QSPI uses current after being disabled
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
Current consumption is too high.

Conditions
After QSPI has been activated by the use of TASKS_ACTIVATE task.

Consequences
Current consumption is too high.

Workaround
Execute the following code before disabling QSPI:

```
*(volatile uint32_t *)0x40029010ul = 1ul;
```

3.31 [127] UARTE: Two stop bit setting is not functional
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
Setting CONFIG.STOP=Two (2 stop bits) has no effect.

Conditions
Always.

Consequences
UARTE traffic with 2 stop bit setting is not supported.

Workaround
None.
3.32 [128] PDM: RATIO register is not functional
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
The RATIO register is not functional.

Conditions
Always.

Consequences
The only supported ratio between PDM_CLK and output audio sample rate is 64.

Workaround
None.

3.33 [131] UARTE: EasyDMA transfer size is limited to 255 bytes
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
DMA transfer is not as long as configured. Only the 8 least significant bits of RXD.MAXCNT and TXD.MAXCNT registers are functional.

Conditions
RXD.MAXCNT and/or TXD.MAXCNT are configured for DMA transfers > 255 bytes.

Consequences
EasyDMA transfer sizes longer than 255 bytes are not supported. Larger size values are treated modulo 256.

Workaround
Split long transfers into chunks of 255 bytes or less.

3.34 [133] CLOCK,RADIO: NRF_RADIO->EVENTS_BCMATCH event might trigger twice
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
A task might be triggered twice by the NRF_RADIO->EVENTS_BCMATCH event.
New and inherited anomalies

Conditions
- The NRF_RADIO->EVENTS_BCMATCH event is used to trigger tasks through PPI or SHORTS.
- BCC is set to match after one more bit than the packet size during TX.

Consequences
Tasks connected through PPI or SHORTS to this event might be triggered twice.

Workaround
None.

3.35 [134] USBD: ISOINCONFIG register is not functional
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
The ISOINCONFIG register is not functional

Conditions
Always.

Consequences
Not possible to change the behavior of the ISO IN endpoint response to an IN token when no data is to be sent. The USBD will not respond to the IN token in this situation.

Workaround
None.

3.36 [135] USBD: SIZE.ISOOUT register does not report empty incoming packets
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
The SIZE.ISOOUT register does not report empty incoming packets in the ZERO field.

Conditions
Always.

Consequences
The firmware cannot rely on the ZERO field to know if a zero-length ISO OUT packet has been received.
3.37 [136] System: Bits in RESETREAS are set when they should not be

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
After pin reset, RESETREAS bits other than RESETPIN might also be set.

**Conditions**
A pin reset has triggered.

**Consequences**
If the firmware evaluates RESETREAS, it might take the wrong action.

**Workaround**
When RESETREAS shows a pin reset (RESETPIN), ignore other reset reason bits.

```
if (NRF_POWER->RESETREAS & POWER_RESETREAS_RESETPIN_Msk) {
    NRF_POWER->RESETREAS = ~POWER_RESETREAS_RESETPIN_Msk;
}
```

This workaround is implemented in MDK version 8.13.0 and later.

3.38 [140] POWER: REG0 External circuitry supply in LDO mode is not functional in System ON IDLE

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
External circuitry supply does not work. A BOR might occur.

**Conditions**
Using REG0 in LDO mode in System ON IDLE.

**Consequences**
External circuitry supply cannot be used to supply current >1 mA in System ON IDLE.
New and inherited anomalies

Workaround
Use REG0 in DCDC mode.

3.39 [142] RADIO: Sensitivity not according to specification
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
Radio receiver sensitivity is 1 dB lower than specified.

Conditions
All radio modes.

Consequences
Reduction in receiver sensitivity.

Workaround
None.

3.40 [143] RADIO: False CRC failures on specific addresses
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
100% CRC failure rate even if the payload is received correctly.

Conditions
Nordic proprietary radio mode. CRCCNF.SKIPADDR = 0. CRC calculation includes the address field.
Logical address 0 and logical address 1 to 7 have the same BASE address MSBs configured.

ADDRLEN=5
BASE0 = 0xAAAAAXXXX
BASE1 = 0xAAAAAXXXX
ADDRLENLEN=4
BASE0 = 0xAAXXXXXX
BASE1 = 0xAAXXXXXX

AND logical address 0 and one of the logical addresses 1 to 7 have the same PREFIX value configured.
The issue is present regardless of which logical address is enabled in RXADDRESSES.
New and inherited anomalies

Consequences

If receiving on logical address 0, the address is reconstructed incorrectly for CRC calculation, resulting in CRCSTATUS.CRCError being returned. However, the received payload bytes are correct. Packet error rate 100 percent. RXMATCH shows the wrong logical address.

Workaround

Use one of the following workarounds:

• Use the ESB and Gazell libraries of SDK v14.0.0 or later.
  This implementation applies the following workaround.
• Set bit 16 in RXADDRESSES to 1.
• Apply the following code before triggering the RXEN task:

```
*(volatile uint32_t *) 0x40001774 = (*((volatile uint32_t *) 0x40001774) & 0xfffffffe) | 0x01000000;
```

This code will reduce sensitivity with 3 dB.

3.41 [144] NFCT: Not optimal NFC performance

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Short NFC read distance or failing NFC connection with peer device.

Conditions

Always.

Consequences

No connection or short read distance to peer device.

Workaround

Execute the following code before using the NFCT peripheral:

```
*(volatile uint32_t *)0x4000561c = 0x1ul;
*(volatile uint32_t *)0x4000562c = 0x3Ful;
*(volatile uint32_t *)0x4000563c = 0x0ul;
*(volatile uint32_t *)0x40005528 = 0xCul;
```

3.42 [145] SPIM: SPIM3 not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.
New and inherited anomalies

Symptoms
The SPIM3 peripheral is not functional.

Conditions
Always.

Consequences
The SPIM3 peripheral is not functional.

Workaround
None.

3.43 [147] CLOCK: LFRC ULP mode not calibrated in production
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
The LFRC oscillator non-calibrated frequency tolerance (ftol_uncal_ifulp) in ULP mode is not according to specification.

Conditions
LFRC in ULP mode.

Consequences
The LFRC ULP oscillator non-calibrated frequency is unreliable.

Workaround
Do calibration after each power-up, after changing mode between normal mode and ULP mode, and if the temperature changes more than 40°C.

3.44 [150] SAADC: EVENT_STARTED does not fire
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
EVENT_STARTED does not fire.

Conditions
ADC started (TASKS_START) with PPI task. Any channel configured to TACQ <= 5 µs.
Consequences
ADC cannot be started (TASKS_START) with PPI if TACQ <= 5 μs.

Workaround
Use TAQC > 5 μs when starting ADC from PPI.

3.45 [151] NVMC: Access to protected memory through Cache
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
CPU stalls.

Conditions
Instruction cache enabled. Parts of Flash protected by ACL against reads. Reading or instruction fetching from a read protected area.

Consequences
CPU stalls and not hardfaults. Only recoverable by an external reset (pin reset or power reset, and watchdog timer if enabled)

Workaround
None.

3.46 [153] RADIO: RSSI parameter adjustment
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
RSSI changes over temperature.

Conditions
Temperature ≤ +10°C or > +30°C.

Consequences
RSSI parameter not within specified accuracy.

Workaround
Add the following compensation to the RSSI sample value based on temperature measurement (the on-chip TEMP peripheral can be used to measure temperature):
• For TEMP ≤ -30°C, RSSISAMPLE = RSSISAMPLE +3
• For TEMP > -30°C and TEMP ≤ -10°C, RSSISAMPLE = RSSISAMPLE +2
New and inherited anomalies

- For TEMP > -10°C and TEMP ≤ +10°C, RSSISAMPLE = RSSISAMPLE + 1
- For TEMP > +10°C and TEMP ≤ +30°C, RSSISAMPLE = RSSISAMPLE + 0
- For TEMP > +30°C and TEMP ≤ +50°C, RSSISAMPLE = RSSISAMPLE - 1
- For TEMP > +50°C and TEMP ≤ +70°C, RSSISAMPLE = RSSISAMPLE - 2
- For TEMP > +70°C, RSSISAMPLE = RSSISAMPLE - 3

3.47 [155] GPIOTE: IN event may occur more than once on input edge

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
IN event occurs more than once on an input edge.

**Conditions**
Input signal edges are closer together than 1.3 µs or >= 750 kHz for a periodic signal.

**Consequences**
Tasks connected through PPI or SHORTS to this event might be triggered twice.

**Workaround**
Apply the following code when any GPIOTE channel is configured to generate an IN event on edges that can occur within 1.3 µs of each other:

```c
*(volatile uint32_t *)(NRF_GPIOTE_BASE + 0x600 + (4 * GPIOTE_CH_USED)) = 1;
```

**Important:** A clock is kept on by the workaround and must be reverted to avoid higher current consumption when GPIOTE is not in use, using the following code:

```c
*(volatile uint32_t *)(NRF_GPIOTE_BASE + 0x600 + (4 * GPIOTE_CH_USED)) = 0;
```

3.48 [156] GPIOTE: Some CLR tasks give unintentional behavior

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
One of the following:
- Current consumption is high when entering IDLE.
- Latency for detection changes on inputs connected to GPIOTE channels becoming longer than expected.
Conditions
Using the following tasks:

<table>
<thead>
<tr>
<th>Address</th>
<th>GPIOTE task</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x060</td>
<td>TASK_CLR[0]</td>
</tr>
<tr>
<td>0x064</td>
<td>TASK_CLR[1]</td>
</tr>
<tr>
<td>0x068</td>
<td>TASK_CLR[2]</td>
</tr>
<tr>
<td>0x06C</td>
<td>TASK_CLR[3]</td>
</tr>
<tr>
<td>0x070</td>
<td>TASK_CLR[4]</td>
</tr>
<tr>
<td>0x074</td>
<td>TASK_CLR[5]</td>
</tr>
<tr>
<td>0x078</td>
<td>TASK_CLR[6]</td>
</tr>
<tr>
<td>0x07C</td>
<td>TASK_CLR[7]</td>
</tr>
</tbody>
</table>

Consequences
High current consumption or too long time from external event to internal triggering of PPI event and/or IRQ from GPIOTE.

Using TASK_CLR[n] for even values of \( n \) has the side effect of setting the system in constant latency mode (see POWER->TASKS_CONSTLAT). Using TASK_CLR[n] for odd values of \( n \) has the side effect of setting the system in low power mode (see POWER->TASKS_LOWPOWER).

Workaround
To set the system back in the mode it was before using the TASK_CLR[\( n \)], triggering of tasks with even \( n \) must be followed by triggering any of the TASK_CLR with odd \( n \) and vice versa.

3.49 [158] RADIO: High power consumption in DISABLED state
This anomaly applies to IC Rev. Engineering A, build codes Q1AA-AA0.

Symptoms
Power consumption is 500 µA when the radio is disabled (should be 40 - 50 µA).

Conditions
RXEN Radio, wait for READY (ramping up), START, and immediately followed by DISABLE.

Consequences
Increased current consumption.

Workaround
Do not trigger DISABLE immediately after START.
3.50 [160] SAADC: VDDHDIV5 not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**

VDDHDIV5 setting on CH[x].PSELP and CH[x].PSELN is not functional.

**Conditions**

Always.

**Consequences**

VDDHDIV5 setting on CH[x].PSELP and CH[x].PSELN is not functional.

**Workaround**

None.

3.51 [164] RADIO: Low sensitivity in long range mode

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**

Lower than specified sensitivity in BLE long range mode.

**Conditions**

Receiving in long range mode.

**Consequences**

Reduced range.

**Workaround**

Add the following code after reset or before enabling the radio, when using BLE long range mode:

```c
*(volatile uint32_t *)0x4000173C |= 0x80000000;
*(volatile uint32_t *)0x4000173C = ((*(volatile uint32_t *)0x4000173C & 0xFFFFFF00) | 0x5C);
```

When using other Radio modes, use the below code to return to original settings before enabling the Radio:

```c
*(volatile uint32_t *)0x4000173C &= ~0x80000000;
```
3.52 [166] USBD: ISO double buffering not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
The double buffering of the ISO EPs of the USBD is not functional.

**Conditions**
Always. With default settings, the buffers overlap.

**Consequences**
During ISO transition, received or transmitted data is likely to be corrupted.

**Workaround**
Reconfigure ISO buffers during initialization of USBD. After each time the USBD peripheral is enabled, apply the following code:

```c
 *((volatile uint32_t *)(NRF_USBD_BASE + 0x800)) = 0x7E3;
 *((volatile uint32_t *)(NRF_USBD_BASE + 0x804)) = 0x40;
```

3.53 [170] I2S: NRF_I2S->PSEL CONNECT fields are not readable

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
- CONNECT field of NRF_I2S->PSEL.MCK is not readable.
- CONNECT field of NRF_I2S->PSEL.SCK is not readable.
- CONNECT field of NRF_I2S->PSEL.LRCK is not readable.
- CONNECT field of NRF_I2S->PSEL.SDIN is not readable.
- CONNECT field of NRF_I2S->PSEL.SDOUT is not readable.

**Conditions**
Always.

**Consequences**
When reading the value of NRF_I2S->PSEL registers, the CONNECT field might not return the same value that has been written to it.

**Workaround**
None.
3.54 [173] GPIO: Writes to LATCH register take several CPU cycles to take effect

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
A bit in the LATCH register reads '1' even after clearing it by writing '1'.

**Conditions**
Reading the LATCH register right after writing to it.

**Consequences**
Old value of the LATCH register is read.

**Workaround**
Have at least 3 CPU cycles of delay between the write and the subsequent read to the LATCH register. This can be achieved by having 3 dummy reads to the LATCH register.

3.55 [176] System: Flash erase through CTRL-AP fails due to watchdog time-out

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

**Symptoms**
Full flash erase through CTRL-AP is not successful.

**Conditions**
WDT is enabled.

**Consequences**
Flash is not erased. If the device has a WDT time-out less than 1 ms and is readback-protected through UICR.APPROTECT, there is a risk of permanently preventing the erasing of the flash.

**Workaround**
Try again.

3.56 [179] RTC: COMPARE event is generated twice from a single RTC compare match

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.
New and inherited anomalies

Symptoms
Tasks connected to RTC COMPARE event through PPI are triggered twice per compare match.

Conditions
RTC registers are being accessed by CPU while RTC is running.

Consequences
Tasks connected to RTC COMPARE event through PPI are triggered more often than expected.

Workaround
Do not access the RTC registers, including the COMPARE event register, from CPU while waiting for the RTC COMPARE event. Note that CPU interrupt from this event can still be enabled.

3.57 [180] USBD: Wrong PLL calibration in production
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
USB PLL frequency is not according to specification.

Conditions
Some engineering devices with date code 1716 and later.

Consequences
USB not functional.

Workaround
None.

3.58 [181] NFCT: Invalid value in FICR for double-size NFCID1
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
NFC not communicating with the peer device.

Conditions
Using NFCID1 values from FICR and using double-size ID. FICR address 0x454 NFC.TAGHEADER1.UD4 is equal to 0x88.
New and inherited anomalies

Consequences
NFC does not communicate reliably with the peer device.

Workaround
Do not use 0x88 value in NFCID1.

3.59 [183] PWM: False SEQEND[0] and SEQEND[1] events
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
False SEQEND[0] and SEQEND[1] events are being generated.

Conditions
Any of the LOOPSDONE_SEQSTARTn shortcuts are enabled. LOOP register is non-zero and sequence 1 is one value long.

Consequences
SEQEND[0] and SEQEND[1] events might falsely trigger other tasks if these are routed through the PPI.

Workaround
Avoid using the LOOPSDONE_SEQSTARTn shortcuts, when LOOP register is non-zero and sequence 1 is one value long.

3.60 [184] NVMC: Erase or write operations from the external debugger fail when CPU is not halted
This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms
The erase or write operation fails or takes longer time than specified.

Conditions
NVMC erase or write operation initiated using an external debugger. CPU is not halted.

Consequences
The NVMC erase or write operation fails or takes longer time than specified.
Workaround

Halt the CPU by writing to DHCSR (Debug Halting Control and Status Register) before starting NVMC erase or write operation from the external debugger. See the ARM infocenter to get the details of the DHCSR register.

Programming tools provided by Nordic Semiconductor comply with this.