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3.57 WDT: WDT configuration is cleared when entering system OFF
3.58 NFCT: Frame delay timing is too short after SLP_REQ
3.59 TWIM: I2C timing spec is violated at 400 kHz
3.60 CPU: RAM is not ready when written
3.61 RADIO: CRC is wrong when data whitening is enabled and address field is included in CRC calculation

4 Fixed anomalies
nRF52832 Revision 2 Errata

This Errata document contains anomalies for the nRF52832 chip, revision Revision 2 (CIAA-Ex0, QFAA-Ex0, QFAB-Ex0, CIAA-EA0, QFAA-EA0).

The document indicates which anomalies are fixed, inherited, or new compared to revision Revision 1.
## Revision history

See the following list for an overview of changes from previous versions of this document.

<table>
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<td>nRF52832 Revision 2 v1.6</td>
<td>09.11.2020</td>
<td>- Added: No. 245. “CRC is wrong when data whitening is enabled and address field is included in CRC calculation”</td>
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<td>nRF52832 Rev 2 v1.5</td>
<td>10.07.2020</td>
<td>- Updated: No. 220. “RAM is not ready when written”</td>
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<td>nRF52832 Rev 2 v1.4</td>
<td>03.12.2019</td>
<td>- Updated: No. 196. “PSEL acquires GPIOs regardless of ENABLE”</td>
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<td>- Added: No. 212. &quot;Events are not generated when switching from scan mode to no-scan mode with burst enabled”</td>
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<td>- Added: No. 218. “Frame delay timing is too short after SLP_REQ”</td>
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<td>- Added: No. 220. “RAM is not ready when written”</td>
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<td>- Updated: No. 141. “HFCLK not stopped when entering SENSE mode”</td>
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<td>- Added: No. 213. “WDT configuration is cleared when entering system OFF”</td>
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<td>- Added: No. 219. “I2C timing spec is violated at 400 kHz”</td>
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<td>nRF52832 Rev 2 v1.2</td>
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<td>- Updated: No. 138. “Spurious emission on GPIO exceeds limits in radiated tests”</td>
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<td>- Added: No. 204. “Switching between TX and RX causes unwanted emissions”</td>
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<td>- Added: No. 210. “Bits in GPIO LATCH register are incorrectly set to 1”</td>
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<td>nRF52832 Rev 2 v1.1</td>
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<td>- Updated: No. 89. “Static 400 µA current while using GPIOTE”</td>
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<td>- Updated: No. 182. “Fixes for anomalies #102, #106, and #107 do not take effect”</td>
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<td>- Added: No. 192. “LFRC frequency offset after calibration”</td>
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<td>- Added: No. 194. “STOP task does not switch off all resources”</td>
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<td>- Added: No. 196. “PSEL acquires GPIOs regardless of ENABLE”</td>
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<td>- Added: No. 201. “EVENTS_HFCLKSTARTED might be generated twice”</td>
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| nRF52832 Rev 2 v1.0 | 11.12.2017 | • Added: No. 12. “Reference ladder is not correctly calibrated”  
• Added: No. 15. “RAM[x].POWERSET/CLR read as zero”  
• Added: No. 20. “Register values are invalid”  
• Added: No. 31. “Calibration values are not correctly loaded from FICR at reset”  
• Added: No. 36. “Some registers are not reset when expected”  
• Added: No. 51. “Aligned stereo slave mode does not work”  
• Added: No. 54. “Wrong LRCK polarity in Aligned mode”  
• Added: No. 55. “RXPTRUPD and TXPTRUPD events asserted after STOP”  
• Added: No. 58. “An additional byte is clocked out when RXD.MAXCNT = 1”  
• Added: No. 64. “Only full bytes can be received or transmitted, but supports 4-bit frame transmit”  
• Added: No. 66. “Linearity specification not met with default settings”  
• Added: No. 67. “Some events cannot be used with the PPI”  
• Added: No. 68. “EVENTS_HFCLKSTARTED can be generated before HFCL is stable”  
• Added: No. 72. “TASKS_ACTIVATE cannot be used with the PPI”  
• Added: No. 74. “Started events fires prematurely”  
• Added: No. 75. “Increased current consumption”  
• Added: No. 76. “READY event is set sooner than it should”  
• Added: No. 77. “RC oscillator is not calibrated when first started”  
• Added: No. 78. “High current consumption when using timer STOP task only”  
• Added: No. 79. “A false EVENTS_FIELDDETECTED event occurs after the field is lost”  
• Added: No. 81. “PIN_CNF is not retained when in debug interface mode”  
• Added: No. 83. “STOPPED event occurs twice if the STOP task is triggered during a transaction”  
• Added: No. 84. “ISOURCE not functional”  
• Added: No. 86. “Triggering START task after offset calibration may write a sample to RAM”  
• Added: No. 87. “Unexpected wake from System ON Idle when using FPU”  
• Added: No. 88. “Increased current consumption when configured to pause in System ON idle”  
• Added: No. 89. “Static 400 µA current while using GPIOTE”  
• Added: No. 91. “Radio performance using CSP package version”  
• Added: No. 97. “High current consumption in System ON Idle mode”  
• Added: No. 101. “Sleep current increases after soft reset”  
• Added: No. 108. “RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode”  
• Added: No. 109. “DMA access transfers might be corrupted”  
• Added: No. 113. “Single-ended mode with external reference is not functional”  
• Added: No. 132. “The LFRC oscillator might not start”  |
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<th>Change</th>
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<tr>
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<td>• Added: No. 136. “Bits in RESETREAS are set when they should not be”</td>
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<td>• Added: No. 138. “Spurious emission on GPIO exceeds limits in radiated tests”</td>
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<td>• Added: No. 141. “HFCLK not stopped when entering SENSE mode”</td>
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<td>• Added: No. 143. “False CRC failures on specific addresses”</td>
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<td>• Added: No. 146. “LFRC frequency deviation”</td>
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<td>• Added: No. 149. “First clock pulse after clock stretching may be too long or too short”</td>
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<td>• Added: No. 176. “Flash erase through CTRL-AP fails due to watchdog time-out”</td>
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<td>• Added: No. 178. “END event firing too early”</td>
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<td>• Added: No. 182. “Fixes for anomalies #102, #106, and #107 do not take effect”</td>
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<td>• Added: No. 183. “False SEQEND[0] and SEQEND[1] events”</td>
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# New and inherited anomalies

The following anomalies are present in revision Revision 2 of the nRF52832 chip.

<table>
<thead>
<tr>
<th>ID</th>
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<td>Some registers are not reset when expected</td>
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<td>51</td>
<td>I2S</td>
<td>Aligned stereo slave mode does not work</td>
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<td>54</td>
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<td>Wrong LRCK polarity in Aligned mode</td>
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<td>RXPRTRUD and TXPRTRUD events asserted after STOP</td>
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<td>SPIM</td>
<td>An additional byte is clocked out when RXD.MAXCNT = 1</td>
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<td>False CRC failures on specific addresses</td>
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<td>LFRC frequency deviation</td>
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<td>TWIM</td>
<td>First clock pulse after clock stretching may be too long or too short</td>
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<td>GPIOTE</td>
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<td>System</td>
<td>Flash erase through CTRL-AP fails due to watchdog time-out</td>
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<td>178</td>
<td>SAADC</td>
<td>END event firing too early</td>
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<td>COMPARE event is generated twice from a single RTC compare match</td>
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<td>Fixes for anomalies #102, #106, and #107 do not take effect</td>
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<tr>
<td>192</td>
<td>CLOCK</td>
<td>LFRC frequency offset after calibration</td>
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New and inherited anomalies

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<tr>
<th>ID</th>
<th>Module</th>
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<th>New in Revision 2</th>
<th>Inherited from Revision 1</th>
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<td>194</td>
<td>I2S</td>
<td>STOP task does not switch off all resources</td>
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<td>X</td>
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Table 1: New and inherited anomalies

3.1 [12] COMP: Reference ladder is not correctly calibrated

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**

COMP does not compare correctly.

**Conditions**

Always.

**Consequences**

COMP module is unusable.

**Workaround**

Execute the following code before enabling the COMP module:

```c
*(volatile uint32_t *)0x40013540 = (*(volatile uint32_t *)0x10000324 & 0x00001F00) >> 8;
```

This workaround is included in MDK version 8.12.0 and later.
3.2 [15] POWER: RAM[x].POWERSET/CLR read as zero

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.

**Symptoms**

RAM[x].POWERSET and RAM[x].POWERCLR read as zero, even though the RAM is on.

**Conditions**

Always.

**Consequences**

Not possible to read the RAM state using RAM[x].POWERSET and RAM[x].POWERCLR registers. Write works as it should.

**Workaround**

Use RAM[x].POWER to read the state of the RAM.

3.3 [20] RTC: Register values are invalid

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.

**Symptoms**

RTC registers will not contain the correct/expected value if read.

**Conditions**

The RTC has been idle.

**Consequences**

RTC configuration cannot be determined by reading RTC registers.

**Workaround**

Execute the below code before you use RTC.

```c
NRF_CLOCK->EVENTS_LFCLKSTARTED = 0;
NRF_CLOCK->TASKS_LFCLKSTART = 1;
while (NRF_CLOCK->EVENTS_LFCLKSTARTED == 0) {};
NRF_RTC0->TASKS_STOP = 0;
```
3.4 [31] CLOCK: Calibration values are not correctly loaded from FICR at reset

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
RCOSC32KICALLENGTH is initialized with the wrong FICR value.

**Conditions**
Always.

**Consequences**
RCOSC32KICALLENGTH default value is wrong.

**Workaround**
Execute the following code after reset:

```c
*(volatile uint32_t *)0x4000053C = ((*(volatile uint32_t *)0x10000244) & 0x0000E000) >> 13;
```

This code is already present in the latest system_nrf52.c file.

3.5 [36] CLOCK: Some registers are not reset when expected

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
After watchdog timeout reset, CPU lockup reset, soft reset, or pin reset, the following CLOCK peripheral registers are not reset:
- CLOCK->EVENTS_DONE
- CLOCK->EVENTS_CTTO
- CLOCK->CTIV

**Conditions**
After watchdog timeout reset, CPU Lockup reset, soft reset, and pin reset.
New and inherited anomalies

**Consequences**
Register reset values might be incorrect. It may cause undesired interrupts in case of enabling interrupts without clearing the DONE or CTTO events.

**Workaround**
Clear affected registers after reset. This workaround has already been added into system_nrf52.c file. This workaround has already been added into system_nrf52840.c file present in MDK 8.11.0 or later.

3.6 [51] I2S: Aligned stereo slave mode does not work
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
Sample values for the left channel are transmitted twice (for both channels within a frame), sample values for the right channel are lost.

**Conditions**
CONFIG.MODE = SLAVE, CONFIG.CHANNELS = STEREO, CONFIG.FORMAT = ALIGNED.

**Consequences**
Aligned format cannot be used for stereo transmission in Slave mode.

**Workaround**
None.

3.7 [54] I2S: Wrong LRCK polarity in Aligned mode
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
In Aligned mode, left and right samples are swapped.

**Conditions**
CONFIG.FORMAT = ALIGNED

**Consequences**
Left and right audio channels are swapped.

**Workaround**
Swap left and right samples in memory.
3.8 [55] I2S: RXPTRUPD and TXPTRUPD events asserted after STOP

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
The RXPTRUPD event is generated when the STOP task is triggered, even though reception (RX) is disabled. Similarly, the TXPTRUPD event is generated when the STOP task is triggered, even though transmission (TX) is disabled.

**Conditions**
A previous transfer has been performed with RX/TX enabled, respectively.

**Consequences**
The indication that RXTXD.MAXCNT words were received/transmitted is false.

**Workaround**
Ignore the RXPTRUPD and TXPTRUPD events after triggering the STOP task. Clear these events before starting the next transfer.

3.9 [58] SPIM: An additional byte is clocked out when RXD.MAXCNT = 1

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
SPIM clocks out additional byte.

**Conditions**
RXD.MAXCNT = 1
TXD.MAXCNT <= 1

**Consequences**
Additional byte is redundant.
Workaround

Use the SPI module (deprecated but still available) or use the following workaround with SPIM:

```c
/**
 * @brief Work-around for transmitting 1 byte with SPIM.
 * @param spim: The SPIM instance that is in use.
 * @param ppi_channel: An unused PPI channel that will be used by the workaround.
 * @param gpiote_channel: An unused GPIOTE channel that will be used by the workaround.
 * @warning Must not be used when transmitting multiple bytes.
 * @warning After this workaround is used, the user must reset the PPI channel and the
 * GPIOTE channel before attempting to transmit multiple bytes.
 */
void setup_workaround_for_ftpan_58(NRF_SPIM_Type * spim, uint32_t ppi_channel, uint32_t gpiote_channel)
{
    // Create an event when SCK toggles.
    NRF_GPIOTE->CONFIG[gpiote_channel] = (GPIOTE_CONFIG_MODE_Event << GPIOTE_CONFIG_MODE_Pos |
                                         spim->PSEL.SCK << GPIOTE_CONFIG_PSEL_Pos |
                                         GPIOTE_CONFIG_POLARITY_Toggle << GPIOTE_CONFIG_POLARITY_Pos);

    // Stop the spim instance when SCK toggles.
    NRF_PPI->CH[ppi_channel].EEP = (uint32_t)&NRF_GPIOTE->EVENTS_IN[gpiote_channel];
    NRF_PPI->CH[ppi_channel].TEP = (uint32_t)&spim->TASKS_STOP;
    NRF_PPI->CHENSET = 1U << ppi_channel;

    // The spim instance cannot be stopped mid-byte, so it will finish
    // transmitting the first byte and then stop. Effectively ensuring
    // that only 1 byte is transmitted.
}
```

3.10 [64] NFCT: Only full bytes can be received or transmitted, but supports 4-bit frame transmit

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.

Symptoms

Data bits are not transmitted, or appear to not be received, if the Frame length is not a multiple of 8 bits (i.e. Frame includes data bits).
New and inherited anomalies

Conditions
Frame length is not a multiple of 8 bits (bytes only). Exception: 4-bit frame transmit supported.

Consequences
Partial bytes cannot be transferred:
- TXD.AMOUNT.TXDATABITS must be 0
- RXD.AMOUNT.RXDATABITS must be 0

Workaround
None

3.11 [66] TEMP: Linearity specification not met with default settings
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
TEMP module provides non-linear temperature readings over the specified temperature range.

Conditions
Always.

Consequences
TEMP module returns out of spec temperature readings.
Workaround

Execute the following code after reset:

```c
NRF_TEMP->A0 = NRF_FICR->TEMP.A0;
NRF_TEMP->A1 = NRF_FICR->TEMP.A1;
NRF_TEMP->A2 = NRF_FICR->TEMP.A2;
NRF_TEMP->A3 = NRF_FICR->TEMP.A3;
NRF_TEMP->A4 = NRF_FICR->TEMP.A4;
NRF_TEMP->A5 = NRF_FICR->TEMP.A5;
NRF_TEMP->B0 = NRF_FICR->TEMP.B0;
NRF_TEMP->B1 = NRF_FICR->TEMP.B1;
NRF_TEMP->B2 = NRF_FICR->TEMP.B2;
NRF_TEMP->B3 = NRF_FICR->TEMP.B3;
NRF_TEMP->B4 = NRF_FICR->TEMP.B4;
NRF_TEMP->B5 = NRF_FICR->TEMP.B5;
NRF_TEMP->T0 = NRF_FICR->TEMP.T0;
NRF_TEMP->T1 = NRF_FICR->TEMP.T1;
NRF_TEMP->T2 = NRF_FICR->TEMP.T2;
NRF_TEMP->T3 = NRF_FICR->TEMP.T3;
NRF_TEMP->T4 = NRF_FICR->TEMP.T4;
```

This code is already present in the latest system_nrf52.c file and in the system_nrf52840.c file released in MDK 8.12.0.

3.12 [67] NFCT, PPI: Some events cannot be used with the PPI

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.

Symptoms

The following NFCT events do not trigger tasks when used with the PPI:

- EVENTS_AUTOCOLRESSTARTED
- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

Conditions

PPI is used to trigger peripheral tasks using the NFCT events.

Consequences

The PPI cannot be used to trigger tasks using the following NFCT events:

- EVENTS_AUTOCOLRESSTARTED
- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED
**Workaround**

The EVENTS_AUTOCOLRESSTARTED cannot be used with the PPI.

Subtract an offset of 0x04 while configuring the PPI event end points for the following NFCT events:

- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

Examples:

```
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_COLLISION) - 0x04;
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_SELECTED) - 0x04;
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_STARTED) - 0x04;
```

---

**3.13 [68] CLOCK: EVENTS_HFCLKSTARTED can be generated before HFCLK is stable**

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.

**Symptoms**

EVENTS_HFCLKSTARTED may come before HFXO is started.

**Conditions**

When using a 32 MHz crystal with start-up longer than 400 µs.

**Consequences**

Performance of radio and peripheral requiring HFXO will be degraded until the crystal is stable.

**Workaround**

32 MHz crystal oscillator startup time must be verified by the user. If the worst-case startup time is shorter than 400 µs, no workaround is required. If the startup time can be longer than 400 µs, the software must ensure, using a timer, that the crystal has had enough time to start up before using peripherals that require the HFXO. The Radio requires the HFXO to be stable before use. The ADC, TIMERS, and TEMP sensor for example can use the HFXO as a reference for improved accuracy.

---

**3.14 [72] NFCT, PPI: TASKS_ACTIVATE cannot be used with the PPI**

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.
New and inherited anomalies

**Symptoms**
The NFCT peripheral does not get activated when the PPI is configured to trigger TASKS_ACTIVATE on any event.

**Conditions**
Always

**Consequences**
The TASKS_ACTIVATE cannot be used with the PPI.

**Workaround**
None

3.15 [74] SAADC: Started events fires prematurely
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
False EVENTS_STARTED

**Conditions**
TACQ <= 5 µs

**Consequences**
The EVENTS_STARTED can come when not expected

**Workaround**
The module must be fully configured before it is enabled, and the TACQ configuration must be the last configuration set before ENABLE.

3.16 [75] MWU: Increased current consumption
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
Increased current consumption in System ON IDLE.

**Conditions**
When MWU is enabled.
Consequences
Increased current consumption in System ON IDLE.

Workaround
Do not use MWU or disable MWU before WFE/WFI, enable it on IRQ.

3.17 [76] LPCOMP: READY event is set sooner than it should
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
May receive unexpected events and wakeups from LPCOMP.

Conditions
LPCOMP is configured to send an event or to wake up the chip. LPCOMPTASKS_START task is set and LPCOMP.EVENTS_READY event has been received.

Consequences
Unpredictable system behavior caused by falsely triggered events and wakeups.

Workaround
Use the following configuration sequence.
1. Configure the LPCOMP to send an event or wake up the chip, but do not enable any PPI channels or IRQ to be triggered from the LPCOMP events.
2. Trigger the LPCOMPTASKS_START task and wait for the LPCOMP.EVENTS_READY event.
3. After receiving the LPCOMP.EVENTS_READY event wait for 115 µs.
4. After 115 µs, clear the LPCOMP.EVENTS_DOWN, LPCOMP.EVENTS_UP, and LPCOMP.EVENTS_CROSS events. LPCOMP is now ready to be used.

3.18 [77] CLOCK: RC oscillator is not calibrated when first started
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
The LFCLK RC oscillator frequency can have a frequency error of up to -25 to +40% after reset. A +/- 2% error is stated in the Product Specification.
**Conditions**
Always.

**Consequences**
The LFCLK RC oscillator frequency is inaccurate.

**Workaround**
Calibrate the LFCLK RC oscillator before its first use after a reset.

### 3.19 [78] TIMER: High current consumption when using timer STOP task only

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
Increased current consumption when the timer has been running and the STOP task is used to stop it.

**Conditions**
The timer has been running (after triggering a START task) and then it is stopped using a STOP task only.

**Consequences**
Increased current consumption.

**Workaround**
Use the SHUTDOWN task after the STOP task or instead of the STOP task.

### 3.20 [79] NFCT: A false EVENTS_FIELDDETECTED event occurs after the field is lost

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
A false EVENTS_FIELDDETECTED event occurs.

**Conditions**
The task TASK_SENSE is triggered within 270 µs of the event EVENTS_FIELDLOST.
New and inherited anomalies

Consequences
EVENTS_FIELDDETECTED will occur after a field is lost. (SHORT between eventfieldlost and taskSense should not be used since a false fieldDetected event will occur from using the task.)

Workaround
- Wait 170 µs after an EVENTS_FIELDLOST event before triggering TASK_SENSE for temperatures ≥ 0°C.
- Wait 270 µs after an EVENTS_FIELDLOST event before triggering TASK_SENSE for temperatures < 0°C.

Important: This anomaly was changed compared to the original publication.

3.21 [81] GPIO: PIN_CNF is not retained when in debug interface mode

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.

Symptoms
GPIO pin configuration is reset on wakeup from System OFF.

Conditions
The system is in debug interface mode.

Consequences
GPIO state unreliable until PIN_CNF is reconfigured.

3.22 [83] TWIS: STOPPED event occurs twice if the STOP task is triggered during a transaction

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.

Symptoms
STOPPED event is set after clearing it.

Conditions
The STOP task is triggered during a transaction.

Consequences
STOPPED event occurs twice: When the STOP task is fired and when the master issues a stop condition on the bus. This could provoke an extra interrupt or a failure in the TWIS driver.
Workaround
The last STOPPED event must be accounted for in software.

3.23 [84] COMP: ISOURCE not functional
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
The programmable current source (ISOURCE) has too high variation. Variance over temp is >20 times specified nominal value

Conditions
Always.

Consequences
Inaccurate current source.

Workaround
None.

3.24 [86] SAADC: Triggering START task after offset calibration may write a sample to RAM
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
The first sample in the result buffer is incorrect, and will be present although the SAMPLE task has never been issued.

Conditions
The START task is triggered after performing calibration (through the CALIBRATEOFFSET task).

Consequences
Incorrect sample data in the result buffer.

Workaround
Calibration should follow the pattern STOP -> STOPPED -> CALIBRATEOFFSET -> CALIBRATEDONE -> STOP -> STOPPED -> START.
3.25 [87] CPU: Unexpected wake from System ON Idle when using FPU

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
The CPU is unexpectedly awoken from System ON Idle.

**Conditions**
The FPU has been used.

**Consequences**
The CPU is awoken from System ON Idle.

**Workaround**
The FPU can generate pending interrupts just like other peripherals, but unlike other peripherals there are no INTENSET, INTENCLR registers for enabling or disabling interrupts at the peripheral level. In order to prevent unexpected wake-up from System ON Idle, add this code before entering sleep:

```c
#if (__FPU_USED == 1)
    __set_FPSCR(__get_FPSCR() & ~(0x0000009F));
    (void) __get_FPSCR();
    NVIC_ClearPendingIRQ(FPU_IRQn);
#endif
__WFE();
```

3.26 [88] WDT: Increased current consumption when configured to pause in System ON idle

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
Using the mode where watchdog is paused in CPU Idle, the current consumption jumps from 3 µA to 400 µA.

**Conditions**
When we enable WDT with the CONFIG option to pause when CPU sleeps:

```c
NRF_WDT->CONFIG = (WDT_CONFIG_SLEEP_Pause<<WDT_CONFIG_SLEEP_Pos);
```
**Consequences**
Reduced battery life.

**Workaround**
Do not enter System ON IDLE within 125 µs after reloading the watchdog.

**3.27 [89] GPIOTE: Static 400 µA current while using GPIOTE**
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
Static current consumption between 400 µA and 450 µA when using SPIM or TWIM in combination with GPIOTE.

**Conditions**
- GPIOTE is configured in event mode
- TWIM/SPIM utilizes EasyDMA

**Consequences**
Current consumption higher than specified.

**Workaround**
Turn the TWIM/SPIM off and back on after it has been disabled. To do so, write 0 followed by 1 to the POWER register (address 0xFFC) of the TWIM/SPIM that must be disabled:

- If TWIM0 or SPIM0 is used:
  ```c
  *(volatile uint32_t *)0x40003FFC = 0;
  *(volatile uint32_t *)0x40003FFC;
  *(volatile uint32_t *)0x40003FFC = 1;
  ```

- If TWIM1 or SPIM1 is used:
  ```c
  *(volatile uint32_t *)0x40004FFC = 0;
  *(volatile uint32_t *)0x40004FFC;
  *(volatile uint32_t *)0x40004FFC = 1;
  ```

- If SPIM2 is used:
  ```c
  *(volatile uint32_t *)0x40023FFC = 0;
  *(volatile uint32_t *)0x40023FFC;
  *(volatile uint32_t *)0x40023FFC = 1;
  ```

Reconfiguration of TWIM/SPIM is required before next usage.
3.28 [91] RADIO: Radio performance using CSP package version

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
WLCSP package has reduced receiver sensitivity compared to QFN packages in LDO and DCDC regulator modes.

Conditions
- Average Sensitivity over all channels degraded in LDO mode by 2 dB.
- Average Sensitivity over all channels degraded in DCDC mode by 4 dB.

Consequences
Reduced receiver sensitivity.

Workaround
None.

3.29 [97] GPIOTE: High current consumption in System ON Idle mode

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
High current consumption (<20 µA) in System ON Idle mode.

Conditions
GPIOTE used with one or more channels in input mode.

Consequences
Higher current consumption.

Workaround
Use Port event to detect transitions on inputs instead of GPIOTE input mode.
3.30 [101] CLOCK: Sleep current increases after soft reset

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
Sleep current with LFXO active is 0.5 µA higher than expected.

**Conditions**
Low frequency crystal oscillator is active, due to use of RTC or WDT, and a soft-reset is issued or a CPU lock-up reset occurs.

**Consequences**
Increased sleep current.

**Workaround**
None.

3.31 [108] RAM: RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
RAM not correctly retained.

**Conditions**
System ON Idle mode or System OFF is used with parts or all RAM retained.

**Consequences**
RAM not correctly retained.

**Workaround**
Apply the following code after any reset:

```c
*(volatile uint32_t *)0x40000EE4 = (*(volatile uint32_t *)0x10000258 & 0x0000004F);
```

This workaround is implemented in MDK version 8.9.0 and newer version. This workaround increases the I_RAM current per 4 KB section from 20nA to 30nA.
3.32 [109] DMA: DMA access transfers might be corrupted

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.

**Symptoms**
The first byte sent out by the peripheral is sometimes wrong.

**Conditions**
System enters IDLE and stops the 64 MHz clock at the same time as the peripheral that is using DMA is started. This problem affects the peripherals PWM, SPI, SPI, TWI, UART, and TWI.

**Consequences**
Wrong data sent to external device.

**Workaround**
Workarounds will be incorporated into SDK v13.0.0. See the following document for a description of the workarounds:

nRF52832 Errata Attachment Anomaly 109 Addendum

3.33 [113] COMP: Single-ended mode with external reference is not functional

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.

**Symptoms**
COMP output is not correct.

**Conditions**
COMP is used in single-ended mode with external reference.

**Consequences**
COMP cannot be used in this mode.

**Workaround**
None.
3.34 [132] CLOCK: The LFRC oscillator might not start
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
The LFRC oscillator does not start and the LFCLKSTARTED event is not triggered.

Conditions
The LFRC oscillator is started in the window [66 µs, 138 µs] after the LFRC oscillator has stopped.

Consequences
The LFRC oscillator might become non-functional until it is reset.

Workaround
Delay starting the LFRC oscillator if it was last stopped [66 µs, 138 µs] ago.

3.35 [136] System: Bits in RESETREAS are set when they should not be
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
After pin reset, RESETREAS bits other than RESETPIN might also be set.

Conditions
A pin reset has triggered.

Consequences
If the firmware evaluates RESETREAS, it might take the wrong action.

Workaround
When RESETREAS shows a pin reset (RESETPIN), ignore other reset reason bits.

Important: RESETREAS bits must be cleared between resets.

Apply the following code after any reset:

```c
if (NRF_POWER->RESETREAS & POWER_RESETREAS_RESETPIN_Msk)
    NRF_POWER->RESETREAS = ~POWER_RESETREAS_RESETPIN_Msk;
```
New and inherited anomalies

This workaround is implemented in MDK version 8.13.0 and later.

3.36 [138] RADIO: Spurious emission on GPIO exceeds limits in radiated tests
This anomaly applies to IC Rev. Revision 2, build codes QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
Spurious emission in RX mode can exceed ETSI limits.

Conditions
Using the Nordic Development Kit or a product built from reference schematic using GPIO P0.25 and P0.26.

Consequences
Product does not conform to ETSI requirements.

Workaround
Use the updated reference schematics and reference layout, version 1.1 or later, available from Reference layout nRF52832.

3.37 [141] NFCT: HFCLK not stopped when entering SENSE mode
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
Higher current consumption than specified in SENSE mode.

Conditions
Going from active mode to SENSE mode.

Consequences
Higher current consumption in SENSE mode than specified.

Workaround
Power cycle the NFCT executing the following code:

```c
*(volatile uint32_t *)0x40005FFC = 0;
*(volatile uint32_t *)0x40005FFC = 1;
```
Then issue the SENSE task to enter SENSE mode.

### 3.38 [143] RADIO: False CRC failures on specific addresses

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0. It was inherited from the previous IC revision Revision 1.

#### Symptoms

100% CRC failure rate even if the payload is received correctly.

#### Conditions

1 Mbit/s and 2 Mbit/s Nordic proprietary radio mode and Bluetooth Low Energy. CRCCNF.SKIPADDR = 0. CRC calculation includes the address field.

Logical address 0 and logical address 1 to 7 have the same BASE address MSBs configured.

| ADDRLEN=5  |
| BASE0 = 0xAAAAAXXX |
| BASE1 = 0xAAAAAXXX |

ADDRLENLEN=4

| BASE0 = 0xAAXXXXXX |
| BASE1 = 0xAAXXXXXX |

AND logical address 0 and one of the logical addresses 1 to 7 have the same PREFIX value configured.

The issue is present regardless of which logical address is enabled in RXADDRESSES.

#### Consequences

If receiving on logical address 0, the address is reconstructed incorrectly for CRC calculation, resulting in CRCSTATUS.CRCError being returned. However, the received payload bytes are correct. Packet error rate 100 percent. RXMATCH shows the wrong logical address.

#### Workaround

Use one of the following workarounds:

- Use the ESB and Gazell libraries of SDK v14.0.0 or later.
  
  This implementation applies the following workaround.

- Set bit 16 in RXADDRESSES to 1.

- Apply the following code before triggering the RXEN task:

  ```c
  *(volatile uint32_t *) 0x40001774 = (*((volatile uint32_t *) 0x40001774) & 0xffffffff) | 0x01000000;
  ```

  This code will reduce sensitivity with 3 dB.
3.39 [146] CLOCK: LFRC frequency deviation
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
The frequency tolerance (fTOL_CAL_LFRC) of the LFRC oscillator is exceeding 250 ppm.

Conditions
Always.

Consequences
Timers using LFRC are not as precise as described in the specification.

Workaround
Account for a frequency tolerance of 500 ppm when using the LFRC oscillator.

3.40 [149] TWIM: First clock pulse after clock stretching may be too long or too short
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
When the TWI slave exits a clock stretching state, the first clock pulse from the master is too long or too short.

The following deviations from the normal clock pulse length can occur:

400 kHz
- Minimum: 0.7 µs
- Maximum: 3.0 µs

100 kHz
- Minimum: 0.7 µs
- Maximum: 11.0 µs

Conditions
TWI slave uses clock stretching.

Consequences
The slave may give an error condition due to a too long or too short clock pulse or the pulse may be lost. This depends on the slave clock stretching behavior.
3.41 [150] SAADC: EVENT_STARTED does not fire

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
EVENT_STARTED does not fire.

**Conditions**
ADC started (TASKS_START) with PPI task. Any channel configured to TACQ <= 5 µs.

**Consequences**
ADC cannot be started (TASKS_START) with PPI if TACQ <= 5 µs.

**Workaround**
Use TAQC > 5 µs when starting ADC from PPI.

3.42 [155] GPIOTE: IN event may occur more than once on input edge

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

**Symptoms**
IN event occurs more than once on an input edge.

**Conditions**
Input signal edges are closer together than 1.3 µs or >= 750 kHz for a periodic signal.

**Consequences**
Tasks connected through PPI or SHORTS to this event might be triggered twice.

**Workaround**
Apply the following code when any GPIOTE channel is configured to generate an IN event on edges that can occur within 1.3 µs of each other:

```
*(volatile uint32_t *) (NRF_GPIOTE_BASE + 0x600 + (4 * GPIOTE_CH_USED)) = 1;
```
**Important:** A clock is kept on by the workaround and must be reverted to avoid higher current consumption when GPIOTE is not in use, using the following code:

```c
*(volatile uint32_t *)(NRF_GPIOTE_BASE + 0x600 + (4 * GPIOTE_CH_USED)) = 0;
```

### 3.43 [156] GPIOTE: Some CLR tasks give unintentional behavior

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.

**Symptoms**

One of the following symptoms may occur:

- Current consumption is high when entering IDLE.
- Latency for detection changes on inputs connected to GPIOTE channels is becoming longer than expected.

**Conditions**

The following tasks are in use:

<table>
<thead>
<tr>
<th>Address</th>
<th>GPIOTE task</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x060</td>
<td>TASKSCLR[0]</td>
</tr>
<tr>
<td>0x068</td>
<td>TASKSCLR[2]</td>
</tr>
<tr>
<td>0x070</td>
<td>TASKSCLR[4]</td>
</tr>
<tr>
<td>0x078</td>
<td>TASKSCLR[6]</td>
</tr>
</tbody>
</table>

**Consequences**

Experiencing high current consumption during System ON Idle, or too long time from external event to internal triggering of PPI event and/or IRQ from GPIOTE.

**Workaround**

Instead of using TASKSCLR[n], set CONFIG[n].POLARITY to HiToLo and trigger TASKSOUT[n], with n = 0, 2, 4, 6.

### 3.44 [173] GPIO: Writes to LATCH register take several CPU cycles to take effect

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.
New and inherited anomalies

Symptoms
A bit in the LATCH register reads '1' even after clearing it by writing '1'.

Conditions
Reading the LATCH register right after writing to it.

Consequences
Old value of the LATCH register is read.

Workaround
Have at least 3 CPU cycles of delay between the write and the subsequent read to the LATCH register. This can be achieved by having 3 dummy reads to the LATCH register.

3.45 [176] System: Flash erase through CTRL-AP fails due to watchdog time-out
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
Full flash erase through CTRL-AP is not successful.

Conditions
WDT is enabled.

Consequences
Flash is not erased. If the device has a WDT time-out less than 1 ms and is readback-protected through UICR.APPROTECT, there is a risk of permanently preventing the erasing of the flash.

Workaround
Try again.

3.46 [178] SAADC: END event firing too early
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
False END events.

Conditions
Offset calibration is run with TACQ < 10 µs before sampling is started.
Consequences
The END event can occur earlier than expected. Data is not ready.

Workaround
Apply one of the following workarounds:
• Run offset calibration with TACQ >=10 µs.
• Apply STOP task after calibration, before sampling. CALIBRATEOFFSET -> CALIBRATEDONE -> STOP -> STOPPED -> START.

3.47 [179] RTC: COMPARE event is generated twice from a single RTC compare match
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
Tasks connected to RTC COMPARE event through PPI are triggered twice per compare match.

Conditions
RTC registers are being accessed by CPU while RTC is running.

Consequences
Tasks connected to RTC COMPARE event through PPI are triggered more often than expected.

Workaround
Do not access the RTC registers, including the COMPARE event register, from CPU while waiting for the RTC COMPARE event. Note that CPU interrupt from this event can still be enabled.

3.48 [182] RADIO: Fixes for anomalies #102, #106, and #107 do not take effect
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

Symptoms
Symptoms as described in anomalies #102, #106, and #107 for nRF52832 Rev. 1 are still visible, even though these anomalies are fixed.

Conditions
You want the fix for anomalies #102, #106, and #107 to take effect.

Consequences
Improvements as described in Informational Notice #105.
### Workaround

After powering the radio, i.e. after every operation that sets register (0xFFC) POWER=enable, set bit 10 of the RADIO register 0x73C to enable the fix.

```c
*(volatile uint32_t *) 0x4000173C |= (1 << 10)
```

### 3.49 [183] PWM: False SEQEND[0] and SEQEND[1] events

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0. It was inherited from the previous IC revision Revision 1.

**Symptoms**

False SEQEND[0] and SEQEND[1] events are being generated.

**Conditions**

Any of the LOOPDONE_SEQSTARTn shortcuts are enabled. LOOP register is non-zero and sequence 1 is one value long.

**Consequences**

SEQEND[0] and SEQEND[1] events might falsely trigger other tasks if these are routed through the PPI.

**Workaround**

Avoid using the LOOPDONE_SEQSTARTn shortcuts, when LOOP register is non-zero and sequence 1 is one value long.

### 3.50 [192] CLOCK: LFRC frequency offset after calibration

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0. It was inherited from the previous IC revision Revision 1.

**Symptoms**

LFRC oscillator frequency is wrong after calibration, exceeding 500 ppm.

**Conditions**

On some devices, when entering System ON Idle while calibration is ongoing.

**Consequences**

After calibration, LFRC has a frequency offset that is outside specification.
3.51 [194] I2S: STOP task does not switch off all resources

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.

**Symptoms**
Current consumption too high (~900 µA) after using the STOP task.

**Conditions**
I2S was running and was stopped by triggering the STOP task.

**Consequences**
Current consumption higher than specified.

**Workaround**

Apply the following code after the STOP task:

\[
* (volatile uint32_t *)0x40025038 = 1;
* (volatile uint32_t *)0x4002503C = 1;
\]

3.52 [196] I2S: PSEL acquires GPIOs regardless of ENABLE

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0.

It was inherited from the previous IC revision Revision 1.

**Symptoms**
I2S controls GPIO even when I2S is not enabled.
### Conditions
When using I2S->PSEL to configure GPIO.

### Consequences
GPIO selected for I2S cannot be used for any other peripheral and will be configured as input.

### Workaround
Do not rely on the pins selected in I2S->PSEL registers being free when I2S->ENABLE is set to DISABLE. Only set the CONNECT bit in the I2S->PSEL registers to CONNECTED immediately before enabling I2S. When disabling I2S, set the CONNECT bit in the I2S->PSEL registers to DISCONNECTED.

### 3.53 [201] CLOCK: EVENTS_HFCLKSTARTED might be generated twice
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0. It was inherited from the previous IC revision Revision 1.

#### Symptoms
EVENTS_HFCLKSTARTED might occur twice, and HFCLKSTAT might be wrong.

#### Conditions
When running HFCLK with crystal.

#### Consequences
HFCLKSTAT might be wrong when reading it after HFCLK is started.

#### Workaround
Disregard HFCLKSTAT and EVENT_HFCLKSTARTED after first EVENT_HFCLKSTARTED. This workaround is included in nRF5 SDK v15.0.0 and SoftDevices S140, S132, and S112 v6.0.0.

### 3.54 [204] RADIO: Switching between TX and RX causes unwanted emissions
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0. It was inherited from the previous IC revision Revision 1.

#### Symptoms
Unwanted emissions are experienced when switching from TX to RX.

#### Conditions
Switching from TX to RX without using DISABLE.
Consequences
Unwanted emissions occur on the channel used for RX.

Workaround
Always use DISABLE when switching from TX to RX.

3.55 [210] GPIO: Bits in GPIO LATCH register are incorrectly set to 1
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
The GPIO.LATCH[n] register is unexpectedly set to 1 (Latched).

Conditions
Set GPIO.PIN_CNF[n].SENSE at low level (3) at the same time as PIN_CNF[n].INPUT is set to Connect (0).

Consequences
The GPIO.LATCH[n] register is set to 1 (Latched). This could have side effects, depending on how the chip is configured to use this LATCH register.

Workaround
Always configure PIN_CNF[n].INPUT before PIN_CNF[n].SENSE.

3.56 [212] SAADC: Events are not generated when switching from scan mode to no-scan mode with burst enabled
This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
SAADC stops working.

Conditions
Any of the following:
• Switching from multiple channels to single channel when BURST is disabled and acquisition time < 10 μs.
• Switching from multiple channels to single channel when BURST is enabled.
New and inherited anomalies

Consequences

SAADC does not generate the expected events.

Workaround

Execute the following code before changing the channel configuration:

```c
volatile uint32_t temp1;
volatile uint32_t temp2;
volatile uint32_t temp3;

temp1 = *(volatile uint32_t *)0x40007640ul;
temp2 = *(volatile uint32_t *)0x40007644ul;
temp3 = *(volatile uint32_t *)0x40007648ul;

*(volatile uint32_t *)0x40007FFCul = 0ul;
*(volatile uint32_t *)0x40007FFCul = 1ul;

*(volatile uint32_t *)0x40007640ul = temp1;
*(volatile uint32_t *)0x40007644ul = temp2;
*(volatile uint32_t *)0x40007648ul = temp3;
```

After the workaround is executed, the SAADC configuration is reset. Before use all registers must be configured again.

3.57 [213] WDT: WDT configuration is cleared when entering system OFF

This anomaly applies to IC Rev. Revision 2, build codes CIAA-EA0, CIAA-Ex0, QFAA-EA0, QFAA-Ex0.

It was inherited from the previous IC revision Revision 1.

Symptoms

WDT configuration has been cleared when device wakes from System OFF.

Conditions

Always.

Consequences

WDT does not resume function as expected.

Workaround

Reconfigure WDT after wake-up from System OFF.
3.58 [218] NFCT: Frame delay timing is too short after SLP_REQ

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.

**Symptoms**
Reader may not accept the response from the tag.

**Conditions**
The time between SLP_REQ and ALL_REQ sent by the Reader is shorter than the time configured in FRAMEDELAYMAX.

**Consequences**
The protocol timing is violated and a Reader may not accept the response from the tag.

**Workaround**
Ensure that FRAMEDELAYMAX is set to the default value when the NFCT is in states IDLE or SLEEP_A. The workaround is included in nRF5 SDK v16.0

3.59 [219] TWIM: I2C timing spec is violated at 400 kHz

This anomaly applies to IC Rev. Revision 2, build codes CIAA-Ex0, QFAA-Ex0, QFAB-Ex0.

It was inherited from the previous IC revision Revision 1.

**Symptoms**
The low period of the SCL clock is too short to meet the I2C specification at 400 kHz. The actual low period of the SCL clock is 1.25 µs while the I2C specification requires the SCL clock to have a minimum low period of 1.3 µs.

**Conditions**
Using TWIM at 400 kHz.

**Consequences**
TWI communication might not work at 400 kHz with I2C compatible devices.

**Workaround**
If communication does not work at 400 kHz with an I2C compatible device that requires the SCL clock to have a minimum low period of 1.3 µs, use 390 kHz instead of 400kHz by writing 0x06200000 to the FREQUENCY register. With this setting, the SCL low period is greater than 1.3 µs.
3.60 [220] CPU: RAM is not ready when written

This anomaly applies to IC Rev. Revision 2, build codes CIAA-EA0, CIAA-Ex0, QFAA-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
Memory is not written in the first cycle after wake-up.

Conditions
The following consecutive events occur:
1. Either 1 MHz or 32 MHz peripheral clock state changes.
2. After one to four 16 MHz cycles the DMA channel stops while the CPU is in sleep.
3. An event or interrupt comes three 64 MHz cycles after the DMA channel stops.

Consequences
The address of the next instruction is not written to the stack. In stack frame, the link register is corrupted.

Workaround
Disable IRQ while using WFE by inserting the following code:

```c
SCB->SCR |= SCB_SCR_SEVONPEND_Msk;
__disable_irq();
__WFE();
__nop();__nop();__nop();__nop();
__enable_irq();
```

This workaround is included in SoftDevice 1xx version 8.0 and later. SoftDevice v7.0.1 includes an alternative workaround which does not support FPU being enabled.

3.61 [245] RADIO: CRC is wrong when data whitening is enabled and address field is included in CRC calculation

This anomaly applies to IC Rev. Revision 2, build codes CIAA-EA0, CIAA-Ex0, QFAA-EA0, QFAA-Ex0, QFAB-Ex0.
It was inherited from the previous IC revision Revision 1.

Symptoms
CRC failures are reported.

Conditions
In RX, if data whitening is enabled and the CRC checker is configured to take the address field into CRC calculations.
Consequences

CRC failures are reported though received packet contents are good.
Fixed anomalies

The anomalies listed in this table are no longer present in the current chip version.

For a detailed description of the fixed anomalies, see the **Errata for revision Revision 1**.

<table>
<thead>
<tr>
<th>ID</th>
<th>Module</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>102</td>
<td>RADIO</td>
<td>PAYLOAD/END events delayed or not triggered after ADDRESS</td>
</tr>
<tr>
<td>106</td>
<td>RADIO</td>
<td>Higher CRC error rates for some access addresses</td>
</tr>
<tr>
<td>107</td>
<td>RADIO</td>
<td>Immediate address match for access addresses containing MSBs 0x00</td>
</tr>
<tr>
<td>163</td>
<td>FICR</td>
<td>Code and RAM size fields do not match chip specification</td>
</tr>
<tr>
<td>181</td>
<td>NFCT</td>
<td>Invalid value in FICR for double-size NFCID1</td>
</tr>
</tbody>
</table>

*Table 2: Fixed anomalies*