

nRF52832 Product Specification v1.3

Key features

- 2.4 GHz transceiver
 - -96 dBm sensitivity in *Bluetooth*® low energy mode
 - 2 Mbps Bluetooth® low energy mode
 - 1 Mbps, 2 Mbps supported data rates
 - TX power -20 to +4 dBm in 4 dB steps
 - Single-pin antenna interface
 - 5.3 mA peak current in TX (0 dBm)
 - 5.4 mA peak current in RX
 - RSSI (1 dB resolution)
- ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz
 - 215 EEMBC CoreMark® score running from flash memory
 - 58 μA/MHz running from flash memory
 - 51.6 μA/MHz running from RAM
 - Data watchpoint and trace (DWT), embedded trace macrocell (ETM), and instrumentation trace macrocell (ITM)
 - Serial wire debug (SWD)
 - Trace port
- Flexible power management
 - Supply voltage range 1.7 V-3.6 V
 - Fully automatic LDO and DC/DC regulator system
 - Fast wake-up using 64 MHz internal oscillator
 - 0.3 µA at 3 V in OFF mode
 - 0.7 μA at 3 V in OFF mode with full 64 kB RAM retention
 - 1.9 μ A at 3 V in ON mode, no RAM retention, wake on RTC
- Memory
 - 512 kB flash/64 kB RAM
 - 256 kB flash/32 kB RAM
- Nordic SoftDevice ready
- Support for concurrent multi-protocol
- Type 2 near field communication (NFC-A) tag with wakeup-on-field and touchto-pair capabilities
- 12-bit, 200 ksps ADC 8 configurable channels with programmable gain
- 64 level comparator
- 15 level low power comparator with wakeup from System OFF mode
- Temperature sensor
- 32 general purpose I/O pins
- 3x 4-channel pulse width modulator (PWM) units with EasyDMA
- Digital microphone interface (PDM)
- 5x 32-bit timers with counter mode
- Up to 3x SPI master/slave with EasyDMA
- Up to 2x I2C compatible 2-Wire master/slave
- I2S with EasyDMA
- UART (CTS/RTS) with EasyDMA
- Programmable peripheral interconnect (PPI)
- Quadrature decoder (QDEC)
- AES HW encryption with EasyDMA
- Autonomous peripheral operation without CPU intervention using PPI and EasyDMA
- 3x real-time counter (RTC)
- External system
 - Single crystal operation
 - On-chip balun (single-ended RF)
 - Few external components
- Package variants
 - QFN48 package, 6 × 6 mm
 - WLCSP package, 3.0 × 3.2 mm

Applications

- Internet of Things (IoT)
 - Home automation
 - Sensor networks
 - Building automation
 - Industria
 - Retai

Personal area networks

- Health/fitness sensor and monitor devices
 - Medical devices
 - Key fobs and wrist watches

Interactive entertainment devices

- Remote controls
 - Gaming controllers

Roacons

- A4WP wireless chargers and devices
- Remote control toys
- Computer peripherals and I/O devices
- • Mouse
 - Keyboard
 - Multi-touch trackpad
 - Gaming

All rights reserved.



Contents

1 Revision history	9
2 About this document	10
2.1 Peripheral naming and abbreviations	
2.2 Register tables	
2.3 Registers	
3 Block diagram	
4 Pin assignments	
4.1 QFN48 pin assignments	
4.2 WLCSP ball assignments	
4.3 GPIO usage restrictions.	
5 Absolute maximum ratings	
6 Recommended operating conditions	
·	
7 CPU	
7.1 Floating point interrupt	
7.2 Electrical specification	
7.3 CPU and support module configuration	
8 Memory	
8.1 RAM - Random access memory	
8.2 Flash - Non-volatile memory	
8.3 Memory map	
8.4 Instantiation	
9 AHB multilayer	26
9.1 AHB multilayer priorities	
10 EasyDMA	
10.1 EasyDMA array list	
11 NVMC — Non-volatile memory controller	
11.1 Writing to Flash	
11.2 Erasing a page in Flash	
11.3 Writing to user information configuration registers (UICR)	
11.4 Erasing user information configuration registers (UICR)	
11.5 Erase all	
11.6 Cache	
11.7 Registers	
11.8 Electrical specification	
12 BPROT — Block protection	
12.1 Registers	
13 FICR — Factory information configuration registers	
13.1 Registers	
14 UICR — User information configuration registers	54
14.1 Registers	54
15 Peripheral interface	68
15.1 Peripheral ID	68
15.2 Peripherals with shared ID	68
15.3 Peripheral registers	
15.4 Bit set and clear	
15.5 Tasks	
15.6 Events	
15.7 Shortcuts	
15.8 Interrupts	70



16	Debug and trace	72
	16.1 DAP - Debug Access Port	
	16.2 CTRL-AP - Control Access Port	73
	16.3 Debug interface mode	74
	16.4 Real-time debug	74
	16.5 Trace	
17	Power and clock management	76
	17.1 Current consumption scenarios	
18	POWER — Power supply	
. •	18.1 Regulators	
	18.2 System OFF mode	
	18.3 System ON mode	
	18.4 Power supply supervisor	
	18.5 RAM sections	
	18.6 Reset	
	18.7 Retained registers	83
	18.8 Reset behavior	83
	18.9 Registers	83
	18.10 Electrical specification	99
19	CLOCK — Clock control	101
	19.1 HFCLK clock controller	101
	19.2 LFCLK clock controller	103
	19.3 Registers	
	19.4 Electrical specification	
20	GPIO — General purpose input/output	111
	20.1 Pin configuration	
	20.2 GPIO located near the RADIO	
	20.3 Registers	113
	20.4 Electrical specification	154
21	GPIOTE — GPIO tasks and events	157
	21.1 Pin events and tasks	157
	21.2 Port event	
	21.3 Tasks and events pin configuration	158
	21.4 Registers	
	21.5 Electrical specification	
22	PPI — Programmable peripheral interconnect	168
	22.1 Pre-programmed channels	
	22.2 Registers	
23	RADIO — 2.4 GHz Radio	
_	23.1 EasyDMA	
	23.2 Packet configuration	
	23.3 Maximum packet length	
	23.4 Address configuration	
	23.5 Data whitening	
	20.0 Data willering	207
	23.6 CRC	
	· · · · · · · · · · · · · · · · · · ·	208
	23.6 CRC	208 209
	23.6 CRC23.7 Radio states	208 209 209
	23.6 CRC	208 209 211 212
	23.6 CRC	208 209 211 212
	23.6 CRC	208 209 211 212
	23.6 CRC	208 209 211 212 213
	23.6 CRC	208 209 211 212 213 213
	23.6 CRC	208 209 211 212 213 213 214
24	23.6 CRC	208209211212213214230
24	23.6 CRC	208209211212213214230234



	24.3 Task delays	
	24.4 Task priority	235
	24.5 Registers	235
	24.6 Electrical specification	241
25	RTC — Real-time counter	242
	25.1 Clock source	
	25.2 Resolution versus overflow and the PRESCALER	
	25.3 COUNTER register	
	25.4 Overflow features	
	25.5 TICK event	
	25.6 Event control feature	
	25.7 Compare feature	
	25.8 TASK and EVENT jitter/delay	
	25.9 Reading the COUNTER register	
	25.10 Registers	
	25.11 Electrical specification	
26	·	
20	RNG — Random number generator	
	26.1 Bias correction	
	26.2 Speed	
	26.3 Registers	
	26.4 Electrical specification	
27	TEMP — Temperature sensor	
	27.1 Registers	
	27.2 Electrical specification	
28	ECB — AES electronic codebook mode encryption	264
	28.1 Shared resources	
	28.2 EasyDMA	
	28.3 ECB data structure	
	28.4 Registers	
	28.5 Electrical specification	
29	CCM — AES CCM mode encryption	
	29.1 Shared resources	
	29.2 Encryption	
	29.3 Decryption	
	29.4 AES CCM and RADIO concurrent operation	
	29.5 Encrypting packets on-the-fly in radio transmit mode	
	29.6 Decrypting packets on-the-fly in radio receive mode	
	29.7 CCM data structure	
	29.8 EasyDMA and ERROR event	
~~	29.9 Registers	
30	AAR — Accelerated address resolver	
	30.1 Shared resources	
	30.2 EasyDMA	
	30.3 Resolving a resolvable address	
	30.4 Use case example for chaining RADIO packet reception with address resolution usin	g
	AAR	
	30.5 IRK data structure	277
	30.6 Registers	
	30.7 Electrical specification	
31	SPIM — Serial peripheral interface master with EasyDMA	281
	31.1 Shared resources	
	31.2 EasyDMA	
	31.3 SPI master transaction sequence	
	31.4 Low power	
	· · · · · PARALIMINIO I I I I I I I I I I I I I I I I I I	∠∪-т
	31.5 Master mode pin configuration	284
		284 285



32	SPIS —	Serial peripheral interface slave with EasyDMA	292
		nared resources	
	32.2 Ea	asyDMA	292
	32.3 SF	PI slave operation	293
		n configuration	
		egisters	
		ectrical specification	
33		I ² C compatible two-wire interface master with EasyDMA	
		nared resources	
		asyDMA	
		aster write sequence	
		aster read sequence	
		aster repeated start sequence	
		w power	
		aster mode pin configuration	
		egisters	
		ectrical specification	
34	TWIS —	I ² C compatible two-wire interface slave with EasyDMA	319
	34.1 Sh	nared resources	321
	34.2 Ea	asyDMA	321
	34.3 TV	VI slave responding to a read command	321
		VI slave responding to a write command	
	34.5 Ma	aster repeated start sequence	323
	34.6 Te	rminating an ongoing TWI transaction	324
		w power	
	34.8 Sl	ave mode pin configuration	324
		egisters	
		Electrical specification	
$\sim E$			
35	UARTE -	 Universal asynchronous receiver/transmitter with EasyDM. 	A 333
35	35.1 Sh	nared resources	333
35	35.1 Sh 35.2 Ea	nared resourcesasyDMA	333 333
35	35.1 Sh 35.2 Ea 35.3 Tr	nared resourcesasyDMAansmission	333 333 334
35	35.1 St 35.2 Ea 35.3 Tr 35.4 Re	nared resourcesasyDMAansmission.	333 333 334
35	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er	nared resourcesasyDMAansmissioneception	333 333 334 334
35	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us	nared resources	333 334 334 336
35	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa	nared resources	333 334 334 336 336
35	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo	nared resources	333 334 334 336 336 336
35	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pi	nared resources	333 334 334 336 336 336 336
35	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pi 35.10 F	nared resources	333 334 336 336 336 337 337
	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pi 35.10 F 35.11 E	nared resources	
	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pi 35.10 F 35.11 E	nared resources	333334334336336336337345
	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pi 35.10 F 35.11 E QDEC — 36.1 Sa	nared resources	333334334336336337337347347
	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 En 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pii 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 LE	nared resources	333334334336336336337347347348
	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pi 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 LE 36.3 De	nared resources	333334334336336336337347347348
	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pii 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 LE 36.3 De 36.4 Ac	nared resources. asyDMA	333334334336336336337347347348349
	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pi 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 Le 36.3 De 36.4 Ao 36.5 Ou	nared resources. asyDMA	333334334336336336337347347348349
	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pi 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 LE 36.3 De 36.4 Ao 36.5 Ou 36.6 Pi	nared resources. asyDMA	333334334336336337347347347349349
	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 En 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pi 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 LE 36.3 De 36.4 Ao 36.5 Ou 36.6 Pi 36.7 Re	nared resources asyDMA	333334334336336336337347347349349
36	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pi 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 LE 36.3 De 36.4 Ao 36.5 Ou 36.6 Pi 36.7 Re 36.8 Ele	nared resources	333334334336336337347347347349349350
36	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pii 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 Le 36.3 De 36.4 Ao 36.5 Ou 36.6 Pii 36.7 Re 36.8 Ele SAADC	nared resources	333334334336336336337347347347349349350356
36	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pi 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 Le 36.3 De 36.4 Ao 36.5 Oo 36.6 Pi 36.7 Re 36.8 Ele 36.8 Ele 37.1 Sh	nared resources	333334334336336336337347347348349349350356357
36	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pi 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 LE 36.3 De 36.4 Ao 36.5 Ou 36.6 Pi 36.7 Re 36.8 Ele SAADC 37.1 Sh 37.2 Ov	nared resources	333334334336336336337347348349349349357357
36	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pi 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 LE 36.3 De 36.4 Ao 36.5 Ou 36.6 Pi 36.7 Re 36.8 Ele SAADC 37.1 Sh 37.2 Ou 37.3 Di	nared resources	333334334336336336337347347347349349350357357
36	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pii 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 LE 36.3 De 36.4 Ao 36.5 Ou 36.6 Pii 36.7 Re 36.8 Ele SAADC 37.1 Sh 37.2 On 37.3 Di 37.4 Ar	nared resources	
36	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pii 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 LE 36.3 De 36.4 Ao 36.5 Ou 36.6 Pii 36.7 Re 36.8 Ele SAADC 37.1 Sh 37.2 Ou 37.3 Di 37.4 Ar 37.5 Op	nared resources asyDMA	333334334336336336337347347347349349350357357357
36	35.1 Sh 35.2 Ea 35.3 Tr 35.4 Re 35.5 Er 35.6 Us 35.7 Pa 35.8 Lo 35.9 Pii 35.10 F 35.11 E QDEC — 36.1 Sa 36.2 LE 36.3 De 36.4 Ao 36.5 Ou 36.6 Pii 36.7 Re 36.8 Ele SAADC 37.1 Sh 37.2 Ou 37.3 Di 37.4 Ar 37.5 Op 37.6 Ea	nared resources	333334334336336336336337347347347349350357357357357358



	37.8 Reference	
	37.9 Acquisition time	
	37.10 Limits event monitoring	
	37.11 Registers	
	37.12 Electrical specification	
	37.13 Performance factors	391
38	COMP — Comparator	392
	38.1 Shared resources	393
	38.2 Differential mode	393
	38.3 Single-ended mode	394
	38.4 Pin configuration	396
	38.5 Registers	396
	38.6 Electrical specification	401
39	LPCOMP — Low power comparator	
	39.1 Shared resources	
	39.2 Pin configuration	
	39.3 Registers	
	39.4 Electrical specification	
40	WDT — Watchdog timer	
	40.1 Reload criteria	
	40.2 Temporarily pausing the watchdog	
	40.3 Watchdog reset	
	40.4 Registers	
	40.5 Electrical specification	
41	SWI — Software interrupts	
•	41.1 Registers	
12	NFCT — Near field communication tag	
42	42.1 Overview	
	42.2 Pin configuration	
	42.3 EasyDMA	
	42.4 Collision resolution	
	42.5 Frame timing controller	
	42.6 Frame assembler	
	42.7 Frame disassembler	
	42.8 Antenna interface	
	42.9 NFCT antenna recommendations	
	42.10 Battery protection	
	42.11 References	
	42.12 Registers	
	42.13 Electrical specification	
43	PDM — Pulse density modulation interface	
70	43.1 Master clock generator	
	43.2 Module operation	
	43.3 Decimation filter	
	43.4 EasyDMA	
	43.5 Hardware example	
	43.6 Pin configuration	
	43.7 Registers	
	43.8 Electrical specification.	
11	I ² S — Inter-IC sound interface	
	44.1 Mode	
	44.1 Mode	
	44.2 Transmitting and receiving	
	44.4 Serial clock (SCK)	
	44.5 Master clock (MCK)	
	44.6 Width, alignment and format	
	· · ·	
	44.7 EasyDMA	450



	44.8 Module operation	450
	44.9 Pin configuration	
	44.10 Registers	
	44.11 Electrical specification	
45	MWU — Memory watch unit	462
	45.1 Registers	462
46	EGU — Event generator unit	
	46.1 Registers	
	46.2 Electrical specification	
47		
47	PWM — Pulse width modulation	
	47.1 Wave counter	
	47.2 Decoder with EasyDMA	
	47.3 Limitations	
	47.4 Pin configuration	504
	47.5 Registers	505
	47.6 Electrical specification	513
48	SPI — Serial peripheral interface master	
	48.1 Functional description	
	48.2 Registers	
	48.3 Electrical specification	
40	TIME 12C compatible two wire interfere	520
49	TWI — I ² C compatible two-wire interface	522
	49.1 Functional description	
	49.2 Master mode pin configuration	
	49.3 Shared resources	
	49.4 Master write sequence	523
	49.5 Master read sequence	524
	49.6 Master repeated start sequence	525
	49.7 Low power	526
	40.0 Destatant	
	49.8 Registers	526
	49.8 Registers	
50	49.9 Electrical specification	530
50	49.9 Electrical specification UART — Universal asynchronous receiver/transmitter	530 532
50	49.9 Electrical specification	530 532
50	49.9 Electrical specification UART — Universal asynchronous receiver/transmitter	530 532 532
50	49.9 Electrical specification UART — Universal asynchronous receiver/transmitter	530532532532
50	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter	530532532533533
50	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter	530532532533533
50	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter. 50.1 Functional description. 50.2 Pin configuration. 50.3 Shared resources. 50.4 Transmission. 50.5 Reception. 50.6 Suspending the UART.	530532532533533533
50	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter	530532532533533533534
50	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter	530532532533533534535
50	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter	530532532533533534535
50	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter	530532532533533534535
50	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter. 50.1 Functional description. 50.2 Pin configuration. 50.3 Shared resources. 50.4 Transmission. 50.5 Reception. 50.6 Suspending the UART. 50.7 Error conditions. 50.8 Using the UART without flow control. 50.9 Parity configuration.	530532532533533534535535
	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter. 50.1 Functional description. 50.2 Pin configuration. 50.3 Shared resources. 50.4 Transmission. 50.5 Reception. 50.6 Suspending the UART. 50.7 Error conditions. 50.8 Using the UART without flow control. 50.9 Parity configuration. 50.10 Registers. 50.11 Electrical specification.	530532532533533534535535
	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter. 50.1 Functional description. 50.2 Pin configuration. 50.3 Shared resources. 50.4 Transmission. 50.5 Reception. 50.6 Suspending the UART. 50.7 Error conditions. 50.8 Using the UART without flow control. 50.9 Parity configuration. 50.10 Registers. 50.11 Electrical specifications. Mechanical specifications.	530532532533533534535535535
	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter. 50.1 Functional description. 50.2 Pin configuration. 50.3 Shared resources. 50.4 Transmission. 50.5 Reception. 50.6 Suspending the UART. 50.7 Error conditions. 50.8 Using the UART without flow control. 50.9 Parity configuration. 50.10 Registers. 50.11 Electrical specifications. Mechanical specifications. 51.1 QFN48 6 x 6 mm package.	530532532533533534535535540541
51	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter	530532532533533534535535535540541541
51	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter	530532532533533534535535540541542
51	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter	530532532533533534535535540541541542543
51	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter. 50.1 Functional description. 50.2 Pin configuration. 50.3 Shared resources. 50.4 Transmission. 50.5 Reception. 50.6 Suspending the UART. 50.7 Error conditions. 50.8 Using the UART without flow control. 50.9 Parity configuration. 50.10 Registers. 50.11 Electrical specifications. 51.1 QFN48 6 x 6 mm package. 51.2 WLCSP package. Ordering information. 52.1 IC marking. 52.2 Box labels.	530532532533533534535540541541542543
51	49.9 Electrical specification UART — Universal asynchronous receiver/transmitter 50.1 Functional description 50.2 Pin configuration 50.3 Shared resources 50.4 Transmission 50.5 Reception 50.6 Suspending the UART 50.7 Error conditions 50.8 Using the UART without flow control 50.9 Parity configuration 50.10 Registers 50.11 Electrical specifications 50.11 QFN48 6 x 6 mm package 51.1 QFN48 6 x 6 mm package 51.2 WLCSP package Ordering information 52.1 IC marking 52.2 Box labels 52.3 Order code	530532532533533534535540541541542543543
51	49.9 Electrical specification UART — Universal asynchronous receiver/transmitter 50.1 Functional description 50.2 Pin configuration 50.3 Shared resources 50.4 Transmission 50.5 Reception 50.6 Suspending the UART 50.7 Error conditions 50.8 Using the UART without flow control 50.9 Parity configuration 50.10 Registers 50.11 Electrical specifications 50.11 QFN48 6 x 6 mm package 51.1 QFN48 6 x 6 mm package 51.2 WLCSP package Ordering information 52.2 Box labels 52.3 Order code 52.4 Code ranges and values	530 532 532 533 533 534 534 535 535 540 541 542 543 543
51	49.9 Electrical specification UART — Universal asynchronous receiver/transmitter 50.1 Functional description 50.2 Pin configuration 50.3 Shared resources 50.4 Transmission 50.5 Reception 50.6 Suspending the UART 50.7 Error conditions 50.8 Using the UART without flow control 50.9 Parity configuration 50.10 Registers 50.11 Electrical specifications 50.11 QFN48 6 x 6 mm package 51.1 QFN48 6 x 6 mm package 51.2 WLCSP package Ordering information 52.1 IC marking 52.2 Box labels 52.3 Order code	530 532 532 533 533 534 534 535 535 540 541 542 543 543
51 52	49.9 Electrical specification UART — Universal asynchronous receiver/transmitter 50.1 Functional description 50.2 Pin configuration 50.3 Shared resources 50.4 Transmission 50.5 Reception 50.6 Suspending the UART 50.7 Error conditions 50.8 Using the UART without flow control 50.9 Parity configuration 50.10 Registers 50.11 Electrical specifications 50.11 QFN48 6 x 6 mm package 51.1 QFN48 6 x 6 mm package 51.2 WLCSP package Ordering information 52.2 Box labels 52.3 Order code 52.4 Code ranges and values	530532532533533534535535540541542543543544544
51 52	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter. 50.1 Functional description. 50.2 Pin configuration. 50.3 Shared resources. 50.4 Transmission. 50.5 Reception. 50.6 Suspending the UART. 50.7 Error conditions. 50.8 Using the UART without flow control. 50.9 Parity configuration. 50.10 Registers. 50.11 Electrical specifications. 51.1 QFN48 6 x 6 mm package. 51.2 WLCSP package. Ordering information. 52.1 IC marking. 52.2 Box labels. 52.3 Order code. 52.4 Code ranges and values. 52.5 Product options. Reference circuitry.	530532532533533534535535540541542543543544544
51 52	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter. 50.1 Functional description. 50.2 Pin configuration. 50.3 Shared resources. 50.4 Transmission. 50.5 Reception. 50.6 Suspending the UART. 50.7 Error conditions. 50.8 Using the UART without flow control. 50.9 Parity configuration. 50.10 Registers. 50.11 Electrical specifications. Mechanical specifications. 51.1 QFN48 6 x 6 mm package. 51.2 WLCSP package. Ordering information. 52.1 IC marking. 52.2 Box labels. 52.3 Order code. 52.4 Code ranges and values. 52.5 Product options. Reference circuitry. 53.1 Schematic QFAA and QFAB QFN48 with internal LDO setup.	530532532533533534535540541541542543543544544545
51 52	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter	530 532 532 533 533 533 534 534 535 540 541 542 543 543 544 544 5545
51 52	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter. 50.1 Functional description. 50.2 Pin configuration. 50.3 Shared resources. 50.4 Transmission. 50.5 Reception. 50.6 Suspending the UART. 50.7 Error conditions. 50.8 Using the UART without flow control. 50.9 Parity configuration. 50.10 Registers. 50.11 Electrical specifications. 51.1 QFN48 6 x 6 mm package. 51.2 WLCSP package. Ordering information. 52.1 IC marking. 52.2 Box labels. 52.3 Order code. 52.4 Code ranges and values. 52.5 Product options. Reference circuitry. 53.1 Schematic QFAA and QFAB QFN48 with internal LDO setup. 53.2 Schematic QFAA and QFAB QFN48 with DC/DC regulator and NFC setup.	530 532 532 533 533 534 534 535 535 540 541 542 543 543 544 544 5545
51 52	49.9 Electrical specification. UART — Universal asynchronous receiver/transmitter	530 532 532 533 533 534 534 535 535 540 541 542 543 543 544 544 5545 546 546 547



53.6 Schematic CIAA WLCSP with DC/DC regulator and NFC setup	551
53.7 PCB guidelines	
53.8 PCB layout example	
54 Liability disclaimer	
54.1 RoHS and REACH statement	
54.2 Life support applications	



1 Revision history

Date	Version	Description
February 2017	1.3	The following content has been added or updated:
		• RADIO — 2.4 GHz Radio on page 205: Introduced 2 Mbps Bluetooth* low energy mode.
		 FICR — Factory information configuration registers on page 43: Updated INFO.PACKAGE register (new package added).
		 UARTE: Corrected the pin configuration table. PPI — Programmable peripheral interconnect on page 168: Timing information corrected.
		Updated the liability disclaimer.
September 2016	1.2	Updated the following:
		 Power and clock management, Current consumption: Ultra-low power on page 77.
		 Power, Current consumption, sleep on page 99
July 2016	1.1	Added documentation for nRF52832 CIAA WLCSP.
		Added or updated the following content:
		Cover: Added Key features.
		 Pin assignments on page 13: Added WLCSP ball assignments. Moved GPIO usage restrictions here from GPIO/Notes on usage and restrictions.
		 Absolute maximum ratings on page 19: Added environmental information for WLCSP to the table.
		 Memory on page 23: Added QFAB and CIAA information to the table.
		 FICR — Factory information configuration registers on page 43: Updated INFO.PACKAGE register.
		 UICR: Updated APPROTECT register.
		 Debug and trace on page 72: Updated DAP - Debug access port.
		 POWER — Power supply on page 78: Updated Pin reset.
		 CLOCK — Clock control on page 101: Updated information on external 32 kHz clock support.
		GPIO — General purpose input/output on page 111: Added GPIO located near the RADIO.
		 RADIO — 2.4 GHz Radio on page 205: Updated Figure 29 and Interframe spacing.
		CCM: Updated SCRATCHPTR register.
		SPIM: Updated Master mode pin configuration.
		 UARTE: Added RXDRDY and TXDRDY events.
		 NFCT: Updated Electrical specifications.
		 PWM — Pulse width modulation on page 496: Updated SEQ[1].REFRESH register.
		 Mechanical specifications on page 541: Added WLCSP package.
		Ordering information on page 543: Updated with CIAA and QFAB information.
		 Reference circuitry on page 546: QFAB information added. CIAA WLCSP schematics
February 2016	1.0	added. First release.
Testually 2010	1.0	i ii st i cicase.



2 About this document

This Product Specification is organized into chapters based on the modules and peripherals that are available in this IC.

The peripheral descriptions are broken into separate sections that include the following information:

- A detailed functional description of the peripheral.
- · Register configuration for the peripheral
- Electrical specification tables providing the specified limits of the chip when tested under the conditions defined in the *Recommended operating conditions* on page 20

2.1 Peripheral naming and abbreviations

Every peripheral has a unique capitalized name or an abbreviation of its name, e.g. TIMER, used for identification and reference. This name is used in chapter headings and references, and it will appear in the ARM® Cortex® Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer to identify the peripheral.

The peripheral instance name, which is different from the peripheral name, is constructed using the peripheral name followed by a numbered postfix, starting with 0, for example, TIMER0. A postfix is normally only used if a peripheral can be instantiated more than once. The peripheral instance name is also used in the CMSIS to identify the peripheral instance.

2.2 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

2.2.1 Fields and values

The Id (Field Id) row specifies the bits that belong to the different fields in the register.

A blank space means that the field is reserved and that it is read as undefined, and must be written as '0' to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column.

If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column. Single-bit bit fields may, however, omit the **Value Id** when values can be substituted with a Boolean type enumerator range, for example, True/False, Disable/Enable, On/Off, and so on.

Values are usually provided as decimal or hexadecimal. Hex values have a '0x' prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example, 1, 3, 9.
- Range of values, e.g. [0..4], that is, all values from and including 0 and 4.
- Implicit values. If no values are indicated in the Value column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value** Id, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with "..".

When an item is marked with the word **Deprecated**, it means this is an attribute applied to a feature to indicate that it should not be used for new designs.



2.3 Registers

Table 1: Register Overview

Register	Offset	Description
DUMMY	0x514	Example of a register controlling a dummy feature

2.3.1 **DUMMY**

Address offset: 0x514

Example of a register controlling a dummy feature

Dit mount on		21	20	20.	20.2	7 7	C 21		4.2	2 2	2 22	1 20	10	10	17	10	1 -	1.4	12	12	11	10	^	0 -	,	с г		2	2	1	0
Bit number		31	. 30	29 .	28 2	/ 2	6 2	o 2	4 2	3 2.	2 2.	I 20) 19	18	1/	16	15	14	13	12	11	10	9	8 7	′ ′	6 5) 4	3	2	1	J
Id					- 1)	D D) [)					С	С	С								В						Α .	Д
Reset 0x000500	2	0	0	0	0 (0	0 0	C) (0	0	0	0	1	0	1	0	0	0	0	0	0	0	0 () (0 0	0	0	0	1	0
ld RW Field	Value Id	Va	lue						D	esc	ript	ion																			
A RW FIELD	_A								Е	xam	ple	of	a fie	eld	witl	ı se	ver	al e	nuı	mer	ate	d va	lue	S							
	Disabled	0 The example feature is disabled																													
	NormalMode	1 The example feature is enabled in normal mode																													
	ExtendedMode	2							Т	he e	exar	nple	e fe	atu	re i	s er	nabl	ed	alo	ng v	vith	ext	ra f	unc	ioi	nalit	у				
B RW FIELD	_В								Е	xam	ple	of	a de	epre	ecat	ed	fiel	d										De	pre	cate	d
	Disabled	0							Т	he c	over	rride	e fe	atu	re i	s di	sab	ed													
	Enabled	1 The override feature is enabled																													
C RW FIELD	_c	Example of a field with a valid range of values																													
	ValidRange	[27] Example of allowed values for this field																													
D RW FIELD	D								Е	xam	ple	of	a fie	eld '	witl	า ทด	re	stri	ctio	n o	n th	e va	alue	es							



3 Block diagram

This block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

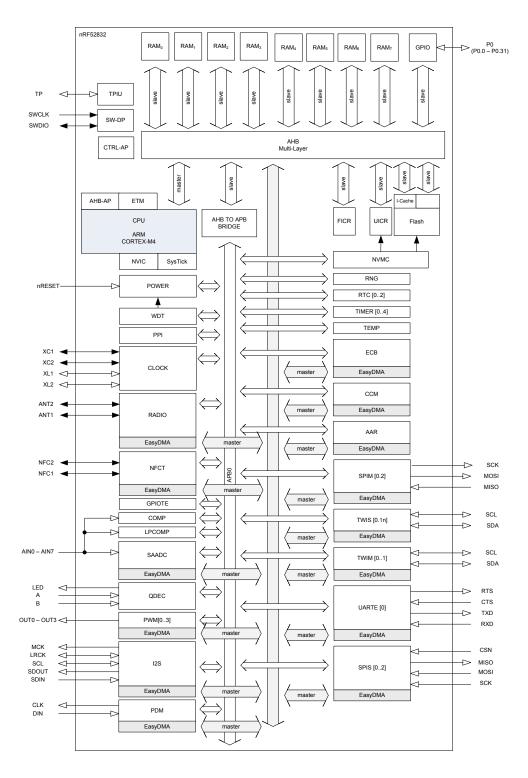


Figure 1: Block diagram



4 Pin assignments

Here we cover the pin assignments for each variant of the chip.

4.1 QFN48 pin assignments

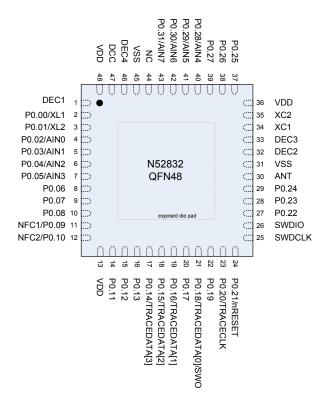


Figure 2: QFN48 pin assignments, top view

Table 2: QFN48 pin assignments

Pin	Name	Туре	Description
Left Side of chip			
1	DEC1	Power	0.9 V regulator digital supply decoupling
2	P0.00	Digital I/O	General purpose I/O
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO)
3	P0.01	Digital I/O	General purpose I/O
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO)
4	P0.02	Digital I/O	General purpose I/O
	AIN0	Analog input	SAADC/COMP/LPCOMP input
5	P0.03	Digital I/O	General purpose I/O
	AIN1	Analog input	SAADC/COMP/LPCOMP input
6	P0.04	Digital I/O	General purpose I/O
	AIN2	Analog input	SAADC/COMP/LPCOMP input
7	P0.05	Digital I/O	General purpose I/O
	AIN3	Analog input	SAADC/COMP/LPCOMP input
8	P0.06	Digital I/O	General purpose I/O
9	P0.07	Digital I/O	General purpose I/O



Pin	Name	Туре	Description
10	P0.08	Digital I/O	General purpose I/O
11	NFC1	NFC input	NFC antenna connection
	P0.09	Digital I/O	General purpose I/O ¹
12	NFC2	NFC input	NFC antenna connection
	P0.10	Digital I/O	General purpose I/O ¹
Bottom side of chip	1 0.10	Digital I/O	deneral purpose 1/0
13	VDD	Power	Power supply
14	P0.11	Digital I/O	General purpose I/O
15	P0.12	Digital I/O	General purpose I/O
16	P0.13	Digital I/O	General purpose I/O
17	P0.14	Digital I/O	General purpose I/O
	TRACEDATA[3]		Trace port output
18	P0.15	Digital I/O	General purpose I/O
		, ,	
19	TRACEDATA[2] P0.16	Digital I/O	Trace port output General purpose I/O
19	PU.16	Digital I/O	General purpose 1/O
	TRACEDATA[1]		Trace port output
20	P0.17	Digital I/O	General purpose I/O
21	P0.18	Digital I/O	General purpose I/O
	TRACEDATA[0] / SWO		Single wire output
			Trace port output
22	P0.19	Digital I/O	General purpose I/O
23	P0.20	Digital I/O	General purpose I/O
	TRACECLK		Trace port clock output
24	P0.21	Digital I/O	General purpose I/O
		- 18.1 1, -	
B. 1. C. 1 . C. 1.	nRESET		Configurable as pin reset
Right Side of chip	CMDCLK	Digital input	Carial wire dabug clask input for dabug
25	SWDCLK	Digital input	Serial wire debug clock input for debug and programming
26	SWDIO	Digital I/O	Serial wire debug I/O for debug and
20	3.75.6	Digital I/O	programming
27	P0.22	Digital I/O	General purpose I/O ²
28	P0.23	Digital I/O	General purpose I/O ²
29	P0.24	Digital I/O	General purpose I/O ²
30	ANT	RF	Single-ended radio antenna connection
31	VSS	Power	Ground (Radio supply)
32	DEC2	Power	1.3 V regulator supply decoupling (Radio
			supply)
33	DEC3	Power	Power supply decoupling
34	XC1	Analog input	Connection for 32 MHz crystal
35	XC2	Analog input	Connection for 32 MHz crystal
36	VDD	Power	Power supply
Top side of chip		21.11.11.12	2
37	P0.25	Digital I/O	General purpose I/O ² General purpose I/O ²
38 39	P0.26 P0.27	Digital I/O Digital I/O	General purpose I/O ² General purpose I/O ²
40	P0.27 P0.28	Digital I/O	General purpose I/O ²
		-	
	AIN4	Analog input	SAADC/COMP/LPCOMP input
41	P0.29	Digital I/O	General purpose I/O ²
	AIN5	Analog input	SAADC/COMP/LPCOMP input
42	P0.30	Digital I/O	General purpose I/O ²
	AIN6	Analog input	SAADC/COMP/LPCOMP input
43	P0.31	Digital I/O	General purpose I/O pin ²
	AIN7	Analog input	SAADC/COMP/LPCOMP input
	/ 111 1/	, maios mpar	State of Court / El Colvil Input



Name	Туре	Description
NC		No connect
		Leave unconnected
VSS	Power	Ground
DEC4	Power	1.3 V regulator supply decoupling
		Input from DC/DC regulator
		Output from 1.3 V LDO
DCC	Power	DC/DC regulator output
VDD	Power	Power supply
VSS	Power	Ground pad
		Exposed die pad must be connected
		to ground (VSS) for proper device
		operation.
	VSS DEC4 DCC VDD	VSS Power DEC4 Power DCC Power VDD Power

4.2 WLCSP ball assignments

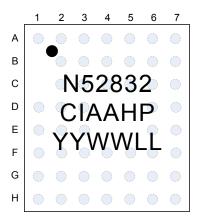


Figure 3: WLCSP ball assignments, top view

Table 3: WLCSP ball assignments

Ball	Name		Description
A1	XC2	Analog input	Connection for 32 MHz crystal
A2	DEC2	Power	1.3 V regulator supply decoupling (Radio
			supply)
A3	P0.28	Digital I/O	General purpose I/O ³
	AIN4	Analog input	SAADC/COMP/LPCOMP input
A4	P0.29	Digital I/O	General purpose I/O ³
	AIN5	Analog input	SAADC/COMP/LPCOMP input
A5	P0.30	Digital I/O	General purpose I/O ³
	AIN6	Analog input	SAADC/COMP/LPCOMP input
A6	DEC4	Power	1.3 V regulator supply decoupling
			Input from DC/DC converter. Output
			from 1.3 V LDO
A7	VDD	Power	Power supply
B2	XC1	Analog input	Connection for 32 MHz crystal
В3	P0.25	Digital I/O	General purpose I/O ³

See *GPIO located near the radio* on page 17 for more information.

See *NFC antenna pins* on page 17 for more information.



Ball	Name		Description
B4	P0.27	Digital I/O	General purpose I/O ³
B5	P0.31	Digital I/O	General purpose I/O ³
	A1A17	-	
B6	AIN7 DCC	Analog input Power	SAADC/COMP/LPCOMP input DC/DC converter output
B7	DEC1	Power	0.9 V regulator digital supply decoupling
C2	DEC3	Power	Power supply decoupling
C3	NC NC	N/A	Not connected
C4	VSS	Power	Ground
C5	VSS	Power	Ground
C6	P0.02	Digital I/O	General purpose I/O
		_	
67	AINO	Analog input	SAADC/COMP/LPCOMP input
C7	P0.01	Digital I/O	General purpose I/O
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO)
D1	ANT	RF	Single-ended radio antenna connection
D2	VSS_PA	Power	Ground (Radio supply)
D3	P0.26	Digital I/O	General purpose I/O ³
D6	P0.03	Digital I/O	General purpose I/O
	AIN1	Analog input	SAADC/COMP/LPCOMP input
D7	P0.00	Digital I/O	General purpose I/O
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO)
E1	P0.24	Digital I/O	General purpose I/O ³
E2	P0.23	Digital I/O	General purpose I/O ³
E3	VSS	Power	Ground
E6	P0.04	Digital I/O	General purpose I/O
	4442	_	
F2	AIN2	Analog input	SAADC/COMP/LPCOMP input
E7	P0.05	Digital I/O	General purpose I/O
	AIN3	Analog input	SAADC/COMP/LPCOMP input
F1	SWDCLK	Digital input	Serial wire debug clock input for debug
			and programming
F2	P0.22	Digital I/O	General purpose I/O ³
F3	P0.19	Digital I/O	General purpose I/O
F4	P0.11	Digital I/O	General purpose I/O
		_	
F5	VSS	Power	Ground
F6	P0.07	Digital I/O	General purpose I/O
F6 F7	P0.07 P0.06	Digital I/O Digital I/O	General purpose I/O General purpose I/O
F6	P0.07	Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and
F6 F7 G1	P0.07 P0.06 SWDIO	Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming
F6 F7	P0.07 P0.06	Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and
F6 F7 G1	P0.07 P0.06 SWDIO P0.20 TRACECLK	Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output
F6 F7 G1 G2	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O
F6 F7 G1 G2 G3 G4	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O
F6 F7 G1 G2	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O
F6 F7 G1 G2 G3 G4	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O
F6 F7 G1 G2 G3 G4	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2	Digital I/O NFC input	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O NFC antenna connection
F6 F7 G1 G2 G3 G4 G5	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10	Digital I/O NFC input Digital I/O NFC input	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O NFC antenna connection General purpose I/O ⁴
F6 F7 G1 G2 G3 G4 G5	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O NFC input Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O NFC antenna connection General purpose I/O ⁴ NFC antenna connection
F6 F7 G1 G2 G3 G4 G5	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09	Digital I/O NFC input Digital I/O NFC input Digital I/O NFC input	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O NFC antenna connection General purpose I/O ⁴ NFC antenna connection General purpose I/O ⁴
F6 F7 G1 G2 G3 G4 G5 G6	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O NFC antenna connection General purpose I/O ⁴ NFC antenna connection General purpose I/O ⁴ General purpose I/O General purpose I/O General purpose I/O General purpose I/O
F6 F7 G1 G2 G3 G4 G5 G6 G7 H1	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21 nRESET	Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O NFC antenna connection General purpose I/O ⁴ NFC antenna connection General purpose I/O ⁴ OF Configurable as pin reset
F6 F7 G1 G2 G3 G4 G5 G6	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21 nRESET P0.18	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O OFF antenna connection General purpose I/O NFC antenna connection General purpose I/O General purpose I/O General purpose I/O Configurable as pin reset General purpose I/O
F6 F7 G1 G2 G3 G4 G5 G6 G7 H1	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21 nRESET P0.18 TRACEDATA[0]	Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O NFC antenna connection General purpose I/O ⁴ NFC antenna connection General purpose I/O ⁴ General purpose I/O Configurable as pin reset General purpose I/O Trace port output
F6 F7 G1 G2 G3 G4 G5 G6 G7 H1	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21 nRESET P0.18	Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O OFF antenna connection General purpose I/O NFC antenna connection General purpose I/O General purpose I/O General purpose I/O Configurable as pin reset General purpose I/O
F6 F7 G1 G2 G3 G4 G5 G6 G7 H1	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21 nRESET P0.18 TRACEDATA[0]	Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O NFC antenna connection General purpose I/O ⁴ NFC antenna connection General purpose I/O ⁴ General purpose I/O Configurable as pin reset General purpose I/O Trace port output
F6 F7 G1 G2 G3 G4 G5 G6 G7 H1	P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21 nRESET P0.18 TRACEDATA[0] P0.16	Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O MFC antenna connection General purpose I/O ⁴ NFC antenna connection General purpose I/O Ceneral purpose I/O General purpose I/O Trace port output General purpose I/O Configurable as pin reset General purpose I/O Trace port output General purpose I/O



Ball	Name		Description
	TRACEDATA[2]		Trace port output
H5	P0.14	Digital I/O	General purpose I/O
	TRACEDATA[3]		Trace port output
Н6	P0.12	Digital I/O	General purpose I/O
H7	VDD	Power	Power supply

4.3 GPIO usage restrictions

4.3.1 GPIO located near the radio

Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current close to the Radio power supply and antenna pins.

Table 4: GPIO recommended usage for QFN48 package on page 17 and Table 5: GPIO recommended usage for WLCSP package on page 17 identify some GPIO that have recommended usage guidelines to maximize radio performance in an application.

Table 4: GPIO recommended usage for QFN48 package

Pin	GPIO	Recommended usage
27	P0.22	Low drive, low frequency I/O only.
28	P0.23	
29	P0.24	
37	P0.25	
38	P0.26	
39	P0.27	
40	P0.28	
41	P0.29	
42	P0.30	
43	P0.31	

Table 5: GPIO recommended usage for WLCSP package

Pin	GPIO	Recommended usage
F2	P0.22	Low drive, low frequency I/O only.
E2	P0.23	
E1	P0.24	
B3	P0.25	
D3	P0.26	
B4	P0.27	
A3	P0.28	
A4	P0.29	
A5	P0.30	
B5	P0.31	

4.3.2 NFC antenna pins

Two physical pins can be configured either as NFC antenna pins (factory default), or as GPIOs, as shown below.

Table 6: GPIO pins used by NFC

NFC pad name	GPIO
NFC1	P0.09
NFC2	P0.10

When configured as NFC antenna pins, the GPIOs on those pins will automatically be set to DISABLE state and a protection circuit will be enabled preventing the chip from being damaged in the presence of a strong NFC field. The protection circuit will short the two pins together if voltage difference exceeds approximately 2 V.

³ See *GPIO located near the radio* on page 17 for more information.

⁴ See *NFC antenna pins* on page 17 for more information.



For information on how to configure these pins as normal GPIOs, see *NFCT* — *Near field communication tag* on page 417 and *UICR* — *User information configuration registers* on page 54. Note that the device will not be protected against strong NFC field damage if the pins are configured as GPIO and an NFC antenna is connected to the device. The pins will always be configured as NFC pins during power-on reset until the configuration is set according to the UICR register.

These two pins will have some limitations when configured as GPIO. The pin capacitance will be higher on these pins, and there is some current leakage between the two pins if they are driven to different logical values. To avoid leakage between the pins when configured as GPIO, these GPIOs should always be at the same logical value whenever entering one of the device power saving modes. See *Electrical specification*.



5 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Table 7: Absolute maximum ratings

	Min.	Max.	Unit
Supply voltages			
VDD	-0.3	+3.9	V
VSS		0	V
I/O pin voltage			
V _{I/O} , VDD ≤3.6 V	-0.3	VDD + 0.3 V	V
V _{I/O} , VDD >3.6 V	-0.3	3.9 V	V
NFC antenna pin current			
I _{NFC1/2}		80	mA
Radio			
RF input level		10	dBm
Environmental QFN48, 6×6 mm package			
Storage temperature	-40	+125	°C
MSL (moisture sensitivity level)		2	
ESD HBM (human body model)		4	kV
ESD CDM (charged device model)		1000	V
Environmental WLCSP, 3.0×3.2 mm package			
Storage temperature	-40	+125	°C
MSL		1	
ESD HBM		2	kV
ESD CDM		500	V
Flash memory			
Endurance	10 000		Write/erase cycles
Retention	10 years at 40°C		





6 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Table 8: Recommended operating conditions

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	Supply voltage, independent of DCDC enable		1.7	3.0	3.6	V
t_{R_VDD}	Supply rise time (0 V to 1.7 V)				60	ms
TĀ	Operating temperature		-40	25	85	°C

Important: The on-chip power-on reset circuitry may not function properly for rise times longer than the specified maximum.



7 CPU

The ARM® Cortex®-M4 processor with floating-point unit (FPU) has a 32-bit instruction set (Thumb®-2 technology) that implements a superset of 16 and 32-bit instructions to maximize code density and performance.

This processor implements several features that enable energy-efficient arithmetic and high-performance signal processing including:

- Digital signal processing (DSP) instructions
- Single-cycle multiply and accumulate (MAC) instructions
- Hardware divide
- 8 and 16-bit single instruction multiple data (SIMD) instructions
- Single-precision floating-point unit (FPU)

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex processor series is implemented and available for the M4 CPU.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the Nested Vectored Interrupt Controller (NVIC).

Executing code from flash will have a wait state penalty on the nRF52 Series. An instruction cache can be enabled to minimize flash wait states when fetching instructions. For more information on cache, see *Cache* on page 30. The section *Electrical specification* on page 21 shows CPU performance parameters including wait states in different modes, CPU current and efficiency, and processing power and efficiency based on the CoreMark® benchmark.

7.1 Floating point interrupt

The floating point unit (FPU) may generate exceptions when used due to e.g. overflow or underflow. These exceptions will trigger the FPU interrupt (see *Instantiation* on page 24). To clear the IRQ line when an exception has occurred, the relevant exception bit within the FPSCR register needs to be cleared. For more information about the FPSCR or other FPU registers, see *Cortex-M4 Devices Generic User Guide*.

7.2 Electrical specification

7.2.1 CPU performance

The CPU clock speed is 64 MHz. Current and efficiency data is taken when in System ON and the CPU is executing the CoreMark[™] benchmark. It includes power regulator and clock base currents. All other blocks are IDLE.

Symbol	Description	Min.	Тур.	Max.	Units
W _{FLASH}	CPU wait states, running from flash, cache disabled	0		2	
W _{FLASHCACHE}	CPU wait states, running from flash, cache enabled	0		3	
W _{RAM}	CPU wait states, running from RAM			0	
I _{DDFLASHCACHE}	CPU current, running from flash, cache enabled, LDO		7.4		mA
I _{DDFLASHCACHEDCDC}	CPU current, running from flash, cache enabled, DCDC 3V		3.7		mA
I _{DDFLASH}	CPU current, running from flash, cache disabled, LDO		8.0		mA
I _{DDFLASHDCDC}	CPU current, running from flash, cache disabled, DCDC 3V		3.9		mA
I _{DDRAM}	CPU current, running from RAM, LDO		6.7		mA
I _{DDRAMDCDC}	CPU current, running from RAM, DCDC 3V		3.3		mA
I _{DDFLASH/MHz}	CPU efficiency, running from flash, cache enabled, LDO		125		μΑ/
					MHz
I _{DDFLASHDCDC/MHz}	CPU efficiency, running from flash, cache enabled, DCDC 3V		58		μΑ/
					MHz



Symbol	Description	Min.	Тур.	Max.	Units
CM_{FLASH}	CoreMark ⁵ , running from flash, cache enabled		215		CoreN
CM _{FLASH/MHz}	CoreMark per MHz, running from flash, cache enabled		3.36		CoreN
					MHz
CM _{FLASH/mA}	CoreMark per mA, running from flash, cache enabled, DCDC 3V		58		CoreN
					mA

7.3 CPU and support module configuration

The ARM® Cortex®-M4 processor has a number of CPU options and support modules implemented on the device.

Option / Module	Description	Implemented
Core options		
NVIC	Nested Vector Interrupt Controller	37 vectors
PRIORITIES	Priority bits	3
WIC	Wakeup Interrupt Controller	NO
Endianness	Memory system endianness	Little endian
Bit Banding	Bit banded memory	NO
DWT	Data Watchpoint and Trace	YES
SysTick	System tick timer	YES
Modules		
MPU	Memory protection unit	YES
FPU	Floating point unit	YES
DAP	Debug Access Port	YES
ETM	Embedded Trace Macrocell	YES
ITM	Instrumentation Trace Macrocell	YES
TPIU	Trace Port Interface Unit	YES
ETB	Embedded Trace Buffer	NO
FPB	Flash Patch and Breakpoint Unit	YES
HTM	AHB Trace Macrocell	NO

⁵ Using IAR v6.50.1.4452 with flags --endian=little --cpu=Cortex-M4 -e --fpu=VFPv4_sp -Ohs --no_size_constraints



8 Memory

The nRF52832 contains flash and RAM that can be used for code and data storage.

The amount of RAM and flash will vary depending on variant, see Table 9: Memory variants on page 23.

Table 9: Memory variants

Device name	RAM	Flash	Comments
nRF52832-QFAA	64 kB	512 kB	
nRF52832-QFAB	32 kB	256 kB	
nRF52832-CIAA	64 kB	512 kB	

The CPU and the EasyDMA can access memory via the AHB multilayer interconnect. The CPU is also able to access peripherals via the AHB multilayer interconnect, as illustrated in *Figure 4: Memory layout* on page 23.

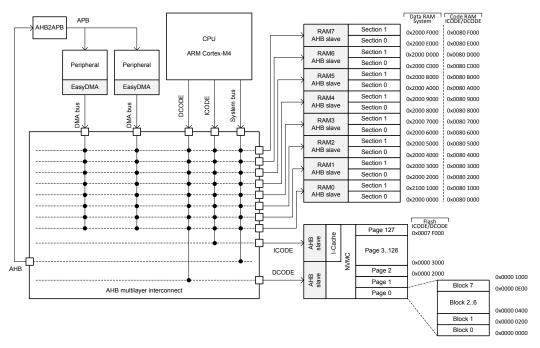


Figure 4: Memory layout

See *AHB multilayer* on page 26 and *EasyDMA* on page 27 for more information about the AHB multilayer interconnect and the EasyDMA.

The same physical RAM is mapped to both the Data RAM region and the Code RAM region. It is up to the application to partition the RAM within these regions so that one does not corrupt the other.

8.1 RAM - Random access memory

The RAM interface is divided into multiple RAM AHB slaves.

Each RAM AHB slave is connected to two 4-kilobyte RAM sections, see Section 0 and Section 1 in *Figure 4: Memory layout* on page 23.

Each of the RAM sections have separate power control for System ON and System OFF mode operation, which is configured via RAM register (see the *POWER — Power supply* on page 78).



8.2 Flash - Non-volatile memory

The Flash can be read an unlimited number of times by the CPU, but it has restrictions on the number of times it can be written and erased and also on how it can be written.

Writing to Flash is managed by the Non-volatile memory controller (NVMC), see *NVMC — Non-volatile memory controller* on page 29.

The Flash is divided into multiple pages that can be accessed by the CPU via both the ICODE and DCODE buses as shown in, *Figure 4: Memory layout* on page 23. Each page is divided into 8 blocks.

8.3 Memory map

The complete memory map is shown in *Figure 5: Memory map* on page 24. As described in *Memory* on page 23, Code RAM and the Data RAM are the same physical RAM.

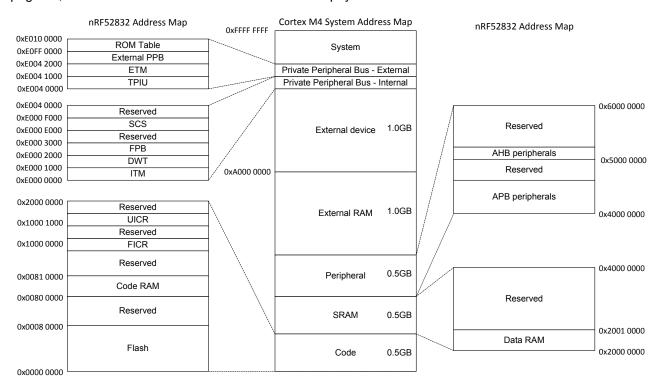


Figure 5: Memory map

8.4 Instantiation

Table 10: Instantiation table

ID	Base Address	Peripheral	Instance	Description	
0	0x40000000	CLOCK	CLOCK	Clock control	
0	0x40000000	POWER	POWER	Power control	
0	0x40000000	BPROT	BPROT	Block Protect	
1	0x40001000	RADIO	RADIO	2.4 GHz radio	
2	0x40002000	UARTE	UARTE0	Universal Asynchronous Receiver/Transmitter with EasyDMA	
2	0x40002000	UART	UART0	Universal Asynchronous Receiver/Transmitter	Deprecated
3	0x40003000	SPIM	SPIM0	SPI master 0	
3	0x40003000	SPIS	SPIS0	SPI slave 0	
3	0x40003000	TWIM	TWIM0	Two-wire interface master 0	
3	0x40003000	TWI	TWI0	Two-wire interface master 0	Deprecated
3	0x40003000	SPI	SPI0	SPI master 0	Deprecated



ID	Base Address	Peripheral	Instance	Description	
3	0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
ļ	0x40003000	SPIM	SPIM1	SPI master 1	
	0x40004000	TWI	TWI1	Two-wire interface master 1	Deprecated
	0x40004000	SPIS	SPIS1	SPI slave 1	Deprecated
	0x40004000	TWIS	TWIS1	Two-wire interface slave 1	
	0x40004000	TWIM	TWIM1	Two-wire interface master 1	
	0x40004000	SPI	SPI1	SPI master 1	Deprecated
	0x40005000	NFCT	NFCT	Near Field Communication Tag	
	0x40006000	GPIOTE	GPIOTE	GPIO Tasks and Events	
	0x40007000	SAADC	SAADC	Analog to digital converter	
	0x40008000	TIMER	TIMER0	Timer 0	
	0x40009000	TIMER	TIMER1	Timer 1	
0	0x4000A000	TIMER	TIMER2	Timer 2	
1	0x4000B000	RTC	RTC0	Real-time counter 0	
2	0x4000C000	TEMP	TEMP	Temperature sensor	
3	0x4000D000	RNG	RNG	Random number generator	
4	0x4000E000	ECB	ECB	AES Electronic Code Book (ECB) mode block encryption	
5	0x4000F000	CCM	CCM	AES CCM Mode Encryption	
5	0x4000F000	AAR	AAR	Acelerated Address Resolver	
6	0x40010000	WDT	WDT	Watchdog timer	
7	0x40011000	RTC	RTC1	Real-time counter 1	
8	0x40012000	QDEC	QDEC	Quadrature decoder	
9	0x40013000	LPCOMP	LPCOMP	Low power comparator	
9	0x40013000	COMP	COMP	General purpose comparator	
0	0x40014000	SWI	SWI0	Software interrupt 0	
0	0x40014000	EGU	EGU0	Event Generator Unit 0	
1	0x40015000	EGU	EGU1	Event Generator Unit 1	
1	0x40015000	SWI	SWI1	Software interrupt 1	
2	0x40016000	SWI	SWI2	Software interrupt 2	
2	0x40016000	EGU	EGU2	Event Generator Unit 2	
.3	0x40017000	SWI	SWI3	Software interrupt 3	
.3	0x40017000	EGU	EGU3	Event Generator Unit 3	
4	0x40018000	EGU	EGU4	Event Generator Unit 4	
4	0x40018000	SWI	SWI4	Software interrupt 4	
5	0x40019000	SWI	SWI5	Software interrupt 5	
5	0x40019000	EGU	EGU5	Event Generator Unit 5	
.6	0x40013000	TIMER	TIMER3	Timer 3	
.7	0x4001B000	TIMER	TIMER4	Timer 4	
.8		PWM			
	0x4001C000		PWM0	Pulse Width Modulation Unit 0	
9	0x4001D000	PDM	PDM	Pulse Density Modulation (Digital Microphone Interface)	
0	0x4001E000	NVMC	NVMC	Non-Volatile Memory Controller	
1	0x4001F000	PPI	PPI	Programmable Peripheral Interconnect	
2	0x40020000	MWU	MWU	Memory Watch Unit	
3	0x40021000	PWM	PWM1	Pulse Width Modulation Unit 1	
4	0x40022000	PWM	PWM2	Pulse Width Modulation Unit 2	
5	0x40023000	SPI	SPI2	SPI master 2	Deprecated
5	0x40023000	SPIS	SPIS2	SPI slave 2	
5	0x40023000	SPIM	SPIM2	SPI master 2	
6	0x40024000	RTC	RTC2	Real-time counter 2	
7	0x40025000	I2S	I2S	Inter-IC Sound Interface	
8	0x40026000	FPU	FPU	FPU interrupt	
)	0x50000000	GPIO	GPIO	General purpose input and output	Deprecated
)	0x50000000	GPIO	PO	General purpose input and output	
1/4	0x10000000	FICR	FICR	Factory Information Configuration	
N/A					



9 AHB multilayer

The CPU and all of the EasyDMAs are AHB bus masters on the AHB multilayer, while the RAM and various other modules are AHB slaves.

See *Block diagram* on page 12 for an overview of which peripherals implement EasyDMA.

The CPU has exclusive access to all AHB slaves except for the RAM that can also be accessed by the EasyDMA.

Access rights to each of the RAM AHB slaves are resolved using the priority of the different bus masters in the system

See AHB multilayer priorities on page 26 for information about the priority of the different AHB bus masters in the system. It is possible for two or more bus masters to have the same priority in cases where it is guaranteed by design that the related masters will never be able to access the same slave at the same time.

9.1 AHB multilayer priorities

Each master connected to the AHB multilayer is assigned a priority.

Table 11: AHB bus masters

Bus master name	Priority	Description
CPU	Highest priority	
SPIS1		Applies to SPIM1, SPIS1, TWIM1, TWIS1
RADIO		
CCM/ECB/AAR		
SAADC		
UARTE		
SERIALO		Applies to SPIMO, SPISO, TWIMO, TWISO
SERIAL2		Applies to SPIM2, SPIS2
NFCT		
12\$		I2S
PDM		PDM
PWM	Lowest priority	Applies to PWM0, PWM1, PWM2



10 EasyDMA

EasyDMA is an easy-to-use direct memory access module that some peripherals implement to gain direct access to Data RAM.

The EasyDMA is an AHB bus master similar to the CPU and it is connected to the AHB multilayer interconnect for direct access to the Data RAM. The EasyDMA is not able to access the Flash.

A peripheral can implement multiple EasyDMA instances, for example to provide a dedicated channel for reading data from RAM into the peripheral at the same time as a second channel is dedicated for writing data to the RAM from the peripheral. This concept is illustrated in *Figure 6: EasyDMA example* on page 27

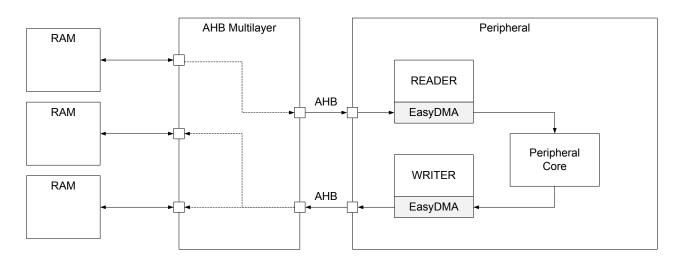


Figure 6: EasyDMA example

An EasyDMA channel is usually exposed to the user in the form illustrated below, but some variations may occur:

```
READERBUFFER_SIZE 5
WRITERBUFFER_SIZE 6

uint8_t readerBuffer[READERBUFFER_SIZE] __at__ 0x20000000;
uint8_t writerBuffer[WRITERBUFFER_SIZE] __at__ 0x20000005;

// Configuring the READER channel
MYPERIPHERAL->READER.MAXCNT = READERBUFFER_SIZE;
MYPERIPHERAL->READER.PTR = &readerBuffer;

// Configure the WRITER channel
MYPERIPHERAL->WRITER.MAXCNT = WRITEERBUFFER_SIZE;
MYPERIPHERAL->WRITER.PTR = &writerBuffer;
```

This example shows a peripheral called MYPERIPHERAL that implements two EasyDMA channels, one for reading, called READER, and one for writing, called WRITER. When the peripheral is started, it is here assumed that the peripheral will read 5 bytes from the readerBuffer located in RAM at address 0x20000000, process the data and then write no more than 6 bytes back to the writerBuffer located in RAM at address 0x20000005. The memory layout of these buffers is illustrated in *Figure 7: EasyDMA memory layout* on page 28.



0x20000000	readerBuffer[0]	readerBuffer[1]	readerBuffer[2]	readerBuffer[3]
0x20000004	readerBuffer[4]	writerBuffer[0]	writerBuffer[1]	writerBuffer[2]
0x20000008	writerBuffer[3]	writerBuffer[4]	writerBuffer[5]	

Figure 7: EasyDMA memory layout

The EasyDMA channel's MAXCNT register cannot be specified larger than the actual size of the buffer. If, for example, the WRITER.MAXCNT register is specified larger than the size of the writerBuffer, the WRITER EasyDMA channel may overflow the writerBuffer.

After the peripheral has completed the EasyDMA transfer, the CPU can read the EasyDMA channel's AMOUNT register to see how many bytes that were transferred, e.g. it is possible for the CPU to read the MYPERIPHERAL->WRITER.AMOUNT register to see how many bytes the WRITER wrote to RAM.

10.1 EasyDMA array list

The EasyDMA is able to operate in a mode called array list.

The EasyDMA array list can be represented by the data structure ArrayList_type illustrated in the code example below.

This data structure includes only a buffer with size equal to READER.MAXCNT. EasyDMA will use the READER.MAXCNT register to determine when the buffer is full.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

```
#define BUFFER_SIZE 4

typedef struct ArrayList
{
   uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type ReaderList[3];

READER.MAXCNT = BUFFER_SIZE;
READER.PTR = &ReaderList;
```

READER.PTR = &ReaderList

Ţ				
0x20000000 : ReaderList[0]	buffer[0]	buffer[1]	buffer[2]	buffer[3]
0x20000004 : ReaderList[1]	buffer[0]	buffer[1]	buffer[2]	buffer[3]
0x20000008 : ReaderList[2]	buffer[0]	buffer[1]	buffer[2]	buffer[3]

Figure 8: EasyDMA array list



11 NVMC — Non-volatile memory controller

The Non-volatile memory controller (NVMC) is used for writing and erasing the internal Flash memory and the UICR.

Before a write can be performed, the NVMC must be enabled for writing in CONFIG.WEN. Similarly, before an erase can be performed, the NVMC must be enabled for erasing in CONFIG.EEN, see *CONFIG* on page 31. The user must make sure that writing and erasing are not enabled at the same time. Failing to do so may result in unpredictable behavior.

11.1 Writing to Flash

When writing is enabled, the Flash is written by writing a full 32-bit word to a word-aligned address in the Flash

The NVMC is only able to write '0' to bits in the Flash that are erased, that is, set to '1'. It cannot write back a bit to '1'.

As illustrated in *Memory* on page 23, the Flash is divided into multiple pages that are further divided into multiple blocks. The same block in the Flash can only be written n_{WRITE} number of times before an erase must be performed using *ERASEPAGE* or *ERASEALL*. See the memory size and organization in *Memory* on page 23 for block size.

Only full 32-bit words can be written to Flash using the NVMC interface. To write less than 32 bits to Flash, write the data as a word, and set all the bits that should remain unchanged in the word to '1'. Note that the restriction about the number of writes (see above) still applies in this case.

The time it takes to write a word to the Flash is specified by t_{WRITE} . The CPU is halted while the NVMC is writing to the Flash.

Only word-aligned writes are allowed. Byte or half-word-aligned writes will result in a hard fault.

11.2 Erasing a page in Flash

When erase is enabled, the Flash can be erased page by page using the ERASEPAGE register.

After erasing a Flash page, all bits in the page are set to '1'. The time it takes to erase a page is specified by $t_{ERASEPAGE}$. The CPU is halted while the NVMC performs the erase operation.

11.3 Writing to user information configuration registers (UICR)

User information configuration registers (UICR) are written in the same way as Flash. After UICR has been written, the new UICR configuration will only take effect after a reset.

UICR can only be written n_{WRITE} number of times before an erase must be performed using ERASEUICR or ERASEALL.

The time it takes to write a word to the UICR is specified by t_{WRITE} . The CPU is halted while the NVMC is writing to the UICR.

11.4 Erasing user information configuration registers (UICR)

When erase is enabled, UICR can be erased using the ERASEUICR register.

After erasing UICR all bits in UICR are set to '1'. The time it takes to erase UICR is specified by $t_{ERASEPAGE}$. The CPU is halted while the NVMC performs the erase operation.



11.5 Erase all

When erase is enabled, the whole Flash and UICR can be erased in one operation by using the ERASEALL register. ERASEALL will not erase the factory information configuration registers (FICR).

The time it takes to perform an ERASEALL command is specified by $t_{ERASEALL}$ The CPU is halted while the NVMC performs the erase operation.

11.6 Cache

An instruction cache (I-Cache) can be enabled for the ICODE bus in the NVMC.

See the Memory map in *Memory map* on page 24 for the location of Flash.

A cache hit is an instruction fetch from the cache, and it has a 0 wait-state delay. The number of wait-states for a cache miss, where the instruction is not available in the cache and needs to be fetched from Flash, depends on the processor frequency and is shown in *CPU* on page 21

Enabling the cache can increase CPU performance and reduce power consumption by reducing the number of wait cycles and the number of flash accesses. This will depend on the cache hit rate. Cache will use some current when enabled. If the reduction in average current due to reduced flash accesses is larger than the cache power requirement, the average current to execute the program code will reduce.

When disabled, the cache does not use current and does not retain its content.

It is possible to enable cache profiling to analyze the performance of the cache for your program using the *ICACHECNF* register. When profiling is enabled, the *IHIT* and *IMISS* registers are incremented for every instruction cache hit or miss respectively. The hit and miss profiling registers do not wrap around after reaching the maximum value. If the maximum value is reached, consider profiling for a shorter duration to get correct numbers.

11.7 Registers

Table 12: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001E000	NVMC	NVMC	Non-Volatile Memory Controller	

Table 13: Register Overview

Register	Offset	Description	
READY	0x400	Ready flag	
CONFIG	0x504	Configuration register	
ERASEPAGE	0x508	Register for erasing a page in Code area	
ERASEPCR1	0x508	Register for erasing a page in Code area. Equivalent to ERASEPAGE.	Deprecated
ERASEALL	0x50C	Register for erasing all non-volatile user memory	
ERASEPCR0	0x510	Register for erasing a page in Code area. Equivalent to ERASEPAGE.	Deprecated
ERASEUICR	0x514	Register for erasing User Information Configuration Registers	
ICACHECNF	0x540	I-Code cache configuration register.	
IHIT	0x548	I-Code cache hit counter.	
IMISS	0x54C	I-Code cache miss counter.	

11.7.1 READY

Address offset: 0x400

Ready flag



Bit	numbe	er		31 3	30 29	9 28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14 :	13 :	12 1	111	0 9	8	7	6	5	4	3	2	1 0
Id																																Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe						De	scri	ipti	on																		
Α	R	READY									ΝV	MC	C is	read	dy c	or bu	ısy															
			Busy	0							ΝV	MC	C is	bus	y (o	n-g	oin	g w	rite	or	era	se c	per	atio	n)							
			Ready	1							ΝV	MC	C is	read	dy																	

11.7.2 **CONFIG**

Address offset: 0x504 Configuration register

Bit number	31	30 29 28 2	7 26 25	24	23 22	21	20	19 1	8 17	16	15	14 1	13 1	2 11	. 10	9	8	7	6	5 -	4 3	2	1 0
Id																							A A
Reset 0x00000000	0	0 0 0 0	0 0	0	0 0	0	0	0 (0 0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0 0
Id RW Field Value	ue Id Val	lue			Descr	iptic	on																
A RW WEN					Progr	am r	nen	nory	acc	ess i	nod	le. It	is s	tron	gly r	ecc	mm	nen	ded				
				1	to on	ly ac	tiva	te e	rase	and	wri	te n	node	s w	hen	the	y ar	e a	ctiv	ely			
					used.	Enal	blin	g wr	ite c	r er	ase	will	inva	lida	te th	ne c	ach	e a	nd k	eep)		
				i	it inva	alida	ted.																
Ren	0				Read	only	acc	ess															
Wei	n 1			,	Write	Ena	ble	d															
Een	2				Erase	enal	bled	t															

11.7.3 ERASEPAGE

Address offset: 0x508

Register for erasing a page in Code area

Bit	numbe	er		31	30	29	28 2	27 :	26 2	25	24 2	3 2	2 21	20	19	18	17 :	16	15 1	14 1	13 1	2 11	. 10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	A A	A	Α /	4 Δ	A A	Α	Α	Α	Α	Α	Α	Α.	A A	A	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0 (0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						0)esc	ripti	ion																		
Α	RW	ERASEPAGE									R	legis	ster	for	star	ting	g era	ise	of a	ра	ge ir	ı Co	de a	rea								
											Т	he v	valu	e is	the	ado	res	s to	the	e pa	ge t	o be	era	sed	l. (A	ddı	ress	es (of			
											f	irst v	wor	d in	pag	ge).	Not	e tl	hat	cod	e er	ase	has	to b	e e	nab	oled	by				
											C	ON	FIG.I	EEN	bet	fore	the	pa	ige (can	be e	erase	ed. A	Atte	mp	ts t	o er	rase	e			
											р	age	s th	at a	re o	uts	ide 1	the	coc	le a	rea	may	res	ult i	in u	nde	esira	able	è			
											b	eha	viou	ır, e	.g. t	the	wro	ng	pag	e m	ay b	e ei	ase	d.								

11.7.4 ERASEPCR1 (Deprecated)

Address offset: 0x508

Register for erasing a page in Code area. Equivalent to ERASEPAGE.

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 1	l7 1	.6 1	5 14	4 1	3 12	11	. 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 4	Δ Δ	Α Α	A	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	ERASEPCR1										Re	giste	er fo	or e	ras	ing	а ра	ige i	in C	ode	are	a. I	Equi	vale	ent	to						

ERASEPAGE.

11.7.5 ERASEALL

Address offset: 0x50C

Register for erasing all non-volatile user memory



Bit	numbe	er		31	L 30	29	28	3 27	7 26	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	:						De	escr	ipti	on																				
Α	RW	ERASEALL										Er	ase	all	non	ı-vo	lati	le r	ner	nor	y in	clu	ding	y UI	CR	reg	iste	rs.	Not	te					
												th	at c	ode	er	ase	has	s to	be	ena	able	d b	у С	ONI	IG.	EEI	N b	efo	re t	he					
												UI	CR	can	be	era	sed	l.																	
			NoOperation	0								No	o op	era	tio	n																			
			Erase	1								St	art	chip	er	ase																			

11.7.6 ERASEPCR0 (Deprecated)

Address offset: 0x510

Register for erasing a page in Code area. Equivalent to ERASEPAGE.

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A A	\ <i>A</i>	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	۱ ۸	4 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW ERASEPCRO											Reg	iste	r fo	r sta	arti	ng e	rase	e of	ар	age	in (Cod	e aı	rea	. Eq	uiv	aleı	nt t	0			
												ER/	SEP	ÞΑG	F																		

11.7.7 ERASEUICR

Address offset: 0x514

Register for erasing User Information Configuration Registers

Bit r	iumbe	r		31	1 30	29	28	3 27	7 20	6 25	5 24	1 23	3 2:	2 2	1 2	0 1	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																				Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							D	esc	rip	tio	n																				
Α	RW	ERASEUICR										Re	egis	ster	rst	arti	ng	era	se	of	all	Use	r Ir	for	ma	tior	Co	nfig	gura	atio	n					
												Re	egis	ster	rs. I	Vot	e t	hat	cc	de	era	se	has	to	be	ena	ble	d by	/							
												C	INC	FIG	.EE	N Ł	efo	ore	th	e U	ICF	ca	n b	e e	ase	ed.										
			NoOperation	0								N	0 0	per	rati	on																				
			Erase	1								St	art	era	ase	of	UIC	CR																		

11.7.8 ICACHECNF

Address offset: 0x540

I-Code cache configuration register.

Bit	numbe	er		31	1 30	29	28	8 27	7 2	6 25	5 2	4 2	3 2	2 2	1 2	0 1	19 1	18 :	17	16	15	14	13	12	11	10	9	8	7 (5 5	4	3	2	1	0
Id																												В							Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	() () () (0) (0	0	0	0	0	0	0	0	0	0	0	0 () (0	C	0	0	0	0
Id	RW	Field	Value Id	Va	alue							C	esc	rip	tior	1																			
Α	RW	CACHEEN										C	ach	e e	nak	le																			
			Disabled	0								C	isal	ole	cac	he.	. In	vali	da	es	all	cac	he (ent	ries										
			Enabled	1								Е	nab	le d	cacl	ne																			
В	RW	CACHEPROFEN										C	ach	e p	rof	ilin	g e	nak	ole																
			Disabled	0								C	isal	ole	cac	he	pro	ofili	ng																
			Enabled	1								E	nab	le d	cacl	ne	pro	filir	ng																

11.7.9 IHIT

Address offset: 0x548
I-Code cache hit counter.



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0						
Id	A A A A A A A A A A A A A A A A A A A						
Reset 0x00000000	$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$						
Id RW Field Value Id	Value Description						
A RW HITS	Number of cache hits						

11.7.10 IMISS

Address offset: 0x54C

I-Code cache miss counter.

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 :	13	12	11 :	LO	9	8	7	6	5	4	3	2 :	1 0)
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 /	ΑА	
Re	set 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				ı
Α	RW	MISSES										Nu	mbe	er o	of ca	che	e m	isse	:S																٦.

11.8 Electrical specification

11.8.1 Flash programming

Symbol	Description	Min.	Typ. N	lax. U	Inits
n _{WRITE,BLOCK}	Amount of writes allowed in a block between erase		18	81	
t _{WRITE}	Time to write one word	67.5	3:	38 μ	.S
t _{ERASEPAGE}	Time to erase one page	2.05	8	9.7 m	ns
t _{ERASEALL}	Time to erase all flash	6.72	2:	95.3 m	ns

11.8.2 Cache size

Symbol	Description	Min.	Тур.	Max.	Units
Size _{ICODE}	I-Code cache size		2048		Bytes



12 BPROT — Block protection

The mechanism for protecting non-volatile memory can be used to prevent application code from erasing or writing to protected blocks.

Non-volatile memory can be protected from erases and writes depending on the settings in the CONFIG registers. One bit in a CONFIG register represents one protected block of 4 kB. There are four CONFIG registers of 32 bits, which means there are 128 protectable blocks in total.

Important: If an erase or write to a protected block is detected, the CPU will hard fault. If an ERASEALL operation is attempted from the CPU while any block is protected, it will be blocked and the CPU will hard fault.

On reset, all the protection bits are cleared. To ensure safe operation, the first task after reset must be to set the protection bits. The only way of clearing protection bits is by resetting the device from any reset source.

The protection mechanism is turned off when in debug interface mode (a debugger is connected) and the DISABLEINDEBUG register is set to disable. For more information, see *Debug and trace* on page 72.

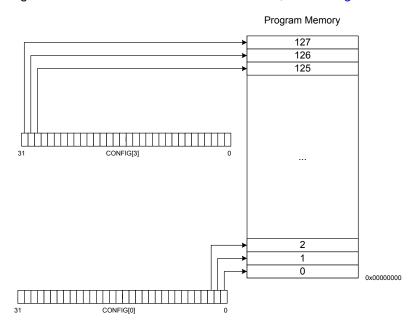


Figure 9: Protected regions of program memory

12.1 Registers

Table 14: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40000000	BPROT	BPROT	Block Protect		

Table 15: Register Overview

Register	Offset	Description	
CONFIG0	0x600	Block protect configuration register 0	
CONFIG1	0x604	Block protect configuration register 1	
DISABLEINDEBUG	0x608	Disable protection mechanism in debug interface mode	
	0x60C		Reserved
CONFIG2	0x610	Block protect configuration register 2	
CONFIG3	0x614	Block protect configuration register 3	



12.1.1 CONFIG0

Address offset: 0x600

Block protect configuration register 0

	numbe	er 							23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	-+ OO	0000000							X W V U T S R Q P O N M L K J I H G F E D C B A 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	0 0 Value	0 0	U	0 0	U	Description
A		REGION0	value lu	value					Enable protection for region 0. Write '0' has no effect.
^	11.00	REGIONO	Disabled	0					Protection disabled
			Enabled	1					Protection enable
В	D\A/	REGION1	Lilabled	_					Enable protection for region 1. Write '0' has no effect.
Ь	NVV	REGIONI	Disabled	0					Protection disabled
			Enabled	1					Protection disabled Protection enable
С	D\A/	REGION2	Lilabled	1					Enable protection for region 2. Write '0' has no effect.
C	NVV	REGIONZ	Disabled	0					Protection disabled
			Enabled	1					Protection disabled Protection enable
D	D\A/	REGION3	Eliablea	1					
U	KVV	REGIONS	6: 11.1	_					Enable protection for region 3. Write '0' has no effect.
			Disabled	0					Protection disabled
_	5111		Enabled	1					Protection enable
E	RW	REGION4	S. 11.1						Enable protection for region 4. Write '0' has no effect.
			Disabled	0					Protection disabled
_			Enabled	1					Protection enable
F	RW	REGION5							Enable protection for region 5. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
G	RW	REGION6							Enable protection for region 6. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
Н	RW	REGION7							Enable protection for region 7. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
I	RW	REGION8							Enable protection for region 8. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
J	RW	REGION9							Enable protection for region 9. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
K	RW	REGION10							Enable protection for region 10. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
L	RW	REGION11							Enable protection for region 11. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
M	RW	REGION12							Enable protection for region 12. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
N	RW	REGION13							Enable protection for region 13. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
0	RW	REGION14							Enable protection for region 14. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
Р	RW	REGION15							Enable protection for region 15. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
Q	RW	REGION16							Enable protection for region 16. Write '0' has no effect.



Bit r	iumbe	er		31 30	29 28	3 27 :	26 25	24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b	a Z	Υ	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0	0000000		0 0	0 0	0	0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			Enabled	1					Protection enable
R	RW	REGION17							Enable protection for region 17. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
S	RW	REGION18							Enable protection for region 18. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
Т	RW	REGION19							Enable protection for region 19. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
U	RW	REGION20							Enable protection for region 20. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
V	RW	REGION21		_					Enable protection for region 21. Write '0' has no effect.
			Disabled	0					Protection disabled
		250,0110	Enabled	1					Protection enable
W	RW	REGION22	5						Enable protection for region 22. Write '0' has no effect.
			Disabled	0					Protection disabled
v	DIM	DECIONAL	Enabled	1					Protection enable
X	KW	REGION23	Disabled	0					Enable protection for region 23. Write '0' has no effect.
			Disabled Enabled	0					Protection disabled
Υ	D\A/	REGION24	Enabled	1					Protection enable
,	NVV	REGION24	Disabled	0					Enable protection for region 24. Write '0' has no effect. Protection disabled
			Enabled	1					Protection enable
Z	RW/	REGION25	Lilabica	_					Enable protection for region 25. Write '0' has no effect.
-		REGIONES	Disabled	0					Protection disabled
			Enabled	1					Protection enable
а	RW	REGION26	Lindoica	-					Enable protection for region 26. Write '0' has no effect.
ŭ			Disabled	0					Protection disabled
			Enabled	1					Protection enable
b	RW	REGION27							Enable protection for region 27. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
С	RW	REGION28							Enable protection for region 28. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
d	RW	REGION29							Enable protection for region 29. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
e	RW	REGION30							Enable protection for region 30. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable
f	RW	REGION31							Enable protection for region 31. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enable

12.1.2 CONFIG1

Address offset: 0x604

Block protect configuration register 1



Protection disabled Protection disabled Protection for region 35, write '0' has no effect. Protection enabled Protection for region 35, write '0' has no effect. Protection enabled Protection for region 36, write '0' has no effect. Protection disabled Protection for region 36, write '0' has no effect. Protection disabled Protection for region 37, write '0' has no effect. Protection enabled Protection enabled Protection for region 37, write '0' has no effect. Protection enabled	Bit r	umbe	r		31 30	29 28	27 2	6 25 :	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
No. Michael Value Valu	Id				f e	d c	b a	a Z	Y X W V U T S R Q P O N M L K J I H G F E D C B A
No. No. No. Commonweal	Rese	t 0x0	0000000		0 0	0 0	0 (0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Basiline	Id	RW	Field	Value Id	Value				Description
Feather Feat	Α	RW	REGION32						Enable protection for region 32. Write '0' has no effect.
B NW REGION33				Disabled	0				Protection disabled
Protection disabled				Enabled	1				Protection enabled
Recipion Protection enabled Protection for region 34, write 0' has no effect. Enabled Enabled Protection for region 34, write 0' has no effect. Enabled Protection for region 35, write 0' has no effect. Protection for region 35, write 0' has no effect. Protection for region 35, write 0' has no effect. Protection for region 35, write 0' has no effect. Protection for region 36, write 0' has no effect. Protection for region 36, write 0' has no effect. Protection for region 36, write 0' has no effect. Protection for region 36, write 0' has no effect. Protection for region 36, write 0' has no effect. Protection for region 37, write 0' has no effect. Protection for region 37, write 0' has no effect. Protection for region 37, write 0' has no effect. Protection for region 38, write 0' has no effect. Protection for region 38, write 0' has no effect. Protection for region 38, write 0' has no effect. Protection for region 38, write 0' has no effect. Protection for region 38, write 0' has no effect. Protection for region 39, write 0' has no effect. Protection for region 39, write 0' has no effect. Protection for region 39, write 0' has no effect. Protection for region 39, write 0' has no effect. Protection for region 40, write 0' has no effect. Protection for region 40, write 0' has no effect. Protection for region 40, write 0' has no effect. Protection for region 41, write 0' has no effect. Protection for region 41, write 0' has no effect. Protection for region 41, write 0' has no effect. Protection for region 41, write 0' has no effect. Protection for region 41, write 0' has no effect. Protection for region 41, write 0' has no effect. Protection for region 41, write 0' has no effect. Protection for region 41, write 0' has no effect. Protection for region 41, write 0' has no effect. Protection for region 41, write 0' has no effect. Protection for region 41, write 0' has no effect. Protection for region 41, write 0' has no effect. Protec	В	RW	REGION33						Enable protection for region 33. Write '0' has no effect.
CR RW REGION34 Doubled 0 Protection of region 34. Write 0' has no effect. D NW REGION35 Cabled 1 Protection of no region 35. Write 0' has no effect. D NW REGION36 Deabled 0 Protection of region 35. Write 0' has no effect. F RW REGION36 Fabled 1 Protection enabled protection for region 36. Write 0' has no effect. F RW REGION37 Disabled 0 Protection enabled protection for region 37. Write 0' has no effect. F RW REGION38 Disabled 0 Protection enabled for region 37. Write 0' has no effect. G RW REGION38 Finalled 1 Protection enabled for region 38. Write 0' has no effect. G RW REGION39 Disabled 0 Protection disabled for region 38. Write 0' has no effect. H RW REGION39 Enabled 0 Protection disabled for region 39. Write 0' has no effect. H RW REGION39 Enabled 1 Protection disabled for region 39. Write 0' has no effect. Disabled 0 Protection disabled for region 39. Write 0' has no effect. R RW REGION41 Enabled 1 Protection disabled for region 39. Write 0' has no effect. D				Disabled	0				Protection disabled
Protection disabled Protection disabled Protection disabled Protection disabled Protection for region 35. Write '0' has no effect.				Enabled	1				Protection enabled
Red	С	RW	REGION34						Enable protection for region 34. Write '0' has no effect.
No. Part				Disabled	0				Protection disabled
Figure Protection disabled Protection disabled Protection disabled Protection disabled Protection disabled Protection for region 36. Write '0' has no effect. Protection disabled Protection for region 36. Write '0' has no effect. Protection disabled Protection for region 37. Write '0' has no effect. Protection disabled Protection for region 37. Write '0' has no effect. Protection disabled Protection for region 38. Write '0' has no effect. Protection disabled Protection for region 38. Write '0' has no effect. Protection disabled P				Enabled	1				Protection enabled
Figure F	D	RW	REGION35						Enable protection for region 35. Write '0' has no effect.
E RW REGION36 Usabled (anabled) Enable protection for region 36. Write '0' has no effect. F RW REGION37 Enabled 1 Protection enabled F RW REGION37 Disabled 0 Protection enabled G RW REGION38 Enabled 1 Protection enabled G RW REGION38 Enabled 1 Protection of disabled G RW REGION39 Enabled 1 Protection enabled G REGION39 Enabled 0 Protection enabled G RW REGION40 1 Protection disabled G Disabled 0 Protection disabled G Disabled 0 Protection disabled G RW REGION41 Enable protection for region 41. Write '0' has no effect. G Protection disabled 0 Protection disabled G Protection disabled 0 Protection disabled G Protection disabled 0 </td <td></td> <td></td> <td></td> <td>Disabled</td> <td>0</td> <td></td> <td></td> <td></td> <td>Protection disabled</td>				Disabled	0				Protection disabled
				Enabled	1				Protection enabled
Figure F	Е	RW	REGION36						Enable protection for region 36. Write '0' has no effect.
Figure F				Disabled	0				Protection disabled
Protection disabled				Enabled	1				Protection enabled
Figure F	F	RW	REGION37						Enable protection for region 37. Write '0' has no effect.
G RW REGION38 Disabled 0 Protection disabled H RW REGION39 — Enabled 1 Protection disabled H RW REGION39 — Enabled 0 Protection disabled I RW REGION40 — Enabled 1 Protection disabled I RW REGION40 — Enabled 0 Protection disabled J RW REGION41 — Enabled 1 Protection disabled J RW REGION41 — Enabled 1 Protection disabled J RW REGION42 — Enabled 1 Protection disabled K RW REGION42 — Enable protection for region 42. Write '0' has no effect. L Disabled 0 Protection enabled Enabled 1 Protection for region 42. Write '0' has no effect. Disabled 0 Protection for region 43. Write '0' has no effect. Disabled 0 Protection enabled Enable protection for region 44. Write '0' ha				Disabled	0				Protection disabled
				Enabled	1				Protection enabled
	G	RW	REGION38						Enable protection for region 38. Write '0' has no effect.
RW REGION39				Disabled	0				Protection disabled
				Enabled	1				Protection enabled
RW REGION40 REGION42 Enabled 1 Protection enabled 1 Protection enabled 1 Protection enabled 1 Protection disabled 1 Protection enabled 1 Prote	Н	RW	REGION39						Enable protection for region 39. Write '0' has no effect.
RW REGION40				Disabled	0				Protection disabled
Disabled				Enabled	1				Protection enabled
Red Protection enabled Protection for region 41. Write '0' has no effect. Protection for region 41. Write '0' has no effect. Protection disabled Protection disabled Protection for region 42. Write '0' has no effect. Protection disabled Protection for region 42. Write '0' has no effect. Protection for region 42. Write '0' has no effect. Protection enabled Protection for region 43. Write '0' has no effect. Protection for region 43. Write '0' has no effect. Protection for region 44. Write '0' has no effect. Protection for region 45. Write '0' has no effect. Protection for region 45. Write '0' has no effect. Protection for region 44. Write '0' has no effect. Protection for region 45. Write '0' has no effect. Protection enabled Protection for region 45. Write '0' has no effect. Protection enabled Protection for region 45. Write '0' has no effect. Protection enabled Protection for region 46. Write '0' has no effect. Protection enabled Protection for region 46. Write '0' has no effect. Protection enabled Protection enabled Protection for region 47. Write '0' has no effect. Protection enabled Protection enabled Protection enabled Protection for region 47. Write '0' has no effect. Protection enabled Protection for region 48. Write '0' has no effect. Protection enabled Protection enabled Protection enabled Protection for region 49. Write '0' has no effect. Protection enabled Protection enabled Protection for region 49. Write '0' has no effect. Protection enabled	I	RW	REGION40						Enable protection for region 40. Write '0' has no effect.
Regional Disabled				Disabled	0				Protection disabled
Disabled				Enabled	1				Protection enabled
R RW REGION42 Protection enabled R RW REGION42 Disabled 0 Protection disabled Enable protection for region 42. Write '0' has no effect. Protection enabled R RW REGION43 Disabled 0 Protection enabled Enable protection for region 43. Write '0' has no effect. Disabled 0 Protection enabled Enable protection for region 43. Write '0' has no effect. Disabled 0 Protection enabled Enable protection for region 44. Write '0' has no effect. Disabled 0 Protection disabled Enable protection for region 44. Write '0' has no effect. Disabled 0 Protection enabled Protection enabled N RW REGION45 Enable Protection for region 45. Write '0' has no effect. Disabled 0 Protection enabled Protection disabled Enable Protection for region 46. Write '0' has no effect. Disabled 0 Protection disabled Protection disabled Protection disabled Protection for region 46. Write '0' has no effect. Protection enabled N REGION47 Enable Protection for region 47. Write '0' has no effect. Disabled 0 Protection disabled Protection disabled Protection disabled Protection for region 48. Write '0' has no effect. Protection disabled Protection disabled Protection for region 48. Write '0' has no effect. Enable protection for region 48. Write '0' has no effect. Protection enabled R RW REGION49 Enabled 0 Protection enabled R RW REGION49 Enabled 0 Protection for region 48. Write '0' has no effect. Enable protection for region 48. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49.	J	RW	REGION41						Enable protection for region 41. Write '0' has no effect.
K RW REGION42 Disabled 0 Protection for region 42. Write '0' has no effect. Disabled 0 Protection disabled Enabled 1 Protection enabled K RW REGION43 Disabled 0 Protection infor region 43. Write '0' has no effect. Disabled 1 Protection enabled M RW REGION44 Disabled 1 Protection enabled M RW REGION44 Disabled 0 Protection for region 44. Write '0' has no effect. Disabled 0 Protection for region 44. Write '0' has no effect. Disabled 0 Protection for region 45. Write '0' has no effect. Disabled 1 Protection for region 45. Write '0' has no effect. Disabled 0 Protection for region 46. Write '0' has no effect. Disabled 0 Protection disabled Enabled 1 Protection enabled Protection disabled Disabled 0 Protection disabled Enabled 1 Protection enabled Protection disabled Disabled 0 Protection disabled Disabled 0 Protection for region 46. Write '0' has no effect. Disabled 0 Protection disabled Protection enabled Protection enabled Protection enabled Disabled 0 Protection for region 47. Write '0' has no effect. Disabled 0 Protection for region 48. Write '0' has no effect. Disabled 0 Protection enabled Protection enabled R RW REGION49 REGION40 REGIO				Disabled	0				Protection disabled
Disabled Disabled Disabled Protection disabled				Enabled	1				Protection enabled
Enabled 1 Protection enabled Enable Protection for region 43. Write '0' has no effect. Disabled 0 Protection disabled Enabled 1 Protection enabled From Protection enabled Protection enabled Protection enabled Protection for region 44. Write '0' has no effect. Disabled 0 Protection disabled Enabled 1 Protection enabled Protection disabled Enabled 1 Protection enabled Protection disabled Enabled 1 Protection enabled Protection enabled Protection disabled Enabled 1 Protection enabled Protection enabled Protection enabled Protection enabled Protection for region 47. Write '0' has no effect. Protection enabled	K	RW	REGION42						Enable protection for region 42. Write '0' has no effect.
E RW REGION43 Protection for region 43. Write '0' has no effect.				Disabled	0				Protection disabled
Protection disabled Enabled Protection enabled Protection for region 44. Write '0' has no effect. Enable protection for region 44. Write '0' has no effect. Enable protection for region 45. Write '0' has no effect. Enable protection for region 45. Write '0' has no effect. Enable protection for region 45. Write '0' has no effect. Enable protection for region 45. Write '0' has no effect. Enable protection disabled Enable protection for region 46. Write '0' has no effect. Enable protection for region 46. Write '0' has no effect. Enable protection for region 46. Write '0' has no effect. Enable protection for region 47. Write '0' has no effect. Enable protection for region 47. Write '0' has no effect. Enable protection for region 48. Write '0' has no effect. Enable protection for region 48. Write '0' has no effect. Enable protection for region 48. Write '0' has no effect. Enable protection for region 48. Write '0' has no effect. Enable protection for region 48. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Enable protection for region				Enabled	1				Protection enabled
R RW REGION44 REGION44 REGION45 REGION46 REGION46 REGION47 REGION48 REGION48 REGION48 REGION49 REGION48 REGION49 REGION4	L	RW	REGION43						Enable protection for region 43. Write '0' has no effect.
RW REGION44 Protection for region 44. Write '0' has no effect. Disabled Disabled				Disabled	0				Protection disabled
Disabled 0 Protection disabled Enabled 1 Protection enabled RW REGION45 Disabled 0 Protection enabled Disabled 0 Protection disabled Enable protection for region 45. Write '0' has no effect. Disabled 0 Protection enabled Disabled 1 Protection enabled Disabled 0 Protection disabled Enable protection for region 46. Write '0' has no effect. Disabled 0 Protection disabled Enable protection for region 47. Write '0' has no effect. Disabled 1 Protection enabled Protection disabled Enable protection for region 47. Write '0' has no effect. Disabled 1 Protection disabled Enable protection for region 48. Write '0' has no effect. Enable protection for region 48. Write '0' has no effect. Disabled 0 Protection disabled Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Protection enabled Enable Protection for region 49. Write '0' has no effect. Protection enabled Enable Protection for region 49. Write '0' has no effect. Protection enabled Enable Protection for region 49. Write '0' has no effect. Protection enabled Enable Protection for region 49. Write '0' has no effect. Protection enabled				Enabled	1				Protection enabled
RW REGION45 RW REGION45 RW REGION46 RW REGION47 RW REGION47 RW REGION47 RW REGION47 RW REGION47 RW REGION48 RW REGION48 REGION48 RW REGION48 REGION48 REGION48 REGION48 REGION48 REGION49 RW REGION49 REGION40	М	RW	REGION44						Enable protection for region 44. Write '0' has no effect.
RW REGION45 REGION45				Disabled	0				Protection disabled
Disabled 0 Protection disabled Protection enabled RW REGION46 Enabled 0 Protection enabled Disabled 0 Protection enabled Enabled 0 Protection for region 46. Write '0' has no effect. Disabled 0 Protection enabled Enabled 1 Protection enabled REGION47 Enabled 0 Protection for region 47. Write '0' has no effect. Disabled 0 Protection disabled Enable protection for region 47. Write '0' has no effect. Protection enabled Enable protection for region 48. Write '0' has no effect. Enable protection for region 48. Write '0' has no effect. Disabled 0 Protection disabled Enable protection for region 49. Write '0' has no effect. Enable protection enabled R REGION49 Enabled 0 Protection for region 49. Write '0' has no effect. Disabled 0 Protection enabled				Enabled	1				Protection enabled
Enabled 1 Protection enabled Protection enabled Enable protection for region 46. Write '0' has no effect. Enable protection disabled Protection enabled Protection enabled Protection enabled Protection enabled Protection for region 47. Write '0' has no effect. Enable protection for region 47. Write '0' has no effect. Disabled Disabled 1 Protection enabled Protection enabled Enable protection for region 48. Write '0' has no effect. Enable protection for region 48. Write '0' has no effect. Disabled Disabled 1 Protection disabled Protection enabled R REGION49 Enable protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Protection enabled Protection disabled Protection disabled Protection disabled Protection disabled Protection enabled	N	RW	REGION45						Enable protection for region 45. Write '0' has no effect.
P RW REGION46 Disabled 0 Protection for region 46. Write '0' has no effect. Disabled 0 Protection disabled Enabled 1 Protection enabled Protection enabled Enable protection for region 47. Write '0' has no effect. Disabled 0 Protection disabled Enabled 1 Protection enabled Protection enabled Enable protection for region 47. Write '0' has no effect. Disabled 0 Protection enabled Enable protection for region 48. Write '0' has no effect. Disabled 0 Protection disabled Enable Protection enabled Enable Protection enabled Enable Protection for region 49. Write '0' has no effect. Protection enabled Enable Protection disabled Enable Protection enabled				Disabled	0				Protection disabled
Disabled 0 Protection disabled Protection disabled Enabled 1 Protection enabled P RW REGION47 Enabled 0 Protection for region 47. Write '0' has no effect. Disabled 0 Protection disabled Protection for region 47. Write '0' has no effect. Enable protection enabled Enabled 1 Protection enabled Enable protection for region 48. Write '0' has no effect. Disabled 0 Protection disabled Enabled 1 Protection enabled R RW REGION49 Enabled 0 Protection for region 49. Write '0' has no effect. Disabled 0 Protection for region 49. Write '0' has no effect. Enable protection for region 49. Write '0' has no effect. Protection disabled Enabled Protection disabled Protection disabled Protection disabled Protection disabled				Enabled	1				Protection enabled
P RW REGION47 Comparison of the company of the com	0	RW	REGION46						Enable protection for region 46. Write '0' has no effect.
P RW REGION47 Disabled 0 Protection for region 47. Write '0' has no effect. Disabled 1 Protection enabled C RW REGION48 Enabled 0 Protection for region 48. Write '0' has no effect. Disabled 0 Protection for region 48. Write '0' has no effect. Disabled 1 Protection enabled R RW REGION49 Enabled 1 Protection enabled Enable Protection for region 49. Write '0' has no effect. Protection disabled Enable Protection for region 49. Write '0' has no effect. Protection disabled Enable Protection disabled Protection disabled Protection enabled				Disabled	0				Protection disabled
Disabled 0 Protection disabled Protection disabled RW REGION48 Enabled 0 Protection enabled Enabled 0 Protection for region 48. Write '0' has no effect. Disabled 0 Protection disabled Enabled 1 Protection enabled RW REGION49 Enabled 0 Protection for region 49. Write '0' has no effect. Disabled 0 Protection for region 49. Write '0' has no effect. Protection disabled Enabled 1 Protection disabled Protection enabled				Enabled	1				Protection enabled
RW REGION48 RW REGION48 RW REGION48 RW REGION48 RW REGION49 RW REGION48 RW REGION49 RW REGION48 RW REGION49 RW REG	Р	RW	REGION47						Enable protection for region 47. Write '0' has no effect.
Q RW REGION48 Disabled 0 Protection for region 48. Write '0' has no effect. Disabled 1 Protection enabled R RW REGION49 Disabled 0 Protection for region 49. Write '0' has no effect. Protection enabled Enable protection for region 49. Write '0' has no effect. Protection disabled Enabled 1 Protection enabled				Disabled	0				Protection disabled
Disabled 0 Protection disabled Enabled 1 Protection enabled R RW REGION49 Enabled 0 Protection for region 49. Write '0' has no effect. Disabled 0 Protection disabled Enabled 1 Protection enabled				Enabled	1				Protection enabled
Enabled 1 Protection enabled R RW REGION49 Enabled 0 Protection disabled Enabled 1 Protection enabled Protection enabled Protection enabled	Q	RW	REGION48						Enable protection for region 48. Write '0' has no effect.
R RW REGION49 Enable protection for region 49. Write '0' has no effect. Disabled 0 Protection disabled Enabled 1 Protection enabled				Disabled	0				Protection disabled
Disabled 0 Protection disabled Enabled 1 Protection enabled				Enabled	1				Protection enabled
Enabled 1 Protection enabled	R	RW	REGION49						Enable protection for region 49. Write '0' has no effect.
				Disabled	0				Protection disabled
S RW REGION50 Enable protection for region 50. Write '0' has no effect.				Enabled	1				Protection enabled
	S	RW	REGION50						Enable protection for region 50. Write '0' has no effect.



Bit r	numbe	er		31 30	2 (9 28	27	26	25 2	24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id											X W V U T S R Q P O N M L K J I H G F E D C B A
	et 0x0	0000000									000000000000000000000000000000000000000
Id	RW	Field	Value Id	Value							Description
			Disabled	0							Protection disabled
			Enabled	1							Protection enabled
Т	RW	REGION51									Enable protection for region 51. Write '0' has no effect.
			Disabled	0							Protection disabled
			Enabled	1							Protection enabled
U	RW	REGION52									Enable protection for region 52. Write '0' has no effect.
			Disabled	0							Protection disabled
			Enabled	1							Protection enabled
V	RW	REGION53									Enable protection for region 53. Write '0' has no effect.
			Disabled	0							Protection disabled
			Enabled	1							Protection enabled
W	RW	REGION54									Enable protection for region 54. Write '0' has no effect.
			Disabled	0							Protection disabled
			Enabled	1							Protection enabled
Χ	RW	REGION55									Enable protection for region 55. Write '0' has no effect.
			Disabled	0							Protection disabled
			Enabled	1							Protection enabled
Υ	RW	REGION56									Enable protection for region 56. Write '0' has no effect.
			Disabled	0							Protection disabled
			Enabled	1							Protection enabled
Z	RW	REGION57									Enable protection for region 57. Write '0' has no effect.
			Disabled	0							Protection disabled
	DIA	DECIONES	Enabled	1							Protection enabled
a	RW	REGION58	Disabled	0							Enable protection for region 58. Write '0' has no effect.
			Disabled Enabled	0							Protection disabled Protection enabled
b	D\A/	REGION59	спаріец	1							Enable protection for region 59. Write '0' has no effect.
b	IVVV	REGIONSS	Disabled	0							Protection disabled
			Enabled	1							Protection enabled
С	RW	REGION60	Litablea	-							Enable protection for region 60. Write '0' has no effect.
ŭ			Disabled	0							Protection disabled
			Enabled	1							Protection enabled
d	RW	REGION61									Enable protection for region 61. Write '0' has no effect.
			Disabled	0							Protection disabled
			Enabled	1							Protection enabled
e	RW	REGION62									Enable protection for region 62. Write '0' has no effect.
			Disabled	0							Protection disabled
			Enabled	1							Protection enabled
f	RW	REGION63									Enable protection for region 63. Write '0' has no effect.
			Disabled	0							Protection disabled
			Enabled	1							Protection enabled

12.1.3 DISABLEINDEBUG

Address offset: 0x608

Disable protection mechanism in debug interface mode

Di+ +	numbe	r		31 30	20	20	27	26	25	24	22	22	21	20	10	10 1	17 -	16	16 '	14	10 1	ר 1	1 1	0 0	0	7	c	С	1	2	2	1 0
	iuiiibe	ı		31 30	25	20	21	20	23	24	23	22	21	20	15.	10.	1/.	10 .	13.	14.	15.		.1 1	0 5	0	′	O	J	4	3	2	1 0
ld																																А
Res	et 0x0	0000001		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 1
Id	RW	Field	Value Id	Value	!						De	scri	ptic	on																		
Α	RW	DISABLEINDEBUG									Dis	able	e th	ie p	rote	ectio	on i	me	cha	nisr	n fo	r N	VM	reg	ions	s wh	ile					
											in (deb	ug i	nte	rfac	e m	nod	e. 1	This	reg	giste	er w	ill c	nly	disa	ble	the	!				
											pro	otec	tior	n m	ech	anis	sm	if th	ne d	levi	ce i	s in	del	oug	inte	rfac	e n	od	e.			
			Disabled	1							Dis	able	e in	del	bug																	



Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A
Reset 0x00000001		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
	Enabled	0	Enable in debug

12.1.4 CONFIG2

Address offset: 0x610

Block protect configuration register 2

Bit	number			31 30 29	28.2	7 26 1	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	ilailibei							X W V U T S R Q P O N M L K J I H G F E D C B A
	et 0x0000	00000						0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Fi		Value Id	Value				Description
A		EGION64	14.40.14	74.40				Enable protection for region 64. Write '0' has no effect.
-			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
В	RW R	EGION65	Lindoled	-				Enable protection for region 65. Write '0' has no effect.
_		20.0.103	Disabled	0				Protection disabled
			Enabled	1				Protection enabled
С	RW/ RF	EGION66	Litablea	-				Enable protection for region 66. Write '0' has no effect.
	11.00	20101400	Disabled	0				Protection disabled
			Enabled	1				Protection disabled
D	D\A/ DI	EGION67	Enabled	1				
U	KW KI	EGIONO/	Disabled	0				Enable protection for region 67. Write '0' has no effect. Protection disabled
_	DIA/ DI	ECIONICO	Enabled	1				Protection enabled
E	KW KI	EGION68	Disabled	0				Enable protection for region 68. Write '0' has no effect.
			Disabled	0				Protection disabled
_	DIA/ DI	ECIONICO	Enabled	1				Protection enabled
F	KW KI	EGION69	Dividity I	•				Enable protection for region 69. Write '0' has no effect.
			Disabled	0				Protection disabled
_		50.01.50	Enabled	1				Protection enabled
G	RW R	EGION70						Enable protection for region 70. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
Н	RW RI	EGION71						Enable protection for region 71. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
I	RW R	EGION72						Enable protection for region 72. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
J	RW R	EGION73						Enable protection for region 73. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
K	RW R	EGION74						Enable protection for region 74. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
L	RW R	EGION75						Enable protection for region 75. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
M	RW R	EGION76						Enable protection for region 76. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
N	RW R	EGION77						Enable protection for region 77. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
0	RW R	EGION78						Enable protection for region 78. Write '0' has no effect.
			Disabled	0				Protection disabled



Rit r	numbe	r		31 30	29 2	8 27	26.7	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	idilibe								X W V U T S R Q P O N M L K J I H G F E D C B A
	et 0x0	0000000							000000000000000000000000000000000000000
Id	RW	Field	Value Id	Value					Description
			Enabled	1					Protection enabled
Р	RW	REGION79							Enable protection for region 79. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Q	RW	REGION80							Enable protection for region 80. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
R	RW	REGION81							Enable protection for region 81. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
S	RW	REGION82							Enable protection for region 82. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Т	RW	REGION83							Enable protection for region 83. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
U	RW	REGION84							Enable protection for region 84. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
٧	RW	REGION85							Enable protection for region 85. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
W	RW	REGION86							Enable protection for region 86. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Χ	RW	REGION87							Enable protection for region 87. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Υ	RW	REGION88							Enable protection for region 88. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Z	RW	REGION89							Enable protection for region 89. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
а	RW	REGION90		_					Enable protection for region 90. Write '0' has no effect.
			Disabled	0					Protection disabled
L	Direc	DECIONO1	Enabled	1					Protection enabled
b	KW	REGION91	Disabled	0					Enable protection for region 91. Write '0' has no effect.
			Disabled	0					Protection disabled
	DVA	PECIONO3	Enabled	1					Protection enabled Enable protection for region 02. Write '0' has no effect
С	KVV	REGION92	Disabled	0					Enable protection for region 92. Write '0' has no effect.
			Disabled	0					Protection disabled
d	DVA	DECIONO3	Enabled	1					Protection enabled
d	KW	REGION93	Disabled	0					Enable protection for region 93. Write '0' has no effect.
			Disabled	0					Protection disabled
	DVA	PECIONO4	Enabled	1					Protection enabled Enable protection for region 04. Write '0' has no effect.
е	ΚW	REGION94	Disabled	0					Enable protection for region 94. Write '0' has no effect.
			Disabled						Protection disabled
£	DVA	RECIONOS	Enabled	1					Protection enabled Enable protection for region 05. Write '0' has no effect.
1	KW	REGION95	Disabled	0					Enable protection for region 95. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled



12.1.5 CONFIG3

Address offset: 0x614

Block protect configuration register 3

	numbe	er							23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld Bas	-+ Ov0	0000000							X W V U T S R Q P O N M L K J I H G F E D C B A 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
res Id		Field	Value Id	0 0 Value	0 0	U	0 (0 0	Description
A		REGION96	value lu	Value					Enable protection for region 96. Write '0' has no effect.
^	11.00	REGIONSO	Disabled	0					Protection disabled
			Enabled	1					Protection disabled
D	D\A/	REGION97	Enabled	1					
В	KVV	REGION97	Disabled	0					Enable protection for region 97. Write '0' has no effect.
			Disabled	0					Protection disabled
_	DIA	DECIONOS	Enabled	1					Protection enabled
С	KVV	REGION98	Disable d	0					Enable protection for region 98. Write '0' has no effect.
			Disabled	0					Protection disabled
_		250,01100	Enabled	1					Protection enabled
D	RW	REGION99							Enable protection for region 99. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
E	RW	REGION100							Enable protection for region 100. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
F	RW	REGION101							Enable protection for region 101. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
G	RW	REGION102							Enable protection for region 102. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
H RW	RW	REGION103							Enable protection for region 103. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
I	RW	REGION104							Enable protection for region 104. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
J	RW	REGION105							Enable protection for region 105. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
K	RW	REGION106							Enable protection for region 106. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
L	RW	REGION107							Enable protection for region 107. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
М	RW	REGION108							Enable protection for region 108. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
N	RW	REGION109	Litablea	-					Enable protection for region 109. Write '0' has no effect.
		REGIONIOS	Disabled	0					Protection disabled
			Enabled	1					Protection enabled
0	D\A/	REGION110	Lilabica	-					Enable protection for region 110. Write '0' has no effect.
J	17.44	REGIONITO	Disabled	0					Protection disabled
n	DVA	DECION111	Enabled	1					Protection enabled
P	KW	REGION111	Disabled	0					Enable protection for region 111. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Q	RW	REGION112							Enable protection for region 112. Write '0' has no effect.
			Disabled	0					Protection disabled



Bitı	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Enabled	1	Protection enabled
R	RW	REGION113			Enable protection for region 113. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
S	RW	REGION114			Enable protection for region 114. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
Т	RW	REGION115			Enable protection for region 115. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
U	RW	REGION116			Enable protection for region 116. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
V	RW	REGION117			Enable protection for region 117. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
W	RW	REGION118			Enable protection for region 118. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
Х	RW	REGION119			Enable protection for region 119. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
Υ	RW	REGION120			Enable protection for region 120. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
Z	RW	REGION121			Enable protection for region 121. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
а	RW	REGION122			Enable protection for region 122. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
b	RW	REGION123			Enable protection for region 123. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
С	RW	REGION124			Enable protection for region 124. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
d	RW	REGION125			Enable protection for region 125. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
e	RW	REGION126			Enable protection for region 126. Write '0' has no effect.
-			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
f	RW	REGION127			Enable protection for region 127. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection disabled
				_	



13 FICR — Factory information configuration registers

Factory information configuration registers (FICR) are pre-programmed in factory and cannot be erased by the user. These registers contain chip-specific information and configuration.

13.1 Registers

Table 16: Instances

Base address	Peripheral	Instance	Description	Configuration
0x10000000	FICR	FICR	Factory Information Configuration	

Table 17: Register Overview

Register	Offset	Description	
CODEPAGESIZE	0x010	Code memory page size	
CODESIZE	0x014	Code memory size	
DEVICEID[0]	0x060	Device identifier	
DEVICEID[1]	0x064	Device identifier	
ER[0]	0x080	Encryption Root, word 0	
ER[1]	0x084	Encryption Root, word 1	
ER[2]	0x088	Encryption Root, word 2	
ER[3]	0x08C	Encryption Root, word 3	
IR[0]	0x090	Identity Root, word 0	
IR[1]	0x094	Identity Root, word 1	
IR[2]	0x098	Identity Root, word 2	
IR[3]	0x09C	Identity Root, word 3	
DEVICEADDRTYPE	0x0A0	Device address type	
DEVICEADDR[0]	0x0A4	Device address 0	
DEVICEADDR[1]	0x0A8	Device address 1	
INFO.PART	0x100	Part code	
INFO.VARIANT	0x104	Part Variant, Hardware version and Production configuration	
INFO.PACKAGE	0x108	Package option	
INFO.RAM	0x10C	RAM variant	
INFO.FLASH	0x110	Flash variant	
	0x114		Reserved
	0x118		Reserved
	0x11C		Reserved
TEMP.A0	0x404	Slope definition A0.	
TEMP.A1	0x408	Slope definition A1.	
TEMP.A2	0x40C	Slope definition A2.	
TEMP.A3	0x410	Slope definition A3.	
TEMP.A4	0x414	Slope definition A4.	
TEMP.A5	0x418	Slope definition A5.	
TEMP.BO	0x41C	y-intercept BO.	
TEMP.B1	0x420	y-intercept B1.	
TEMP.B2	0x424	y-intercept B2.	
TEMP.B3	0x428	y-intercept B3.	
TEMP.B4	0x42C	y-intercept B4.	
TEMP.B5	0x430	y-intercept B5.	
TEMP.TO	0x434	Segment end TO.	
TEMP.T1	0x438	Segment end T1.	
TEMP.T2	0x43C	Segment end T2.	
TEMP.T3	0x440	Segment end T3.	
TEMP.T4	0x444	Segment end T4.	



Register	Offset	Description
NFC.TAGHEADER0	0x450	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER1	0x454	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER2	0x458	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER3	0x45C	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.

13.1.1 CODEPAGESIZE

Address offset: 0x010 Code memory page size

Bit	num	ber		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Re	set O	(FFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RV	V Field	Value Id	Value Description
	_	600504655175		

A R CODEPAGESIZE Code memory page size

13.1.2 CODESIZE

Address offset: 0x014 Code memory size

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A R CODESIZE		Code memory size in number of pages

Total code space is: CODEPAGESIZE * CODESIZE

13.1.3 DEVICEID[0]

Address offset: 0x060

Device identifier

Bit	numbe	r		31	. 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15 1	14 1	.3 12	2 11	10	9 8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	А А	Α	Α	4 Α	A	Α	Α	Α	Α	Α .	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1	1 1	. 1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																	
Α	R	DEVICEID										64	bit ı	uni	que	de	vice	e ide	enti	ifier												
												DE	VICE	EID[[0]	con	tain	ıs th	ne le	east	t sig	nific	ant	oits (of th	e de	evic	e				
												ide	ntif	ier.	DE	VIC	EID	[1]	con	ntair	ns th	ne m	ost s	igni	icar	t bi	ts o	f th	e			
												de	vice	ide	enti	fier																

13.1.4 DEVICEID[1]

Address offset: 0x064

Device identifier

Bit number		31	30	29	28	3 27	7 26	25	24	23	22	21	20	19	18 1	L7 1	.6 1	5 1	4 13	12	11	10	9	8	7	6	5 4	4 3	3 2	1	0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Α,	Δ ,	A /	A A	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	A А	Α	Α
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	l 1	1	1	1	1	1	1	1	1	1 :	1 1	1	1
Id RW Field	Value Id	Va	lue							De	scri	ptic	n																		

A R DEVICEID 64 bit unique device identifier



Reset 0xFFFFFFFF 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
2 10	1 1 1 1 1 1 1 1 1 1 1 1 1
Id	. A A A A A A A A A A A
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 1	4 13 12 11 10 9 8 7 6 5 4 3 2 1 0

DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier.

13.1.5 ER[0]

Address offset: 0x080 Encryption Root, word 0

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A R FR		Encryption Root, word n

13.1.6 ER[1]

Address offset: 0x084 Encryption Root, word 1

Bit r	numbe	er		31	1 30	29	9 28	3 2	7 26	5 25	24	23	22	21	20	19	18	17 :	16	15 1	14 :	13 1	.2 1	1 10	9	8	7	6	5	4	3	2 1	. 0
Id				Α	Α	Α	. A	. Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ ,	Α Α	Α	Α	Α	Α	Α	Α	Α /	4 <i>A</i>	А
Res	et OxF	FFFFFF		1	1	1	. 1	. 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	l 1	1	1	1	1	1	1	1	1 1	. 1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	on																		
Α	R	ER										En	cryp	otio	n R	oot,	wc	ord	n														

13.1.7 ER[2]

Address offset: 0x088 Encryption Root, word 2

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value Description
A R ER		Encryption Root, word n

13.1.8 ER[3]

Address offset: 0x08C Encryption Root, word 3

Bit r	umbe	er		31	30	29	28	27	26	25	24	23 :	22 2	21 2	20 1	9 1	8 17	7 16	15	14	13	L2 1	1 1	0 9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ /	A A	Α	Α	Α	Α	Α ,	Δ Α	Δ Δ	. A	Α	Α	Α	Α	А А	Α	Α
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	l 1	1	1	1	1	1 :	1 :	l 1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	R	ER										Enc	ryp	tion	Ro	ot,	wor	d n														

13.1.9 IR[0]

Address offset: 0x090 Identity Root, word 0



Bit r	umbe	er		31	30	29	28	27	26	25	24	23 :	22 2	21 2	20 1	9 1	.8 1	7 1	6 1	5 14	1 13	12	11	10	9	8	7	6	5 -	4 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	Δ,	4 4	A 4	4 A	. A	Α	Α	Α	Α	Α	Α	Α	A .	Д Д	A	Α	Α
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	L 1	1 1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	R	IR										lder	ntity	/ Rc	ot,	wo	rd r	ı															_

13.1.10 IR[1]

Address offset: 0x094 Identity Root, word 1

Bit	numb	er		33	1 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	1 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	. Α	. A	Α	Α	Α	Α	Α	Α.	А А
Res	et 0x	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	V	alue	•						De	scri	pti	on																		
Α	R	IR										Ide	nti	ty R	oot	, w	ord	n															

13.1.11 IR[2]

Address offset: 0x098 Identity Root, word 2

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Ĺ
Id	RW	Field	Value Id	Va	lue							De	scr	pti	on																				
Α	R	IR										Ide	nti	ty R	001	t, w	ord	l n																	-

13.1.12 IR[3]

Address offset: 0x09C Identity Root, word 3

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A R IR		Identity Root, word n

13.1.13 DEVICEADDRTYPE

Address offset: 0x0A0

Device address type

Bit	numb	er		31 30 29	9 28	27	26	25 2	24 2	3 22	21	20	19 1	18 1	7 1	6 15	14	13	12	11 1	0 9	8	7	6	5	4	3 2	2 1	1 0
Id																													Α
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				1 :	1 1	1	1	1	1 :	1 1	. 1	1	1	1	1 :	L 1	1	1	1	1	1	1 :	L 1	1 1	
Id	RW	Field	Value Id	Value		escr	iptio	on																					
Α	R	DEVICEADDRTYPE			[evice	e ad	dre	ss ty	/pe																			
			Public	0	P	ublic	ado	dres	S																				
			Random			F	Rando	om a	addr	ess																			

13.1.14 **DEVICEADDR**[0]

Address offset: 0x0A4

Device address 0

the device address. Only bits [15:0] of ${\tt DEVICEADDR[1]}$ are used.



Bit	numbe	er		31	L 30	29	28	8 27	7 26	25	24	23	22 2	21 2	0 19	9 18	17	16	15	14 1	13 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	A	Α	Α	Α	Α	A	A A	A A	Α	Α	Α	Α	Α	A A	A A	Α	Α	Α	Α	Α	Α	A	А А	Α	Α
Res	et 0xF	FFFFFF		1	1	1	1	. 1	1	1	1	1	1	1 1	۱ 1	1	1	1	1	1	1 :	۱ 1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	alue	•						Des	crip	tior	1																	
Α	R	DEVICEADDR										48	oit d	levio	e ac	ddre	ess															
															OR[O	•				leas	_											

13.1.15 **DEVICEADDR**[1]

Address offset: 0x0A8

Device address 1

Bit	numbe	er		31	30	29	28	27	26	25 :	24 :	23 2	22 2	21 2	20 19	9 18	8 17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 :	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A ,	Д Д	A	A	Α	Α	Α	Α .	A A	A A	Α	Α	Α	Α	Α	Α	A	Α Α	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	. 1	1	1	1	1	1 1	l 1	1	1	1	1	1	1	1 :	L 1	l 1
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	tio	n																	
Α	R	DEVICEADDR									4	48 k	oit d	levi	ce a	ddr	ess															
											i	add	ress	s. D	DR[0 EVIC add	ΈΑΙ	DDR	[1]	con	tain	s th	e mo	ost s	igni	fica	nt b	its	of				

13.1.16 INFO.PART

Address offset: 0x100

Part code

Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 1	.6 :	15 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Д	A	4 Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	А А	A	Α						
Rese	t 0x0	0052832		52832 0x52832											0	0	1	0	1	0 (0 1	. 0	1	0	0	0	0	0	1	1	0 0	1	0
ld	RW	Field	Value Id	Va	lue						De	scri	ptic	n																			
Α	R	PART										Pa	rt cc	de																			
			N52832	0x	528	32						nR	F52	832																			
			Unspecified	0x	FFFI	FFF	FF					Un	spe	cifie	ed																		

13.1.17 INFO.VARIANT

Address offset: 0x104

Part Variant, Hardware version and Production configuration

Bit n	umbe	er		31	. 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Rese	t Ox4	1414142		0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	on																				
Α	R	VARIANT										Par	t V	aria	nt,	На	rdv	var	e ve	ersi	on	and	Pro	du	ctic	n c	onf	igu	rati	ion,	,				_
												enc	od	ed a	as A	SC	II																		
			AAAA	0x	414	141	L41					AA	AA																						
			AAAB	0x	414	141	L42	2				AA	ΑB																						
			AABA	0x	414	142	241					AAI	ВА																						
			AABB	0x	414	142	242	2				AAI	ВВ																						
			Unspecified	0x	FFFF	FFF	FF					Uns	spe	cifie	ed																				

13.1.18 INFO.PACKAGE

Address offset: 0x108

Package option



Bitı	numbe	r		31	30	29	28	27	26	25	24	23	22 :	21 2	20 2	19 1	18 1	17 :	16	15	14	13	12	11 :	10 !	Э	8 7	7 6	5 5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ	A A	A A	Α Δ	A	Α	Α	A A
Res	et 0x0	0002000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0 () (0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scrip	otio	n																		
Α	R	PACKAGE										Pac	kag	e o	otic	n																	
			QF	0x	200	0						QF	κх -	48-p	pin	QF	N																
			СН	0x	200	1						CH	xx -	7x8	WI	LCS	P 56	6 ba	alls														
			CI	0x	200	2						Clx	x - 7	'x8 \	WL	CSP	56	ba	lls														
			Unspecified	0x	FFFI	FFF	FF					Un	spec	ifie	d																		

13.1.19 INFO.RAM

Address offset: 0x10C

RAM variant

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21 2	20 :	19	18 :	17 1	16	15 :	14 1	.3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α Α	Δ Δ	. A	Α	Α	Α	Α	Α	Α	Α	A ,	А А
Res	et 0x0	0000040		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	1	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scrip	ptio	n																		
Α	R	RAM										RAI	M v	aria	nt																		
			K16	0x10 0x20 0x40								16	kBy	te R	AN	1																	
			K32	0x10 0x20								32	kBy	te R	AN	1																	
			K64	0x	40							64	kBy	te R	AN	1																	
			Unspecified	0x	FFFF	FFI	FF					Un	spe	cifie	d																		

13.1.20 INFO.FLASH

Address offset: 0x110

Flash variant

Ri	t ni	ımbe	ar.		21	30	20	28	27	26	25	2/	23	77 .	21 1	20 1	10 1	10 1	7 -	16	15 '	1/1 1	2 1	12 1	1 1	n (י ב	2 -	7 6	: 1	5 /	1 :	3 2	1	0
		שמוווג	:1																																
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α.	Α.	Α.	A	A	A	Α .	A A	۱ /	A /	۱ ۸	4 /	\ <i>F</i>	۱ ۱	4 Α	۱ /	A A	Α	Α
R	ese	t 0x0	0000200		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () 1	L) () () (0 0) (0	0	0
Id		RW	Field	Value Id	Va	alue								scrip	otio	n																			
Α		R	FLASH										Fla	sh v	aria	nt																			
				K128	0x80							128	3 kB	yte	FLA	SΗ																			
				K256	0x	100							256	5 kB	yte	FLA	SΗ																		
				K512	0x	200							512	2 kB	yte	FLA	SΗ																		
				Unspecified	0x	FFF	FFF	FF					Un:	spe	ifie	d																			

13.1.21 TEMP.A0

Address offset: 0x404 Slope definition A0.

Bit r	numbe	er		31	. 30	29	28	27 2	26 2	25 2	24 :	23 2	22 2	1 2	20 1	9 1	8 1	7 16	5 15	14	13	12 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id																							A A	A A	. Α	Α	Α	Α	Α	Α ,	Δ.	А А
Res	et OxC	00000320		0	0	0	0	0	0	0	0	0	0 ()	0 () () (0	0	0	0	0	0 () 1	. 1	0	0	1	0	0 (0	0 0
Id	RW	Field	Value Id	Va	lue						1	Des	crip	tio	n																	
Α	R	А									,	4 (s	lope	de	efini	tio	n) re	egist	er.													

13.1.22 TEMP.A1

Address offset: 0x408 Slope definition A1.



Bit	numb	oer			31	30 2	9	28 :	27 2	26 2	25 2	24 2	23 2	22 2	1 20) 19	18	17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3	2	1 ()
Id																							Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	L
Res	et 0x	ο0	000343		0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0	0	1	1	0	1	0	0	0	0	1 1	
Id	RW	v 1	Field	Value Id	Va	lue							Desc	crip	tion																			١
Α	R		A									A	A (sl	оре	det	initi	ion)	reg	iste	er.														

13.1.23 TEMP.A2

Address offset: 0x40C Slope definition A2.

Bitı	numbe	er		31	30 2	9 :	28	27 2	26 :	25 2	24	23 :	22 2	21 2	0 1	9 1	8 1	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	ı
Id																							Α	Α	Α	Α	Α	Α	Α	Α	Α /	Δ,	А А	ı
Res	et 0x0	000035D		0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	1	1	0	1	0	1	1	1 (0 1	ı
Id	RW	Field	Value Id	Val	lue							Des	crip	tio	n																			l
Α	R	Α										4 (s	lope	e de	efini	tior	n) re	gis	er.															١

13.1.24 TEMP.A3

Address offset: 0x410 Slope definition A3.

Bit n	iumbe	er		31 .	30 2	9 2	28 2	7 2	6 2	5 2	4 2	3 2	2 2	1 2	0 1	9 1	.8	17 :	16	15	14 :	13	12	11	10	9	8	7	6	5	4	3	2	1)
Id																								Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ
Rese	et 0x0	0000400		0	0 (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																													
Id	RW	Field	Value Id	Valu	ıe						D	esc	rip	tio	n																				ı
Α	R	Α									Α	(sle	оре	de	fin	tio	n) ı	egi	ste	r.															7

13.1.25 TEMP.A4

Address offset: 0x414 Slope definition A4.

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12	11 10 9 8 7	7 6 5 4 3 2 1 0
Id					A A A A	A A A A A A A
Reset 0x00000452		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 1 0 0 0	0 1 0 1 0 0 1 0
Id RW Field	Value Id	Value	Description			
A R A			A (slope definition) r	register		

13.1.26 TEMP.A5

Address offset: 0x418 Slope definition A5.

Bitı	numbe	er		31	30	29	28	27 2	26 2	25 2	4 2	3 2	22 2	1 2	0 1	9 1	8 1	7 1	6 1	.5 1	.4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 ()
Id																							Δ	. A	Α	Α	. A	Α	Α	Α	Α	Α	Α ,	A
Res	et 0x0	000037В		0	0	0	0	0	0 (0 (0	0	0 () (0 () () () () (0	0	0 (0	0	1	1	0	1	1	1	1	0	1	L
Id	RW	Field	Value Id	Va	lue)es	crip	tio	n																			
Α	R	А									P	\ (s	lope	de	fini	tioi	n) r	egis	ter															7

13.1.27 TEMP.B0

Address offset: 0x41C y-intercept B0.



Dia			_		21	20	20	20.2	7 20	25	24	22.	22.2	11 2	0 10	10	17	10	1 -	1 1 1	2 1	2 1	1 10		0	7	_	_	4	2	2 .	1 0
BII	ı nu	ımbe	ır		31	. 30	29	28 2	/ 26	25	24	23 .	22 2	1 2	0 15	18	1/	16	15	14]	13 1	.2 1.	1 10	9	8	/	Ь	5	4	3	۷.	1 0
Id																					A	ДД	Α	Α	Α	Α	Α	Α	Α	Α	A	А А
Re	eset	Oxu	0003FCC		0	0	0	0 (0	0	0	0	0	0 () 0	0	0	0	0	0	1	1 1	. 1	1	1	1	1	0	0	1	1 (0 0
Id		RW	Field	Value Id	Va	lue						Des	crip	tior	1																	
													•																			
Δ		R	R									R (v	-int	erce	nt)																	

13.1.28 TEMP.B1

Address offset: 0x420

y-intercept B1.

Bit n	umb	er		31	30	29	28 2	27 2	6 2	5 2	4 23	3 22	2 2:	1 2	0 19	9 18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id																					Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	4 A	Α	A
Rese	t OxC	0003F98		0	0	0	0	0 (0	0	0	0	0) (0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1	1 0	0	0
Id	RW	Field	Value Id	Va	lue						D	esc	ript	tior	,																		
Α	R	В									В	(v-i	inte	erce	pt)																		

13.1.29 TEMP.B2

Address offset: 0x424

y-intercept B2.

В	it nı	umbe	er		31 3	0 29	28	27 2	26 2	25 2	24 2	3 2	2 2:	1 20) 19	18	17	16	15	14	13	12	11 :	10 !	9	8	7	6	5	4	3 2	! 1	0
lo	ł																				Α	Α	Α	Α ,	Δ.	Α .	Α	Α .	Α.	A ,	Д Д	A	Α
R	ese	t 0x0	0003F98		0 (0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1	1 0	0	0
Ic	i	RW	Field	Value Id	Valu	e					D	esc	ript	ion																			

13.1.30 TEMP.B3

Address offset: 0x428

y-intercept B3.

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 2	0 19 18 17	16 15 1	4 13 12	11 10	9 8	8 7	6	5 4	3 2	1 0
Id						АА	АА	A A	4 А	Α.	А А	АА	. A A
Reset 0x0000	012	0 0 0 0 0 0	0000000	0 0 0	0 0 0	0 0	0 0	0 (0 0	0	0 1	0 0	1 0
Id RW Fie	d Value Id	Value	Description	1									
A R B			B (y-interce	ept)									

13.1.31 TEMP.B4

Address offset: 0x42C

y-intercept B4.

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	17 16 15 14 13	3 12 11 10	9 8 7	6 5	4 3 2	2 1 0
Id				А	A A A	ААА	. A A	. A A A	А А А
Reset 0x0000004	D	0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0	0 0 0	1 0	0 1 :	1 0 1
ld RW Field	Value Id	Value	Description						
A R B			B (y-intercept)						

13.1.32 TEMP.B5

Address offset: 0x430

y-intercept B5.



Bit	num	per		31	30 2	9 2	28 27	7 26	25	24	23 2	22 2	21 2	0 1	9 1	8 17	16	15	14	13	12 1	.1 1	9	8	7	6	5	4	3	2 :	1 0
Id																				Α	Α.	4 Δ	Α	Α	Α	Α	Α	Α	Α	A A	4 А
Res	et O	00003E10		0	0 () (0 0	0	0	0	0	0	0	0 () (0	0	0	0	1	1	1 1	1	0	0	0	0	1	0	0 (0 0
Id	RV	/ Field	Value Id	Va	lue						Des	crip	tio	n																	
Α	R	В									B (v	-int	erc	ept)																	

13.1.33 TEMP.T0

Address offset: 0x434 Segment end T0.

Bit	number		31 30	29 28 27	26 25	24 23	3 22 2	21 20	19 1	.8 17	16	15 1	4 13	12 13	10	9 8	7	6	5	4	3 2	1	0
Id																	Α	Α	Α.	A A	4 A	Α	Α
Res	et 0x0000	00E2	0 0	0 0 0	0 0	0 0	0 (0 0	0	0 0	0	0 0	0	0 0	0	0 0	1	1	1	0 (0 0	1	0
Id	RW Fie	ld Value	ld Value			D	escrip	tion															
_	ъ т					-	,		- 13														

A R T T (segment end)register.

13.1.34 TEMP.T1

Address offset: 0x438 Segment end T1.

Bit number		31 30 29 28 2	27 26 25 24 23 22 21 20 19 18 17	7 16 15 14 13 12 11 10	9876543210
Id					A A A A A A A
Reset 0x00000000		0 0 0 0	0 0 0 0 0 0 0 0 0 0	0000000	0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description		
A R T			T (segment end)registe	ter	

13.1.35 TEMP.T2

Address offset: 0x43C Segment end T2.

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000014		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 1 0 1 0 0
Id RW Field	Value Id	Value	Description		
A R T			T (segment end)registe	er	

13.1.36 TEMP.T3

Address offset: 0x440 Segment end T3.

Bit	numb	er		31	30	29	28 2	7 26	5 25	5 24	23	22	21	20 1	9 1	8 1	7 16	15	14	13 3	L2 1	1 1	0 9	8	7	6	5	4	3 2	1	1 0
Id																									Α	Α	Α	Α	A A	. 4	A A
Re	set 0x(0000019		0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0	0	1	1 0	C	0 1
Id	RW	Field	Value Id	Va	lue						De	scri	otic	n																	
Α	R	Т									T (:	segr	ner	t en	d)r	egis	ter.														

13.1.37 TEMP.T4

Address offset: 0x444 Segment end T4.



Bit number	31 30 29 28	3 27 26 25 24 23 22 21 20 19 18 17 1	16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id				A A A A A A A
Reset 0x00000050	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 1 0 1 0 0 0 0
ld RW Field Va	lue Id Value	Description		
ΔRT		T (segment end)register	-	

13.1.38 NFC.TAGHEADER0

Address offset: 0x450

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bitı	numbe	er		31	30	29	28	27	26	25	24	23 :	22 2	21 2	20 1	9 1	8 1	7 1	5 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				D	D	D	D	D	D	D	D	С	С	С	C (2 (2 0	C C	В	В	В	В	В	В	В	В	Α	Α	Α	Α .	ДД	A	Α
Res	et OxF	FFFF5F		1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	. 1	1	1	1	1	1	1	1	1	0	1	0	1	1 1	. 1	1
Id	RW	Field	Value Id	Va	lue	!						Des	crip	tio	n																		
Α	R	MFGID										Def	ault	Ma	anu	fact	ure	r ID	: Nc	ordi	c Se	mico	ond	uct	or A	SΑ	has	IC	M				
												0x5	F																				
В	R	UD1										Uni	que	ide	ntii	ier	byt	e 1															
С	R	UD2										Uni	que	ide	ntii	ier	byt	e 2															
D	R	UD3										Uni	que	ide	ntii	ier	bvt	e 3															

13.1.39 NFC.TAGHEADER1

Address offset: 0x454

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 :	21	20	19 :	18	17 1	16 1	L5 1	4 13	12	11	10	9	8	7	6	5 -	4	3 2	1	0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	ВЕ	3 B	В	В	В	В	В.	Α	Α	A .	Α /	4 A	Α	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	l 1	1	1	1	1	1	1	1	1	1 :	l 1	1	1
Id	RW	Field	Value Id	Va	lue							De	scrip	otic	n																		
Α	R	UD4										Un	ique	e id	enti	fier	by	te 4	ļ														
В	R	UD5										Un	ique	e id	enti	fier	by	te 5	,														
С	R	UD6										Un	ique	ide	enti	fier	by	te 6	;														
D	R	UD7										Un	ique	ide	enti	fier	by	te 7	,														

13.1.40 NFC.TAGHEADER2

Address offset: 0x458

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 :	20 :	L9 1	18 :	17 :	16	15	14 :	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	В	В	В	В	В	В	В	В.	Α	Α	Α	Α	A A	A A	A A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			
Α	R	UD8										Uni	que	ide	enti	fier	by	te 8	3															
В	R	UD9										Uni	que	ide	enti	fier	by	te 9)															
С	R	UD10										Uni	que	ide	enti	fier	by	te 1	0															
D	R	UD11										Uni	que	ide	enti	fier	by	te 1	1															

13.1.41 NFC.TAGHEADER3

Address offset: 0x45C

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.



Bit r	iumbe	er		31	. 30	29	28	27	26	25 2	24 :	23 2	22 2	1 20	0 19	18	17	16	15	L4 13	3 12	11	10	9 8	7	6	5	4	3	2	1 0
Id				D	D	D	D	D	D	D	D	С	C (C C	C C	С	С	С	В	в в	В	В	В	ВЕ	, Δ	. A	Α	Α	Α	Α	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1 1	L 1	. 1	1	1	1	1	1 1	1	1	1	1 1	. 1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	alue	:					ı	Des	crip	tion	1																
Α	R	UD12									- 1	Unio	que	ider	ntifie	er b	yte	12													
В	R	UD13									- 1	Unio	que	ider	ntifie	er b	yte	13													
С	R	UD14									- 1	Unio	que	ider	ntifie	er b	yte	14													
D	R	UD15									ı	Unio	que	ider	ntifie	er b	yte	15													



14 UICR — User information configuration registers

The user information configuration registers (UICRs) are non-volatile memory (NVM) registers for configuring user specific settings.

For information on writing UICR registers, see the *NVMC — Non-volatile memory controller* on page 29 and *Memory* on page 23 chapters.

14.1 Registers

Table 18: Instances

Base address	Peripheral	Instance	Description	Configuration
0x10001000	UICR	UICR	User Information Configuration	

Table 19: Register Overview

Register	Offset	Description	
	0x000		Reserved
	0x004		Reserved
	0x008		Reserved
	0x010		Reserved
NRFFW[0]	0x014	Reserved for Nordic firmware design	
NRFFW[1]	0x018	Reserved for Nordic firmware design	
NRFFW[2]	0x01C	Reserved for Nordic firmware design	
NRFFW[3]	0x020	Reserved for Nordic firmware design	
NRFFW[4]	0x024	Reserved for Nordic firmware design	
NRFFW[5]	0x028	Reserved for Nordic firmware design	
NRFFW[6]	0x02C	Reserved for Nordic firmware design	
NRFFW[7]	0x030	Reserved for Nordic firmware design	
NRFFW[8]	0x034	Reserved for Nordic firmware design	
NRFFW[9]	0x038	Reserved for Nordic firmware design	
NRFFW[10]	0x03C	Reserved for Nordic firmware design	
NRFFW[11]	0x040	Reserved for Nordic firmware design	
NRFFW[12]	0x044	Reserved for Nordic firmware design	
NRFFW[13]	0x048	Reserved for Nordic firmware design	
NRFFW[14]	0x04C	Reserved for Nordic firmware design	
NRFHW[0]	0x050	Reserved for Nordic hardware design	
NRFHW[1]	0x054	Reserved for Nordic hardware design	
NRFHW[2]	0x058	Reserved for Nordic hardware design	
NRFHW[3]	0x05C	Reserved for Nordic hardware design	
NRFHW[4]	0x060	Reserved for Nordic hardware design	
NRFHW[5]	0x064	Reserved for Nordic hardware design	
NRFHW[6]	0x068	Reserved for Nordic hardware design	
NRFHW[7]	0x06C	Reserved for Nordic hardware design	
NRFHW[8]	0x070	Reserved for Nordic hardware design	
NRFHW[9]	0x074	Reserved for Nordic hardware design	
NRFHW[10]	0x078	Reserved for Nordic hardware design	
NRFHW[11]	0x07C	Reserved for Nordic hardware design	
CUSTOMER[0]	0x080	Reserved for customer	
CUSTOMER[1]	0x084	Reserved for customer	
CUSTOMER[2]	0x088	Reserved for customer	
CUSTOMER[3]	0x08C	Reserved for customer	
CUSTOMER[4]	0x090	Reserved for customer	
CUSTOMER[5]	0x094	Reserved for customer	
CUSTOMER[6]	0x098	Reserved for customer	



Register	Offset	Description
CUSTOMER[7]	0x09C	Reserved for customer
CUSTOMER[8]	0x0A0	Reserved for customer
CUSTOMER[9]	0x0A4	Reserved for customer
CUSTOMER[10]	0x0A8	Reserved for customer
CUSTOMER[11]	0x0AC	Reserved for customer
CUSTOMER[12]	0x0B0	Reserved for customer
CUSTOMER[13]	0x0B4	Reserved for customer
CUSTOMER[14]	0x0B8	Reserved for customer
CUSTOMER[15]	0x0BC	Reserved for customer
CUSTOMER[16]	0x0C0	Reserved for customer
CUSTOMER[17]	0x0C4	Reserved for customer
CUSTOMER[18]	0x0C8	Reserved for customer
CUSTOMER[19]	0x0CC	Reserved for customer
CUSTOMER[20]	0x0D0	Reserved for customer
CUSTOMER[21]	0x0D4	Reserved for customer
CUSTOMER[22]	0x0D8	Reserved for customer
CUSTOMER[23]	0x0DC	Reserved for customer
CUSTOMER[24]	0x0E0	Reserved for customer
CUSTOMER[25]	0x0E4	Reserved for customer
CUSTOMER[26]	0x0E8	Reserved for customer
CUSTOMER[27]	0x0EC	Reserved for customer
CUSTOMER[28]	0x0F0	Reserved for customer
CUSTOMER[29]	0x0F4	Reserved for customer
CUSTOMER[30]	0x0F8	Reserved for customer
CUSTOMER[31]	0x0FC	Reserved for customer
PSELRESET[0]	0x200	Mapping of the nRESET function (see POWER chapter for details)
PSELRESET[1]	0x204	Mapping of the nRESET function (see POWER chapter for details)
APPROTECT	0x208	Access Port protection
NFCPINS	0x20C	Setting of pins dedicated to NFC functionality: NFC antenna or GPIO

14.1.1 NRFFW[0]

Address offset: 0x014

Reserved for Nordic firmware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value Description
A RW NRFFW		Reserved for Nordic firmware design

14.1.2 NRFFW[1]

Address offset: 0x018

Reserved for Nordic firmware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFFW	Reserved for Nordic firmware design

14.1.3 NRFFW[2]

Address offset: 0x01C

Reserved for Nordic firmware design



14.1.4 NRFFW[3]

Address offset: 0x020

Reserved for Nordic firmware design

14.1.5 NRFFW[4]

Address offset: 0x024

Reserved for Nordic firmware design

14.1.6 NRFFW[5]

Address offset: 0x028

Reserved for Nordic firmware design

RW NRFFW Reserved for Nordic firmware design

14.1.7 NRFFW[6]

Address offset: 0x02C

Reserved for Nordic firmware design

A RW NRFFW Reserved for Nordic firmware design

14.1.8 NRFFW[7]

Address offset: 0x030

Reserved for Nordic firmware design

RW NRFFW Reserved for Nordic firmware design



14.1.9 NRFFW[8]

Address offset: 0x034

Reserved for Nordic firmware design

Bit r	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20 1	9 1	8 1	7 16	15	14	13	12 1	1 1) 9	8	7	6	5	4	3	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	A	Α	Α	Α	Α.	A A	A	Α	Α	Α	Α	Α	Α ,	4 4	A A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1 1	1
Id	RW	Field	Value Id	Va	lue							De	scrip	otic	n																	
Α	RW	NRFFW										Res	erv	ed	for I	Vor	dic f	irm	war	e de	sigr	1										

14.1.10 NRFFW[9]

Address offset: 0x038

Reserved for Nordic firmware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFFW		Reserved for Nordic firmware design

14.1.11 NRFFW[10]

Address offset: 0x03C

Reserved for Nordic firmware design

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16 :	15 1	.4 1	13 1	.2 1	l1 1	0 9	9 (3 7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α	Δ.	A ,	Α Α	Α Α	A A	. A	Α	Α	Α	Α	Α	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	lue							De	cri	ptic	on																			
Α	RW	NRFFW										Res	erv	ed	for	Noi	dic	firr	nw	are	des	ign												_

14.1.12 NRFFW[11]

Address offset: 0x040

Reserved for Nordic firmware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value Description
A RW NRFFW		Reserved for Nordic firmware design

14.1.13 NRFFW[12]

Address offset: 0x044

Reserved for Nordic firmware design

Bit number	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15	5 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id	A A A A A A A	A A A A A A A A		A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1111111	1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description		

A RW NRFFW Reserved for Nordic firmware design

14.1.14 NRFFW[13]

Address offset: 0x048

Reserved for Nordic firmware design



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFFW	Reserved for Nordic firmware design

14.1.15 NRFFW[14]

Address offset: 0x04C

Reserved for Nordic firmware design

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	.8 1	7 1	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	4 Δ	\ A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A <i>A</i>	A A
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	۱ 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	l 1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	NRFFW										Res	erv	ed f	for N	Vor	dic f	irm	war	e d	esig	n											

14.1.16 NRFHW[0]

Address offset: 0x050

Reserved for Nordic hardware design

Bit	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 1	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α	RW	NRFHW										Re	serv	/ed	for	No	rdic	ha	rdw	/are	de	sigi	n												7

14.1.17 NRFHW[1]

Address offset: 0x054

Reserved for Nordic hardware design

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 :	16	15	14	13	12 :	11	10	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	. Α	AA
Res	et 0xl	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																			
^	D\A/	NIDELINA										Doc		- d	£~~	NIO	.di.c	h a .	- d			.i	_											

RW NRFHW Reserved for Nordic hardware design

14.1.18 NRFHW[2]

Address offset: 0x058

Reserved for Nordic hardware design

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19 1	18 :	17 1	16	15 :	14 :	13 1	12 1	.1 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α.	Α	Α	Α	Α	Α .	4 Α	. Α	. A	Α	Α	Α	Α	Α	Α	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	NRFHW										Res	erv	ed '	for	Nor	dic	har	dw	/are	de	sigr	ı										

14.1.19 NRFHW[3]

Address offset: 0x05C

Reserved for Nordic hardware design

Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 :	16 1	15 1	l4 1	3 1	2 1:	10	9	8	7	6	5	4	3 2	2 1	L 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	A A	A /	A A	Α	Α	Α	Α	Α	Α	Α	A A	A A	A A
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	l 1	1	1	1	1	1	1	1	1 :	L 1	. 1
Id RW Field	Value Id	Va	lue							De	scri	ptic	on																		

RW NRFHW Reserved for Nordic hardware design



14.1.20 NRFHW[4]

Address offset: 0x060

Reserved for Nordic hardware design

Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	LO	9	8	7	6	5	4	3	2	1	C
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α	Α .	Δ,	Α	Δ
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1	1
Id RW Field	Value Id	Va	lue							De	scr	ipti	on																				
A RW NRFHW										Re	ser	ved	for	· No	rdio	: ha	rdv	vare	e de	sig	n												7

Reserved for Nordic hardware design

14.1.21 NRFHW[5]

Address offset: 0x064

Reserved for Nordic hardware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFHW		Reserved for Nordic hardware design

14.1.22 NRFHW[6]

Address offset: 0x068

Reserved for Nordic hardware design

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	L8 1	.7 1	16 1	.5 1	4 1	3 1	2 1	1 1	9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	Δ ,	A A	Δ,	Δ ,	Δ ,	۱ ۸	4 Α	A	Α	Α	Α	Α	Α	Α	A	A	4
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 :	1	ι :	ı	1 1	. 1	1	1	1	1	1	1	1	1	L
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	NRFHW										Res	serv	ed	for	Nor	dic	har	dw	are	des	ign												Ξ.

14.1.23 NRFHW[7]

Address offset: 0x06C

Reserved for Nordic hardware design

Bit n	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 1	.6 1	L5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ.	A A	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α	Α
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	l 1	1	1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
Α	RW	NRFHW										Res	erv	ed '	for	Noi	dic	har	dw	are	desi	gn											

14.1.24 NRFHW[8]

Address offset: 0x070

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15	5 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id	A A A A A A A	A A A A A A A A		A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1111111	1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description		

A RW NRFHW Reserved for Nordic hardware design

14.1.25 NRFHW[9]

Address offset: 0x074

Reserved for Nordic hardware design



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFHW		Reserved for Nordic hardware design

14.1.26 NRFHW[10]

Address offset: 0x078

Reserved for Nordic hardware design

Bit number		31 30 29 28	8 27 26 25	24 23 22 21 20 19	18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id		A A A A	A A A	A A A A A	A A A A A A A A	A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1	1 1 1	1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value		Description		
A RW NRFHW				Reserved for No	ordic hardware design	

14.1.27 NRFHW[11]

Address offset: 0x07C

Reserved for Nordic hardware design

Bit	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 1	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α	RW	NRFHW										Re	serv	/ed	for	No	rdic	ha	rdw	/are	de	sigi	n												7

14.1.28 CUSTOMER[0]

Address offset: 0x080 Reserved for customer

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5 4	4 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	A ,	Α,	4 Α	λ Α	A	Α	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	. 1	1	1
Id	RW	Field	Value Id	Vi	alue							De	scri	ptic	on																			
Α	RW	CUSTOMER										Re	serv	/ed	for	cus	ton	ner																

14.1.29 CUSTOMER[1]

Address offset: 0x084 Reserved for customer

Bitı	numbe	er		31 30 29 28 2	7 26 25 24 23 22	21 20 19 18 17	16 15 14 13 12 1	11 10 9 8 7	6 5 4 3 2 1 0
Id				AAAAA	4 A A A A A	AAAAA	A A A A A	A A A A	A A A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1	1 1 1 1 1	1 1 1 1 1	1 1 1 1 1 :	1 1 1 1 1	1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Descri	iption			
Α	RW	CUSTOMER			Reserv	ved for customer			

14.1.30 CUSTOMER[2]

Address offset: 0x088 Reserved for customer

Bit number	31 30 29 28 2	27 26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A	A A A A A A A A A A A A A A A A A A A	A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1	1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description	

A RW CUSTOMER Reserved for customer



14.1.31 CUSTOMER[3]

Address offset: 0x08C Reserved for customer

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	4 A
Res	et 0xl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1 1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
^	DIA	CLICTOMACD										n -			c																			

A RW CUSTOMER Reserved for customer

14.1.32 CUSTOMER[4]

Address offset: 0x090 Reserved for customer

Id RW Field Value Description	
Reset 0xFFFFFFF 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	111111111111111
Id A A A A A A A A A A A A A A A A A A A	A A A A A A A A A A A A A
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15	14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

A RW CUSTOMER Reserved for customer

14.1.33 CUSTOMER[5]

Address offset: 0x094 Reserved for customer

Bit	numbe	er		31	L 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 A
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1 1
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																			
Α	RW	CUSTOMER										Res	serv	ed	for	cus	ton	ner																

14.1.34 CUSTOMER[6]

Address offset: 0x098 Reserved for customer

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Re	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.35 CUSTOMER[7]

Address offset: 0x09C Reserved for customer

Bit number	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15	5 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id	A A A A A A A	A A A A A A A A		A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1111111	1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description		

A RW CUSTOMER Reserved for customer

14.1.36 CUSTOMER[8]

Address offset: 0x0A0 Reserved for customer



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0											
Id		A A A A A A A A A A A A A A A A A A A											
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1											
Id RW Field	Value Id	Value Description											
A RW CUSTOMER		Reserved for customer											

14.1.37 CUSTOMER[9]

Address offset: 0x0A4
Reserved for customer

Bit	numb	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Re	set 0xl	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.38 CUSTOMER[10]

Address offset: 0x0A8
Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW CUSTOMER	Reserved for customer

14.1.39 CUSTOMER[11]

Address offset: 0x0AC Reserved for customer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

14.1.40 CUSTOMER[12]

Address offset: 0x0B0 Reserved for customer

Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 .	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Α.	А А
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1	1 1
Id	RW	Field	Value Id	Va	alue							De	scr	ipti	on																			
Α	RW	CUSTOMER										Re	ser	ved	for	cus	stoi	mer	-															

14.1.41 CUSTOMER[13]

Address offset: 0x0B4 Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18	8 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description	

A RW CUSTOMER Reserved for customer



14.1.42 CUSTOMER[14]

Address offset: 0x0B8 Reserved for customer

Bit n	umbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 -	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A .	A ,	4 A	Α	. A
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																			
Α	RW	CUSTOMER		Value Description Reserved for customer																														

14.1.43 CUSTOMER[15]

Address offset: 0x0BC Reserved for customer

В	Bit n	umb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	L 0
le	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	4 Δ	A A
R	lese	t Oxl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1
I	d	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Δ	١	RW	CUSTOMER										Res	serv	/ed	for	cus	ton	ner																

14.1.44 CUSTOMER[16]

Address offset: 0x0C0 Reserved for customer

Bit	numbe	r		33	1 30	29	28	3 27	7 26	25	24	23	22	21	20	19	18	17	16 :	15 1	.4 1	3 1	2 1:	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	. A	. A	Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α ,	A A	A	A	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	. 1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	1	. 1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	V	alue	•						De	scr	iptio	on																		
Α	RW	CUSTOMER										Re	ser	ved	for	cus	ton	ner															

14.1.45 CUSTOMER[17]

Address offset: 0x0C4
Reserved for customer

Bit	numb	er		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A	A A A A A A A A A A A A A A A A A A A
Re	set OxF	FFFFFF		1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	CUSTOMER			Reserved for customer

14.1.46 CUSTOMER[18]

Address offset: 0x0C8
Reserved for customer

Bit num	ber			31	. 30	29	28	3 27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7 (s !	5 4	1 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ,	Α ,	4 4	A	Α	Α	Α
Reset 0	xFF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	ι :	1 1	1	1	1	1
ld RV	V	Field	Value Id	Va	alue	•						De	scri	ptic	on																			
A RV	v	CUSTOMER										Re	serv	/ed	for	CIIS	ton	ner																

14.1.47 CUSTOMER[19]

Address offset: 0x0CC Reserved for customer



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

14.1.48 CUSTOMER[20]

Address offset: 0x0D0 Reserved for customer

Bit	numb	er		31	1 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13 :	12 :	11 1	.0 9	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ ,	Δ.	A A	Д	Α.	Α	Α /	4 A	Α	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1	1 :	1	1	1	1 :	1 1	1	1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	on																			
Α	RW	CUSTOMER										Res	erv	/ed	for	cus	ton	ner																

14.1.49 CUSTOMER[21]

Address offset: 0x0D4 Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW CUSTOMER	Reserved for customer

14.1.50 CUSTOMER[22]

Address offset: 0x0D8 Reserved for customer

Bitı	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.51 CUSTOMER[23]

Address offset: 0x0DC Reserved for customer

Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 .	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Α.	А А
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1	1 1
Id	RW	Field	Value Id	Va	alue							De	scr	ipti	on																			
Α	RW	CUSTOMER										Re	ser	ved	for	cus	stoi	mer	-															

14.1.52 CUSTOMER[24]

Address offset: 0x0E0 Reserved for customer

Bit number	31 30 29 28 2	27 26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A	A A A A A A A A A A A A A A A A A A A	A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1	1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description	

A RW CUSTOMER Reserved for customer



14.1.53 CUSTOMER[25]

Address offset: 0x0E4 Reserved for customer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

14.1.54 CUSTOMER[26]

Address offset: 0x0E8 Reserved for customer

D.:					24	2				7 20	25		22	22	24	20	10	40	47	1.0	4.5		12.4	2 4		^ ′			,	_	_		· .		1 0
Bit	nun	nbe	r		31	. 30) 29	28	2,	/ 26	25	24	23	22	21	20	19	18	1/	16	15	14 :	13 1	.2 1	.1 1	.0 9) 8	3 ,	/	6	5	4	3.	2 :	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ.	Δ ,	A /	۸ ۸	A A	۱ ۱	Α	Α	Α	A A	A A	А А
Res	et ()xFI	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	ι :	L 1	L	1	1	1	1 :	L 1	1 1
Id	R	w	Field	Value Id	Va	lue	•						De	scri	ptio	on																			
			CUCTOMATE										_																						

A RW CUSTOMER Reserved for customer

14.1.55 CUSTOMER[27]

Address offset: 0x0EC Reserved for customer

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	A A
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	CUSTOMER										Re	serv	/ed	for	cus	tor	ner																

Reserved for customer

14.1.56 CUSTOMER[28]

Address offset: 0x0F0 Reserved for customer

Bit	numbe	er		31	L 30	29	28	27	26	25	24	23 :	22 2	1 2	0 19	18	17	16	15	14 :	13 1	L2 1	1 10	9	8	7	6	5	4	3 2	1	L O
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۱ ۸	4 А	Α	Α	Α	Α	Α	Α	A A	A A	Α	Α	Α	Α	Α	Α	ΑА	. 4	A A
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1 1	L :	1 1	1	1	1	1	1	1	1 :	l 1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Va	alue							Des	crip	tio	n																	
Α	RW	CUSTOMER										Res	erve	d f	or cu	ısto	mei															

14.1.57 CUSTOMER[29]

Address offset: 0x0F4 Reserved for customer

E	3it nu	mbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 :	LO	9	8	7	6	5	4	3 2	2 1	1 0	
1	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A.	A	Α.	Α	Α	Α	Α	A A	\ A	4 A	
F	Reset	0xFI	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1 1	1 1	
ı	d	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
-	Δ	RW/	CUSTOMER										Ros	orι	haı	for	CIIC	ton	nor																	

A RW CUSTOMER

14.1.58 CUSTOMER[30]

Address offset: 0x0F8 Reserved for customer



Bit r	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 1	L4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	Δ .	۱ ۸	Δ Δ	. A	Α	Α	Α	Α	Α	Α	Α	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	ι :	L 1	. 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	CUSTOMER										Re	serv	ed	for	cus	ton	ner															

14.1.59 CUSTOMER[31]

Address offset: 0x0FC Reserved for customer

Bit r	numbe	r		31 30 29 28 2	7 26 25 24	23 22 21 20 19	18 17 16 15 14	13 12 11 10 9 8	3 7 6 5 4	3 2 1 0	
Id				AAAAA	4 A A A	A A A A A	A A A A	A A A A A	4 A A A A	A A A A	
Res	et OxF	FFFFFF		1 1 1 1 1	1111	1 1 1 1 1	1 1 1 1 1	1 1 1 1 1 1	1111	1 1 1 1	
Id	RW	Field	Value Id	Value		Description					
Α	RW	CUSTOMER		Reserved for customer							

14.1.60 PSELRESET[0]

Address offset: 0x200

Mapping of the nRESET function (see POWER chapter for details)

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If they don't, there will be no nRESET function exposed on a GPIO, and the device will always start independently of the levels present on any of the GPIOs.

Bit number				31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	АААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		21	GPIO number P0.n onto which Reset is exposed
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

14.1.61 PSELRESET[1]

Address offset: 0x204

Mapping of the nRESET function (see POWER chapter for details)

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If they don't, there will be no nRESET function exposed on a GPIO, and the device will always start independently of the levels present on any of the GPIOs.

Bit number				31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		21	GPIO number P0.n onto which Reset is exposed
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

14.1.62 APPROTECT

Address offset: 0x208
Access Port protection

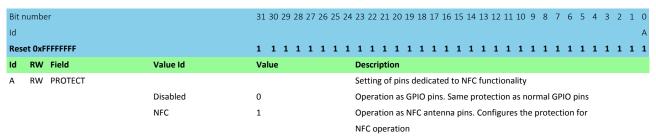


Bitı	numbe	er		31 3	0 29	28	8 27	7 26	25	24	23	22 2	1 2	0 19	9 18	3 17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																									4	Α	Α	Α .	Α Α	A A	Α
Res	et OxF	FFFFFF		1 1	l 1	1	. 1	1	1	1	1	1 1	1 1	1	. 1	1	1	1	1	1	1 1	l 1	1	1	ı	1	1	1	1 :	۱ 1	1
Id	RW	Field	Value Id	Valu	e						Des	crip	tior	1																	
Α	RW	PALL									Ena	ble o	or d	isab	ole A	Acce	ss F	ort	pro	tect	ion	. Any	oth	er v	alu	e th	nan				
	0x						0xFF being written to this field will enable protection.																								
											See	Deb	oug	and	tra	ce c	n p	age	72	for 1	nor	e inf	orm	atio	١.						
			Disabled	0xFF							Dis	able																			
			Enabled	0x00)						Ena	ble																			

14.1.63 NFCPINS

Address offset: 0x20C

Setting of pins dedicated to NFC functionality: NFC antenna or GPIO





15 Peripheral interface

Peripherals are controlled by the CPU by writing to configuration registers and task registers. Peripheral events are indicated to the CPU by event registers and interrupts if they are configured for a given event.

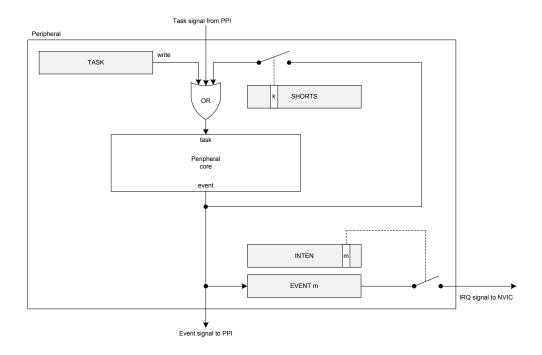


Figure 10: Tasks, events, shortcuts, and interrupts

15.1 Peripheral ID

Every peripheral is assigned a fixed block of 0x1000 bytes of address space, which is equal to 1024 x 32 bit registers.

See *Instantiation* on page 24 for more information about which peripherals are available and where they are located in the address map.

There is a direct relationship between the peripheral ID and base address. For example, a peripheral with base address 0x40000000 is assigned ID=0, a peripheral with base address 0x40001000 is assigned ID=1, and a peripheral with base address 0x4001F000 is assigned ID=31.

Peripherals may share the same ID, which may impose one or more of the following limitations:

- Some peripherals share some registers or other common resources.
- Operation is mutually exclusive. Only one of the peripherals can be used at a time.
- Switching from one peripheral to another must follow a specific pattern (disable the first, then enable the second peripheral).

15.2 Peripherals with shared ID

In general, and with the exception of ID 0, peripherals sharing an ID and base address may not be used simultaneously. The user can only enable one at the time on this specific ID.

When switching between two peripherals that share an ID, the user should do the following to prevent unwanted behavior:

Disable the previously used peripheral



- · Remove any PPI connections set up for the peripheral that is being disabled
- Clear all bits in the INTEN register, i.e. INTENCLR = 0xFFFFFFFF.
- Explicitly configure the peripheral that you enable and do not rely on configuration values that may be inherited from the peripheral that was disabled.
- Enable the now configured peripheral.

For each of the rows in the following table, the instance ID listed is shared by the peripherals in the same row.

Table 20: Peripherals sharing an ID

Instance						
ID 2 (0x40002000)	UARTE	UART				
-						
ID 3 (0x40003000)	SPIM	SPIS	SPI	TWIM	TWIS	TWI
ID 4 (0x40004000)	SPIM	SPIS	SPI	TWIM	TWIS	TWI
ID 35 (0x40023000)	SPIM	SPIS	SPI			
-						
ID 15 (0x4000F000)	AAR	CCM				
-						
ID 19 (0x40013000)	COMP	LPCOMP				
-						
ID 20 (0x40014000)	SWI	EGU				
ID 21 (0x40015000)	SWI	EGU				
ID 22 (0x40016000)	SWI	EGU				
ID 23 (0x40017000)	SWI	EGU				
ID 24 (0x40018000)	SWI	EGU				
ID 25 (0x40019000)	SWI	EGU				

15.3 Peripheral registers

Most peripherals feature an ENABLE register. Unless otherwise specified in the relevant chapter, the peripheral registers (in particular the PSEL registers) must be configured before enabling the peripheral.

Note that the peripheral must be enabled before tasks and events can be used.

15.4 Bit set and clear

Registers with multiple single-bit bit fields may implement the "set-and-clear" pattern. This pattern enables firmware to set and clear individual bits in a register without having to perform a read-modify-write operation on the main register.

This pattern is implemented using three consecutive addresses in the register map where the main register is followed by a dedicated SET and CLR register in that order.

The SET register is used to set individual bits in the main register while the CLR register is used to clear individual bits in the main register. Writing a '1' to a bit in the SET or CLR register will set or clear the same bit in the main register respectively. Writing a '0' to a bit in the SET or CLR register has no effect. Reading the SET or CLR registers returns the value of the main register.

Restriction: The main register may not be visible and hence not directly accessible in all cases.

15.5 Tasks

Tasks are used to trigger actions in a peripheral, for example, to start a particular behavior. A peripheral can implement multiple tasks with each task having a separate register in that peripheral's task register group.

A task is triggered when firmware writes a '1' to the task register or when the peripheral itself or another peripheral toggles the corresponding task signal. See *Figure 10: Tasks, events, shortcuts, and interrupts* on page 68.



15.6 Events

Events are used to notify peripherals and the CPU about events that have happened, for example, a state change in a peripheral. A peripheral may generate multiple events with each event having a separate register in that peripheral's event register group.

An event is generated when the peripheral itself toggles the corresponding event signal, and the event register is updated to reflect that the event has been generated. See *Figure 10: Tasks, events, shortcuts, and interrupts* on page 68. An event register is only cleared when firmware writes a '0' to it.

Events can be generated by the peripheral even when the event register is set to '1'.

15.7 Shortcuts

A shortcut is a direct connection between an event and a task within the same peripheral. If a shortcut is enabled, its associated task is automatically triggered when its associated event is generated.

Using a shortcut is the equivalent to making the same connection outside the peripheral and through the PPI. However, the propagation delay through the shortcut is usually shorter than the propagation delay through the PPI.

Shortcuts are predefined, which means their connections cannot be configured by firmware. Each shortcut can be individually enabled or disabled through the shortcut register, one bit per shortcut, giving a maximum of 32 shortcuts for each peripheral.

15.8 Interrupts

All peripherals support interrupts. Interrupts are generated by events.

A peripheral only occupies one interrupt, and the interrupt number follows the peripheral ID. For example, the peripheral with ID=4 is connected to interrupt number 4 in the Nested Vectored Interrupt Controller (NVIC).

Using the INTEN, INTENSET and INTENCLR registers, every event generated by a peripheral can be configured to generate that peripheral's interrupt. Multiple events can be enabled to generate interrupts simultaneously. To resolve the correct interrupt source, the event registers in the event group of peripheral registers will indicate the source.

Some peripherals implement only INTENSET and INTENCLR, and the INTEN register is not available on those peripherals. Refer to the individual chapters for details. In all cases, however, reading back the INTENSET or INTENCLR register returns the same information as in INTEN.

Each event implemented in the peripheral is associated with a specific bit position in the INTEN, INTENSET and INTENCLR registers.

The relationship between tasks, events, shortcuts, and interrupts is shown in *Figure 10: Tasks, events, shortcuts, and interrupts* on page 68.

15.8.1 Interrupt clearing

When clearing an interrupt by writing "0" to an event register, or disabling an interrupt using the INTENCLR register, it can take up to four CPU clock cycles to take effect. This means that an interrupt may reoccur immediatelly even if a new event has not come, if the program exits an interrupt handler after the interrupt is cleared or disabled, but before four clock cycles have passed.

Important: To avoid an interrupt reoccurring before a new event has come, the program should perform a read from one of the peripheral registers, for example, the event register that has been cleared, or the INTENCLR register that has been used to disable the interrupt.

This will cause a one to three-cycle delay and ensure the interrupt is cleared before exiting the interrupt handler. Care should be taken to ensure the compiler does not remove the read operation as an optimization. If the program can guarantee a four-cycle delay after event clear or interrupt disable another way, then a read of a register is not required.





16 Debug and trace

The debug and trace system offers a flexible and powerful mechanism for non-intrusive debugging.

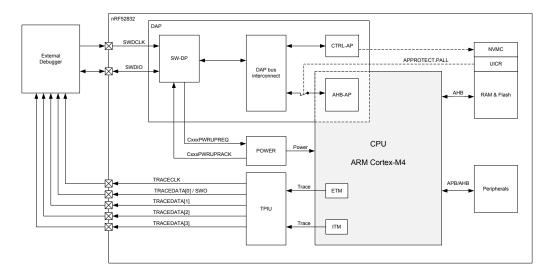


Figure 11: Debug and trace overview

The main features of the debug and trace system are:

- Two-pin Serial Wire Debug (SWD) interface
- Flash Patch and Breakpoint Unit (FPB) supports:
 - Two literal comparators
 - Six instruction comparators
- Data Watchpoint and Trace Unit (DWT)
 - Four comparators
- Instrumentation Trace Macrocell (ITM)
- Embedded Trace Macrocell (ETM)
- Trace Port Interface Unit (TPIU)
 - · 4-bit parallel trace of ITM and ETM trace data
 - · Serial Wire Output (SWO) trace of ITM data

16.1 DAP - Debug Access Port

An external debugger can access the device via the DAP.

The DAP implements a standard ARM® CoreSight™ Serial Wire Debug Port (SW-DP).

The SW-DP implements the Serial Wire Debug protocol (SWD) that is a two-pin serial interface, see SWDCLK and SWDIO in *Figure 11: Debug and trace overview* on page 72.

In addition to the default access port in the CPU (AHB-AP), the DAP includes a custom Control Access Port (CTRL-AP). The CTRL-AP is described in more detail in CTRL-AP - Control Access Port on page 73.

Important:

- The SWDIO line has an internal pull-up resistor.
- The SWDCLK line has an internal pull-down resistor.



16.2 CTRL-AP - Control Access Port

The Control Access Port (CTRL-AP) is a custom access port that enables control of the device even if the other access ports in the DAP are being disabled by the access port protection.

Access port protection blocks the debugger from read and write access to all CPU registers and memory-mapped addresses. See the UICR register *APPROTECT* on page 66 for more information about enabling access port protection.

This access port enables the following features:

- Soft reset, see Reset on page 82 for more information
- Disable access port protection

Access port protection can only be disabled by issuing an ERASEALL command via CTRL-AP. This command will erase the Flash, UICR, and RAM.

16.2.1 Registers

Table 21: Register Overview

Register	Offset	Description
RESET	0x000	Soft reset triggered through CTRL-AP
ERASEALL	0x004	Erase all
ERASEALLSTATUS	0x008	Status register for the ERASEALL operation
APPROTECTSTATUS	0x00C	Status register for access port protection
IDR	0x0FC	CTRL-AP Identification Register, IDR

RESET

Address offset: 0x000

Soft reset triggered through CTRL-AP

Bit number	31 30 2	29 28 27 26 25 24 23 22 21 20	0 19 18 17 16 15 14 13 12 11	10 9 8 7 6 5 4 3 2 1 0
Id				A
Reset 0x00000000	0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0
Id RW Field Va	lue Id Value	Description	l	
A RW RESET		Soft reset tr	riggered through CTRL-AP. See	Reset Behaviour in
		POWER cha	pter for more details.	
No	oReset 0	Reset is not	active	
Re	eset 1	Reset is acti	ive. Device is held in reset	

ERASEALL

Address offset: 0x004

Erase all

Bitı	numbe	er		31 30	29	28	27	26	25 2	24 2	23 2	2 2	1 2	0 19	18	17	16	15	14 1	.3 1	2 11	. 10	9	8	7	6	5	4	3	2 1	1 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0 (0	0 (0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Value)					0	Desc	crip	tion	1																	
Α	W	ERASEALL								Е	ras	e al	l FL	ASH	and	l RA	М														
			NoOperation	0						١	No c	per	ratio	on																	
			Erase	1						Е	ras	e al	l FL	ASH	and	l RA	М														

ERASEALLSTATUS

Address offset: 0x008

Status register for the ERASEALL operation



Bitı	numbe	er		31 30	29	28	3 27	26	25	24	23	22	21	20	19	18 1	.7 1	.6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4 3	2	1	0
Id																																Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Valu	е						Des	scri	ptic	on																		
Α	R	ERASEALLSTATUS									Sta	tus	reg	iste	r fo	r th	e E	RAS	EAL	L op	era	tior	1									
			Ready	0							ER/	ASE	ALL	is r	ead	У																
			Busy	1							ER/	ASE	ALL	is b	usy	(or	n-gc	ing)													

APPROTECTSTATUS

Address offset: 0x00C

Status register for access port protection

Bit	numbe	er		31 3	30 2	9 2	8 2	7 2	26 2	25 2	24 2	23 2	22 :	21 2	20 1	9 1	8 1	7 1	6 15	5 14	1 13	12	11	10	9 :	3 7	' 6	5	4	3	2	1 0
Id																																Α
Res	et 0x0	0000000		0	0 (0 (0 0) (0 (0 (0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe							Des	crip	otio	n																	
Α	R	APPROTECTSTATUS									9	Stat	us	regi	ste	r fo	r ac	cess	5 ро	rt p	rote	ecti	on									
			Enabled	0							A	Acc	ess	por	t pı	ote	ctic	n e	nab	led												
			Disabled	1							A	Acc	ess	por	t pr	ote	ctic	n n	ot e	nal	oled											

IDR

Address offset: 0x0FC

CTRL-AP Identification Register, IDR

Bit r	iumbe	er		31	30 2	29	28 2	7 26	5 25	24	23	22 2	21 2	0 1	9 18	3 17	16	15	14	l3 1	2 11	10	9	8 7	6	5	4	3	2 :	1 0
Id				Ε	Ε	Ε	E C	D	D	D	С	С	C (0	C	С	В	В	В	В				Α	Α	Α	Α	Α	A A	А А
Res	et 0x0	2880000		0	0	0	0 0	0	1	0	1	0	0 () 1	١ 0	0	0	0	0	0 (0	0	0	0 0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						De	scrip	tio	ı																
Α	R	APID									ΑP	Ider	tific	atio	on															
В	R	CLASS									Ac	cess	Por	t (A	P) cl	ass														
			NotDefined	0x	0						No	defi	ned	cla	SS															
			MEMAP	0x	8						Me	emor	у А	cces	s Po	ort														
С	R	JEP106ID									JEC	DEC J	EP1	06 i	iden	tity	cod	e												
D	R	JEP106CONT									JEC	DEC J	EP1	.06	cont	tinua	atio	n co	de											
Ε	R	REVISION									Re	visio	n																	

16.3 Debug interface mode

Before the external debugger can access the CPU's access port (AHB-AP) or the Control Access Port (CTRL-AP), the debugger must first request the device to power up via CxxxPWRUPREQ in the SWJ-DP.

As long as the debugger is requesting power via CxxxPWRUPREQ, the device will be in debug interface mode. If the debugger is not requesting power via CxxxPWRUPREQ, the device will be in normal mode.

Some peripherals will behave differently in debug interface mode compared to normal mode. These differences are described in more detail in the chapters of the peripherals that are affected.

When a debug session is over, the external debugger must make sure to put the device back into normal mode since the overall power consumption will be higher in debug interface mode compared to normal mode.

For details on how to use the debug capabilities please read the debug documentation of your IDE.

If the device is in System OFF when power is requested via CxxxPWRUPREQ, the system will wake up and the DIF flag in *RESETREAS* on page 85 will be set.

16.4 Real-time debug

The nRF52832 supports real-time debugging.



Real-time debugging will allow interrupts to execute to completion in real time when breakpoints are set in Thread mode or lower priority interrupts. This enables the developer to set a breakpoint and single-step through their code without a failure of the real-time event-driven threads running at higher priority. For example, this enables the device to continue to service the high-priority interrupts of an external controller or sensor without failure or loss of state synchronization while the developer steps through code in a low-priority thread.

16.5 Trace

The device supports ETM and ITM trace.

Trace data from the ETM and the ITM is sent to an external debugger via a 4-bit wide parallel trace port (TPIU), see TRACEDATA[0] through TRACEDATA[3] and TRACECLK in *Figure 11: Debug and trace overview* on page 72.

In addition to parallel trace, the TPIU supports serial trace via the Serial Wire Output (SWO) trace protocol.

Parallel and serial trace cannot be used at the same time.

ETM trace is only supported in parallel trace mode while ITM trace is supported in both parallel and serial trace modes.

For details on how to use the trace capabilities, please read the debug documentation of your IDE.

TPIU's trace pins are multiplexed with GPIOs, and SWO and TRACEDATA[0] use the same GPIO, see *Pin assignments* on page 13 for more information.

Trace speed is configured in the *TRACECONFIG* on page 108 register.

The speed of the trace pins depends on the DRIVE setting of the GPIOs that the trace pins are multiplexed with, see *PIN_CNF[14]* on page 142, *PIN_CNF[15]* on page 143, *PIN_CNF[16]* on page 144, *PIN_CNF[18]* on page 145 and *PIN_CNF[20]* on page 146. Only S0S1 and H0H1 drives are suitable for debugging. S0S1 is the default DRIVE at reset. If parallel or serial trace port signals are not fast enough in the debugging conditions, all GPIOs in use for tracing should be set to high drive (H0H1). The user shall make sure that these GPIOs' DRIVE is not overwritten by software during the debugging session.

16.5.1 Electrical specification

Trace port

Symbol	Description	Min.	Тур.	Max.	Units
T _{cyc}	Clock period, as defined by ARM (See ARM Infocenter,	62.5		500	ns
	Embedded Trace Macrocell Architecture Specification, Trace				
	Port Physical Interface, Timing specifications)				



17 Power and clock management

Power and clock management in nRF52832 is optimized for ultra-low power applications.

The core of the power and clock management system is the Power Management Unit (PMU) illustrated in *Figure 12: Power Management Unit* on page 76.

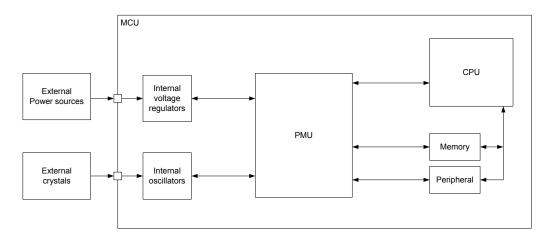


Figure 12: Power Management Unit

The user application is not required to actively control power and clock, since the PMU is able to automatically detect which resources are required by the different components in the system at any given time. The PMU will continuously optimize the system based on this information to achieve the lowest power consumption possible without user interaction.

17.1 Current consumption scenarios

As the system is being constantly tuned by the PMU, estimating the energy consumption of an application can be challenging if the designer is not able to do measurements on the hardware directly. See *Electrical specification* on page 76 for application scenarios showing average current drawn from the VDD supply.

Each scenario specifies a set of active operations and conditions applying to the given scenario. *Table 22: Current consumption scenarios, common conditions* on page 76 shows the conditions used for a scenario unless otherwise is stated in the scenario description.

Table 22: Current consumption scenarios, common conditions

Condition	Value
VDD	3 V
Temperature	25°C
CPU	WFI/WFE sleep
Peripherals	All idle
Clock	Not running
Clock Regulator	DCDC

17.1.1 Electrical specification

Current consumption: Radio

			_			
Symbol	Description	Min.	Тур.	Max.	Units	
I _{RADIO_TX0}	0 dBm TX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO		7.1		mA	
I _{RADIO_TX1}	-40 dBm TX @ 1 Mb/s Bluetooth Low Energy mode, Clock =		4.1		mA	
	HFXO					
I _{RADIO RXO}	Radio RX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO		6.5		mA	



Current consumption: Radio protocol configurations

Symbol	Description	Min.	Тур.	Max.	Units
I _{SO}	CPU running CoreMark from Flash, Radio 0 dBm TX @ 1 Mb/s		9.6		mA
	Bluetooth Low Energy mode, Clock = HFXO, Cache enabled				
I _{S1}	CPU running CoreMark from Flash, Radio RX @ 1 Mb/s		9.0		mA
	Bluetooth Low Energy mode, Clock = HFXO, Cache enabled				

Current consumption: Ultra-low power

Symbol	Description	Min.	Тур.	Max.	Units
I _{ON_RAMOFF_EVENT}	System ON, No RAM retention, Wake on any event		1.2		μΑ
I _{ON_RAMON_EVENT}	System ON, Full RAM retention, Wake on any event		1.5		μΑ
I _{ON_RAMOFF_RTC}	System ON, No RAM retention, Wake on RTC		1.9		μΑ
I _{OFF_RAMOFF_RESET}	System OFF, No RAM retention, Wake on reset		0.3		μΑ
I _{OFF_RAMOFF_GPIO}	System OFF, No RAM retention, Wake on GPIO		1.2		μΑ
I _{OFF_RAMOFF_LPCOMP}	System OFF, No RAM retention, Wake on LPCOMP		1.9		μΑ
I _{OFF_RAMOFF_NFC}	System OFF, No RAM retention, Wake on NFC field		0.7		μΑ
I _{OFF_RAMON_RESET}	System OFF, Full 64 kB RAM retention, Wake on reset		0.7		μΑ



18 POWER — Power supply

This device has the following power supply features:

- On-chip LDO and DC/DC regulators
- Global System ON/OFF modes
- Individual RAM section power control for all system modes
- Analog or digital pin wakeup from System OFF
- Supervisor HW to manage power on reset, brownout, and power fail
- Auto-controlled refresh modes for LDO and DC/DC regulators to maximize efficiency
- Automatic switching between LDO and DC/DC regulator based on load to maximize efficiency

Note: Two additional external passive components are required to use the DC/DC regulator.

18.1 Regulators

The following internal power regulator alternatives are supported:

- Internal LDO regulator
- Internal DC/DC regulator

The LDO is the default regulator.

The DC/DC regulator can be used as an alternative to the LDO regulator and is enabled through the DCDCEN on page 88 register. Using the DC/DC regulator will reduce current consumption compared to when using the LDO regulator, but the DC/DC regulator requires an external LC filter to be connected, as shown in *Figure 14: DC/DC regulator setup* on page 79.

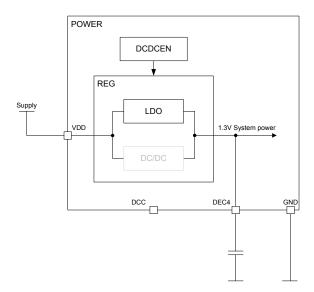


Figure 13: LDO regulator setup



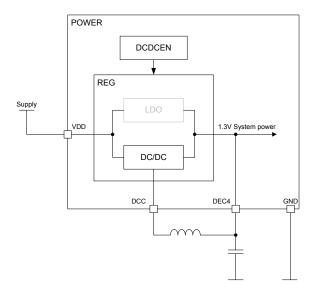


Figure 14: DC/DC regulator setup

18.2 System OFF mode

System OFF is the deepest power saving mode the system can enter. In this mode, the system's core functionality is powered down and all ongoing tasks are terminated.

The device can be put into System OFF mode using the POWER register interface. When in System OFF mode, the device can be woken up through one of the following signals:

- 1. The DETECT signal, optionally generated by the GPIO peripheral
- 2. The ANADETECT signal, optionally generated by the LPCOMP module
- 3. The SENSE signal, optionally generated by the NFC module to "wake-on-field"
- 4. A reset

When the system wakes up from System OFF mode, it gets reset. For more details, see *Reset behavior* on page 83.

One or more RAM sections can be retained in System OFF mode depending on the settings in the RAM[n].POWER registers.

RAM[n].POWER are retained registers, see *Reset behavior*. Note that these registers are usually overwritten by the startup code provided with the nRF application examples.

Before entering System OFF mode, the user must make sure that all on-going EasyDMA transactions have been completed. This is usually accomplished by making sure that the EasyDMA enabled peripheral is not active when entering System OFF.

18.2.1 Emulated System OFF mode

If the device is in debug interface mode, System OFF will be emulated to secure that all required resources needed for debugging are available during System OFF.

See *Debug and trace* on page 72 for more information. Required resources needed for debugging include the following key components: *Debug and trace* on page 72, *CLOCK* — *Clock control* on page 101, *POWER* — *Power supply* on page 78, *NVMC* — *Non-volatile memory controller* on page 29, CPU, Flash, and RAM. Since the CPU is kept on in an emulated System OFF mode, it is recommended to add an infinite loop directly after entering System OFF, to prevent the CPU from executing code that normally should not be executed.



18.3 System ON mode

System ON is the default state after power-on reset. In System ON, all functional blocks such as the CPU or peripherals, can be in IDLE or RUN mode, depending on the configuration set by the software and the state of the application executing.

Register *RESETREAS* on page 85 provides information about the source that caused the wakeup or reset.

The system can switch on and off the appropriate internal power sources, depending on how much power is needed at any given time. The power requirement of a peripheral is directly related to its activity level, and the activity level of a peripheral is usually raised and lowered when specific tasks are triggered or events are generated.

18.3.1 Sub power modes

In System ON mode, when both the CPU and all the peripherals are in IDLE mode, the system can reside in one of the two sub power modes.

The sub power modes are:

- Constant latency
- Low power

In constant latency mode the CPU wakeup latency and the PPI task response will be constant and kept at a minimum. This is secured by forcing a set of base resources on while in sleep. The advantage of having a constant and predictable latency will be at the cost of having increased power consumption. The constant latency mode is selected by triggering the CONSTLAT task.

In low power mode the automatic power management system, described in *System ON mode* on page 80, ensures the most efficient supply option is chosen to save the most power. The advantage of having the lowest power possible will be at the cost of having varying CPU wakeup latency and PPI task response. The low power mode is selected by triggering the LOWPWR task.

When the system enters System ON mode, it will, by default, reside in the low power sub-power mode.

18.4 Power supply supervisor

The power supply supervisor initializes the system at power-on and provides an early warning of impending power failure.

In addition, the power supply supervisor puts the system in a reset state if the supply voltage is too low for safe operation (brownout). The power supply supervisor is illustrated in *Figure 15: Power supply supervisor* on page 81.



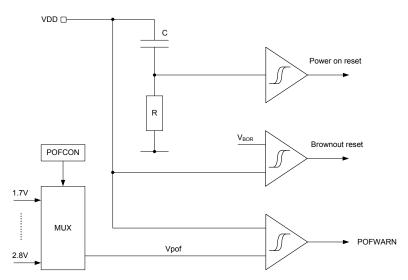


Figure 15: Power supply supervisor

18.4.1 Power-fail comparator

The power-fail comparator (POF) can provide the CPU with an early warning of impending power failure. It will not reset the system, but give the CPU time to prepare for an orderly power-down.

The comparator features a hysteresis of V_{HYST} , as illustrated in *Figure 16: Power-fail comparator (BOR = Brownout reset)* on page 81. The threshold V_{POF} is set in register *POFCON* on page 86. If the POF is enabled and the supply voltage falls below V_{POF} , the POFWARN event will be generated. This event will also be generated if the supply voltage is already below V_{POF} at the time the POF is enabled, or if V_{POF} is reconfigured to a level above the supply voltage.

If power-fail warning is enabled and the supply voltage is below V_{POF} the power-fail comparator will prevent the NVMC from performing write operations to the NVM. See NVMC - Non-volatile memory controller on page 29 for more information about the NVMC.

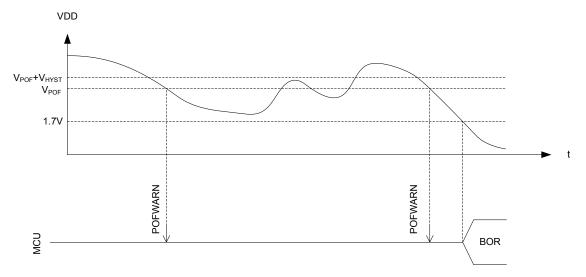


Figure 16: Power-fail comparator (BOR = Brownout reset)

To save power, the power-fail comparator is not active in System OFF or in System ON when HFCLK is not running.



18.5 RAM sections

RAM section power control is used for retention in System OFF mode and for powering down unused sections in System ON mode.

Each RAM section can power up and down independently in both System ON and System OFF mode. See chapter *Memory* on page 23 for more information on RAM sections.

18.6 Reset

There are multiple sources that may trigger a reset.

After a reset has occurred, register *RESETREAS* can be read to determine which source generated the reset.

18.6.1 Power-on reset

The power-on reset generator initializes the system at power-on.

The system is held in reset state until the supply has reached the minimum operating voltage and the internal voltage regulators have started.

A step increase in supply voltage of 300 mV or more, with rise time of 300 ms or less, within the valid supply range, may result in a system reset.

18.6.2 Pin reset

A pin reset is generated when the physical reset pin on the device is asserted.

Pin reset is configured via the *PSELRESET[0]* and *PSELRESET[1]* registers.

Note: Pin reset is not available on all pins.

18.6.3 Wakeup from System OFF mode reset

The device is reset when it wakes up from System OFF mode.

The DAP is not reset following a wake up from System OFF mode if the device is in debug interface mode. Refer to chapter *Debug and trace* on page 72 for more information.

18.6.4 Soft reset

A soft reset is generated when the SYSRESETREQ bit of the Application Interrupt and Reset Control Register (AIRCR register) in the ARM® core is set.

Refer to ARM documentation for more details.

A soft reset can also be generated via the RESET on page 73 register in the CTRL-AP.

18.6.5 Watchdog reset

A Watchdog reset is generated when the watchdog times out.

Refer to chapter WDT — Watchdog timer on page 410 for more information.

18.6.6 Brown-out reset

The brown-out reset generator puts the system in reset state if the supply voltage drops below the brownout reset (BOR) threshold.

Refer to section *Power fail comparator* on page 99 for more information.



18.7 Retained registers

A retained register is a register that will retain its value in System OFF mode and through a reset, depending on reset source. See individual peripheral chapters for information of which registers are retained for the various peripherals.

18.8 Reset behavior

Reset source	Reset target CPU	Peripherals	GPIO	Debug ^a	SWJ-DP	RAM	WDT	Retained registers	RESETREAS
CPU lockup ⁶	x	х	x						
Soft reset	x	х	x						
Wakeup from System OFF mode reset	х	x		x ⁷		x ⁸			
Watchdog reset 9	x	х	x	х		х	x	x	
Pin reset	x	x	x	x		x	x	х	
Brownout reset	X	х	X	х	х	х	x	x	X
Power on reset	х	х	х	х	х	х	х	х	х

Note: The RAM is never reset, but depending on reset source, RAM content may be corrupted.

18.9 Registers

Table 23: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40000000	POWER	POWER	Power control	

Table 24: Register Overview

Register	Offset	Description	
TASKS_CONSTLAT	0x078	Enable constant latency mode	
TASKS_LOWPWR	0x07C	Enable low power mode (variable latency)	
EVENTS_POFWARN	0x108	Power failure warning	
EVENTS_SLEEPENTER	0x114	CPU entered WFI/WFE sleep	
EVENTS_SLEEPEXIT	0x118	CPU exited WFI/WFE sleep	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
RESETREAS	0x400	Reset reason	
RAMSTATUS	0x428	RAM status register	Deprecated
SYSTEMOFF	0x500	System OFF register	
POFCON	0x510	Power failure comparator configuration	
GPREGRET	0x51C	General purpose retention register	
GPREGRET2	0x520	General purpose retention register	
RAMON	0x524	RAM on/off register (this register is retained)	Deprecated
RAMONB	0x554	RAM on/off register (this register is retained)	Deprecated
DCDCEN	0x578	DC/DC enable register	
RAM[0].POWER	0x900	RAM0 power control register	

^a All debug components excluding SWJ-DP. See *Debug and trace* on page 72 chapter for more information about the different debug components in the system.

⁶ Reset from CPU lockup is disabled if the device is in debug interface mode. CPU lockup is not possible in System OFF.

⁷ The Debug components will not be reset if the device is in debug interface mode.

RAM is not reset on wakeup from OFF mode, but depending on settings in the RAM register parts, or the whole RAM, may not be retained after the device has entered System OFF mode.

⁹ Watchdog reset is not available in System OFF.



Register	Offset	Description
RAM[0].POWERSET	0x904	RAM0 power control set register
RAM[0].POWERCLR	0x908	RAM0 power control clear register
RAM[1].POWER	0x910	RAM1 power control register
RAM[1].POWERSET	0x914	RAM1 power control set register
RAM[1].POWERCLR	0x918	RAM1 power control clear register
RAM[2].POWER	0x920	RAM2 power control register
RAM[2].POWERSET	0x924	RAM2 power control set register
RAM[2].POWERCLR	0x928	RAM2 power control clear register
RAM[3].POWER	0x930	RAM3 power control register
RAM[3].POWERSET	0x934	RAM3 power control set register
RAM[3].POWERCLR	0x938	RAM3 power control clear register
RAM[4].POWER	0x940	RAM4 power control register
RAM[4].POWERSET	0x944	RAM4 power control set register
RAM[4].POWERCLR	0x948	RAM4 power control clear register
RAM[5].POWER	0x950	RAM5 power control register
RAM[5].POWERSET	0x954	RAM5 power control set register
RAM[5].POWERCLR	0x958	RAM5 power control clear register
RAM[6].POWER	0x960	RAM6 power control register
RAM[6].POWERSET	0x964	RAM6 power control set register
RAM[6].POWERCLR	0x968	RAM6 power control clear register
RAM[7].POWER	0x970	RAM7 power control register
RAM[7].POWERSET	0x974	RAM7 power control set register
RAM[7].POWERCLR	0x978	RAM7 power control clear register

18.9.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit nun	mber			31	30 2	29 2	8 27	7 26	25 2	24 2	23 22	2 21	20	19 1	8 1	7 16	15	14	13 1	12 11	10	9	8 7	' 6	5 5	4	3	2	1 0
Id																								(В			Α	
Reset (0x00	000000		0	0	0 0	0	0	0	0	0 0	0	0	0 (0	0	0	0	0	0 0	0	0	0 () (0	0	0	0 (0 0
Id R	RW	Field	Value Id	Val	lue					0	Desci	riptio	on																
A R	RW	POFWARN								١	Write	1'1	to E	nabl	e in	terr	upt	for I	POF	WAR	N ev	ent							
										5	See E	VEN	ITS_	POF	WA	RN													
			Set	1						E	Enabl	le																	
			Disabled	0						F	Read	: Dis	able	d															
			Enabled	1						F	Read	: Ena	able	d															
B R	RW :	SLEEPENTER								١	Write	'1' t	to E	nabl	e in	terr	upt	for S	SLEE	PEN ⁻	TER	ever	nt						
										5	See E	VEN	ITS_	SLEE	PEN	NTER	?												
			Set	1						E	Enabl	le																	
			Disabled	0						F	Read	: Dis	able	d															
			Enabled	1						F	Read	: Ena	able	d															
C R	RW :	SLEEPEXIT								١	Write	1'1	to E	nabl	e in	terr	upt	for S	SLEE	PEXI	Tev	ent							
										5	See E	VEN	ITS_	SLEE	PEX	(IT													
			Set	1						E	Enabl	le																	
			Disabled	0						F	Read	: Dis	able	d															
			Enabled	1						F	Read	: Ena	able	d															

18.9.2 INTENCLR

Address offset: 0x308 Disable interrupt



Bit n	umbe	er		31	30 2	29 2	8 27	7 26	25	24	23 2:	2 2:	1 20	19	18	17	16	15 :	14 1	.3 1	2 13	10	9	8	7 (5 5	4	3	2 1	L 0
Id																									(СВ		,	Д	
Rese	t 0x0	0000000		0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0 () (0	0	0	0 0	0 (
Id	RW	Field	Value Id	Va	lue						Desc	ript	tion																	
Α	RW	POFWARN									Write	e '1'	' to [Disa	ble	inte	erru	ıpt 1	for I	OF\	WAF	RN e	ven	t						
											See E	EVE	NTS_	_PO	FW	ARN	1													
			Clear	1							Disab	ble																		
			Disabled	0							Read	l: Di	isabl	ed																
			Enabled	1							Read	l: Er	nable	ed																
В	RW	SLEEPENTER									Write	e '1'	' to [Disa	ble	inte	erru	ıpt f	for S	LEE	PEN	TER	eve	nt						
											See E	EVE	NTS_	SLE	EPE	ENT	ER													
			Clear	1							Disab	ble																		
			Disabled	0							Read	l: Di	isabl	ed																
			Enabled	1							Read	l: Er	nable	ed																
С	RW	SLEEPEXIT									Write	e '1'	' to [Disa	ble	inte	erru	ıpt f	for S	LEE	PEX	IT e	vent							
											See E	EVE	NTS_	SLE	EPE	EXIT	•													
			Clear	1							Disab	ble																		
			Disabled	0							Read	l: Di	isabl	ed																
			Enabled	1							Read	l: Er	nable	ed																

18.9.3 RESETREAS

Address offset: 0x400

Reset reason

Unless cleared, the RESETREAS register will be cumulative. A field is cleared by writing '1' to it. If none of the reset sources are flagged, this indicates that the chip was reset from the on-chip reset generator, which will indicate a power-on-reset or a brownout reset.

Bit r	numbe	er		31	30 2	29 2	28 2	7 2	6 25	5 24	1 23	3 22	2 21	20	19	18	17	16	15	14 1	.3 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id															Н	G	F	Ε											ı	ОС	В	Α
Rese	et 0x0	0000000		0	0	0	0 0) (0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 () 0	0	0
Id	RW	Field	Value Id	Va	lue						De	esci	riptic	on																		
Α	RW	RESETPIN									Re	eset	t fror	n p	in-r	ese	t de	ete	tec	l												
			NotDetected	0							No	ot d	detec	tec	t																	
			Detected	1							De	ete	cted																			
В	RW	DOG									Re	eset	t fror	n w	vatc	hdo	og d	ete	cte	d												
			NotDetected	0							No	ot d	detec	tec	t																	
			Detected	1							De	ete	cted																			
С	RW	SREQ									Re	eset	t fror	n s	oft r	ese	et d	ete	cte	t												
			NotDetected	0							No	ot d	detec	tec	t																	
			Detected	1							De	ete	cted																			
D	RW	LOCKUP									Re	eset	t fror	m C	PU I	ocl	k-up	de	tec	ted												
			NotDetected	0							No	ot d	detec	tec	t																	
			Detected	1							De	ete	cted																			
Е	RW	OFF									Re	eset	t due	to	wal	ke ι	ıp f	ron	ı Sy	ster	n O	FF r	noc	e w	hen	wal	keu	p is				
											tri	igge	ered	fro	m D	ETE	ECT	sig	nal	fror	n G	PIO										
			NotDetected	0							No	ot d	detec	tec	t																	
			Detected	1							De	ete	cted																			
F	RW	LPCOMP									Re	eset	t due	to	wal	ke ι	ıp f	ron	ı Sy	ster	n O	FF r	nod	e wl	hen	wal	keu	p is				
											tri	igge	ered	fro	m A	NA	DET	EC	T si	gnal	fro	m L	.PCC	MP								
			NotDetected	0							No	ot d	detec	tec	t																	
			Detected	1							De	ete	cted																			
G	RW	DIF									Re	eset	t due	to	wal	ke ι	ıp f	ron	ı Sy	ster	n O	FF r	nod	e wl	hen	wal	keu	p is				
											tri	igge	ered	fro	m e	nte	ring	g in	to d	ebu	ıg ir	nter	face	mo	de							
			NotDetected	0							No	ot d	detec	tec	t																	
			Detected	1							De	ete	cted																			



Bit r	numbe	r		33	1 30	29	28	3 27	7 26	5 25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id																Н	G	F	Ε												D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	V	alue	:						De	escri	ptic	n																			
Н	RW	NFC		Value								Re	set	due	to	wa	ke ı	up 1	froi	n S	yste	em (OFF	mo	de	by	NFC	fie	ld					
												de	tect																					
			NotDetected	0								No	ot de	etec	ted																			
			Detected	0 1							De	etect	ed																					

18.9.4 RAMSTATUS (Deprecated)

Address offset: 0x428 RAM status register

Since this register is deprecated the following substitutions have been made: RAM block 0 is equivalent to a block comprising RAM0.S0 and RAM1.S0, RAM block 1 is equivalent to a block comprising RAM2.S0 and RAM3.S0, RAM block 2 is equivalent to a block comprising RAM4.S0 and RAM5.S0 and RAM block 3 is equivalent to a block comprising RAM6.S0 and RAM7.S0. A RAM block field will indicate ON as long as any of the RAM sections associated with a block are on.

Bit r	numbe	er		31	30 29	9 2	8 27	26	25	24	23 2	22 2	21 20	1	9 18	3 17	7 16	15	14	13 1	2 13	10	9	8	7	6	5	4 3	3 2	1	0
Id																												0) C	В	Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	otion																		
Α	R	RAMBLOCK0									RAN	1 bl	lock () is	on	or	off/	pow	erir/	ıg up)										
			Off	0							Off																				
			On	1							On																				
В	R	RAMBLOCK1									RAN	1 bl	lock :	1 is	on	or	off/	pow	/erir	ıg up)										
			Off	0							Off																				
			On	1							On																				
С	R	RAMBLOCK2									RAN	1 bl	lock 2	2 is	on	or	off/	pow	erir/	ıg up)										
			Off	0							Off																				
			On	1							On																				
D	R	RAMBLOCK3									RAN	1 bl	lock 3	3 is	on	or	off/	pow	/erir	ıg up)										
			Off	0							Off																				
			On	1							On																				

18.9.5 SYSTEMOFF

Address offset: 0x500 System OFF register

Bit	numb	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					А
Re	set 0x	00000000		0 0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value	Paradiation.
		rieid	value iu	value	Description
Α	W	SYSTEMOFF	value id	value	Enable System OFF mode

18.9.6 POFCON

Address offset: 0x510

Power failure comparator configuration

Bit r	umbe	er		31 30 29 28 27 2	6 2	5 24	23 2	22 2	21 20	19	18	17	16 1	15 1	4 1	3 12	11	10	9 1	3 7	6	5	4	3	2 1	0
Id																							В	В	ВВ	ВА
Rese	et OxC	0000000		0 0 0 0 0	0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0 (0 0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Value			Des	crip	tion																	
Α	RW	POF					Enal	ble	or d	sabl	e po	we	r fai	ilur	e co	mpa	rato	r								
			Disabled	0			Disa	ble																		



Bitı	numbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					вввва
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Enabled	1	Enable
В	RW	THRESHOLD			Power failure comparator threshold setting
			V17	4	Set threshold to 1.7 V
			V18	5	Set threshold to 1.8 V
			V19	6	Set threshold to 1.9 V
			V20	7	Set threshold to 2.0 V
			V21	8	Set threshold to 2.1 V
			V22	9	Set threshold to 2.2 V
			V23	10	Set threshold to 2.3 V
			V24	11	Set threshold to 2.4 V
			V25	12	Set threshold to 2.5 V
			V26	13	Set threshold to 2.6 V
			V27	14	Set threshold to 2.7 V
			V28	15	Set threshold to 2.8 V

18.9.7 GPREGRET

Address offset: 0x51C

General purpose retention register

Bit	numbe	r		31	30	29	28	27	26	25 :	24	23 2	22 2	1 2	0 19	18	17	16	15 3	14 1	3 12	2 11	10	9	8	7	6	5 4	3	2	1	0
Id																										Α	Α,	4 Δ	A	Α	Α	А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cript	ion	,																	
Α	Id RW Field Value Id Value A RW GPREGRET											Gen	eral	pu	rpos	e re	eten	tior	ı reg	giste	r											

This register is a retained register

18.9.8 GPREGRET2

Address offset: 0x520

General purpose retention register

Bit n	umbe	er		31	. 30	29	28	27 :	26 :	25 :	24 :	23 2	22 2	21 2	20 :	19 1	18 1	17 1	.6 :	15 1	4 1	3 1	2 1:	1 10	9	8	7	6	5	4	3 2	2 :	1 0
Id																											Α	Α	Α	Α	A A	۱ ۸	A A
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 () () 0
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																													
Α	RW	GPREGRET		General purpose retention register																													

This register is a retained register

18.9.9 RAMON (Deprecated)

Address offset: 0x524

RAM on/off register (this register is retained)

Since this register is deprecated the following substitutions have been made: RAM block 0 is equivalent to a block comprising RAM0.S0 and RAM0.S1 and RAM block 1 is equivalent to a block comprising RAM1.S0 and RAM1.S1. For new designs it is recommended to use the POWER.RAM-0.POWER and its sibling registers instead.

Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			D C B A
Reset 0x00000003		0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
A RW ONRAMO			Keep RAM block 0 on or off in system ON Mode
	RAM0Off	0	Off



Bit	numb	er		31	30 2	9 2	8 27	7 26	25	24 :	23 2	2 21	20	19	18	17	16	15 3	L4 1	3 12	11	10	9	8	7	6 !	5 4	3	2	1 0
Id																D	С													ВА
Res	et 0x0	00000003		0	0 (0	0 0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0 ()	0 (0	0	0	1 1
Id	RW	Field	Value Id	Val	ue					ı	Desc	ripti	on																	
			RAM0On	1						(On																			
В	RW	ONRAM1								- 1	Keep	RAN	√l b	lock	10	on d	r of	f in	syst	em (I NC	Mod	le							
			RAM1Off	0						(Off																			
			RAM10n	1						(On																			
С	RW	OFFRAM0								-	Keep	rete	enti	on (on f	RAN	1 blo	ock	0 wl	nen I	RAN	1 blo	ock	is sv	vito	hec	off			
			RAM0Off	0						(Off																			
			RAM0On	1						(On																			
D	RW	OFFRAM1								ı	Keep	rete	enti	on (on f	RAN	1 blo	ock	1 wl	nen I	RAN	1 blo	ock	is sv	vito	hec	off			
			RAM1Off	0						(Off																			
			RAM10n	1						(On																			

18.9.10 RAMONB (Deprecated)

Address offset: 0x554

RAM on/off register (this register is retained)

Since this register is deprecated the following substitutions have been made: RAM block 2 is equivalent to a block comprising RAM2.S0 and RAM2.S1 and RAM block 3 is equivalent to a block comprising RAM3.S0 and RAM3.S1. For new designs it is recommended to use the POWER.RAM-0.POWER and its sibling registers instead.

Bit r	numbe	er		31	30 29	2	8 27	7 26	5 25	24	23 2	2 2	1 20) 1:	9 18	17	16	15	14	13	12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id																D	С														В	Α
Rese	et 0x0	0000003		0	0 0	(0 0	0	0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	1	1
Id	RW	Field	Value Id	Va	lue						Desc	rip	tion																			
Α	RW	ONRAM2									Keep	R/	AM b	olo	ck 2	on	or c	ff i	ı sy	/ste	m C	N I	Mod	de								
			RAM2Off	0							Off																					
			RAM2On	1							On																					
В	RW	ONRAM3									Keep	R/	AM b	olo	ck 3	on	or c	ff ii	ı sy	/ste	m C	N I	Mod	de								
			RAM3Off	0							Off																					
			RAM3On	1							On																					
С	RW	OFFRAM2									Keep	re	tent	ion	n on	RAI	M b	lock	ر 2	whe	n R	ΑN	1 blo	ock	is s	wit	che	d off				
			RAM2Off	0							Off																					
			RAM2On	1							On																					
D	RW	OFFRAM3									Keep	re	tent	ion	n on	RAI	M b	lock	3	whe	n R	ΑN	1 blo	ock	is s	wit	che	d off				
			RAM3Off	0							Off																					
			RAM3On	1							On																					

18.9.11 DCDCEN

Address offset: 0x578 DC/DC enable register

Bitı	numbe	er		3	1 30	29	9 2	8 2	7 2	26	25	24	23	22	21	20	19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	٧	alu	е							De	scri	pti	on																			
Α	RW	DCDCEN											Ena	ble	01	di	sab	le I	DC/I	OC (conv	/ert	er												
			Disabled	0									Dis	abl	e																				
			Enabled	1									Ena	ble	9																				

18.9.12 RAM[0].POWER

Address offset: 0x900

RAM0 power control register



Bit num	nber		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Reset 0	x0000FFFF		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id R	W Field	Value Id	Value	Description
A R	W SOPOWER			Keep RAM section S0 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in SORETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
B R\	W S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in S1RETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
C R\	W SORETENTION			Keep retention on RAM section S0 when RAM section is in OFF
		Off	0	Off
		On	1	On
D R	W S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
		Off	0	Off
		On	1	On

18.9.13 RAM[0].POWERSET

Address offset: 0x904

RAM0 power control set register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	30 2	9 2	28 27	7 2	6 25	24	23 2	22 :	21 2	0 1	9 1	8 1	7 1	5 15	5 14	13	12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id																[) (:													В	3 A
Res	et 0x0	000FFFF		0	0 (0	0 0) (0	0	0	0	0 () (0 0) (0	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1
Id	RW	Field	Value Id	Va	lue						Des	crip	ptior	1																		
Α	W	SOPOWER									Kee	рR	AM	sec	tion	SC	of	RAN	/10 d	on c	or o	ff in	Sys	ten	n O	Νn	nod	e				
			On	1							On																					
В	W	S1POWER									Kee	p R	MA	sec	tion	S1	of.	RAN	/10 d	on c	or o	ff ir	Sys	ten	n O	Νn	nod	e				
			On	1							On																					
С	W	SORETENTION									Kee	p re	eten	tio	n on	R/	MA	sect	ion	S0	wh	en F	RAM	se	ctio	n is						
											swit	tche	ed o	ff																		
			On	1							On																					
D	W	S1RETENTION									Kee	p re	eten	tio	n on	R/	MA	sect	ion	S1	wh	en F	RAM	se	ctio	n is						
											swit	tche	ed o	ff																		
			On	1							On																					

18.9.14 RAM[0].POWERCLR

Address offset: 0x908

RAM0 power control clear register

Bit r	numbe	er		31	30	29	28 2	27 2	26 2	25 2	24 :	23 2	2 2	1 2	0 1	9 1	8 17	7 16	5 15	14	13	12 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id																	D	С														ВА
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0 0) () () (0	0	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	tior	1																	
Α	W	SOPOWER									ı	Kee	o RA	M:	sec	tior	S0	of I	RAN	10 o	n oı	off	in S	yste	m C)N r	noc	le				
			Off	1							(Off																				
В	W	S1POWER									ı	Kee	o RA	M:	sec	tior	S1	of I	RAN	10 o	n oı	off	in S	yste	m C)N r	noc	le				



Bit	numbe	er		31	30	29	28 2	27	26	25	24	23	22	2 2:	1 20	0 1	9 1	8 1	7 10	5 15	5 14	1 13	12	11	10	9	8 7	7 (5 5	4	3	2	1	0
Id																		D) C														В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	() (0	0	1	1	1	1	1	1	1	1 :	L :	l 1	. 1	. 1	1	1	1
Id	RW	Field	Value Id	Va	lue							De	SCI	ript	tion																			
			Off	1								Of	f																					
С	W	SORETENTION										Ke	ер	ret	tent	ior	or	RA	M	ect	ion	SO	whe	n R	AM	sec	tion	is						
												SW	itc	hec	d of	f																		
			Off	1								Of	f																					
D	W	S1RETENTION										Ke	ер	ret	tent	ior	n on	RA	M	ect	ion	S1	whe	n R	AM	sec	tion	is						
												SW	itc	hec	d of	f																		
			Off	1								Of	f																					

18.9.15 RAM[1].POWER

Address offset: 0x910

RAM1 power control register

Bitı	numbe	er		31	30	29	28	27	26	25	24	1 23	22	21 2	0 1	19 18	3 1	7 1	6 1	.5 1	L4 1	13 1	2 1:	l 10	9	8	7	6	5 4	1 3	2	1	0
Id																	- [) (2													В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0 0	(0)	1	1	1 1	1	1	1	1	1	1	1 :	l 1	1	1	1
Id	RW	Field	Value Id	Va	lue							De	scri	iptio	n																		
Α	RW	SOPOWER										Kee	ep I	RAM	sec	tion	SC	00	l o	r Ol	FF i	n Sy	ster	10 m	N m	ode							
												RAI	M s	sectio	ns	are	alv	vays	re	tai	nec	l wh	en (ON, I	but	can	als	o be	e				
												ret	ain	ed w	her	n OF	Fd	ере	nd	ent	t on	the	set	ting	s in	SOF	RETE	NT	ION				
												All	RA	M se	ctic	ons v	vill	be	OF	F ir	ı Sy	ster	n O	FF m	ode	.							
			Off	0								Off																					
			On	1								On																					
В	RW	S1POWER										Kee	ep I	RAM	sec	tion	S1	. 01	l 0	r Ol	FF i	n Sy	ster	n Ol	N m	ode							
												RAI	M s	sectio	ns	are	alv	vays	re	tai	nec	l wh	en (ON, I	but	can	als	b be	9				
												ret	ain	ed w	her	n OF	Fd	ере	nd	ent	t on	the	set	ting	s in	S1F	RETE	NT	ION				
												All	RA	M se	ctic	ons v	vill	be	OF	F ir	ı Sy	ster	n O	FF m	ode	<u>.</u>							
			Off	0								Off																					
			On	1								On																					
С	RW	SORETENTION										Kee	ері	reten	tio	n on	RA	M	sec	tio	n S) wh	nen	RAN	1 se	ctio	n is	in (OFF				
			Off	0								Off																					
			On	1								On																					
D	RW	S1RETENTION										Kee	ер і	reten	tio	n on	RA	M/	sec	tio	n S	1 wh	nen	RAN	1 se	ctio	n is	in (OFF				
			Off	0								Off																					
			On	1								On																					

18.9.16 RAM[1].POWERSET

Address offset: 0x914

RAM1 power control set register

Bitı	numbe	er		3:	1 30	29	28	3 27	7 26	5 25	5 24	4 2	3 2	22 2	21 2	20	19	18	3 17	10	5 1	5 1	4 1	.3 1	.2 :	11	10	9	8	7	6	5	4	3	2	1	0
Id																			D	C																В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	() (0	0	0	0	0	0	0	1	۱ :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	V	alue	:						D	es	crip	otio	n																					
Α	W	SOPOWER										K	eel	p R.	ΑM	se	cti	on	S0	of	RA	М1	on	or	off	in	Sys	ten	n O	N r	noc	le					
			On	1								0	n																								
В	W	S1POWER										K	eel	p R	ΑM	se	cti	on	S1	of	RA	М1	on	or	off	in	Sys	ten	n O	N r	noc	le					
			On	1								0	n																								
С	W	SORETENTION										K	eel	p re	eter	ntic	on (on	RA	M s	sec	tio	n S() w	her	n R	AΜ	se	ctio	n is	5						
												S١	wit	che	ed c	off																					
			On	1								0	n																								



Bit r	numbe	er		33	1 30	29	28	8 27	7 26	25	24	23	22	21	20	19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	С															В	Α
Res	et 0x0	000FFFF		0 0 0 0 0 0 0 0									0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id									De	scr	ipti	on																				
D	W	S1RETENTION										Ke	ер	rete	enti	on	on	RAI	M s	ecti	ion	S1	wh	en F	AN	se	ctic	n is	,						
												SW	itcl	hed	off																				
			On	1								On																							

18.9.17 RAM[1].POWERCLR

Address offset: 0x918

RAM1 power control clear register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	. 30	29	28	27	26 :	25 2	24 2	23 2	2 2	21 2	0 1	9 1	8 1	.7 1	16 1	15 1	.4 1	3 12	2 11	10	9	8	7	6	5	4	3	2 1	1 0
Id																	- 1)	С													E	3 A
Res	et 0x0	0000FFFF		0	0	0	0	0	0	0	0	0 (0	0 ()	0 () (0	0	1	1 :	l 1	. 1	1	1	1	1	1	1	1	1	1 1	1 1
Id	RW	Field	Value Id	Va	lue							Desc	crip	tio	1																		
Α	W	SOPOWER									k	(eep	o R	AΜ	sec	tio	n SC	of	RA	M1	on	or c	off in	Sy:	ster	n O	Νn	nod	le				
			Off	1							(Off																					
В	W	S1POWER									k	(eep	o R	ΑM	sec	tio	ո S 1	L of	RA	M1	on	or c	off in	Sy:	ster	n O	Νn	nod	le				
			Off	1							(Off																					
С	W	SORETENTION									k	(eep	o re	ten	tio	n or	n RA	٩M	sec	tio	n SC) wh	en l	RAN	1 se	ctic	n is	5					
											S	wit	che	ed o	ff																		
			Off	1							(Off																					
D	W	S1RETENTION									k	(eep	o re	ten	tio	n or	n RA	٩M	sec	tio	n S1	. wh	en l	RAN	1 se	ctic	n is	S					
											S	wit	che	ed o	ff																		
			Off	1							(Off																					

18.9.18 RAM[2].POWER

Address offset: 0x920

RAM2 power control register

Id			21	JU 2		.0 27	20 2	25 2	4 23	3 2	2 21	20	19	18	1/1	16 1	15 1	4 1:	3 12	11	10	9 8	5 /	6	5 4	- 3	2	1 0
iu															D	С												ВА
Reset 0x0	000FFFF		0	0	0 (0 0	0	0 (0 0	C	0 0	0	0	0	0	0	1 :	1 1	1	1	1	1 1	1	1	1 1	. 1	1	1 1
ld RW	Field	Value Id	Va	lue					D	esc	ripti	on																
A RW	SOPOWER								Ke	eep	RAN	VI se	ectio	n S	0 0	Νo	r Ol	F in	Sys	tem	ON	mod	de.					
									RA	٩M	1 sect	tion	s ar	e al	way	s re	etaiı	ned	whe	n O	N, bı	ut ca	an al	so b	e			
									re	tai	ined	whe	en C	FF (dep	end	lent	on	the s	sett	ings	in S	ORET	ENT	ION			
									Αl	II R	AM s	sect	ions	wil	ll be	OF	F in	Sys	tem	OFI	F mo	de.						
		Off	0						Of	ff																		
		On	1						0	n																		
B RW	S1POWER								Ke	eep	RAN	M se	ectio	n S	1 0	Νo	r Ol	F in	Sys	tem	ON	mod	de.					
									RA	٩M	1 sect	tion	s ar	e al	way	s re	etaiı	ned	whe	n O	N, bı	ut ca	an al	so b	e			
									re	tai	ined	whe	en C	FF (dep	end	lent	on	the s	sett	ings	in S	1RET	ENT	ION			
									Αl	II R	AM s	sect	ions	wil	ll be	OF	F in	Sys	tem	OFI	F mo	de.						
		Off	0						0	ff																		
		On	1						0	n																		
C RW	SORETENTION								Ke	eep	rete	enti	on c	n R	AM	sec	ctio	n SO	whe	en R	AM:	sect	ion i	s in	OFF			
		Off	0						0	ff																		
		On	1						0	n																		
D RW	S1RETENTION								Ke	eep	rete	enti	on c	n R	AM	sec	tio	n S1	whe	en R	AM:	sect	ion i	s in	OFF			
		Off	0						O	ff																		
		On	1						0	n																		



18.9.19 RAM[2].POWERSET

Address offset: 0x924

RAM2 power control set register

When read, this register will return the value of the POWER register.

Bitı	numbe	er		31	30 2	29 2	28 2	7 26	5 25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 1	.0 9	Э	8	7 (5 5	5 4	3	2	1	0
Id																	D	С														В	Α
Res	et OxO	0000FFFF		0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1 :	1	1 :	L :	L 1	L 1	. 1	1	1	1
Id	RW	Field	Value Id	Va	lue						De	scri	iptio	on																			
Α	W	SOPOWER									Ke	ep l	RAN	1 se	ecti	on:	S0 (of R	AM	2 o	n or	off	in S	syst	em	ON	mo	ode					
			On	1							On	1																					
В	W	S1POWER									Ke	ep I	RAN	1 se	ecti	on:	S1 (of R	AM	2 o	n or	off	in S	Syst	em	ON	mo	ode					
			On	1							On	1																					
С	W	SORETENTION									Ke	ері	rete	ntio	on (on l	RAI	VI s	ecti	on S	0 w	her	n RA	M	sec	tior	is						
											sw	itch	ned	off																			
			On	1							On	1																					
D	W	S1RETENTION									Ke	ері	rete	ntio	on (on l	RAI	VI s	ecti	on S	1 w	her	n RA	M	sec	tior	is						
											sw	itch	ned	off																			
			On	1							On	1																					

18.9.20 RAM[2].POWERCLR

Address offset: 0x928

RAM2 power control clear register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	30 2	29 :	28 2	7 2	6 25	5 24	4 23	22	21 2	20	19	18	17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5	4 3	2	1	0
Id																	D	С													В	Α
Res	et 0x0	000FFFF		0	0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	1	1	1 :	L 1	. 1	1	1	1	1	1	1 1	. 1	1	1
Id	RW	Field	Value Id	Va	lue						De	scr	iptio	n																		
Α	W	SOPOWER									Ke	ер І	RAM	se	ctio	on S	50 c	of R	AΜ	2 or	or	off i	n Sy	ste	m O	Νn	node	е				
			Off	1							Of	f																				
В	W	S1POWER									Ke	ер І	RAM	se	ctio	on S	51 c	of R	ΑM	2 or	or	off i	n Sy	ste	m O	Νn	node	е				
			Off	1							Of	f																				
С	W	SORETENTION									Ke	ер	reter	ntic	on o	on f	RAN	∕l se	ctio	n S) wl	nen	RAI	∕l se	ctic	n is						
											sw	itch	ned c	ff																		
			Off	1							Of	f																				
D	W	S1RETENTION									Ke	ер	reter	ntic	on o	on f	RAN	∕l se	ctio	n S	1 wl	nen	RAI	∕l se	ctic	n is						
											SW	itch	ned c	off																		
			Off	1							Of	f																				

18.9.21 RAM[3].POWER

Address offset: 0x930

RAM3 power control register

Bit r	numbe	er		31	L 30	29	28	8 27	7 2	26 2	25	24	23	22	2 21	1 20	19	9 18	3 1	7 1	6 1	.5 1	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																			D) (2															В	Α
Res	et 0x0	000FFFF		0	0	0	0	0 ()	0 (0	0	0	0	0	0	0	0	0	()	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	alue	:							De	SCI	ript	ion																					
Α	RW	SOPOWER												·															ode can		so l	эe					
													ret	taiı	ned	wh	en	OF	F d	ере	end	ent	t or	n th	ie s	etti	ngs	in	SOF	RET	EN	TIO	N.				
													All	R/	MΑ	sec	tio	ns v	vill	be	OF	F ir	n Sy	/ste	m	OFF	m	ode	2.								
			Off	0									Off	f																							
			On	1									On	1																							
В	RW	S1POWER											Ke	ер	RA	M s	ect	ion	S1	10	N O	r O	FF i	in S	yst	em	O١	l m	ode	.							



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		D C
Reset 0x0000FFFF		0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
		RAM sections are always retained when ON, but can also be
		retained when OFF dependent on the settings in S1RETENTION.
		All RAM sections will be OFF in System OFF mode.
	Off	0 Off
	On	1 On
C RW SORETENTI	ON	Keep retention on RAM section SO when RAM section is in OFF
	Off	0 Off
	On	1 On
D RW S1RETENTI	ON	Keep retention on RAM section S1 when RAM section is in OFF
	Off	0 Off
	On	1 On

18.9.22 RAM[3].POWERSET

Address offset: 0x934

RAM3 power control set register

When read, this register will return the value of the POWER register.

Bit	numbe	er		31	30	29	28	27	26 2	25 2	4 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id																	D	С														Е	3 A
Res	et 0x0	000FFFF		0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1 1
Id	RW	Field	Value Id	Va	alue						D	escri	ptic	n																			
Α	W	SOPOWER									Ke	eep l	RAN	l se	ctic	n S	о 0	f R	٩M	3 or	or	off	in	Sys	ten	n O	Νn	nod	e				
			On	1							0	n																					
В	W	S1POWER									Ke	eep l	RAN	l se	ctic	on S	1 o	f R	٩M	3 or	or	off	in	Sys	ten	n O	Νn	nod	e				
			On	1							0	n																					
С	W	SORETENTION									Ke	еер	ete	ntic	on c	n F	RAN	1 se	ctic	on S	0 w	he	n R	ΑM	se	ctio	n is						
											SV	vitch	ed (off																			
			On	1							0	n																					
D	W	S1RETENTION									Ke	еер	ete	ntic	on c	n F	RAN	1 se	ctic	on S	1 w	he	n R	AM	se	ctio	n is						
											SV	vitch	ed o	off																			
			On	1							0	n																					

18.9.23 RAM[3].POWERCLR

Address offset: 0x938

RAM3 power control clear register

Bit r	numbe	er		31	30	29 :	28 2	7 2	6 2	5 24	1 23	3 22	21	20	19	18	17	16	15	14 :	L3 1	.2 1	1 1	9	8	7	6	5	4	3 2	2 1	0
Id																	D	С													В	Α
Rese	et OxO	0000FFFF		0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	1	1	1	1 1	L 1	. 1	1	1	1	1	1	1 1	l 1	1
Id	RW	Field	Value Id	Va	lue						D	escr	iptic	n																		
Α	W	SOPOWER									Ke	еер	RAN	1 se	ctic	n S	о 0	f R	AΜ	3 or	or	off	in S	yste	m C	ı NC	nod	e				
			Off	1							0	ff																				
В	W	S1POWER									Ke	еер	RAN	1 se	ctic	n S	1 o	f R	AΜ	3 or	or	off	in S	yste	m C	ı NC	nod	e				
			Off	1							0	ff																				
С	W	SORETENTION									Ke	еер	rete	ntic	n o	n F	RΑN	1 se	ctio	on S) w	hen	RA	M s	ectio	on i	S					
											sv	witch	ned (off																		
			Off	1							0	ff																				
D	W	S1RETENTION									Ke	еер	rete	ntic	n o	n F	RAN	1 se	ctio	on S	1 w	hen	RA	M s	ectio	on i	S					
											SV	witch	ned (off																		
			Off	1							0	ff																				



18.9.24 RAM[4].POWER

Address offset: 0x940

RAM4 power control register

	numbe	er		31 30	29	28 27	7 26	5 25	24 2	23	22 2	21 2	0 1	.9 18			15	14	13 1	2 1:	10	9	8	7	6 5	4	3	_	1 0
Id															D) C													ВА
Res	et 0x0	000FFFF		0 0	0	0 0	0	0	0	0	0	0 () (0 0	0	0	1	1	1 :	l 1	1	1	1	1	1 1	. 1	1	1	1 1
Id	RW	Field	Value Id	Value					ı	Des	scrip	ptior	1																
Α	RW	SOPOWER							ŀ	Kee	ep R	RAM	sec	tion	S0	ON	or (OFF	in Sy	ster	n Ol	N m	ode						
									ı	RAI	M se	ectio	ns	are a	alw	ays	reta	ine	d wh	en (ON,	but	can	also	be				
									1	ret	aine	ed w	hen	OFF	F de	eper	nde	nt o	n the	e set	ting	s in	SOR	ETE	NTI	ON.			
									1	ΑII	RAN	VI se	ctio	ns w	vill	be C	OFF	in S	/ster	n O	Fm	ode	.						
			Off	0					(Off																			
			On	1					(On																			
В	RW	S1POWER							ŀ	Kee	ep R	RAM	sec	tion	S1	ON	or (OFF	in Sy	ster	n Ol	N m	ode						
									ı	RAI	M se	ectio	ns	are a	alw	ays	reta	ine	d wh	en (ON,	but	can	also	be				
									1	ret	aine	ed w	hen	OFF	F de	eper	nde	nt o	n the	e set	ting	s in	S1R	ETE	NTI	ON.			
									,	All	RAN	M se	ctio	ns w	vill	be C	OFF	in S	/ster	n O	Fm	ode	<u>.</u>						
			Off	0					(Off																			
			On	1					(On																			
С	RW	SORETENTION							ı	Kee	ep re	eten	tior	n on	RA	M s	ecti	on S	0 wl	nen	RAN	1 se	ctio	n is	in O	FF			
			Off	0					(Off																			
			On	1					(On																			
D	RW	S1RETENTION							ı	Kee	ep re	eten	tior	n on	RA	M s	ecti	on S	1 wl	nen	RAN	1 se	ctio	n is	in O	FF			
			Off	0					(Off																			
			On	1					(On																			

18.9.25 RAM[4].POWERSET

Address offset: 0x944

RAM4 power control set register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	30	29	28 2	27 2	26 2	5 2	4 2	23 2	2 21	L 20	19	9 18	3 17	7 16	5 15	14	13	12 :	l1 1	.0 9) 8	3 7	6	5	4	3	2 :	1 0
Id																	D	С													E	3 A
Res	et 0x0	000FFFF		0	0	0	0	0	0 (0)	0 (0	0	0	0	0	0	1	1	1	1	1	1 1		L 1	. 1	1	1	1	1 1	l 1
Id	RW	Field	Value Id	Va	lue						0	Desc	ript	ion																		
Α	W	SOPOWER									K	(eep	RA	M s	ect	tion	S0	of I	RAN	14 o	n oı	off	in S	yste	em	ON	mo	de				
			On	1							C	On																				
В	W	S1POWER									K	(eep	RA	M s	ect	tion	S1	of I	RAIV	14 o	n oı	off	in S	yste	em	ON	mo	de				
			On	1							C	On																				
С	W	SORETENTION									K	(eep	ret	ent	ion	on	RA	M s	ecti	on S	50 v	hei	n RA	M s	ect	ion	is					
											S	wite	chec	off	f																	
			On	1							C	On																				
D	W	S1RETENTION									K	(eep	ret	ent	ion	on	RA	M s	ecti	on S	51 v	hei	n RA	M s	ect	ion	is					
											S	wite	chec	off	f																	
			On	1							C	On																				

18.9.26 RAM[4].POWERCLR

Address offset: 0x948

RAM4 power control clear register



Bit r	numbe	er		31	30	29 :	28 2	7 2	6 2	5 24	4 2	3 22	2 21	20	19	18	3 17	' 16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id																	D	С														В	Α
Res	et 0x0	000FFFF		0	0	0	0 (0 (0 0	0	(0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	lue						D	esci	ripti	on																			
Α	W	SOPOWER									K	еер	RAN	VI se	ecti	ion	S0	of F	RAN	14 o	n o	r of	f in	Sys	ten	10 r	۷n	ode	е				
			Off	1							О	ff																					
В	W	S1POWER									K	еер	RAN	VI se	ecti	ion	S1	of F	RAN	14 o	n o	r of	f in	Sys	ten	10 r	۱m	ode	е				
			Off	1							C	ff																					
С	W	SORETENTION									K	eep	rete	enti	on	on	RA	M s	ecti	on :	S0 v	vhe	n R	AM	sec	ctio	n is						
											S	witc	hed	off																			
			Off	1							С	ff																					
D	W	S1RETENTION									K	eep	rete	enti	on	on	RA	M s	ecti	on !	S1 ν	vhe	n R	AM	sec	tio	n is						
											S	witc	hed	off																			
			Off	1							C	ff																					

18.9.27 RAM[5].POWER

Address offset: 0x950

RAM5 power control register

	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 1	
Id			D C	ВА
Res	set 0x0000FFFF		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW Field	Value Id	Value Description	
Α	RW SOPOWER		Keep RAM section S0 ON or OFF in Sy	ystem ON mode.
			RAM sections are always retained wh	nen ON, but can also be
			retained when OFF dependent on the	e settings in SORETENTION.
			All RAM sections will be OFF in System	m OFF mode.
		Off	0 Off	
		On	1 On	
В	RW S1POWER		Keep RAM section S1 ON or OFF in Sy	ystem ON mode.
			RAM sections are always retained wh	nen ON, but can also be
			retained when OFF dependent on the	e settings in S1RETENTION.
			All RAM sections will be OFF in System	m OFF mode.
		Off	0 Off	
		On	1 On	
С	RW SORETENTION		Keep retention on RAM section S0 w	hen RAM section is in OFF
		Off	0 Off	
		On	1 On	
D	RW S1RETENTION		Keep retention on RAM section S1 w	hen RAM section is in OFF
		Off	0 Off	
		On	1 On	

18.9.28 RAM[5].POWERSET

Address offset: 0x954

RAM5 power control set register

Bit	numbe	er		31 30	29	28 2	27 2	26 2	5 24	4 23	3 22	21	20	19	18	17	16	15 1	L4 1	.3 1	2 11	. 10	9	8	7	6	5 4	4 3	2	1	0
Id																D	С													В	Α
Res	et 0x0	000FFFF		0 0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	1	1	1 1	. 1	1	1	1	1	1	1 :	1 1	1	1	1
Id	RW	Field	Value Id	Value						D	escr	ipti	on																		
Α	W	SOPOWER								K	еер	RAN	VI se	ectio	on S	о 0	f RA	M5	on	or (off in	Sy:	sten	n ON	N m	ode	:				
			On	1						0	n																				
В	W	S1POWER								Ke	еер	RAN	VI se	ectio	on S	1 o	f RA	M5	on	or o	off in	Sy:	sten	n ON	N m	ode	:				
			On	1						0	n																				



Bit	numbe	er		33	1 30	29	2	8 27	7 2	26 2	25	24	23	22	21	20	19	9 1	8 1	7 1	.6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																			ı)	С															В	Α
Res	et 0x0	0000FFFF		0	0	0	C	0)	0	0	0	0	0	0	0	0	C) (0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	V	alue								De	scr	ipti	on																					
С	W	SORETENTION											Ke	ер	rete	nti	ion	on	RA	٩M	se	ctio	on S	60 v	vhe	n F	RAN	∕l se	ecti	on i	S						
													sw	itch	ned	off	f																				
			On	1									On																								
D	W	S1RETENTION											Ke	ер	rete	nti	ion	on	R	٩M	se	ctio	on S	51 ۷	vhe	n F	RAN	/I se	ecti	on i	S						
													sw	itch	ned	off	f																				
			On	1									On																								

18.9.29 RAM[5].POWERCLR

Address offset: 0x958

RAM5 power control clear register

When read, this register will return the value of the POWER register.

Bitı	numbe	er		31	30 2	29 2	28 2	7 2	6 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id																	D	С														В	Α
Res	et 0x0	000FFFF		0	0	0	0 0) (0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Va	lue						D	escr	iptio	on																			
Α	W	SOPOWER									K	еер	RAN	∕l se	ecti	on:	SO o	of R	ΑM	5 о	n o	r of	f in	Sys	ten	10 r	۱m	node	е				
			Off	1							0	ff																					
В	W	S1POWER									K	еер	RAN	∕l se	ecti	on:	S1 (of R	ΑM	5 o	n o	r of	f in	Sys	ten	10 r	۱m	node	е				
			Off	1							0	ff																					
С	W	SORETENTION									K	еер	rete	nti	on (on I	RAI	VI s	ecti	on :	S0 v	vhe	n R	ΑM	se	tio	ı is						
											S۷	witcl	ned	off																			
			Off	1							0	ff																					
D	W	S1RETENTION									Ke	еер	rete	nti	on (on l	RAI	VI s	ecti	on !	S1 ۷	vhe	n R	AM	se	tio	ı is						
											SV	witcl	ned	off																			
			Off	1							0	ff																					

18.9.30 RAM[6].POWER

Address offset: 0x960

RAM6 power control register

	number		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Res	et 0x0000FFFF		0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW Field	Value Id	Value	Description
Α	RW SOPOWER			Keep RAM section S0 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in SORETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
В	RW S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in S1RETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
С	RW SORETENTION			Keep retention on RAM section S0 when RAM section is in OFF
		Off	0	Off
		On	1	On
D	RW S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
		Off	0	Off



Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			D C
Reset 0x0000FFFF		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value	Description
	On	1	On

18.9.31 RAM[6].POWERSET

Address offset: 0x964

RAM6 power control set register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	30	29 :	28 2	7 2	6 2	5 2	4 2	3 22	2 2:	1 20	0 1	9 1	8 1	17 1	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		D	С															В	Α
Res	et 0x0	0000FFFF		0	0	0	0 (0	0 (0	(0 0	0	0	(0 (0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	lue						D	esc	ript	ion																					
Α	W	SOPOWER									K	еер	RA	M s	sec	tior	n S(of C	R/	١M	6 o	n o	r of	ff in	Sys	ter	n O	N r	nod	e					
			On	1							C)n																							
В	W	S1POWER									K	еер	RA	M s	sec	tior	n Si	1 of	R/	MA	6 o	n o	r of	ff in	Sys	ter	n O	N r	nod	e					
			On	1							C	n																							
С	W	SORETENTION									K	еер	ret	ent	ior	n or	n R	ΑM	se	ctic	on S	60 v	vhe	en F	RAIV	l se	ctic	n is	S						
											S	witc	chec	d of	f																				
			On	1							C	n																							
D	W	S1RETENTION									K	еер	ret	ent	ior	n or	n R	ΑM	se	ctic	on S	51 ۷	vhe	en F	RAIV	l se	ctic	n is	S						
											S	witc	chec	d of	f																				
			On	1							C	n																							

18.9.32 RAM[6].POWERCLR

Address offset: 0x968

RAM6 power control clear register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	. 30 2	9 :	28 2	7 2	6 2	5 2	4 2	3 2	2 2	21 2	0 1	19 1	18 :	17	16	15	14	13 :	12 :	11 :	.0	9 .	8 7	7 (6	5 -	4 3	2	1	0
Id																		D	С														В	Α
Res	et 0x0	0000FFFF		0	0	0	0 () (0 0) () (0	0	0 (0	0	0	0	0	1	1	1	1	1	1	1	1 :	1 1	1	1	1 1	. 1	1	1
Id	RW	Field	Value Id	Va	lue						D	esc	rip	otion	n																			
Α	W	SOPOWER									K	eep	R	AM	sec	ctio	n S	0 о	f R	٩M	6 oı	or	off	in S	yst	em	ON	mo	ode	è				
			Off	1							C	ff																						
В	W	S1POWER									K	eep	R/	AM	sec	ctio	n S	1 o	f R	٩M	6 oı	or	off	in S	yst	em	ON	mo	ode	è				
			Off	1							C	ff																						
С	W	SORETENTION									K	eep	re	eten	tio	n o	n R	ΑN	1 se	ctio	on S	0 w	her	n RA	M	sec	tion	is						
											S	wite	che	ed o	ff																			
			Off	1							C	ff																						
D	W	S1RETENTION									K	eep	re	eten	tio	n o	n R	ΑN	1 se	ctio	on S	1 w	her	n RA	M	sec	tion	is						
											S	wite	che	ed o	ff																			
			Off	1							C	ff																						

18.9.33 RAM[7].POWER

Address offset: 0x970

RAM7 power control register

Bit r	number	31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Id			D C B	Α
Res	et 0x0000FFFF	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1	1
Id	RW Field Value Id	Value	Description	
Α	RW SOPOWER		Keep RAM section SO ON or OFF in System ON mode.	



number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
			D C B A
et 0x0000FFFF		0 0 0 0 0 0 0	footnotemark
RW Field	Value Id	Value	Description
			RAM sections are always retained when ON, but can also be
			retained when OFF dependent on the settings in SORETENTION.
			All RAM sections will be OFF in System OFF mode.
	Off	0	Off
	On	1	On
RW S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
			RAM sections are always retained when ON, but can also be
			retained when OFF dependent on the settings in S1RETENTION.
			All RAM sections will be OFF in System OFF mode.
	Off	0	Off
	On	1	On
RW SORETENTION			Keep retention on RAM section SO when RAM section is in OFF
	Off	0	Off
	On	1	On
RW S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
	Off	0	Off
	On	1	On
	RW S1POWER RW SORETENTION	eet 0x00000FFFF RW Field Value Id Off On RW S1POWER Off On RW SORETENTION Off On RW S1RETENTION Off On Off On Off On Off On Off On Off On Off On Off On Off On Off	Off On 1 RW SORETENTION Off On 1 RW S1RETENTION Off On 1 RW S1RETENTION Off On 1

18.9.34 RAM[7].POWERSET

Address offset: 0x974

RAM7 power control set register

When read, this register will return the value of the POWER register.

B A 1 1 1
1 1 1

18.9.35 RAM[7].POWERCLR

Address offset: 0x978

RAM7 power control clear register

Bit r	umbe	er		31	30 2	29 2	28 2	27 2	26 2	5 2	4 2	23 2	2 2	1 2	0 1	19 1	L8 1	17 1	16	15	14	13	12	11	10	9	3 7	7 6	5	4	3	2	1	0
Id																		D	С														В	Α
Res	t 0x0	000FFFF		0	0	0	0	0	0 (0 ()	0 (0	0 (0	0	0	0	0	1	1	1	1	1	1	1	1 :	L 1	. 1	1	1	1	1	1
Id	RW	Field	Value Id	Val	ue						ı	Desc	rip	tio	n																			
Α	W	SOPOWER									ŀ	Keep	R/	MΑ	sec	tio	n S(0 of	f RA	١M	7 o	n o	r of	fin	Syst	em	ON	mo	de					
			Off	1							(Off																						
В	W	S1POWER									ŀ	Keep	R/	AΜ	sec	tio	n S	1 of	f RA	١M	7 o	n o	r of	fin	Syst	em	ON	mo	de					
			Off	1							(Off																						



Bitı	numbe	er		31	1 30	29	28	8 27	7 26	6 25	5 2	4 2	3 2	2 2	21 2	20 2	19	18	17	16	15	14	13	12	2 11	. 10	9	8	7	6	5	4	3	2	1	0
Id																			D	С															В	Α
Res	et OxO	000FFFF		0	0	0	0	0	0	0	(0 () () (0 (0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	alue							D	esc	rip	tio	n																				
С	W	SORETENTION										K	eep	re	ten	ntio	n c	n F	RAN	Λs	ect	on	S0	wh	en	RAI	VI se	ecti	on i	s						
												S	wito	che	d o	ff																				
			Off	1								С	ff																							
D	W	S1RETENTION										K	eep	re	ten	ntio	n c	n F	RAN	∕l s	ect	on	S1	wh	en	RAI	VI se	ecti	on i	S						
												S	wito	che	d o	ff																				
			Off	1								С	ff																							

18.10 Electrical specification

18.10.1 Current consumption, sleep

Symbol	Description	Min.	Тур.	Max.	Units
I _{OFF}	System OFF current, no RAM retention		0.3		μΑ
I _{ON}	System ON base current, no RAM retention		1.2		μΑ
I _{RAM}	Additional RAM retention current per 4 KB RAM section		20		nA

18.10.2 Device startup times

Symbol	Description	Min.	Тур.	Max.	Units
t _{POR}	Time in Power on Reset after VDD reaches 1.7 V for all supply				
	voltages and temperatures. Dependent on supply rise time. ¹⁰				
t _{POR,10us}	VDD rise time 10us		1		ms
t _{POR,10ms}	VDD rise time 10ms		9		ms
t _{POR,60ms}	VDD rise time 60ms		23		ms
t _{PINR}	If a GPIO pin is configured as reset, the maximum time taken				
	to pull up the pin and release reset after power on reset.				
	Dependent on the pin capacitive load (C) ¹¹ : t=5RC, R = 13kOhm				
t _{PINR,500nF}	C = 500nF			32.5	ms
t _{PINR,10uF}	C = 10uF			650	ms
t _{R2ON}	Time from reset to ON (CPU execute)				
t _{R2ON,NOTCONF}	If reset pin not configured	tPOR			ms
t _{R2ON,CONF}	If reset pin configured	tPOR +			ms
		tPINR			
t _{OFF2ON}	Time from OFF to CPU execute		16.5		μs
t _{IDLE2CPU}	Time from IDLE to CPU execute		3.0		μs
t _{EVTSET,CL1}	Time from HW event to PPI event in Constant Latency System		0.0625		μs
	ON mode				
t _{EVTSET,CLO}	Time from HW event to PPI event in Low Power System ON		0.0625		μs
	mode				

18.10.3 Power fail comparator

Symbol	Description	Min.	Тур.	Max.	Units
I _{POF}	Current consumption when enabled 12		<4		μΑ
V_{POF}	Nominal power level warning thresholds (falling supply voltage).	1.7		2.8	V
	Levels are configurable between Min. and Max. in 100mV				
	increments.				
V_{POFTOL}	Threshold voltage tolerance		±1	±5	%

A step increase in supply voltage of 300 mV or more, with rise time of 300 ms or less, within the valid supply range, may result in a system reset.

To decrease maximum time a device could hold in reset, a strong external pullup resistor can be used.

To save power, POF will not operate nor consume in System OFF, or while HFCLK is not running, even if left enabled by software



Symbol	Description	Min.	Тур.	Max.	Units
$V_{POFHYST}$	Threshold voltage hysteresis		50		mV
$V_{BOR,OFF}$	Brown out reset voltage range SYSTEM OFF mode	1.2		1.7	V
V _{BOR,ON}	Brown out reset voltage range SYSTEM ON mode	1.5		1.7	V



19 CLOCK — Clock control

The clock control system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. Clock distribution is automated and grouped independently by module to limit current consumption in unused branches of the clock tree.

Listed here are the main features for CLOCK:

- 64 MHz on-chip oscillator
- 64 MHz crystal oscillator, using external 32 MHz crystal
- 32.768 kHz +/-250 ppm RC oscillator
- 32.768 kHz crystal oscillator, using external 32.768 kHz crystal
- · 32.768 kHz oscillator synthesized from 64 MHz oscillator
- Firmware (FW) override control of oscillator activity for low latency start up
- Automatic oscillator and clock control, and distribution for ultra-low power

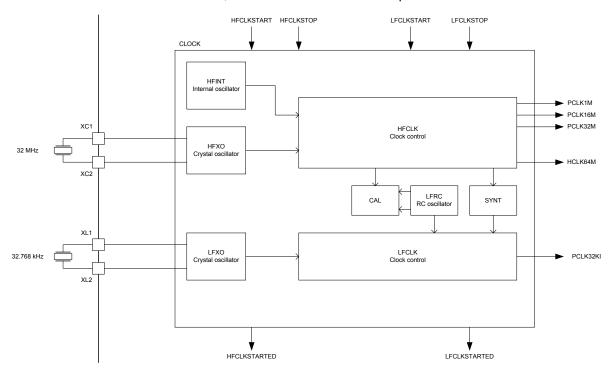


Figure 17: Clock control

19.1 HFCLK clock controller

The HFCLK clock controller provides the following clocks to the system.

- HCLK64M: 64 MHz CPU clock
- PCLK1M: 1 MHz peripheral clock
- PCLK16M: 16 MHz peripheral clock
- PCLK32M: 32 MHz peripheral clock

The HFCLK controller supports the following high frequency clock (HFCLK) sources:

- 64 MHz internal oscillator (HFINT)
- 64 MHz crystal oscillator (HFXO)

For illustration, see Figure 17: Clock control on page 101.



When the system requests one or more clocks from the HFCLK controller, the HFCLK controller will automatically provide them. If the system does not request any clocks provided by the HFCLK controller, the controller will enter a power saving mode.

These clocks are only available when the system is in ON mode. When the system enters ON mode, the internal oscillator (HFINT) clock source will automatically start to be able to provide the required HFCLK clock(s) for the system.

The HFINT will be used when HFCLK is requested and HFXO has not been started. The HFXO is started by triggering the HFCLKSTART task and stopped using the HFCLKSTOP task. A HFCLKSTARTED event will be generated when the HFXO has started and its frequency is stable.

The HFXO must be running to use the RADIO, NFC module or the calibration mechanism associated with the 32.768 kHz RC oscillator.

19.1.1 64 MHz crystal oscillator (HFXO)

The 64 MHz crystal oscillator (HFXO) is controlled by a 32 MHz external crystal

The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet.

Figure 18: Circuit diagram of the 64 MHz crystal oscillator on page 102 shows how the 32 MHz crystal is connected to the 64 MHz crystal oscillator.

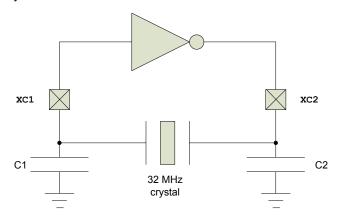


Figure 18: Circuit diagram of the 64 MHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{\left(C1' \cdot C2'\right)}{\left(C1' + C2'\right)}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

 $C2' = C2 + C_{pcb2} + C_{pin}$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. For more information, see *Reference circuitry* on page 546. C_{pcb1} and C_{pcb2} are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the xc1 and xc2 pins. See table *64 MHz crystal oscillator (HFXO)* on page 109. The load capacitors C1 and C2 should have the same value.

For reliable operation, the crystal load capacitance, shunt capacitance, equivalent series resistance, and drive level must comply with the specifications in table 64 MHz crystal oscillator (HFXO) on page 109. It is recommended to use a crystal with lower than maximum load capacitance and/or shunt capacitance. A low load capacitance will reduce both start up time and current consumption.



19.2 LFCLK clock controller

The system supports several low frequency clock sources.

As illustrated in *Figure 17: Clock control* on page 101, the system supports the following low frequency clock sources:

- 32.768 kHz RC oscillator (LFRC)
- 32.768 kHz crystal oscillator (LFXO)
- 32.768 kHz synthesized from HFCLK (LFSYNT)

The LFCLK clock is started by first selecting the preferred clock source in register *LFCLKSRC* on page 108 and then triggering the LFCLKSTART task. If the LFXO is selected as the clock source, the LFCLK will initially start running from the 32.768 kHz LFRC while the LFXO is starting up and automatically switch to using the LFXO once this oscillator is running. The LFCLKSTARTED event will be generated when the LFXO has been started.

The LFCLK clock is stopped by triggering the LFCLKSTOP task.

It is not allowed to write to register LFCLKSRC on page 108 when the LFCLK is running.

A LFCLKSTOP task will stop the LFCLK oscillator. However, the LFCLKSTOP task can only be triggered after the STATE field in register *LFCLKSTAT* on page 107 indicates a 'LFCLK running' state.

The LFCLK clock controller and all of the LFCLK clock sources are always switched off when in OFF mode.

19.2.1 32.768 kHz RC oscillator (LFRC)

The default source of the low frequency clock (LFCLK) is the 32.768 kHz RC oscillator (LFRC).

The LFRC frequency will be affected by variation in temperature. The LFRC oscillator can be calibrated to improve accuracy by using the HFXO as a reference oscillator during calibration. See Table 32.768 kHz RC oscillator (LFRC) on page 109 for details on the default and calibrated accuracy of the LFRC oscillator. The LFRC oscillator does not require additional external components.

19.2.2 Calibrating the 32.768 kHz RC oscillator

After the 32.768 kHz RC oscillator is started and running, it can be calibrated by triggering the CAL task. In this case, the HFCLK will be temporarily switched on and used as a reference.

A DONE event will be generated when calibration has finished. The calibration mechanism will only work as long as HFCLK is generated from the HFCLK crystal oscillator, it is therefore necessary to explicitly start this crystal oscillator before calibration can be started, see HFCLKSTART task.

19.2.3 Calibration timer

The calibration timer can be used to time the calibration interval of the 32.768 kHz RC oscillator.

The calibration timer is started by triggering the CTSTART task and stopped by triggering the CTSTOP task. The calibration timer will always start counting down from the value specified in CTIV and generate a CTTO timeout event when it reaches 0. The Calibration timer will stop by itself when it reaches 0.

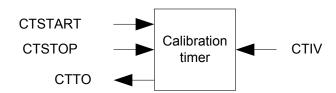


Figure 19: Calibration timer

Due to limitations in the calibration timer, only one task related to calibration, that is, CAL, CTSTART and CTSTOP, can be triggered for every period of LFCLK.



19.2.4 32.768 kHz crystal oscillator (LFXO)

For higher LFCLK accuracy (when better than +/- 250 ppm accuracy is required), the low frequency crystal oscillator (LFXO) must be used.

The following external clock sources are supported:

- Low swing clock signal applied to the XL1 pin. The XL2 pin shall then be grounded.
- Rail-to-rail clock signal applied to the XL1 pin. The XL2 pin shall then be grounded or left unconnected.

The *LFCLKSRC* on page 108 register controls the clock source, and its allowed swing. The truth table for various situations is as follows:

Table 25: LFCLKSRC configuration depending on clock source

SRC	EXTERNAL	BYPASS	Comment
0	0	0	Normal operation, RC is source
0	0	1	DO NOT USE
0	1	Χ	DO NOT USE
1	0	0	Normal XTAL operation
1	1	0	Apply external low swing signal to XL1, ground XL2
1	1	1	Apply external full swing signal to XL1, leave XL2 grounded or unconnected
1	0	1	DO NOT USE
2	0	0	Normal operation, synth is source
2	0	1	DO NOT USE
2	1	X	DO NOT USE

To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. *Figure 20: Circuit diagram of the 32.768 kHz crystal oscillator* on page 104 shows the LFXO circuitry.

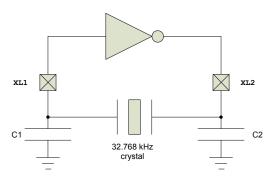


Figure 20: Circuit diagram of the 32.768 kHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{\left(C1' \cdot C2'\right)}{\left(C1' + C2'\right)}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

 $C2' = C2 + C_{pcb2} + C_{pin}$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_{pcb1} and C_{pcb2} are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the XC1 and XC2 pins (see 32.768 kHz crystal oscillator (LFXO) on page 109). The load capacitors C1 and C2 should have the same value.

For more information, see *Reference circuitry* on page 546.



19.2.5 32.768 kHz synthesized from HFCLK (LFSYNT)

LFCLK can also be synthesized from the HFCLK clock source. The accuracy of LFCLK will then be the accuracy of the HFCLK.

Using the LFSYNT clock avoids the requirement for a 32.768 kHz crystal, but increases average power consumption as the HFCLK will need to be requested in the system.

19.3 Registers

Table 26: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40000000	CLOCK	CLOCK	Clock control	

Table 27: Register Overview

Register	Offset	Description	
TASKS_HFCLKSTART	0x000	Start HFCLK crystal oscillator	
TASKS_HFCLKSTOP	0x004	Stop HFCLK crystal oscillator	
TASKS_LFCLKSTART	0x008	Start LFCLK source	
TASKS_LFCLKSTOP	0x00C	Stop LFCLK source	
TASKS_CAL	0x010	Start calibration of LFRC oscillator	
TASKS_CTSTART	0x014	Start calibration timer	
TASKS_CTSTOP	0x018	Stop calibration timer	
EVENTS_HFCLKSTARTED	0x100	HFCLK oscillator started	
EVENTS_LFCLKSTARTED	0x104	LFCLK started	
EVENTS_DONE	0x10C	Calibration of LFCLK RC oscillator complete event	
EVENTS_CTTO	0x110	Calibration timer timeout	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
HFCLKRUN	0x408	Status indicating that HFCLKSTART task has been triggered	
HFCLKSTAT	0x40C	HFCLK status	
LFCLKRUN	0x414	Status indicating that LFCLKSTART task has been triggered	
LFCLKSTAT	0x418	LFCLK status	
LFCLKSRCCOPY	0x41C	Copy of LFCLKSRC register, set when LFCLKSTART task was triggered	
LFCLKSRC	0x518	Clock source for the LFCLK	
CTIV	0x538	Calibration timer interval	Retained
TRACECONFIG	0x55C	Clocking options for the Trace Port debug interface	

19.3.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	number			31 3	30 29	9 28	3 27	26 2	25 24	1 23	22 2	21 20	0 1	9 18	3 17	16	15	14 1	3 12	11	10	9	8	7 (6 5	4	3	2 :	1 0
Id																										D	С	E	3 A
Res	et 0x0000	00000		0	0 0	0	0	0	0 0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0	0 (0 0
Id	RW Fi	eld	Value Id	Valu	ıe					Des	scrip	otion	1																
Α	RW H	CLKSTARTED								Wr	ite '	1' to	Ena	able	int	erru	pt f	or HI	CLK	STA	RTE	D e	ven	t					
										See	e <i>EV</i>	ENTS	5_ <i>H</i>	FCL	KST	4RT	ED												
			Set	1						Ena	able																		
			Disabled	0						Rea	ad: [Disab	led	ł															
			Enabled	1						Rea	ad: E	nabl	led																
В	RW LF	CLKSTARTED								Wr	ite '	1' to	Ena	able	int	erru	pt f	or LF	CLKS	STAF	RTEE) e	vent						
										See	e <i>EV</i>	ENTS	<u>5_</u> LI	FCLK	(STA	RTE	D												
			Set	1						Ena	able																		
			Disabled	0						Rea	ad: [Disab	led	ł															
			Enabled	1						Rea	ad: E	Enabl	led																



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
C RW DONE		Write '1' to Enable interrupt for DONE event
		See EVENTS_DONE
	Set	1 Enable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
D RW CTTO		Write '1' to Enable interrupt for CTTO event
		See EVENTS_CTTO
	Set	1 Enable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled

19.3.2 INTENCLR

Address offset: 0x308

Disable interrupt

		'			
Bit	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value	Description
Α	RW	HFCLKSTARTED			Write '1' to Disable interrupt for HFCLKSTARTED event
					See EVENTS_HFCLKSTARTED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	LFCLKSTARTED			Write '1' to Disable interrupt for LFCLKSTARTED event
					See EVENTS_LFCLKSTARTED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	DONE			Write '1' to Disable interrupt for DONE event
					See EVENTS_DONE
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	СТТО			Write '1' to Disable interrupt for CTTO event
					See EVENTS_CTTO
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

19.3.3 HFCLKRUN

Address offset: 0x408

Status indicating that HFCLKSTART task has been triggered

Bit	num	ber			31	30	29	28 :	27	26	25 :	24	23	22 :	21 :	20 :	19 :	18 :	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			Α
Re	set 0	x000	00000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RV	N Fi	ield	Value Id	Val	ue							Des	crip	otio	n																			
Α	R	ST	TATUS										HFC	CLKS	STA	RT 1	task	tri	gge	rec	d o	r nc	t												
				NotTriggered	0								Tas	k no	ot t	rigg	ere	d																	
				Triggered	1								Tas	k tr	igge	erec	t																		



19.3.4 HFCLKSTAT

Address offset: 0x40C

HFCLK status

Bit	numbe	er		31	30 2	29	28	27	26	25	2	4 2	3 2	2 :	21	20	19	18	3 1	7 1	6 1	.5 1	4	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				E	3																Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0) () (0	0	0	0	0	0	C) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							D	eso	crip	ptic	n																					
Α	R	SRC										S	our	ce	of	HF	CL	<																			
			RC	0								6	4 N	⁄Н	z in	ter	rna	l os	cil	ato	or (HFI	NT)													
			Xtal	1								6	4 N	⁄Н	z cr	yst	tal	osc	illa	tor	(H	FΧ	O)														
В	R	STATE										Н	IFC	LK	sta	te																					
			NotRunning	0								Н	IFC	LK	not	ru	ınn	ing																			
			Running	1								Н	IFC	LK	rur	nir	ng																				

19.3.5 LFCLKRUN

Address offset: 0x414

Status indicating that LFCLKSTART task has been triggered

Bit r	numb	er		31 30	29	28	27 2	26 2	25 24	4 2	3 22	2 21	20	19	18 1	.7 1	6 1	5 14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																														Α
Res	et 0x0	0000000		0 0	0	0	0	0	0 0) (0	0	0	0	0	0	0 0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value	•					D	escr	ripti	on																	
Α	R	STATUS								L	FCLK	(STA	RT 1	task	trig	ger	ed o	or no	ot											
			NotTriggered	0						Т	ask ı	not	trigg	gere	ed															
			Triggered	1						Т	ask 1	trigg	gere	d																

19.3.6 LFCLKSTAT

Address offset: 0x418

LFCLK status

Bit	numbe	er		31	30	29 :	28 2	7 2	6 25	5 24	1 23	22	21 2	0 1	9 1	8 17	16	15	14	13 1	12 1	1 10	9	8	7	6	5 4	4 3	2	1 0
Id																	В													A A
Res	et 0x0	0000000		0	0	0	0 (0	0 0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0 0
Id	RW	Field	Value Id	Va	lue						De	scri	ptio	n																
Α	R	SRC									So	urce	e of I	.FCI	_K															
			RC	0							32	.768	3 kHz	RC	osc	illat	or													
			Xtal	1							32	.768	3 kHz	cry	/sta	osc	illat	or												
			Synth	2							32	.768	3 kHz	syı	nthe	size	d fr	om	HF	CLK										
В	R	STATE									LF	CLK	state	9																
			NotRunning	0							LF	CLK	not	runi	ning															
			Running	1								CLK	runr	ing																

19.3.7 LFCLKSRCCOPY

Address offset: 0x41C

Copy of LFCLKSRC register, set when LFCLKSTART task was triggered

Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A R SRC			Clock source
	RC	0	32.768 kHz RC oscillator
	Xtal	1	32.768 kHz crystal oscillator
	Synth	2	32.768 kHz synthesized from HFCLK



19.3.8 LFCLKSRC

Address offset: 0x518

Clock source for the LFCLK

Bit r	numbe	er		31	30 29	9 28	27	26 2	5 2	4 23 :	22 :	21 20	0 1	9 18	3 17	7 16	15	14	13	12 1	1 10	9	8	7	6	5 4	4 3	2	1 0
Id															С	В													A A
Res	et 0x0	0000000		0	0 0	0	0	0 () (0 0	0	0 0) (0 0	0	0	0	0	0	0 (0	0	0	0	0	0 (0 0	0	0 0
Id	RW	Field	Value Id	Val	ue					Des	crip	ption																	
Α	RW	SRC								Clo	ck s	ourc	e																
			RC	0						32.	768	kHz	RC	osc	illat	tor													
			Xtal	1						32.	768	kHz	cry	/stal	oso	cilla	tor												
			Synth	2						32.	768	kHz	syr	nthe	size	ed fi	rom	HF	CLK										
В	RW	BYPASS								Ena	ble	or d	isal	ble l	оур	ass	of L	FCL	K cr	/stal	osc	illat	or w	ith	ext	erna	ıl		
										clo	ck s	ource	е																
			Disabled	0						Disa	able	e (use	e w	ith)	Ktal	or	low-	-sw	ing e	xter	nal	sour	ce)						
			Enabled	1						Ena	ble	(use	wi	th r	ail-t	to-r	ail e	xte	rnal	soui	ce)								
С	RW	EXTERNAL								Ena	ble	or d	isal	ble e	exte	erna	l so	urc	e for	LFC	LK								
			Disabled	0						Disa	able	e exte	ern	al so	our	ce (ı	use	wit	h Xta	al)									
			Enabled	1						Ena	ble	use	of (exte	rna	l so	urce	e in	stea	d of	Xtal	(SR	C ne	eds	to	be			
										set	to)	Xtal)																	

19.3.9 CTIV (Retained)

Address offset: 0x538

This register is a retained register

Calibration timer interval

Bitı	numb	er		31 30	29	28 2	7 26	25	5 24	23	22	21 2	20 1	9 1	3 17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3	2	1 ()
Id																									Α	Α	Α	Α .	Α,	A A	Δ
Res	et 0x(0000000		0 0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 ()
Id	RW	Field	Value Id	Value						De	scri	ptio	n																		ı
Α	RW	CTIV								Ca	libra	ition	tim	er i	nter	val	in n	nult	iple	of (.25	sec	ond	s. R	ang	ge:					
				0.25 seconds to 31.75 seconds.																											

19.3.10 TRACECONFIG

Address offset: 0x55C

Clocking options for the Trace Port debug interface

This register is a retained register. Reset behavior is the same as debug components.

Bit	numbe	er		31	30 2	9 2	28 2	27 2	26 2	5 2	4 2	23 22	2 2	1 20) 1	9 18	3 1	7 16	5 15	14	13	12	11	10	9	8	7	6 5	5 4	3	2	1	0
Id																	В	В														Α	Α
Res	et 0x0	0000000		0	0	0	0 (0	0 () (0 (0 0) (0	C	0	0	0	0	0	0	0	0	0	0	0 (כ	0 (0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						0)esc	rip	tion																			
Α	RW	TRACEPORTSPEED									S	pee	d o	f Tra	ace	Poi	rt c	lock	. N	ote	that	the	e TR	ACE	CL	K pi	n w	/ill					
											C	utp	ut t	this	clo	ck d	livi	ded	by	two													
			32MHz	0							3	2 M	lHz	Tra	ce	Port	clo	ock	(TR	ACE	CLK	= 1	6 M	Hz)									
			16MHz	1							1	.6 M	lHz	Tra	ce	Port	clo	ock	(TR	ACE	CLK	= 8	MH	lz)									
			8MHz	2							8	МН	Iz T	race	e P	ort (clo	ck (1	RA	CEC	LK =	4 N	ИHZ)									
			4MHz	3							4	МН	Iz T	race	e P	ort (clo	ck (1	RA	CEC	LK =	2 1	ИHZ)									
В	RW	TRACEMUX									P	in m	nult	tiple	xir	ig of	ftra	ace	sigr	als.													
			GPIO	0							C	SPIO	s n	nulti	ple	xed	or	ito a	all t	race	-pir	IS											
			Serial	1							S	wo	mı	ultip	lex	ed (ont	o P	0.18	3, G	PIO	mul	ltipl	exe	d o	nto	otł	ner					
											t	race	pi	ns																			
			Parallel	2							Т	RAC	CEC	LK a	nd	TRA	ACE	DA	ΓAr	nult	iple	xed	on	to P	0.2	20, P	0.1	.8,					
											P	0.16	6, P	0.15	5 aı	nd P	0.1	4.															



19.4 Electrical specification

19.4.1 64 MHz internal oscillator (HFINT)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_HFINT}	Nominal output frequency		64		MHz
f _{TOL_HFINT}	Frequency tolerance		<±1.5	<±6	%
I _{HFINT}	Run current		60		μΑ
I _{START_HFINT}	Average startup current		I_HFINT		μΑ
t _{START_HFINT}	Startup time		3		us

19.4.2 64 MHz crystal oscillator (HFXO)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_HFXO}	Nominal output frequency		64		MHz
f _{XTAL_HFXO}	External crystal frequency		32		MHz
f_{TOL_HFXO}	Frequency tolerance requirement for 2.4 GHz proprietary radio			±60	ppm
	applications				
f _{TOL_HFXO_BLE}	Frequency tolerance requirement, Bluetooth low energy			±40	ppm
	applications				
C_{L_HFXO}	Load capacitance			12	pF
C _{0_HFXO}	Shunt capacitance			7	pF
R _{S_HFXO_7PF}	Equivalent series resistance C0 = 7 pF			60	ohm
R _{S_HFXO_5PF}	Equivalent series resistance C0 = 5 pF			80	ohm
R _{S_HFXO_3PF}	Equivalent series resistance C0 = 3 pF			100	ohm
P _{D_HFXO}	Drive level			100	uW
C _{PIN_HFXO}	Input capacitance XC1 and XC2		4		pF
I _{STBY_X32M}	Core standby current ¹³		50		μΑ
I _{HFXO}	Run current		250		μΑ
I _{START_HFXO}	Average startup current, first 1 ms		0.4		mA
t _{START_HFXO}	Startup time		0.36		ms

19.4.3 32.768 kHz RC oscillator (LFRC)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_LFRC}	Nominal frequency		32.768		kHz
f _{TOL_LFRC}	Frequency tolerance			±2	%
f _{TOL_CAL_LFRC}	Frequency tolerance for LFRC after calibration ¹⁴			±250	ppm
I _{LFRC}	Run current for 32.768 kHz RC oscillator		0.6	1	μΑ
t _{START_LFRC}	Startup time for 32.768 kHz RC oscillator		600		us

19.4.4 32.768 kHz crystal oscillator (LFXO)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_LFXO}	Crystal frequency		32.768		kHz
f _{TOL_LFXO_BLE}	Frequency tolerance requirement for BLE stack			±250	ppm
f _{TOL_LFXO_ANT}	Frequency tolerance requirement for ANT stack			±50	ppm
C _{L_LFXO}	Load capacitance			12.5	pF
C _{0_LFXO}	Shunt capacitance			2	pF
R _{S_LFXO}	Equivalent series resistance			100	kohm
P _{D_LFXO}	Drive level			1	uW
C _{pin}	Input capacitance on XL1 and XL2 pads		4		pF
I _{LFXO}	Run current for 32.768 kHz crystal oscillator		0.25		μΑ

Current drawn if HFXO is forced on through for instance using the low latency power mode. Constant temperature within ± 0.5 °C and calibration performed at least every 8 seconds



Symbol	Description	Min.	Тур.	Max.	Units
t _{START_LFXO}	Startup time for 32.768 kHz crystal oscillator		0.25		S
$V_{AMP_IN_XO_LOW}$	Peak to peak amplitude for external low swing clock. Input	200		1000	mV
	signal must not swing outside supply rails.				

19.4.5 32.768 kHz synthesized from HFCLK (LFSYNT)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_LFSYNT}	Nominal frequency		32.768		kHz
f _{TOL_LFSYNT}	Frequency tolerance in addition to HFLCK tolerance ¹⁵		8		ppm
I _{LFSYNT}	Run current for synthesized 32.768 kHz		100		μΑ
t _{START_LFSYNT}	Startup time for synthesized 32.768 kHz		100		us

¹⁵ Frequency tolerance will be derived from the HFCLK source clock plus the LFSYNT tolerance



20 GPIO — General purpose input/output

The general purpose input/output (GPIO) is organized as one port with up to 32 I/Os (dependent on package) enabling access and control of up to 32 pins through one port. Each GPIO can be accessed individually.

GPIO has the following user-configurable features:

- Up to 32 GPIO
- 8 GPIO with Analog channels for SAADC, COMP or LPCOMP inputs
- Configurable output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on state changes on any pin
- All pins can be used by the PPI task/event system
- One or more GPIO outputs can be controlled through PPI and GPIOTE channels
- · All pins can be individually mapped to interface blocks for layout flexibility
- GPIO state changes captured on SENSE signal can be stored by LATCH register

The GPIO Port peripheral implements up to 32 pins, PIN0 through PIN31. Each of these pins can be individually configured in the PIN_CNF[n] registers (n=0..31).

The following parameters can be configured through these registers:

- Direction
- · Drive strength
- Enabling of pull-up and pull-down resistors
- Pin sensing
- Input buffer disconnect
- Analog input (for selected pins)

The PIN_CNF registers are retained registers. See *POWER* — *Power supply* on page 78 chapter for more information about retained registers.

20.1 Pin configuration

Pins can be individually configured, through the SENSE field in the PIN_CNF[n] register, to detect either a high level or a low level on their input.

When the correct level is detected on any such configured pin, the sense mechanism will set the DETECT signal high. Each pin has a separate DETECT signal, and the default behaviour, as defined by the DETECTMODE register, is that the DETECT signal from all pins in the GPIO Port are combined into a common DETECT signal that is routed throughout the system, which then can be utilized by other peripherals, see *Figure 21: GPIO Port and the GPIO pin details* on page 112. This mechanism is functional in both ON and OFF mode.



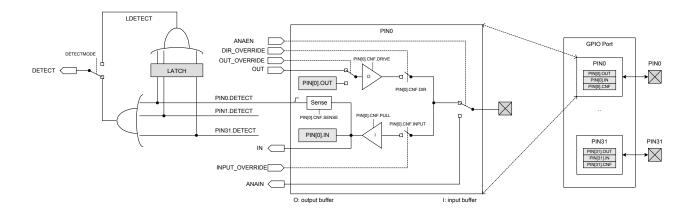


Figure 21: GPIO Port and the GPIO pin details

Figure 21: GPIO Port and the GPIO pin details on page 112 illustrates the GPIO port containing 32 individual pins, where PINO is illustrated in more detail as a reference. All the signals on the left side of the illustration are used by other peripherals in the system, and therefore, are not directly available to the CPU.

Make sure that a pin is in a level that cannot trigger the sense mechanism before enabling it. Detect will go high immediately if the sense condition configured in the PIN_CNF registers is met when the sense mechanism is enabled. This will trigger a PORT event if the DETECT signal was low before enabling the sense mechanism. See *GPIOTE* — *GPIO tasks and events* on page 157.

See the following peripherals for more information about how the DETECT signal is used:

- POWER: uses the DETECT signal to exit from System OFF.
- GPIOTE: uses the DETECT signal to generate the PORT event.

When a pin's PINx.DETECT signal goes high, a flag will be set in the LATCH register, e.g. when the PIN0.DETECT signal goes high, bit 0 in the LATCH register will be set to '1'.

The LATCH register will only be cleared if the CPU explicitly clears it by writing a '1' to the bit that shall be cleared, i.e. the LATCH register will not be affected by a PINx.DETECT signal being set low.

If the CPU performs a clear operation on a bit in the LATCH register when the associated PINx.DETECT signal is high, the bit in the LATCH register will not be cleared.

The LDETECT signal will be set high when one or more bits in the LATCH register are '1'. The LDETECT signal will be set low when all bits in the LATCH register are successfully cleared to '0'.

If one or more bits in the LATCH register are '1' after the CPU has performed a clear operation on the LATCH registers, a rising edge will be generated on the LDETECT signal, this is illustrated in *Figure 22: DETECT signal behavior* on page 113.

Important: The CPU can read the LATCH register at any time to check if a SENSE condition has been met on one or more of the the GPIO pins even if that condition is no longer met at the time the CPU queries the LATCH register. This mechanism will work even if the LDETECT signal is not used as the DETECT signal.

The LDETECT signal is by default not connected to the GPIO port's DETECT signal, but via the DETECTMODE register it is possible to change the behaviour of the GPIO port's DETECT signal from the default behaviour described above to instead be derived directly from the LDETECT signal, see *Figure 21: GPIO Port and the GPIO pin details* on page 112. *Figure 22: DETECT signal behavior* on page 113 illustrates the DETECT signals behaviour for these two alternatives.



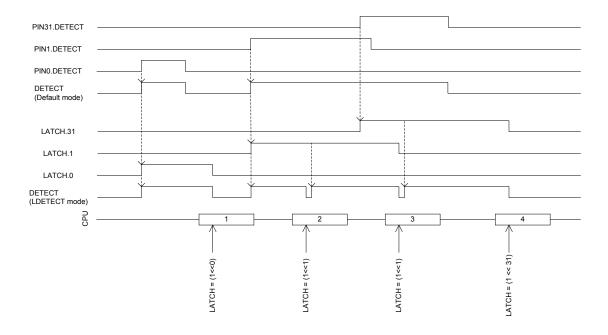


Figure 22: DETECT signal behavior

The input buffer of a GPIO pin can be disconnected from the pin to enable power savings when the pin is not used as an input, see *Figure 21: GPIO Port and the GPIO pin details* on page 112. Inputs must be connected in order to get a valid input value in the IN register and for the sense mechanism to get access to the pin.

Other peripherals in the system can attach themselves to GPIO pins and override their output value and configuration, or read their analog or digital input value, see *Figure 21: GPIO Port and the GPIO pin details* on page 112.

Selected pins also support analog input signals, see ANAIN in *Figure 21: GPIO Port and the GPIO pin details* on page 112. The assignment of the analog pins can be found in *Pin assignments* on page 13.

Important: When a pin is configured as digital input, care has been taken in the nRF52832 design to minimize increased current consumption when the input voltage is between V_{IL} and V_{IH} . However, it is a good practice to ensure that the external circuitry does not drive that pin to levels between V_{IL} and V_{IH} for a long period of time.

20.2 GPIO located near the RADIO

Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current close to the radio power supply and antenna pins.

Refer to *Pin assignments* on page 13 for recommended usage guidelines to maximize radio performance in an application.

20.3 Registers

Table 28: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x50000000	GPIO	GPIO	General purpose input and output		Deprecated
0x50000000	GPIO	P0	General purpose input and output		



Table 29: Register Overview

Register	Offset	Description
OUT	0x504	Write GPIO port
OUTSET	0x508	Set individual bits in GPIO port
OUTCLR	0x50C	Clear individual bits in GPIO port
IN	0x510	Read GPIO port
DIR	0x514	Direction of GPIO pins
DIRSET	0x518	DIR set register
DIRCLR	0x51C	DIR clear register
LATCH	0x520	Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE
		registers
DETECTMODE	0x524	Select between default DETECT signal behaviour and LDETECT mode
PIN_CNF[0]	0x700	Configuration of GPIO pins
PIN_CNF[1]	0x704	Configuration of GPIO pins
PIN_CNF[2]	0x708	Configuration of GPIO pins
PIN_CNF[3]	0x70C	Configuration of GPIO pins
PIN_CNF[4]	0x710	Configuration of GPIO pins
PIN_CNF[5]	0x714	Configuration of GPIO pins
PIN_CNF[6]	0x718	Configuration of GPIO pins
PIN_CNF[7]	0x71C	Configuration of GPIO pins
PIN_CNF[8]	0x720	Configuration of GPIO pins
PIN_CNF[9]	0x724	Configuration of GPIO pins
PIN_CNF[10]	0x728	Configuration of GPIO pins
PIN_CNF[11]	0x72C	Configuration of GPIO pins
PIN_CNF[12]	0x730	Configuration of GPIO pins
PIN_CNF[13]	0x734	Configuration of GPIO pins
PIN_CNF[14]	0x738	Configuration of GPIO pins
PIN_CNF[15]	0x73C	Configuration of GPIO pins
PIN_CNF[16]	0x740	Configuration of GPIO pins
PIN_CNF[17]	0x744	Configuration of GPIO pins
PIN_CNF[18]	0x748	Configuration of GPIO pins
PIN_CNF[19]	0x74C	Configuration of GPIO pins
PIN_CNF[20]	0x750	Configuration of GPIO pins
PIN_CNF[21]	0x754	Configuration of GPIO pins
PIN_CNF[22]	0x758	Configuration of GPIO pins
PIN_CNF[23]	0x75C	Configuration of GPIO pins
PIN_CNF[24]	0x760	Configuration of GPIO pins
PIN_CNF[25]	0x764	Configuration of GPIO pins
PIN_CNF[26]	0x768	Configuration of GPIO pins
PIN_CNF[27]	0x76C	Configuration of GPIO pins
PIN_CNF[28]	0x770	Configuration of GPIO pins
PIN_CNF[29]	0x774	Configuration of GPIO pins
PIN_CNF[30]	0x778	Configuration of GPIO pins
PIN_CNF[31]	0x77C	Configuration of GPIO pins

20.3.1 OUT

Address offset: 0x504 Write GPIO port

Bit r	numbe	er		31	L 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	L3 1	2 1	1 1) 9	8	7	6	5	4	3	2	1 0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U	Т	S	R	Q	Р	О	N 1	/ I	L K	J	- 1	Н	G	F	Ε	D	C I	ВА
Rese	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	alue	:						De	scri	ptic	on																		
Α	RW	PIN0										Pir	0																				
			Low	0								Pir	dri	ver	is l	ow																	
			High	1								Pir	dri	ver	is ŀ	nigh	1																
В	RW	PIN1										Pir	1																				



Bit r	numbe	er		31 30	29 28	27	26 2	25 24	23 22	2 21 2	0 19	18 1	.7 16	5 15	14 13	3 12 1	11 10	9	8 7	7 6	5	4	3 2	1 (
Id				f e																				
Res	et 0x0	0000000		0 0	0 0	0	0 (0 0	0 0	0 (0 0	0 (0 0	0	0 0	0	0 0	0	0 (0	0	0	0 0	0 (
Id	RW	Field	Value Id	Value					Descr	ription	n													
			Low	0					Pin dr	river i	s low													
			High	1					Pin dr	river i	s high													
С	RW	PIN2							Pin 2															
			Low	0					Pin dr	river i	s low													
			High	1						river i	s high													
D	RW	PIN3							Pin 3															
			Low	0						river i														
			High	1						river i	s high													
Ε	RW	PIN4		•					Pin 4															
			Low	0						river i														
F	D\A/	PIN5	High	1					Pin ar	river i	s nign													
Г	KVV	PINS	Low	0						river i	c low													
			High	1						river i														
G	RW	PIN6	riigii	1					Pin 6		s mgn													
J		•0	Low	0						river i	s low													
			High	1						river i														
Н	RW	PIN7	6	-					Pin 7		J													
			Low	0						river i	s low													
			High	1					Pin dr	river i	s high													
ı	RW	PIN8							Pin 8															
			Low	0					Pin dr	river i	s low													
			High	1					Pin dr	river i	s high													
J	RW	PIN9							Pin 9															
			Low	0					Pin dr	river i	s low													
			High	1					Pin dr	river i	s high													
K	RW	PIN10							Pin 10	0														
			Low	0					Pin dr	river i	s low													
			High	1					Pin dr	river i	s high													
L	RW	PIN11							Pin 11															
			Low	0						river i														
			High	1						river i	s high													
М	RW	PIN12							Pin 12															
			Low	0						river i														
N	DIA	PIN13	High	1					Pin dr	river i:	s migh													
IN	KVV	PIN13	Low	0					Pin dr		c low													
			High	1						river i														
0	RW/	PIN14	111611	-					Pin 14		3 111511													
•			Low	0						· river i:	s low													
			High	1						river i														
Р	RW	PIN15							Pin 15		Ü													
			Low	0					Pin dr		s low													
			High	1					Pin dr	river i	s high													
Q	RW	PIN16							Pin 16															
			Low	0					Pin dr	river i	s low													
			High	1					Pin dr	river i	s high													
R	RW	PIN17							Pin 17	7														
			Low	0					Pin dr	river i	s low													
			High	1					Pin dr	river i	s high													
S	RW	PIN18							Pin 18	8														
			Low	0					Pin dr	river i	s low													
			High	1					Pin dr	river i	s high													
T	RW	PIN19							Pin 19															
			Low	0					Pin dr	river i	s low													



Bit r	numbe	er		31 30	29	9 28	27	26	25	24	2	3 22 2	21	20 :	19	18 :	17 :	16	15	14 :	13 1	2 1	1 1	0 9) 8	3 7	6	5	4	3	2	1	0
Id				f e	d	С	b	а	Ζ	Υ	Х	(W	V	U	Т	S	R	Q	Р	О	N 1	И	LI	< J	ı	Н	G	i F	Ε	D	С	В	Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0) (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Value							D	escrip	tic	n																			
			High	1							Pi	in driv	er	is h	igh																		
U	RW	PIN20									Pi	in 20																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
٧	RW	PIN21									Pi	in 21																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
W	RW	PIN22									Pi	in 22																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
Χ	RW	PIN23									Pi	in 23																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
Υ	RW	PIN24									Pi	in 24																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
Z	RW	PIN25									Pi	in 25																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
а	RW	PIN26									Pi	in 26																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
b	RW	PIN27									Pi	in 27																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
С	RW	PIN28									Pi	in 28																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1								in driv	er	is h	igh																		
d	RW	PIN29									Pi	in 29																					
			Low	0							Pi	in driv	er	is lo	w																		
			High	1							Pi	in driv	er	is h	igh																		
е	RW	PIN30										in 30																					
			Low	0								in driv																					
			High	1								in driv	er	is h	igh																		
f	RW	PIN31										in 31																					
			Low	0								in driv																					
			High	1							Pi	in driv	er	is h	igh																		

20.3.2 OUTSET

Address offset: 0x508

Set individual bits in GPIO port

Read: reads value of OUT register.

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5 5 4 3 2 1 0
Id		fedcbaZYXWVUTSRQPONMLKJIH (F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0
Id RW Field	Value Id	Value Description	
A RW PINO		Pin 0	
	Low	0 Read: pin driver is low	
	High	1 Read: pin driver is high	
	Set	1 Write: writing a '1' sets the pin high; writing a '0' has no e	effect
B RW PIN1		Pin 1	
	Low	0 Read: pin driver is low	



Bitı	numbe	er		31 30 29 28 27	7 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id						X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0	0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value		Description
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
С	RW	PIN2				Pin 2
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
-	DIA	DINIO	Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
D	KW	PIN3	Loui	0		Pin 3
			Low High	1		Read: pin driver is low Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
E	RW	PIN4	Sec	•		Pin 4
_			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
F	RW	PIN5				Pin 5
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
G	RW	PIN6				Pin 6
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
Н	RW	PIN7				Pin 7
			Low	0		Read: pin driver is low
			High Set	1		Read: pin driver is high Write: writing a '1' sets the pin high; writing a '0' has no effect
	RW	PIN8	Set	1		Pin 8
•			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
J	RW	PIN9				Pin 9
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
K	RW	PIN10				Pin 10
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
L	RW	PIN11	Laur	0		Pin 11
			Low High	0		Read: pin driver is low Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
М	RW	PIN12		-		Pin 12
••			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
N	RW	PIN13				Pin 13
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
0	RW	PIN14				Pin 14
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
Р	RW	PIN15				Pin 15



Bit n	numbe	er		31 30	29 28	27 26	5 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0	0000000						0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Q	RW	PIN16						Pin 16
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
	D\A/	DINIA 7	Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
R	KVV	PIN17	Low	0				Pin 17 Read: pin driver is low
			High	1				Read: pin driver is low
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
S	RW	PIN18		-				Pin 18
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Т	RW	PIN19						Pin 19
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
U	RW	PIN20						Pin 20
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
.,	DVA	DINIDA	Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
V	RW	PIN21	Low	0				Pin 21
			Low High	1				Read: pin driver is low Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
w	RW	PIN22	Jet	-				Pin 22
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Х	RW	PIN23						Pin 23
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Υ	RW	PIN24						Pin 24
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
-	DVA	DINIOS	Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Z	KW	PIN25	Low	0				Pin 25
			Low High	0				Read: pin driver is low Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
a	RW	PIN26	550	•				Pin 26
-		·- 	Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
b	RW	PIN27						Pin 27
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
С	RW	PIN28						Pin 28
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect



Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id				f	е	d	С	b	а	Z	Υ	Х	W	V	U	Т	S	R	Q	Р	О	N I	VI	L K	J	-1	Н	G	F	Е	0	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	tio	n																		
d	RW	PIN29									ı	Pin	29																				
			Low	0							-	Rea	ıd: p	in (driv	/er	is lo	wc															
			High	1							-	Rea	ıd: p	in (driv	/er	is h	igh															
			Set	1							,	Wri	te:	wri	ting	g a '	'1' s	sets	th	e pi	n h	igh;	wri	ting	a '0	' ha	s no	eff	ect				
е	RW	PIN30									-	Pin	30																				
			Low	0							ı	Rea	ıd: p	in (driv	/er	is lo	ow															
			High	1							ı	Rea	ıd: p	in (driv	/er	is h	igh															
			Set	1							١	Wri	te:	wri	ting	g a ˈ	1' s	sets	th	e pi	n h	igh;	wri	ting	a '0	' ha	s no	eff	ect				
f	RW	PIN31									ı	Pin	31																				
			Low	0							ı	Rea	ıd: p	in (driv	/er	is lo	ow															
			High	1							- 1	Rea	ıd: p	in (driv	/er	is h	igh															
			Set	1							,	Wri	te:	wri	ting	g a '	1' s	sets	th	e pi	n h	igh;	wri	ting	a '0	' ha	s no	eff	ect				

20.3.3 OUTCLR

Address offset: 0x50C

Clear individual bits in GPIO port Read: reads value of OUT register.

Bit	numb	er		31	30 2	29 2	8 27	7 26	25	24	23 22	21	20	19	18	17	16	15	14	13	12 1	1 10) 9	8	7	6	5	4	3	2 1	L O
Id				f	e	d c	b	а	Z	Υ	X W	٧	U	Т	S	R	Q	Р	0	N	M	_ K	J	1	Н	G	F	Е	D (C E	3 A
Res	et 0x	00000000		0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 () (0
Id	RW	/ Field	Value Id	Val	ue						Descri	otic	on																		
Α	RW	PIN0									Pin 0																				
			Low	0							Read:	oin	driv	ver	is l	ow															
			High	1							Read:	oin	driv	ver	is h	igh															
			Clear	1							Write:	wr	itin	g a	'1'	sets	th	e pi	n lo	w;	writ	ing a	'0'	has	no	effe	ect				
В	RW	PIN1									Pin 1																				
			Low	0							Read:	oin	driv	ver	is l	ow															
			High	1							Read:	oin	driv	ver	is h	igh															
			Clear	1							Write:	wr	itin	g a	'1' :	sets	th	e pi	n lo	w;	writ	ing a	'0'	has	no	effe	ect				
С	RW	PIN2									Pin 2																				
			Low	0							Read:	oin	driv	ver	is l	ow															
			High	1							Read:	oin	driv	ver	is h	igh															
			Clear	1							Write:	wr	itin	g a	'1'	sets	th	e pi	n lo	w;	writ	ing a	'0'	has	no	effe	ect				
D	RW	PIN3									Pin 3																				
			Low	0							Read:	oin	driv	ver	is l	ow															
			High	1							Read:	oin	driv	ver	is h	igh															
			Clear	1							Write:	wr	itin	g a	'1'	sets	th	e pi	n lo	w;	writ	ing a	'0'	has	no	effe	ect				
Ε	RW	PIN4									Pin 4																				
			Low	0							Read:	oin	driv	ver	is l	ow															
			High	1							Read:	oin	driv	ver	is h	igh															
			Clear	1							Write:	wr	itin	g a	'1'	sets	th	e pi	n lo	w;	writ	ing a	'0'	has	no	effe	ect				
F	RW	PIN5									Pin 5																				
			Low	0							Read:	oin	driv	ver	is l	ow															
			High	1							Read:	oin	driv	ver	is h	igh															
			Clear	1							Write:	wr	itin	g a	'1'	sets	th	e pi	n lo	w;	writ	ing a	'0'	has	no	effe	ect				
G	RW	PIN6									Pin 6																				
			Low	0							Read:	oin	driv	ver	is l	ow															
			High	1							Read:	oin	driv	ver	is h	igh															
			Clear	1							Write:	wr	itin	g a	'1'	sets	th	e pi	n lo	w;	writ	ing a	'0'	has	no	effe	ect				
Н	RW	PIN7									Pin 7																				
			Low	0							Read:	oin	driv	ver	is l	ow															
			High	1							Read:	oin	driv	ver	is h	igh															



Bit n	umbe	r		31 30	29 28	27	26 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b	a Z	Y	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Rese	t 0x0	0000000		0 0	0 0	0	0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
I	RW	PIN8							Pin 8
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
J	RW	PIN9							Pin 9
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
K	RW	PIN10							Pin 10
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
L	RW	PIN11							Pin 11
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
М	RW	PIN12							Pin 12
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
N	RW	PIN13		_					Pin 13
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
_	DVA	DINI4.4	Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
0	RW	PIN14	Law	0					Pin 14
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high Write: writing a '1' sets the pin low; writing a '0' has no effect
Р	D\A/	PIN15	Clear	1					Pin 15
-	11.00	LIMID	Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
Q	R\M	PIN16	Cicai	1					Pin 16
Q	11.00	11110	Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
R	RW	PIN17	Cicui	-					Pin 17
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
S	RW	PIN18							Pin 18
-		-	Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
Т	RW	PIN19							Pin 19
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
U	RW	PIN20							Pin 20
-		-	Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
V	RW	PIN21							Pin 21
			Low	0					Read: pin driver is low



DILL	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e d c b a Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
W	RW	PIN22			Pin 22
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
Χ	RW	PIN23			Pin 23
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
Υ	RW	PIN24			Pin 24
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
-	D)4/	DINIOS	Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
Z	KW	PIN25	La	0	Pin 25
			Low	0	Read: pin driver is low
			High Clear	1	Read: pin driver is high Write: writing a '1' sets the pin low; writing a '0' has no effect
a	D\A/	PIN26	Cledi	1	Pin 26
а	IVV	FINZO	Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
b	RW	PIN27			Pin 27
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
С	RW	PIN28			Pin 28
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
d	RW	PIN29			Pin 29
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
е	RW	PIN30			Pin 30
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
f	RW	PIN31			Pin 31
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect

20.3.4 IN

Address offset: 0x510 Read GPIO port

Bitı	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20 :	19	18 :	17	16	15	14	13	12 :	11 :	10	9	8	7	6	5	4	3	2	1 0
Id				f	е	d	С	b	а	Z	Υ	Х	W	٧	U	Т	S	R	Q	Р	О	N	М	L	K	J	I	Н	G	F	Ε	D	C I	ВА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	alue	:						De	scri	ptic	n																			
Α	R	PIN0										Pin	0																					
			Low	0								Pin	inp	ut i	s lo	w																		
			High	1								Pin	inp	ut i	s hi	gh																		



Bit r	numbe	er		31 30	29 2	8 27	' 26 2	25 24	1 23	22 21	20	19 1	8 17	16	15 1	14 13	3 12	11 :	10 9	8 (7	6 !	5 4	3	2	1 0
Id										W V																
Res	et 0x0	0000000		0 0	0 (0 0	0	0 0	0	0 0	0	0 (0 0	0	0	0 0	0	0	0 (0	0	0 (0 0	0	0	0 0
Id	RW	Field	Value Id	Value					De	scripti	on															
В	R	PIN1								n 1																
			Low	0						n input																
			High	1						n input	is h	nigh														
С	R	PIN2	Law	0						12	:- 1.															
			Low	0						n input n input																
D	R	PIN3	High	1						1 iliput 1 3	15 11	ııgıı														
		11145	Low	0						n input	is lo	οw														
			High	1						n input																
E	R	PIN4	-							n 4																
			Low	0					Pir	n input	is lo	ow														
			High	1					Pir	n input	is h	nigh														
F	R	PIN5							Pir	า 5																
			Low	0					Pir	n input	is lo	ow														
			High	1					Pir	n input	is h	nigh														
G	R	PIN6								า 6																
			Low	0						n input																
	_		High	1						n input –	is h	nigh														
Н	R	PIN7	Low	0						17	ia la															
			Low High	0						n input n input																
	R	PIN8	riigii	1						1 III put 1 8	13 11	ııgıı														
•		1110	Low	0						n input	is lo	οw														
			High	1						n input																
J	R	PIN9	-							1 9																
			Low	0					Pir	n input	is lo	ow														
			High	1					Pir	n input	is h	nigh														
K	R	PIN10							Pir	า 10																
			Low	0					Pir	n input	is lo	ow														
			High	1					Pir	n input	is h	nigh														
L	R	PIN11								า 11																
			Low	0						n input																
		DINI42	High	1						n input	is h	nigh														
М	R	PIN12	Low	0						n 12 n input	ic le	014														
			High	1						input input																
N	R	PIN13	111611	-						1 13	13 11															
			Low	0						n input	is lo	ow														
			High	1						n input																
0	R	PIN14								n 14																
			Low	0					Pir	n input	is lo	ow														
			High	1					Pir	n input	is h	nigh														
Р	R	PIN15							Pir	า 15																
			Low	0						n input																
			High	1						n input	is h	nigh														
Q	R	PIN16		_						n 16																
			Low	0						n input																
Р	P	PIN17	High	1						n input	is h	iigh														
R	R	FIIV1/	Low	0						n 17 n input	is la	OW/														
			High	1						input input																
S	R	PIN18		-						າ 18	.5 11	0''														
-		-	Low	0						n input	is lo	ow														
			High	1						n input																
Т	R	PIN19								n 19																



Bit r	iumbe	er		31 30	29	28	27	26	25 2	4 2	23 22 2	1 2	20 19	9 1	8 17	7 1	6 1	.5 1	4 1	3 12	2 13	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				f e	d	С	b	а	ΖY	,	x w v	V	U T	٠,	s R	. (Q	P	1 C	N N	1 L	K	J	1	Н	G	F	Е	D (В	, Α
Rese	et 0x0	0000000		0 0	0	0	0	0	0 0)	0 0 (0	0 0) (0 0	(0 (0	0 (0 0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Value							Descrip	tio	n																		
			Low	0						F	Pin inpu	ut i:	s low	,																	
			High	1						F	Pin inpu	ut i	s hig	h																	
U	R	PIN20								F	Pin 20																				
			Low	0						F	Pin inpu	ut i	s low	,																	
			High	1						F	Pin inpu	ut i	s hig	h																	
٧	R	PIN21								F	Pin 21																				
			Low	0						F	Pin inpu	ut i	s low	,																	
			High	1						F	Pin inpu	ut i	s hig	h																	
W	R	PIN22								F	Pin 22																				
			Low	0						F	Pin inpu	ut i	s low	,																	
			High	1						F	Pin inpu	ut i	s hig	h																	
Χ	R	PIN23								F	Pin 23																				
			Low	0						F	Pin inpu	ut i	s low	,																	
			High	1						F	Pin inpu	ut i	s hig	h																	
Υ	R	PIN24								F	Pin 24																				
			Low	0						F	Pin inpu	ut i	s low	/																	
			High	1						F	Pin inpu	ut i	s hig	h																	
Z	R	PIN25								F	Pin 25																				
			Low	0						F	Pin inpu	ut i	s low	/																	
			High	1						F	Pin inpu	ut i	s hig	h																	
а	R	PIN26								F	Pin 26																				
			Low	0						F	Pin inpu	ut i	s low	/																	
			High	1						F	Pin inpu	ut i	s hig	h																	
b	R	PIN27								F	Pin 27																				
			Low	0						F	Pin inpu	ut i	s low	/																	
			High	1							Pin inpu	ut i	s hig	h																	
С	R	PIN28									Pin 28																				
			Low	0							Pin inpu																				
			High	1							Pin inpu	ut i	s hig	h																	
d	R	PIN29									Pin 29																				
			Low	0							Pin inpu																				
			High	1							Pin inpu	ıt i	s hig	h																	
е	R	PIN30									Pin 30																				
			Low	0							Pin inpu																				
			High	1							Pin inpu	ut i:	s hig	h																	
f	R	PIN31									Pin 31																				
			Low	0							Pin inpu																				
			High	1						F	Pin inpu	ut i	s hig	h																	

20.3.5 DIR

Address offset: 0x514 Direction of GPIO pins

Rit r	numbe	or .		21	30	29	28	3 27	26	25	2/	23	22	21	20	19	12	17	16	15	1/1	13 1	12 1	1 1	n a	Q	7	6	5	1	3	γ .	1 0
	idilibe	-1																													_	_	
Id				Ť	е	d	С	b	а	2	Υ	Х	W	V	U	1	5	R	Q	Р	O	N I	M	L K	(J	- 1	Н	G	F	E	D	C	ВА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	PIN0										Pir	n 0																				
			Input	0								Pir	set	t as	inp	ut																	
			Output	1								Pir	set	t as	out	tput	:																
В	RW	PIN1										Pir	1																				
			Input	0								Pir	set	t as	inp	ut																	
			Output	1								Pir	set	t as	out	tput	:																
С	RW	PIN2										Pir	1 2																				



D.:				24.20	20.20	 	. 24	22 22 2	4 20	10.1	0 47	10	15.4	4.40	12.1	1 10	0	0 -	, ,		2 2	1
Bit r	iumbe	er ·						23 22 2 X W \														
	et 0x0	000000						0 0 0														
		Field	Value Id	Value				Descrip														
			Input	0				Pin set a		ut												
			Output	1				Pin set a	s out	put												
D	RW	PIN3						Pin 3														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	as out	put												
Ε	RW	PIN4						Pin 4														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	as out	put												
F	RW	PIN5						Pin 5														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	s out	put												
G	RW	PIN6						Pin 6														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	s out	put												
Н	RW	PIN7						Pin 7														
			Input	0				Pin set a														
			Output	1				Pin set a	as out	put												
I	RW	PIN8						Pin 8														
			Input	0				Pin set a														
	DIA	DINIO	Output	1				Pin set a	as out	put												
J	RW	PIN9		•				Pin 9														
			Input	0				Pin set a														
K	D\A/	PIN10	Output	1				Pin set a Pin 10	is out	put												
K	NVV	PINIO	Input	0				Pin set a	oc inn													
			Output	1				Pin set a														
L	RW	PIN11	Catput	•				Pin 11	is out	put												
-			Input	0				Pin set a	as inpi	ut												
			Output	1				Pin set a														
М	RW	PIN12	·					Pin 12														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	as out	put												
N	RW	PIN13						Pin 13														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	s out	put												
0	RW	PIN14						Pin 14														
			Input	0				Pin set a	as inp	ut												
			Output	1				Pin set a	s out	put												
Р	RW	PIN15						Pin 15														
			Input	0				Pin set a														
			Output	1				Pin set a	s out	put												
Q	RW	PIN16						Pin 16	_													
			Input	0				Pin set a														
_			Output	1				Pin set a	s out	put												
R	KW	PIN17	Lament	0				Pin 17														
			Input	0				Pin set a														
c	DIA	DINI19	Output	1				Pin set a	is out	.put												
S	ĸw	PIN18	Innut	0				Pin 18	inn.	+												
			Input					Pin set a														
Т	B/V	PIN19	Output	1				Pin set a	is out	.µut												
	ΚVV	LINTA	Innut	0					ic inn	ut												
			Input Output	1				Pin set a														
U	B/V	PIN20	σαιραι	1				Pin set a	is out	.pul												
J	11.00		Input	0				Pin set a	ıç inn	ut												
			put	J					.5 mp	J.												



Bitı	numbe	er		31 30	29	28 2	27 26	25	24	23 2	22 21	20 1	9 18	3 17	16	15	14 1	3 12	11	10 9	9 8	3 7	6	5	4	3 2	1	0
Id				f e	d	С	b a	Z	Υ	Χ١	w v	U T	S	R	Q	Р	0 1	N M	L	Κ.	JI	Н	G	F	Е	D C	В	Α
Res	et 0x0	0000000		0 0	0	0	0 0	0	0	0	0 0	0 0	0	0	0	0	0 (0	0	0 (0 (0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value						Des	criptio	on																
			Output	1						Pin s	set as	outp	ut															
٧	RW	PIN21								Pin 2	21																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
W	RW	PIN22								Pin 2	22																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
Χ	RW	PIN23								Pin 2	23																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
Υ	RW	PIN24								Pin 2	24																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
Z	RW	PIN25								Pin 2	25																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
а	RW	PIN26								Pin 2	26																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
b	RW	PIN27								Pin 2	27																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
С	RW	PIN28								Pin 2	28																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
d	RW	PIN29								Pin 2	29																	
			Input	0						Pin s	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															
е	RW	PIN30								Pin 3	30																	
			Input	0						Pin	set as	inpu	t															
			Output	1						Pin	set as	outp	ut															
f	RW	PIN31								Pin 3	31																	
			Input	0						Pin	set as	inpu	t															
			Output	1						Pin s	set as	outp	ut															

20.3.6 DIRSET

Address offset: 0x518

DIR set register

Read: reads value of DIR register.

Bit n	umbe	er		31	. 30	29	28	27	26 2	25 :	24	23	22	21 2	20	19	18	17	16	15	14 :	13 1	L2 1	1 1	9	8	7	6	5	4	3	2 1	. 0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	V	U	Т	S	R	Q	Р	0	N I	M I	. k	J	-1	Н	G	F	Ε	D	C E	3 A
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0 0
Id	RW	Field	Value Id	Va	lue							De	scrip	otio	n																		
Α	RW	PIN0										Set	as	out	put	pir	0																
			Input	0								Rea	ad: p	oin :	set	as i	npı	ut															
			Output	1									ad: p	oin :	set	as (out	put															
			Set	1								Wr	ite:	wri	ting	g a '	1' s	ets	pir	to	out	put	; wı	itin	ga'	0' h	as r	no e	ffe	ct			
В	RW	PIN1										Set	as	out	put	pir	1																
			Input	0								Rea	ad: p	oin :	set	as i	npı	ut															
			Output	1								Rea	ad: p	oin :	set	as (out	put															
			Set	1									ite:	wri	ting	g a '	1' s	ets	pir	to	out	put	; wı	itin	g a '	0' h	as r	io e	ffe	ct			
С	RW	PIN2										Set	as	out	put	pir	2																



Bit r	iumbe	er		31 30	29 28	27 26	25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	ΖY	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0 0	0 (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value				Description
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
_		B.1.1.0	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
D	RW	PIN3		•				Set as output pin 3
			Input	0				Read: pin set as input
			Output Set	1				Read: pin set as output Write: writing a '1' sets pin to output; writing a '0' has no effect
E	RW/	PIN4	Jei	1				Set as output pin 4
-		11144	Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
F	RW	PIN5						Set as output pin 5
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
G	RW	PIN6						Set as output pin 6
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Н	RW	PIN7						Set as output pin 7
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
I	RW	PIN8						Set as output pin 8
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
		B.11.0	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
J	RW	PIN9		•				Set as output pin 9
			Input	0				Read: pin set as input
			Output Set	1				Read: pin set as output Write: writing a '1' sets pin to output; writing a '0' has no effect
K	R\M/	PIN10	Set	1				Set as output pin 10
K	IVV	FINIO	Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
L	RW	PIN11		_				Set as output pin 11
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
М	RW	PIN12						Set as output pin 12
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
N	RW	PIN13						Set as output pin 13
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
0	RW	PIN14						Set as output pin 14
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Р	RW	PIN15						Set as output pin 15
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect



Bit	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5	4 3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGF	E D C B A
Res	set 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	00000
Id	RW Field	Value Id	Value Description	
Q	RW PIN16		Set as output pin 16	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
_	D	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no eff	ect
R	RW PIN17		Set as output pin 17	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
_	DIA DINIAO	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no eff	ect
S	RW PIN18	lanut	Set as output pin 18 O Read: pin set as input	
		Input	·	
		Output	1 Read: pin set as output Write: writing a '1' sets pin to output; writing a '0' has no eff	a a t
Т	RW PIN19	Set	Set as output pin 19	ect
•	VAN LIINTA	Innut	0 Read: pin set as input	
		Input	·	
		Output Set	 Read: pin set as output Write: writing a '1' sets pin to output; writing a '0' has no eff 	act
U	RW PIN20	Set	Set as output pin 20	eci
U	NW PINZU	Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no eff	act
V	RW PIN21	361	Set as output pin 21	
٠	NVV 111VZ1	Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no eff	ert
W	RW PIN22	360	Set as output pin 22	
••	111122	Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no eff	ect
Χ	RW PIN23	500	Set as output pin 23	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no eff	ect
Υ	RW PIN24		Set as output pin 24	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no eff	ect
Z	RW PIN25		Set as output pin 25	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no eff	ect
а	RW PIN26		Set as output pin 26	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no eff	ect
b	RW PIN27		Set as output pin 27	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no eff	ect
С	RW PIN28		Set as output pin 28	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no eff	ect
d	RW PIN29		Set as output pin 29	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	



Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20 1	.9 1	.8 1	7 16	15	14	13	L2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U .	Т :	S F	Q	P	О	N	M	L K	J	1	Н	G	F	ЕΙ	ОС	В	Α
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue	!						De	scri	ptic	n																	
			Set	1								W	rite:	wri	ting	a ':	1' se	ts p	in to	ο οι	ıtpu	; w	ritin	g a '	0' ha	as n	o e	ffec	t			
е	RW	PIN30		0								Se	t as	out	put	pin	30															
			Input	0								Re	ad: ¡	pin	set a	as ii	npu	t														
			Output	1								Re	ad: ¡	pin	set a	as o	utp	ut														
			Set	1								W	rite:	wri	ting	a ':	1' se	ts p	in to	οι	ıtpu	; w	ritin	g a '	0' ha	as n	o e	ffec	t			
f	RW	PIN31		1								Se	t as	out	put	pin	31															
			Input	0								Re	ad: ¡	pin	set a	as ii	npu	t														
			Output	1									ad: ¡	pin	set a	as o	utp	ut														
			Set	1										wri	ting	a ':	1' se	ts p	in to	οι	ıtpu	; w	ritin	g a '	0' ha	as n	o e	ffec	t			

20.3.7 DIRCLR

Address offset: 0x51C

DIR clear register

Read: reads value of DIR register.

Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
Α	RW PINO		Set as input pin 0
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
В	RW PIN1		Set as input pin 1
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
С	RW PIN2		Set as input pin 2
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
D	RW PIN3		Set as input pin 3
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
Е	RW PIN4		Set as input pin 4
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
F	RW PIN5		Set as input pin 5
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
G	RW PIN6		Set as input pin 6
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
Н	RW PIN7		Set as input pin 7
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
I	RW PIN8		Set as input pin 8
		Input	0 Read: pin set as input



Bitı	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCB
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
J	RW PIN9		Set as input pin 9
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
K	RW PIN10		Set as input pin 10
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
	DW DINIA	Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
L	RW PIN11	lanut	Set as input pin 11 O Read: pin set as input
		Input Output	0 Read: pin set as input 1 Read: pin set as output
		Clear	Write: writing a '1' sets pin to input; writing a '0' has no effect
М	RW PIN12	Clear	
141	1744 1 114TC	Input	Set as input pin 12 O Read: pin set as input
		Output	1 Read: pin set as input 1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
N	RW PIN13	Cicai	Set as input pin 13
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
0	RW PIN14		Set as input pin 14
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
Р	RW PIN15		Set as input pin 15
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
Q	RW PIN16		Set as input pin 16
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
R	RW PIN17		Set as input pin 17
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
S	RW PIN18		Set as input pin 18
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
_		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
Т	RW PIN19		Set as input pin 19
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
	DIA DINIZO	Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
U	RW PIN20	lpo::+	Set as input pin 20
		Input	0 Read: pin set as input 1 Read: pin set as output
		Output	1 Read: pin set as output Write: writing a '1' sets pin to input: writing a '0' has no effect
V	RW PIN21	Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect Set as input pin 21
٧	VAN LINST	Input	Set as input pin 21 O Read: pin set as input
		Input Output	0 Read: pin set as input 1 Read: pin set as output
		Clear	Read: pin set as output Write: writing a '1' sets pin to input; writing a '0' has no effect
\^/	RW PIN22	Ciedi	
W	IVAN LINTY		Set as input pin 22



Bit	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZ	Y X W V U T S R Q P O N M L K J I H G F E D C B A
Res	set 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
Χ	RW PIN23			Set as input pin 23
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
Υ	RW PIN24			Set as input pin 24
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
Z	RW PIN25			Set as input pin 25
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
а	RW PIN26			Set as input pin 26
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
b	RW PIN27			Set as input pin 27
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
С	RW PIN28			Set as input pin 28
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
d	RW PIN29			Set as input pin 29
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
е	RW PIN30			Set as input pin 30
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
f	RW PIN31			Set as input pin 31
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect

20.3.8 LATCH

Address offset: 0x520

Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers

Bit	numb	er		31	30	29	28 2	27 2	26 2	5 2	24 2	3 2	2 21	1 20	19	18	17	16	15	14 1	.3 1	2 11	. 10	9	8	7	6	5	4	3 2	1	0
Id				f	e	d	С	b	a Z	Z	Υ 2	< V	V V	U	Т	S	R	Q	Р	0	N N	1 L	K	J	1	Н	G	F	Е	0 0	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0 (0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						C	esc	ript	ion																		
Α	RW	PIN0											us o	n wl	neth	her	PIN) ha	as m	et o	rite	ria s	et ir	n PII	N_C	NF	O.SE	NS	E			
												egis	ster.	Wr	ite '	1' t	o cle	ar.														
			NotLatched	0									eria l	has	not	bee	en m	net														
			Latched	1									eria l	has	bee	n m	et															
В	RW	PIN1											us o	n wl	neth	her	PIN:	1 ha	as m	et o	rite	ria s	et ir	n PII	N_C	NF:	1.SE	NS	E			
														Wr	ite '	1' t	o cle	ear.														



Bitı	number	r		31 30	29 28	3 27	26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00	0000000		0 0	0 0	0	0 (0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	•				Description
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
С	RW	PIN2							Status on whether PIN2 has met criteria set in PIN_CNF2.SENSE
									register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
D	RW	PIN3							Status on whether PIN3 has met criteria set in PIN_CNF3.SENSE
				_					register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
_	D\A/	DINIA	Latched	1					Criteria has been met
E	RW	PIN4							Status on whether PIN4 has met criteria set in PIN_CNF4.SENSE
			NotLatched	0					register. Write '1' to clear. Criteria has not been met
			Latched	1					Criteria has been met
F	RW	PIN5	Laterica	_					Status on whether PIN5 has met criteria set in PIN_CNF5.SENSE
									register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
G	RW	PIN6							Status on whether PIN6 has met criteria set in PIN_CNF6.SENSE
									register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
Н	RW	PIN7							Status on whether PIN7 has met criteria set in PIN_CNF7.SENSE
									register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
I	RW	PIN8							Status on whether PIN8 has met criteria set in PIN_CNF8.SENSE
				_					register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
	D\A/	DINO	Latched	1					Criteria has been met
J	RW	PIN9							Status on whether PIN9 has met criteria set in PIN_CNF9.SENSE
			NotLatched	0					register. Write '1' to clear. Criteria has not been met
			Latched	1					Criteria has been met
K	RW	PIN10	Luterieu	-					Status on whether PIN10 has met criteria set in
									PIN_CNF10.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
L	RW	PIN11							Status on whether PIN11 has met criteria set in
									PIN_CNF11.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
M	RW	PIN12							Status on whether PIN12 has met criteria set in
									PIN_CNF12.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
N	RW	PIN13							Status on whether PIN13 has met criteria set in
									PIN_CNF13.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
0	RW	PIN14							Status on whether PIN14 has met criteria set in
			Not atched	0					PIN_CNF14.SENSE register. Write '1' to clear.
			NotLatched Latched	0					Criteria has not been met Criteria has been met
			Latched	1					Criteria nas peen met



Bit r	numbe	er		31 30	29 28	3 27	26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et OxO	0000000		0 0	0 0	0	0	0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value					Description
Р	RW	PIN15							Status on whether PIN15 has met criteria set in
									PIN_CNF15.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
	DIA	PIN16	Latched	1					Criteria has been met
Q	KVV	PINTO							Status on whether PIN16 has met criteria set in PIN_CNF16.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
R	RW	PIN17							Status on whether PIN17 has met criteria set in
									PIN_CNF17.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
S	RW	PIN18							Status on whether PIN18 has met criteria set in
									PIN_CNF18.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
_	5144		Latched	1					Criteria has been met
Т	RW	PIN19							Status on whether PIN19 has met criteria set in
			NotLatched	0					PIN_CNF19.SENSE register. Write '1' to clear. Criteria has not been met
			Latched	1					Criteria has been met
U	RW	PIN20	20101160	-					Status on whether PIN20 has met criteria set in
									PIN_CNF20.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
V	RW	PIN21							Status on whether PIN21 has met criteria set in
									PIN_CNF21.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
W	RW	PIN22							Status on whether PIN22 has met criteria set in
			NotLatched	0					PIN_CNF22.SENSE register. Write '1' to clear. Criteria has not been met
			Latched	1					Criteria has been met
Χ	RW	PIN23	20101100	-					Status on whether PIN23 has met criteria set in
									PIN_CNF23.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
Υ	RW	PIN24							Status on whether PIN24 has met criteria set in
									PIN_CNF24.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
_	5144		Latched	1					Criteria has been met
Z	RW	PIN25							Status on whether PIN25 has met criteria set in
			NotLatched	0					PIN_CNF25.SENSE register. Write '1' to clear. Criteria has not been met
			Latched	1					Criteria has been met
а	RW	PIN26	Editified	-					Status on whether PIN26 has met criteria set in
									PIN_CNF26.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
b	RW	PIN27							Status on whether PIN27 has met criteria set in
									PIN_CNF27.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
С	RW	PIN28							Status on whether PIN28 has met criteria set in
			Notletahad	0					PIN_CNF28.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met



Bit number		31	30 29	28 2	7 26	25 2	4 23	22 21	20 1	19 18	3 17	16	15 1	4 13	12	11 1	0 9	8	7	6 5	5 4	3	2 :	L 0
Id		f	e d	c b	а	ΖY	′ X	w v	U	T S	R	Q	P (O N	М	L k	J	1	Н	G F	E	D	C E	3 A
Reset 0x0000	0000	0	0 0	0 0	0	0 (0	0 0	0	0 0	0	0	0 (0 0	0	0 0	0	0	0	0 0	0	0	0 (0
Id RW Fie	ld Value Id	Va	lue				Des	cription	on															
	Latched	1					Crit	eria h	as be	een r	net													
d RW PIN	N29						Sta	tus on	whe	ether	PIN	29 h	as n	net o	rite	ria se	t in							
							PIN	_CNF2	29.SE	NSE	regi	ster	. Wr	ite '	l' to	clear								
	NotLatche	d 0					Crit	eria h	as no	ot be	en n	net												
	Latched	1					Crit	eria h	as be	een r	net													
e RW PIN	130						Sta	tus on	whe	ether	PIN	30 h	as n	net o	rite	ria se	t in							
							PIN	_CNF3	30.SE	NSE	regi	ster	. Wr	ite '	l' to	clear								
	NotLatche	d 0					Crit	eria h	as no	ot be	en n	net												
	Latched	1					Crit	eria h	as be	een r	net													
f RW PIN	N31						Sta	tus on	whe	ether	PIN	31 h	as n	net o	rite	ria se	t in							
							PIN	_CNF3	31.SE	NSE	regi	ster	. Wr	ite '	l' to	clear								
	NotLatche	d 0					Crit	eria h	as no	ot be	en n	net												
	Latched	1					Crit	eria h	as be	een r	net													

20.3.9 DETECTMODE

Address offset: 0x524

Select between default DETECT signal behaviour and LDETECT mode

Bit	numbe	er		3	31 30	0 29	2	8 27	7 2	6 2	5 2	24 2	23 2	2 2:	1 20) 19	18	17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1	0
Id																																		Α
Re	et 0x0	0000000		0	0	0	0	0) () () (0	0 (0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0
Id	RW	RW Field Value Id Value										0	Desc	ript	ion																			
Α	RW											S	Sele	ct b	etw	een	de	faul	t Di	ETE	CT s	ign	al b	ehav	iou	ır ar	ıd L	DET	ECT	Γ				
												n	nod	e																				
			Default	0									DETE	CT	dire	ectly	со	nne	cte	d to	II9 c	N DI	TE	CT si	gna	ıls								
	LDETECT 1										ι	Jse 1	the	lato	hed	LD	ETE	CT	beh	avi	our													

20.3.10 PIN_CNF[0]

Address offset: 0x700

Di+ »	numb	o.r		21	20	20	20.	77.	20.2	ר ה	24.	23 2	2 21	20	10	10	17	10	1 [11	12 1	2 1	1 10		8	7	6	5	Δ	3 2	1	0
	lumb	er		31	. 30	29	28 .	21.	20 2	25 2	24 .	23 Z.	2 21	. 20	19	10			15	14	13 1	.2 1				/	O	Э				
Id																	Ε	E					D	D	D					C C		Α
Res	et Ox(00000002		0	0	0	0	0	0 (0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0) 1	0
Id	RW	Field	Value Id	Va	lue						- 1	Desc	ripti	on																		
Α	RW	DIR									ı	Pin d	irec	tion	. Sa	me	ph	ysic	al r	egi	ster	as [IR r	egis	ter							
			Input	0							(Conf	igur	e pii	n as	an	inp	ut	pin													
			Output	1							(Conf	igur	e pii	n as	an	ou	tpu	t piı	n												
В	RW	INPUT									(Conr	ect	or d	lisco	onn	ect	inp	ut k	ouff	er											
			Connect	0							(Conr	ect	inpı	ut b	uff	er															
			Disconnect	1							1	Disco	nne	ct i	npu	t bı	uffe	r														
С	RW	PULL									ı	Pull	onf	igur	atic	n																
			Disabled	0							ı	No р	ull																			
			Pulldown	1							F	Pull	dow	n or	n piı	า																
			Pullup	3							ı	Pull ı	ıp o	n pi	n																	
D	RW	DRIVE									ı	Drive	cor	nfigu	urat	ion																
			S0S1	0							9	Stan	dard	'0',	sta	nda	ard	'1'														
			H0S1	1							ı	High	driv	e '0	', st	and	dard	d '1'														
			SOH1	2							9	Stan	dard	'0',	hig	h d	lrive	e '1'														
			H0H1	3							ı	High	driv	e '0	', hi	gh	'dri	ve '	1"													
			D0S1	4							1	Disco	nne	ct '	0' st	an	dar	d '1'	' (no	orm	ally	use	d fo	r wi	red-	or						
											(conn	ecti	ons)																	



Bit number		31 3	30 29	28	8 27	26	25	24	23 2	2 21	20	19	18 :	17 1	16 1	L5 1	4 13	3 12	11	10	9	8	7 (5 5	5 4	3	2	1	0
Id														Е	E					D	D	D				С	С	В	Α
Reset 0x00000002		0 (0 0	0	0	0	0	0	0 0	0 0	0	0	0	0	0 (0 (0 0	0	0	0	0	0 () (0 (0	0	0	1	0
ld RW Field	Value Id	Valu	ıe						Desc	ripti	on																		
	D0H1	5							Disco	onne	ct '(0', h	igh	driv	⁄e '1	L' (n	orm	ally	use	d fo	r w	ired	or						
									conn	nectio	ons))																	
	SOD1	6						:	Stan	dard	'0'.	disc	oni	nect	t '1'	(nc	rma	lly u	sed	for	iiw	ed-	nd						
									conn	nectio	ons))																	
	H0D1	7							High	driv	e '0	', dis	cor	nne	ct '1	L' (n	orm	ally	use	d fo	r w	ired	an	d					
									conn	nectio	ons))																	
E RW SENSE									Pin s	ensii	ng n	necł	nani	sm															
	Disabled	0							Disal	bled																			
	High	2						:	Sens	e for	hig	gh le	vel																
	Low	3						:	Sens	e for	lov	v lev	el																

20.3.11 PIN_CNF[1]

Address offset: 0x704

Configuration of GPIO pins

Bit n	umbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Rese	t 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.12 PIN_CNF[2]

Address offset: 0x708



Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E D D D C C B A
Res	et 0x0	0000002		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.13 PIN_CNF[3]

Address offset: 0x70C Configuration of GPIO pins

Bit r	numbe	er		31	30	29 2	28 2	7 2	6 25	5 24	23	22	21	20	19 1	18 1	17 :	16 :	15 1	4 1	3 1	2 1:	l 10	9	8	7	6	5	4 3	2	1	0
Id																	E	Ε					D	D	D				C	С	В	Α
Rese	et OxC	0000002		0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0	0	1	0
Id	RW	Field	Value Id	Va	lue						Des	scri	ptic	n																		
Α	RW	DIR									Pin	dir	ecti	on.	San	ne į	phy	sic	al re	gist	er a	as D	IR re	egis	ter							
			Input	0							Cor	nfig	ure	pin	as a	an i	inpı	ut p	in													
			Output	1							Cor	nfig	ure	pin	as a	an d	out	put	pin													
В	RW	INPUT									Cor	nne	ct o	r di	iscoı	nne	ect i	npi	ut b	uffe	r											
			Connect	0							Cor	nne	ct ii	npu	t bu	ffe	r															
			Disconnect	1							Disc	con	nec	t in	put	but	ffer	•														
С	RW	PULL									Pul	l co	nfig	gura	atior	1																
			Disabled	0							No	pu	II																			
			Pulldown	1							Pull	l do	own	on	pin																	
			Pullup	3							Pull	l up	o on	pir	1																	
D	RW	DRIVE									Driv	ve o	cont	figu	ratio	on																
			S0S1	0							Sta	nda	ard	'0',	stan	daı	rd '	1'														
			H0S1	1							Hig	h d	rive	'0'	, sta	nda	ard	'1'														
			S0H1	2							Sta	nda	ard	'0',	high	dr	ive	'1'														
			H0H1	3							Hig	h d	rive	'0'	, hig	h 'c	driv	e '1	."													
			DOS1	4							Disc	con	nec	t '0)' sta	nd	ard	'1'	(no	rma	lly	use	d for	wi	red-	or						
											con	ne	ctio	ns)																		



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	E E DDD CCBA
Reset 0x00000002	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value Description
D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
	connections)
SOD1	6 Standard '0'. disconnect '1' (normally used for wired-and
	connections)
H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
	connections)
E RW SENSE	Pin sensing mechanism
Disabled	0 Disabled
High	2 Sense for high level
Low	3 Sense for low level

20.3.14 PIN_CNF[4]

Address offset: 0x710

Configuration of GPIO pins

	<u> </u>		
Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E E D D D C C B A
Reset 0x00000002		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW DIR			Pin direction. Same physical register as DIR register
	Input	0	Configure pin as an input pin
	Output	1	Configure pin as an output pin
B RW INPUT			Connect or disconnect input buffer
	Connect	0	Connect input buffer
	Disconnect	1	Disconnect input buffer
C RW PULL			Pull configuration
	Disabled	0	No pull
	Pulldown	1	Pull down on pin
	Pullup	3	Pull up on pin
D RW DRIVE			Drive configuration
	S0S1	0	Standard '0', standard '1'
	H0S1	1	High drive '0', standard '1'
	SOH1	2	Standard '0', high drive '1'
	H0H1	3	High drive '0', high 'drive '1"
	DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
			connections)
	D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or connections)
	SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
	11004	_	connections)
	H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
F DW CENCE			connections)
E RW SENSE	Disabled	0	Pin sensing mechanism
	Disabled	0	Disabled
	High	2	Sense for high level
	Low	3	Sense for low level

20.3.15 PIN_CNF[5]

Address offset: 0x714



Bit r	numbe	er		31	30 2	29 28	27	26 2	25 24	4 23	3 22	21 2	0 1	9 18	17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3 2	1	0
Id															Ε	Ε					[) [D					c c	В	Α
Res	et OxC	0000002		0	0 (0 0	0	0	0 0	0	0	0 (0 0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0 0	1	0
Id	RW	Field	Value Id	Val	ue					D	escri	ptior	n																	
Α	RW	DIR								Pi	in dii	ectio	n. S	ame	e ph	iysic	cal ı	regis	ster	as	DIR	regi	ster							
			Input	0						Co	onfig	ure p	oin a	as ar	n inp	out	pin													
			Output	1						Co	onfig	ure p	oin a	as ar	n ou	itpu	t pi	n												
В	RW	INPUT								Co	onne	ct or	dis	conr	nect	inp	ut	buff	er											
			Connect	0						Co	onne	ct in	put	buff	er															
			Disconnect	1						Di	iscor	nect	inp	ut b	uffe	er														
С	RW	PULL								Pι	ull co	nfigu	urat	ion																
			Disabled	0						N	lo pu	II																		
			Pulldown	1						Pι	ull d	own o	on p	in																
			Pullup	3						Pι	ull u	on p	pin																	
D	RW	DRIVE								D	rive	confi	gura	atior	1															
			S0S1	0						St	tand	ard 'C)', st	and	ard	'1'														
			HOS1	1						Hi	igh c	rive '	'0', s	stan	dar	d '1'	•													
			S0H1	2						St	tand	ard 'C)', h	igh c	driv	e '1'	'													
			H0H1	3						Hi	igh c	rive '	'0', I	nigh	'dri	ive '	1"													
			DOS1	4						Di	iscor	nect	'0'	stan	dar	d '1	' (n	orm	ally	/ us	ed fo	or w	/ired	l-or						
										cc	onne	ction	ıs)																	
			D0H1	5								nect ction		higł	n dr	ive	'1' ((nor	ma	lly ι	ısed	for	wir	ed-o	r					
			S0D1	6								ard 'C	•			a+ 11	11/-		المد		. a d f			4	ام					
			3001	О								ction		iscoi	ine	CL J	L (I	10111	Idli	y us	eu i	OI V	vire	u-ai	ıu					
			H0D1	7						Hi	igh c	rive '	'0', d	disco	onn	ect '	'1' (nor	ma	lly ι	ısed	for	wir	ed-a	nd					
										cc	onne	ction	ıs)																	
Е	RW	SENSE								Pi	in se	nsing	me	cha	nisn	n														
			Disabled	0						Di	isabl	ed																		
			High	2						Se	ense	for h	igh	leve	el															
			Low	3						Se	ense	for lo	ow I	evel																

20.3.16 PIN_CNF[6]

Address offset: 0x718

Bit r	numbe	er		31	30	29 2	28 2	7 2	6 25	5 24	23	22	21	20	19 1	18 1	17 :	16 :	15 1	4 1	3 1	2 1:	l 10	9	8	7	6	5	4 3	2	1	0
Id																	E	Ε					D	D	D				C	С	В	Α
Rese	et OxC	0000002		0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0	0	1	0
Id	RW	Field	Value Id	Va	lue						Des	scri	ptic	n																		
Α	RW	DIR									Pin	dir	ecti	on.	San	ne į	phy	sic	al re	gist	er a	as D	IR re	egis	ter							
			Input	0							Cor	nfig	ure	pin	as a	an i	inpı	ut p	in													
			Output	1							Cor	nfig	ure	pin	as a	an d	out	put	pin													
В	RW	INPUT									Cor	nne	ct o	r di	iscoı	nne	ect i	npi	ut b	uffe	r											
			Connect	0							Cor	nne	ct ii	npu	t bu	ffe	r															
			Disconnect	1							Disc	con	nec	t in	put	but	ffer	•														
С	RW	PULL									Pul	l co	nfig	gura	atior	1																
			Disabled	0							No	pu	II																			
			Pulldown	1							Pull	l do	own	on	pin																	
			Pullup	3							Pull	l up	o on	pir	1																	
D	RW	DRIVE									Driv	ve o	cont	figu	ratio	on																
			S0S1	0							Sta	nda	ard	'0',	stan	daı	rd '	1'														
			H0S1	1							Hig	h d	rive	'0'	, sta	nda	ard	'1'														
			S0H1	2							Sta	nda	ard	'0',	high	dr	ive	'1'														
			H0H1	3							Hig	h d	rive	'0'	, hig	h 'c	driv	e '1	."													
			DOS1	4							Disc	con	nec	t '0)' sta	nd	ard	'1'	(no	rma	lly	use	d for	wi	red-	or						
											con	ne	ctio	ns)																		



Bit number		31 3	30 29	28	8 27	26	25	24	23 2	2 21	20	19	18 :	17 1	16 1	L5 1	4 13	3 12	11	10	9	8	7 (5 5	5 4	3	2	1	0
Id														Е	E					D	D	D				С	С	В	Α
Reset 0x00000002		0 (0 0	0	0	0	0	0	0 0	0 0	0	0	0	0	0 (0 (0 0	0	0	0	0	0 () (0 (0	0	0	1	0
ld RW Field	Value Id	Valu	ıe						Desc	ripti	on																		
	D0H1	5							Disco	onne	ct '(0', h	igh	driv	⁄e '1	L' (n	orm	ally	use	d fo	r w	ired	or						
									conn	nectio	ons))																	
	SOD1	6						:	Stan	dard	'0'.	disc	oni	nect	t '1'	(nc	rma	lly u	sed	for	iiw	ed-	nd						
									conn	nectio	ons))																	
	H0D1	7							High	driv	e '0	', dis	cor	nne	ct '1	L' (n	orm	ally	use	d fo	r w	ired	an	d					
									conn	nectio	ons))																	
E RW SENSE									Pin s	ensii	ng n	necł	nani	sm															
	Disabled	0							Disal	bled																			
	High	2						:	Sens	e for	hig	gh le	vel																
	Low	3						:	Sens	e for	lov	v lev	el																

20.3.17 PIN_CNF[7]

Address offset: 0x71C

Configuration of GPIO pins

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		E E DDD CCB
Reset 0x00000002		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW DIR		Pin direction. Same physical register as DIR register
	Input	0 Configure pin as an input pin
	Output	1 Configure pin as an output pin
B RW INPUT		Connect or disconnect input buffer
	Connect	0 Connect input buffer
	Disconnect	1 Disconnect input buffer
C RW PULL		Pull configuration
	Disabled	0 No pull
	Pulldown	1 Pull down on pin
	Pullup	3 Pull up on pin
D RW DRIVE		Drive configuration
	S0S1	0 Standard '0', standard '1'
	H0S1	1 High drive '0', standard '1'
	S0H1	2 Standard '0', high drive '1'
	H0H1	3 High drive '0', high 'drive '1"
	DOS1	4 Disconnect '0' standard '1' (normally used for wired-or
		connections)
	D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
		connections)
	SOD1	6 Standard '0'. disconnect '1' (normally used for wired-and
		connections)
	H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
	Disabled	0 Disabled
	High	2 Sense for high level
	Low	3 Sense for low level

20.3.18 PIN_CNF[8]

Address offset: 0x720



Bit	number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E E DDD CCBA
Res	et 0x00000002		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW DIR			Pin direction. Same physical register as DIR register
		Input	0	Configure pin as an input pin
		Output	1	Configure pin as an output pin
В	RW INPUT			Connect or disconnect input buffer
		Connect	0	Connect input buffer
		Disconnect	1	Disconnect input buffer
С	RW PULL			Pull configuration
		Disabled	0	No pull
		Pulldown	1	Pull down on pin
		Pullup	3	Pull up on pin
D	RW DRIVE			Drive configuration
		SOS1	0	Standard '0', standard '1'
		H0S1	1	High drive '0', standard '1'
		S0H1	2	Standard '0', high drive '1'
		H0H1	3	High drive '0', high 'drive '1"
		DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
				connections)
		D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
				connections)
		SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
				connections)
		H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
				connections)
Ε	RW SENSE			Pin sensing mechanism
		Disabled	0	Disabled
		High	2	Sense for high level
		Low	3	Sense for low level

20.3.19 PIN_CNF[9]

Address offset: 0x724

ССВА
0 0 1 0



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.20 PIN_CNF[10]

Address offset: 0x728

Configuration of GPIO pins

	<u> </u>		
Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E E D D D C C B A
Reset 0x00000002		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
ld RW Field	Value Id	Value	Description
A RW DIR			Pin direction. Same physical register as DIR register
	Input	0	Configure pin as an input pin
	Output	1	Configure pin as an output pin
B RW INPUT			Connect or disconnect input buffer
	Connect	0	Connect input buffer
	Disconnect	1	Disconnect input buffer
C RW PULL			Pull configuration
	Disabled	0	No pull
	Pulldown	1	Pull down on pin
	Pullup	3	Pull up on pin
D RW DRIVE			Drive configuration
	S0S1	0	Standard '0', standard '1'
	H0S1	1	High drive '0', standard '1'
	SOH1	2	Standard '0', high drive '1'
	H0H1	3	High drive '0', high 'drive '1"
	D0S1	4	Disconnect '0' standard '1' (normally used for wired-or
			connections)
	D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or connections)
	SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
	11004	-	connections)
	H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
F DW CENCE			connections)
E RW SENSE	Disabled	0	Pin sensing mechanism
	Disabled	0	Disabled
	High	2	Sense for law level
	Low	3	Sense for low level

20.3.21 PIN_CNF[11]

Address offset: 0x72C



Bit	number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E E DDD CCBA
Res	et 0x00000002		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW DIR			Pin direction. Same physical register as DIR register
		Input	0	Configure pin as an input pin
		Output	1	Configure pin as an output pin
В	RW INPUT			Connect or disconnect input buffer
		Connect	0	Connect input buffer
		Disconnect	1	Disconnect input buffer
С	RW PULL			Pull configuration
		Disabled	0	No pull
		Pulldown	1	Pull down on pin
		Pullup	3	Pull up on pin
D	RW DRIVE			Drive configuration
		S0S1	0	Standard '0', standard '1'
		H0S1	1	High drive '0', standard '1'
		S0H1	2	Standard '0', high drive '1'
		H0H1	3	High drive '0', high 'drive '1"
		D0S1	4	Disconnect '0' standard '1' (normally used for wired-or
				connections)
		D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
				connections)
		S0D1	6	Standard '0'. disconnect '1' (normally used for wired-and
				connections)
		H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
				connections)
Ε	RW SENSE			Pin sensing mechanism
		Disabled	0	Disabled
		High	2	Sense for high level
		Low	3	Sense for low level

20.3.22 PIN_CNF[12]

Address offset: 0x730 Configuration of GPIO pins

ССВА
0 0 1 0



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.23 PIN_CNF[13]

Address offset: 0x734

Configuration of GPIO pins

Bit n	umbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Rese	t 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.24 PIN_CNF[14]

Address offset: 0x738



Bit r	numbe	er		31	30 2	9 2	8 27	7 26	5 25	5 24	23	3 2	22 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																	Ε	Ε						D	D	D					C (В	А
Res	et 0x0	0000002		0	0 (0 (0 0	0	0	0	0	(0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () 1	. 0
Id	RW	Field	Value Id	Val	ue						De	esc	criptio	on																			
Α	RW	DIR									Piı	n c	direct	ion	ı. Sa	me	ph	ıysi	al ı	regi	ste	as	DIR	re	gist	er							
			Input	0							Co	onf	figure	e pi	n as	an	inp	out	pin														
			Output	1							Co	onf	figure	e pi	n as	an	ou	tpu	t pi	in													
В	RW	INPUT									Co	onr	nect o	or c	disco	onn	ect	inp	ut	buf	fer												
			Connect	0							Co	nr	nect i	npı	ut b	uff	er																
			Disconnect	1							Di	isc	onne	ct i	npu	t b	uffe	er															
С	RW	PULL									Ρu	ull	confi	gur	atic	n																	
			Disabled	0							No	о р	oull																				
			Pulldown	1							Pu	ull	dowr	n or	n pii	า																	
			Pullup	3							Pu	ull	up or	n pi	n																		
D	RW	DRIVE									Dr	rive	e con	fig	urat	ion	1																
			S0S1	0							St	an	ndard	'0',	, sta	nda	ard	'1'															
			H0S1	1							Hi	igh	drive	e '0	', st	and	dar	d '1	'														
			S0H1	2							St	an	ndard	'0',	, hig	h d	lriv	e '1	1														
			H0H1	3							Hi	igh	drive	e '0	l', hi	gh	'dri	ve '	1"														
			DOS1	4							Di	isc	onne	ct '	0' st	an	dar	d '1	' (n	orn	nall	y us	ed 1	for	wir	ed-	or						
											со	onr	nectio	ons)																		
			D0H1	5									onne			nigh	n dr	ive	'1'	(nor	ma	lly ι	ısed	d fo	rw	/ire	d-oı						
			SOD1	6							St	an	ndard	'0'.	. dis	cor	nne	ct ':	L' (r	norr	nall	y u	sed	for	wi	red	-an	t					
													nectio		•																		
			H0D1	7								_	n drive			SCC	onn	ect	1'	(noı	ma	lly t	ısec	d to	or w	/ire	d-aı	nd					
_	DIA:	CENCE											nectic																				
E	KW	SENSE	Disabled	^									sensir	ıg r	nec	nar	nısr	n															
			Disabled	0									bled	L:																			
			High	2									se for	•			I																
			Low	3							Se	ens	se for	IOV	w le	vel																	

20.3.25 PIN_CNF[15]

Address offset: 0x73C Configuration of GPIO pins

numb	er		31	. 30	29	28	27	26 2	25	24	23 2	22	21	20	19 :	18	17	16	15 1	.4 :	13 :	12 :	11 1	0 9	8	7	6	5	4	3	2	1 (
																	Ε	Ε					ı) D	D					С	С	В
et 0x(00000002		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	1 (
RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
RW	DIR										Pin	dir	ecti	on.	Sar	ne	phy	/sic	al re	gis	ter	as	OIR	regi	ster							
		Input	0								Con	fig	ure	pin	as	an	inp	ut p	oin													
		Output	1								Con	fig	ure	pin	as	an	out	put	pin													
RW	INPUT										Con	ine	ct c	r di	isco	nne	ect	inp	ut b	uff	er											
		Connect	0								Con	ine	ct i	npu	t bu	ıffe	r															
		Disconnect	1								Disc	con	nec	t in	put	bu	ffe	-														
RW	PULL										Pull	со	nfig	gura	atio	า																
		Disabled	0								Nο	pul	II																			
		Pulldown	1								Pull	do	wn	on	pin																	
		Pullup	3								Pull	up	on	pir	1																	
RW	DRIVE										Driv	e d	conf	igu	rati	on																
		S0S1	0								Star	nda	ard	0',	star	nda	rd '	1'														
		H0S1	1								High	h d	rive	'0'	, sta	ınd	ard	'1'														
		S0H1	2								Star	nda	ard	0',	high	n dr	ive	'1'														
		H0H1	3								High	h d	rive	'0'	, hig	gh '	driv	e ':	L''													
		DOS1	4								Disc	con	nec	t '0)' sta	and	lard	'1'	(no	rm	ally	use	d f	or w	irec	l-or						
											con	no	ctio	ns)																		
	RW RW	RW Field RW DIR RW INPUT RW PULL RW DRIVE	RW Field Value Id RW DIR Input Output RW INPUT Connect Disconnect RW PULL Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 HOH1	RW Field Value Id Val	RW Field Value Id Val	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3 THE SOH1 2 HOH1 3 TO T	RW Field Value Id Input O Output I I ID	RW Field Value Id Val	RW Field Value Id Value Id Value Id Value Id RW DIR RW INPUT Connect Disconnect 1 Pulldown 1 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 5 SOH1 1 SOH1 1 HOH1 3 SUBSTITE STATE	RW Field Value Id Value RW DIR Input 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	RW Field Value Id Value	RW Field Value Id Value	RW Field Value Id Val	RW Field Value Id Value Valu	No No No No No No No No	RW Field Value Id Value	RW Field Value Id Value	RW Field Value Market Pin direction. Same physical Pin direction. Same physical	RW Field Value Id Value Pin direction. Same physical reference Pin d	RW Field Value Id Value Pin direction. Same physical register	RW Field Value Id Value Id Value Id Description Pin direction. Same physical register Configure pin as an input pin Configure pin as an output pin Connect or disconnect input buffer Disconnect Dis	RW Field Value Id Val	RW Field Value Id Value Pin direction. Same physical register as DIR	RW Field Value Id Value Pin direction. Same physical register as DIR register	RW Field Value Id Value	RW Field Value Id Value Id Pin direction. Same physical register as DIR regist	RW Field Value Id Value Id Pindirection. Same physical register as DIR registe	RW Field Value Id Value	RW Field Value Id Value Valu	NPUT	RW Field Value Id Value Valu



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.26 PIN_CNF[16]

Address offset: 0x740

Configuration of GPIO pins

Bit n	umbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Rese	t 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.27 PIN_CNF[17]

Address offset: 0x744



Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Res	et 0x0	0000002		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.28 PIN_CNF[18]

Address offset: 0x748
Configuration of GPIO pins

Bit r	iumbe	er		31	30	29	28 2	27 2	26 2	5 24	4 23	22	21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																	Ε	Ε					D	D	D				(СС	: В	Α
Rese	et OxC	0000002		0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 0) 1	0
Id	RW	Field	Value Id	Va	llue						De	scr	ipti	on																		
Α	RW	DIR									Pin	n di	rect	tion	. Sa	ne	ph	ysic	al r	egis	ter	as [IR r	egis	ter							
			Input	0							Co	nfig	gure	e pir	n as	an	inp	ut	oin													
			Output	1							Co	nfig	gure	e pir	n as	an	ou	tpu	t pir	ı												
В	RW	INPUT									Co	nne	ect (or d	lisco	nn	ect	inp	ut k	ouff	er											
			Connect	0							Co	nne	ect i	inpu	ut bu	ıffe	er															
			Disconnect	1							Dis	co	nne	ct ii	nput	: bu	ıffe	r														
С	RW	PULL									Pul	II c	onfi	gur	atio	n																
			Disabled	0							No	pι	ıll																			
			Pulldown	1							Pul	ll d	owr	n or	n pin																	
			Pullup	3							Pul	ll u	no q	n pi	n																	
D	RW	DRIVE									Dri	ive	con	figu	ırati	on																
			S0S1	0							Sta	and	lard	'0',	stai	nda	ırd	'1'														
			H0S1	1							Hig	gh d	driv	e '0	', sta	and	larc	i '1'														
			SOH1	2							Sta	and	lard	'0',	hig	n dı	rive	'1'														
			H0H1	3							Hig	gh d	driv	e '0	', hi	gh '	dri	ve '	1''													
			DOS1	4							Dis	co	nne	ct '(O' st	anc	dar	d '1'	(no	orm	ally	use	d fo	r wi	red-	or						
											100	nne	ectio	ons))																	



Bit number	31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
S0D1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.29 PIN_CNF[19]

Address offset: 0x74C

Configuration of GPIO pins

	<u> </u>		
Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E E D D D C C B A
Reset 0x00000002		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW DIR			Pin direction. Same physical register as DIR register
	Input	0	Configure pin as an input pin
	Output	1	Configure pin as an output pin
B RW INPUT			Connect or disconnect input buffer
	Connect	0	Connect input buffer
	Disconnect	1	Disconnect input buffer
C RW PULL			Pull configuration
	Disabled	0	No pull
	Pulldown	1	Pull down on pin
	Pullup	3	Pull up on pin
D RW DRIVE			Drive configuration
	S0S1	0	Standard '0', standard '1'
	H0S1	1	High drive '0', standard '1'
	SOH1	2	Standard '0', high drive '1'
	H0H1	3	High drive '0', high 'drive '1"
	DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
			connections)
	D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or connections)
	SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
	11004	_	connections)
	H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
F DW CENCE			connections)
E RW SENSE	Disabled	0	Pin sensing mechanism
	Disabled	0	Disabled
	High	2	Sense for high level
	Low	3	Sense for low level

20.3.30 PIN_CNF[20]

Address offset: 0x750 Configuration of GPIO pins



Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Res	et 0x0	0000002		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.31 PIN_CNF[21]

Address offset: 0x754 Configuration of GPIO pins

ССВА
0 0 1 0



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.32 PIN_CNF[22]

Address offset: 0x758

Configuration of GPIO pins

-	9	diation of of 10 p			
Bit	numb	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E D D D C C B A
Res	et 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			SOS1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
Ε	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.33 PIN_CNF[23]

Address offset: 0x75C

Configuration of GPIO pins



Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E D D D C C B A
Res	et 0x0	0000002		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			SOS1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
_	DIA	CENCE			connections)
E	KW	SENSE	6: 11 1		Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.34 PIN_CNF[24]

Address offset: 0x760 Configuration of GPIO pins

Bit r	iumbe	er		31	30	29	28 2	27 2	26 2	5 24	4 23	22	21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																	Ε	Ε					D	D	D				(СС	: В	Α
Rese	et OxC	0000002		0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 0) 1	0
Id	RW	Field	Value Id	Va	llue						De	scr	ipti	on																		
Α	RW	DIR									Pin	n di	rect	tion	. Sa	ne	ph	ysic	al r	egis	ter	as [IR r	egis	ter							
			Input	0							Co	nfig	gure	e pir	n as	an	inp	ut	oin													
			Output	1							Co	nfig	gure	e pir	n as	an	ou	tpu	t pir	ı												
В	RW	INPUT									Co	nne	ect (or d	lisco	nn	ect	inp	ut k	ouff	er											
			Connect	0							Co	nne	ect i	inpu	ut bu	ıffe	er															
			Disconnect	1							Dis	co	nne	ct ii	nput	: bu	ıffe	r														
С	RW	PULL									Pul	II c	onfi	gur	atio	n																
			Disabled	0							No	pι	ıll																			
			Pulldown	1							Pul	ll d	owr	n or	n pin																	
			Pullup	3							Pul	ll u	no q	n pi	n																	
D	RW	DRIVE									Dri	ive	con	figu	ırati	on																
			S0S1	0							Sta	and	lard	'0',	stai	nda	ırd	'1'														
			H0S1	1							Hig	gh d	driv	e '0	', sta	and	larc	i '1'														
			SOH1	2							Sta	and	lard	'0',	hig	n dı	rive	'1'														
			H0H1	3							Hig	gh d	driv	e '0	', hi	gh '	dri	ve '	1''													
			DOS1	4							Dis	co	nne	ct '(O' st	anc	dar	d '1'	(no	orm	ally	use	d fo	r wi	red-	or						
											100	nne	ectio	ons))																	



Bit number		31 30 29 28	27 26 25	5 24	23 22 2	21 20	19 1	8 17	16	15 1	.4 13	12 1	1 10	9	8	7	6 5	5 4	3	2 1	. 0
Id								Е	Ε				D	D	D				С	СВ	Α
Reset 0x00000002		0 0 0 0	0 0 0	0	0 0	0 0	0 (0	0	0 (0 0	0	0 0	0	0	0	0 0	0	0	0 1	. 0
ld RW Field	Value Id	Value			Descrip	otion															
	D0H1	5			Discon	nect '	0', hi	gh dr	ive '	1' (n	orma	ally u	sed f	or w	/ired	-or					
					connec	tions)														
	SOD1	6			Standa	rd '0'.	. disc	onne	ct '1	.' (nc	rmal	ly us	ed fo	r wi	red-	and					
					connec	tions)														
	H0D1	7			High dr	rive '0)', dis	conn	ect '	1' (n	orma	ally u	sed f	or w	vired	l-an	d				
					connec	tions)														
E RW SENSE					Pin sen	nsing r	mech	anisr	n												
	Disabled	0			Disable	ed															
	High	2			Sense f	for hig	gh lev	el													
	Low	3			Sense f	for lov	w leve	el													

20.3.35 PIN_CNF[25]

Address offset: 0x764

Configuration of GPIO pins

	<u> </u>		
Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E E D D D C C B A
Reset 0x00000002		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW DIR			Pin direction. Same physical register as DIR register
	Input	0	Configure pin as an input pin
	Output	1	Configure pin as an output pin
B RW INPUT			Connect or disconnect input buffer
	Connect	0	Connect input buffer
	Disconnect	1	Disconnect input buffer
C RW PULL			Pull configuration
	Disabled	0	No pull
	Pulldown	1	Pull down on pin
	Pullup	3	Pull up on pin
D RW DRIVE			Drive configuration
	S0S1	0	Standard '0', standard '1'
	H0S1	1	High drive '0', standard '1'
	SOH1	2	Standard '0', high drive '1'
	H0H1	3	High drive '0', high 'drive '1"
	DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
			connections)
	D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or connections)
	SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
	11004	_	connections)
	H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
F DW CENCE			connections)
E RW SENSE	Disabled	0	Pin sensing mechanism
	Disabled	0	Disabled
	High	2	Sense for high level
	Low	3	Sense for low level

20.3.36 PIN_CNF[26]

Address offset: 0x768

Configuration of GPIO pins



Bit r	numbe	er		31 3	0 29	28	27 2	6 25	5 24	23	22 2	21 20	0 19	18	17	16	15	14 1	.3 1	2 13	1 10	9	8	7	6	5 4	1 3	2	1	0
Id															Ε	Ε					D	D	D				С	С	В	Α
Res	et OxC	00000002		0 (0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0 0	0	1	0
Id	RW	Field	Value Id	Valu	e					De	escrip	tion	l																	
Α	RW	DIR								Pir	n dire	ctio	n. S	ame	e ph	iysic	al r	egist	er a	as D	IR re	egist	er							
			Input	0						Со	nfigu	ıre p	in a	s an	inp	out	pin													
			Output	1						Со	nfigu	ıre p	in a	s an	ou	tpu	t pi	n												
В	RW	INPUT								Со	nnec	t or	disc	onn	nect	inp	ut l	ouffe	er											
			Connect	0						Со	nnec	t inp	out b	ouff	er															
			Disconnect	1						Dis	sconr	nect	inpı	ut b	uffe	er														
С	RW	PULL								Pu	ıll cor	nfigu	rati	on																
			Disabled	0						No	pull																			
			Pulldown	1						Pu	ıll dov	wn o	n pi	n																
			Pullup	3						Pu	ıll up	on p	in																	
D	RW	DRIVE								Dri	ive co	onfig	gura	tion	1															
			S0S1	0						Sta	andaı	rd '0	', sta	anda	ard	'1'														
			H0S1	1						Hig	gh dr	ive '	0', s	tano	dard	d '1'														
			S0H1	2						Sta	andaı	rd '0	', hi	gh d	irive	e '1'														
			H0H1	3						Hig	gh dr	ive '	0', h	igh	'dri	ve '	1''													
			DOS1	4						Dis	sconr	nect	'0' s	tan	dar	d '1	' (n	orma	ally	used	d for	vir	ed-	or						
										COI	nnec	tions	s)																	
			D0H1	5						Dis	sconr	nect	'0',	high	n dri	ive '	'1' (norn	nall	y us	ed f	or w	/ire	d-or						
										COI	nnec	tions	s)																	
			SOD1	6						Sta	andaı	rd '0	'. di	scor	nne	ct '1	L' (n	orm	ally	use	d fo	r wi	red	and	i					
										COI	nnec	tions	s)																	
			H0D1	7						Hig	gh dr	ive '	0', d	isco	onne	ect '	'1' (norn	nall	y us	ed f	or w	/ire	d-an	ıd					
										COI	nnec	tions	s)																	
Ε	RW	SENSE									n sen	-	me	char	nisn	n														
			Disabled	0							sable																			
			High	2						Sei	nse f	or hi	igh I	eve	1															
			Low	3						Sei	nse f	or lo	w le	evel																

20.3.37 PIN_CNF[27]

Address offset: 0x76C Configuration of GPIO pins

Bit r	numbe	er		31	30	29 2	28 2	7 2	6 25	5 24	23	22	21	20	19 1	18 1	17 :	16 :	15 1	4 1	3 1	2 1:	l 10	9	8	7	6	5	4 3	2	1	0
Id																	E	Ε					D	D	D				C	С	В	Α
Rese	et Ox0	0000002		0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0	0	1	0
Id	RW	Field	Value Id	Va	lue						Des	scri	ptic	n																		
Α	RW	DIR									Pin	dir	ecti	on.	San	ne į	phy	sic	al re	gist	er a	as D	IR re	egis	ter							
			Input	0							Cor	nfig	ure	pin	as a	an i	inpı	ut p	in													
			Output	1							Cor	nfig	ure	pin	as a	an d	out	put	pin													
В	RW	INPUT									Cor	nne	ct o	r di	iscoı	nne	ect i	npi	ut b	uffe	r											
			Connect	0							Cor	nne	ct ii	npu	t bu	ffe	r															
			Disconnect	1							Disc	con	nec	t in	put	but	ffer	•														
С	RW	PULL									Pul	l co	nfig	gura	atior	1																
			Disabled	0							No	pu	II																			
			Pulldown	1							Pull	l do	own	on	pin																	
			Pullup	3							Pull	l up	o on	pir	1																	
D	RW	DRIVE									Driv	ve o	cont	figu	ratio	on																
			S0S1	0							Sta	nda	ard	'0',	stan	daı	rd '	1'														
			H0S1	1							Hig	h d	rive	'0'	, sta	nda	ard	'1'														
			S0H1	2							Sta	nda	ard	'0',	high	dr	ive	'1'														
			H0H1	3							Hig	h d	rive	'0'	, hig	h 'c	driv	e '1	."													
			DOS1	4							Disc	con	nec	t '0)' sta	nd	ard	'1'	(no	rma	lly	use	d for	wi	red-	or						
											con	ne	ctio	ns)																		



Bit number		31 3	30 29	28	8 27	26	25	24	23 2	2 21	20	19	18 :	17 1	16 1	L5 1	4 13	3 12	11	10	9	8	7 (5 5	5 4	3	2	1	0
Id														Е	E					D	D	D				С	С	В	Α
Reset 0x00000002		0 (0 0	0	0	0	0	0	0 0	0 0	0	0	0	0	0 (0 (0 0	0	0	0	0	0 () (0 (0	0	0	1	0
ld RW Field	Value Id	Valu	ıe						Desc	ripti	on																		
	D0H1	5							Disco	onne	ct '(0', h	igh	driv	⁄e '1	L' (n	orm	ally	use	d fo	r w	ired	or						
									conn	nectio	ons))																	
	SOD1	6						:	Stan	dard	'0'.	disc	oni	nect	t '1'	(nc	rma	lly u	sed	for	iiw	ed-	nd						
									conn	nectio	ons))																	
	H0D1	7							High	driv	e '0	', dis	cor	nne	ct '1	L' (n	orm	ally	use	d fo	r w	ired	an	d					
									conn	nectio	ons))																	
E RW SENSE									Pin s	ensii	ng n	necł	nani	sm															
	Disabled	0							Disal	bled																			
	High	2						:	Sens	e for	hig	gh le	vel																
	Low	3						:	Sens	e for	lov	v lev	el																

20.3.38 PIN_CNF[28]

Address offset: 0x770

Configuration of GPIO pins

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		E E DDD CCB
Reset 0x00000002		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW DIR		Pin direction. Same physical register as DIR register
	Input	0 Configure pin as an input pin
	Output	1 Configure pin as an output pin
B RW INPUT		Connect or disconnect input buffer
	Connect	0 Connect input buffer
	Disconnect	1 Disconnect input buffer
C RW PULL		Pull configuration
	Disabled	0 No pull
	Pulldown	1 Pull down on pin
	Pullup	3 Pull up on pin
D RW DRIVE		Drive configuration
	S0S1	0 Standard '0', standard '1'
	H0S1	1 High drive '0', standard '1'
	S0H1	2 Standard '0', high drive '1'
	H0H1	3 High drive '0', high 'drive '1"
	DOS1	4 Disconnect '0' standard '1' (normally used for wired-or
		connections)
	D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
		connections)
	SOD1	6 Standard '0'. disconnect '1' (normally used for wired-and
		connections)
	H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
	Disabled	0 Disabled
	High	2 Sense for high level
	Low	3 Sense for low level

20.3.39 PIN_CNF[29]

Address offset: 0x774

Configuration of GPIO pins



Bit r	numbe	er		31	30	29 :	28 2	27 2	26 2	5 24	1 23	3 2	22 21	1 20	0 19	9 18	3 17	7 16	15	14	13	12	11 1	0 9	8 (7	6	5	4	3	2 1	L 0
Id																	Ε	Ε					[) [) D					С	C E	3 A
Res	et OxC	0000002		0	0	0	0 (0	0 0	0	0)	0 0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 1	١ ٥
Id	RW	Field	Value Id	Va	lue						D	es	cript	ion																		
Α	RW	DIR									Pi	in	direc	tio	n. S	am	e pl	hysi	cal	reg	ister	as	DIR	regi	ste							
			Input	0							Co	on	nfigur	e p	in a	as aı	n in	put	pir	1												
			Output	1							Co	on	nfigur	e p	in a	as aı	า ดเ	utpu	ut p	in												
В	RW	INPUT									Co	on	nnect	or	dis	con	nec	t in	put	but	fer											
			Connect	0							Co	on	nect	inp	ut	buf	fer															
			Disconnect	1							Di	isc	conne	ect i	inp	ut b	uff	er														
С	RW	PULL									Pι	ull	l conf	figu	rati	ion																
			Disabled	0							N	lo p	pull																			
			Pulldown	1							Pι	ull	l dow	n o	n p	in																
			Pullup	3							Pι	ull	l up o	n p	in																	
D	RW	DRIVE									D	riv	ve co	nfig	ura	atio	n															
			S0S1	0							St	tar	ndard	'0' b	', st	and	lard	1'1'														
			H0S1	1							Hi	igł	h driv	/e '(0', s	stan	dar	'd '1	.'													
			SOH1	2							St	tar	ndard	'0' b	', hi	igh (driv	⁄e '1	.'													
			H0H1	3							Hi	igł	h driv	/e '(0', ł	nigh	'dr	ive	'1"													
			D0S1	4							Di	isc	conne	ect	'0'	star	ıdaı	rd ':	L' (r	orr	nally	/ us	ed fo	or w	/ire	l-or						
											cc	on	necti	ions	5)																	
			D0H1	5									conne inecti			hig	h dı	rive	'1'	(no	rma	lly ι	ısed	for	wir	ed-c	or					
			SOD1	6									ndaro			isco	nne	ect '	1' (nor	mall	y us	sed f	or v	vire	d-ar	nd					
			H0D1	7								_	h driv			disc	onn	ect	'1'	(no	rma	lly ι	ısed	for	wir	ed-a	ınd					
E	RW	SENSE											sensi			cha	nisı	m														
			Disabled	0									abled	_																		
			High	2									se fo		gh	leve	el															
			Low	3							Se	en:	se fo	r lo	w I	eve	ı															

20.3.40 PIN_CNF[30]

Address offset: 0x778 Configuration of GPIO pins

numb	er		31	. 30	29	28	27	26 2	25 :	24	23 2	22	21 :	20	19 1	18 :	17 :	16	15 1	.4 :	13 :	12 :	l1 1	0 9	8	7	6	5	4	3	2	1 (
																	Е	E					1) [D					С	C I	ВА
et 0x(00000002		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1 (
RW	Field	Value Id	Va	lue							Des	cri	ptio	n																		
RW	DIR										Pin	dir	ecti	on.	Sar	ne	phy	sic	al re	gis	ter	as	DIR	regi	ster							
		Input	0								Con	fig	ure	pin	as	an i	inpı	ut p	in													
		Output	1								Con	fig	ure	pin	as	an (out	put	pin													
RW	INPUT										Con	ne	ct o	r di	sco	nne	ect i	np	ut b	uff	er											
		Connect	0								Con	ne	ct ir	npu	t bu	ffe	r															
		Disconnect	1								Disc	on	nec	t in	put	bu	ffer															
RW	PULL										Pull	со	nfig	gura	tioi	1																
		Disabled	0								No p	pul	I																			
		Pulldown	1								Pull	do	wn	on	pin																	
		Pullup	3								Pull	up	on	pir	1																	
RW	DRIVE										Driv	e c	onf	igu	rati	on																
		S0S1	0							:	Star	nda	rd '	0',	star	ıda	rd '	1'														
		H0S1	1								High	n d	rive	'0'	, sta	nd	ard	'1'														
		S0H1	2							:	Star	nda	rd '	0',	high	dr	ive	'1'														
		H0H1	3								High	n di	rive	'0'	, hig	h 'd	driv	e '1	L''													
		DOS1	4								Disc	on	nec	t '0	' sta	nd	ard	'1'	(no	rm	ally	use	ed f	or w	ired	l-or						
											con	nor	rtio	ns)																		
	RW RW	RW Field RW DIR RW INPUT RW PULL RW DRIVE	RW Field Value Id RW DIR Input Output RW INPUT Connect Disconnect RW PULL Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 HOH1	RW Field Value Id Val	RW Field Value Id Val	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3 THE SOH1 2 HOH1 3 TO T	RW Field Value Id Id Id Value Id Id Id Value Id	RW Field Value Id Val	RW Field Value Id Value Id Value Id Value Id RW DIR RW INPUT Connect Disconnect 1 RW PULL Disabled O Pulldown 1 Pullup 3 RW DRIVE SOS1	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3 DOS1 4	RW Field Value Id Value RW DIR Input Output 1 Connect Disconnect Disconnect Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 SOH1 SOH1 SOH1 SOH1 SOS1 HOHI DISCON SON OUTPUT	RW Field Value Id Value	RW Field Value Id Val	RW Field Value Id Value	RW Field Value Martin Pin direction. San Pin direction. San	RW Field Value Id Value Valu	RW Field Value Id Value	RW Field Value Market Pin direction. Same physical	RW Field Value Id Value Pin direction. Same physical reference Pin d	RW Field Value Id Value Pin direction. Same physical register	RW Field Value Id Value Id Value Id Description Pin direction. Same physical register Configure pin as an input pin Configure pin as an output pin Connect or disconnect input buffer Disconnect Dis	RW Field Value Id Value Valu	RW Field Value Id Value Pin direction. Same physical register as DIR	RW Field	RW Field Value Id Value	RW Field Value Id Value Id Pin direction. Same physical register as DIR regist	RW Field Value Id Pind irection. Same physical register as DIR register NPUT	RW Field Value Id Value	RW Field Value Id Value Valu	NPUT	RW Field Value Id Value Valu



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.41 PIN_CNF[31]

Address offset: 0x77C

Configuration of GPIO pins

t number			31 30 29	9 28 27	7 26 25	24 23	3 22	21 2	20 1	9 18	17	16	15 14	4 13	3 12	11 10	9	8	7	6 !	5 4	3	2	1
											Ε	Ε				D	D	D				С	С	В
eset 0x0000	00002		0 0 0	0 0	0 0	0 0	0	0	0	0 0	0	0	0 0	0	0	0 0	0	0	0	0 (0 0	0	0	1
RW Fie	eld	Value Id	Value			D	escr	iptio	n															
RW DI	R					Pi	in di	recti	on.	Same	e ph	ysic	al re	giste	er as	DIR r	egis	ter						
		Input	0			C	onfi	gure	pin	as ar	n inp	ut p	oin											
		Output	1			C	onfi	gure	pin	as ar	out	put	pin											
RW IN	PUT					C	onne	ect o	r dis	con	nect	inp	ut bu	ıffeı	r									
		Connect	0			C	onne	ect in	put	buff	er													
		Disconnect	1			D	isco	nnec	t in	out b	uffe	r												
RW PL	JLL					Pi	ull c	onfig	ura	tion														
		Disabled	0			N	lo pu	III																
		Pulldown	1			Pi	ull d	own	on	pin														
		Pullup	3			Pi	ull u	p on	pin															
RW DF	RIVE					D	rive	conf	igur	atior	1													
		S0S1	0			St	tand	ard '	0', s	tand	ard	'1'												
		H0S1	1			Н	igh o	drive	'0',	stan	dard	l '1'												
		S0H1	2			St	tand	ard '	0', h	igh o	drive	'1'												
		H0H1	3			Н	igh (drive	'0',	high	'driv	/e '1	ι"											
		D0S1	4			D	isco	nnec	t '0'	stan	dard	1 '1'	(nor	mal	lly us	ed fo	r wi	red-	or					
						co	onne	ection	ns)															
		D0H1	5					nnec ection		, higl	n dri	ve '	1' (no	orm	ally u	ised 1	or v	wire	d-or					
		SOD1	6					ard '		lisco	nnec	t '1	' (no	rma	ılly us	ed fo	or w	ired	-and	t				
		H0D1	7				-	drive		disco	onne	ct '	1' (no	orm	ally ι	ised t	or v	wire	d-ar	nd				
RW SE	NSF							nsin	•	ocha	nicm													
IVV JL		Disabled	0				isab		ь ''''	cciia	111311	•												
		High	2					for l	high	leve	d													
		Low	3						-	level														

20.4 Electrical specification

20.4.1 GPIO Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
V _{IH}	Input high voltage	0.7 x VDI	D	VDD	V



Symbol	Description	Min.	Тур.	Max.	Units
V _{IL}	Input low voltage	VSS		0.3 x VDI) V
$V_{OH,SD}$	Output high voltage, standard drive, 0.5 mA, VDD ≥1.7	VDD-0.	4	VDD	V
V _{OH,HDH}	Output high voltage, high drive, 5 mA, VDD >= 2.7 V	VDD-0.	4	VDD	V
V _{OH,HDL}	Output high voltage, high drive, 3 mA, VDD >= 1.7 V	VDD-0.	4	VDD	V
V _{OL,SD}	Output low voltage, standard drive, 0.5 mA, VDD ≥1.7	VSS		VSS+0.4	V
V _{OL,HDH}	Output low voltage, high drive, 5 mA, VDD >= 2.7 V	VSS		VSS+0.4	V
V _{OL,HDL}	Output low voltage, high drive, 3 mA, VDD >= 1.7 V	VSS		VSS+0.4	V
I _{OL,SD}	Current at VSS+0.4 V, output set low, standard drive, VDD ≥1.7	1	2	4	mA
I _{OL,HDH}	Current at VSS+0.4 V, output set low, high drive, VDD >= 2.7 V	6	10	15	mA
I _{OL,HDL}	Current at VSS+0.4 V, output set low, high drive, VDD >= 1.7 V	3			mA
I _{OH,SD}	Current at VDD-0.4 V, output set high, standard drive, VDD ≥1.7	1	2	4	mA
I _{OH,HDH}	Current at VDD-0.4 V, output set high, high drive, VDD >= 2.7 V	6	9	14	mA
I _{OH,HDL}	Current at VDD-0.4 V, output set high, high drive, VDD >= 1.7 V	3			mA
t _{RF,15pF}	Rise/fall time, low drive mode, 10-90%, 15 pF load ¹		9		ns
t _{RF,25pF}	Rise/fall time, low drive mode, 10-90%, 25 pF load ¹		13		ns
t _{RF,50pF}	Rise/fall time, low drive mode, 10-90%, 50 pF load ¹		25		ns
t _{HRF,15pF}	Rise/Fall time, high drive mode, 10-90%, 15 pF load ¹		4		ns
t _{HRF,25pF}	Rise/Fall time, high drive mode, 10-90%, 25 pF load ¹		5		ns
t _{HRF,50pF}	Rise/Fall time, high drive mode, 10-90%, 50 pF load ¹		8		ns
R _{PU}	Pull-up resistance	11	13	16	kΩ
R _{PD}	Pull-down resistance	11	13	16	kΩ
C _{PAD}	Pad capacitance		3		pF
C _{PAD_NFC}	Pad capacitance on NFC pads		4		pF
I _{NFC_LEAK}	Leakage current between NFC pads when driven to different		2	10	μΑ
	states				

The current drawn from the battery when GPIO is active as an output is calculated as follows:

 I_{GPIO} = V_{DD} C_{load} f

 C_{load} being the load capacitance and "f" is the switching frequency.

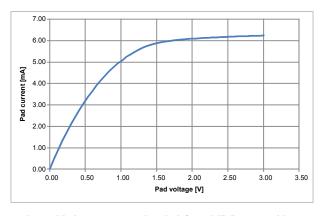


Figure 23: GPIO drive strength vs Voltage, standard drive, VDD = 3.0 V

¹ Rise and fall times based on simulations



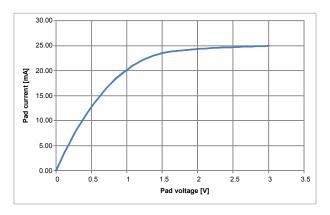


Figure 24: GPIO drive strength vs Voltage, high drive, VDD = 3.0 V

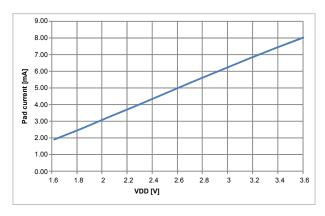


Figure 25: Max sink current vs Voltage, standard drive

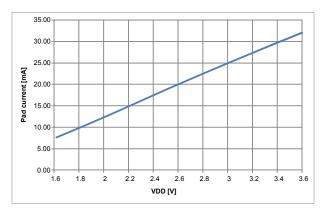


Figure 26: Max sink current vs Voltage, high drive

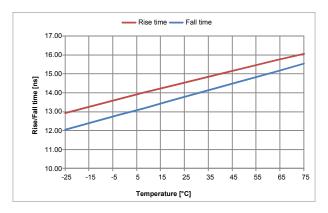


Figure 27: Rise and fall time vs Temperature, 10%-90%, 25pF load capacitance, VDD = 3.0 V



21 GPIOTE — GPIO tasks and events

The GPIO tasks and events (GPIOTE) module provides functionality for accessing GPIO pins using tasks and events. Each GPIOTE channel can be assigned to one pin.

A GPIOTE block enables GPIOs to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system. Low power detection of pin state changes is possible when in System ON or System OFF.

Table 30: GPIOTE properties

Instance	Number of GPIOTE channels
GPIOTE	8

Up to three tasks can be used in each GPIOTE channel for performing write operations to a pin. Two tasks are fixed (SET and CLR), and one (OUT) is configurable to perform following operations:

- Set
- Clear
- Toggle

An event can be generated in each GPIOTE channel from one of the following input conditions:

- · Rising edge
- Falling edge
- · Any change

21.1 Pin events and tasks

The GPIOTE module has a number of tasks and events that can be configured to operate on individual GPIO pins.

The tasks (SET[n], CLR[n] and OUT[n]) can be used for writing to individual pins, and the events (IN[n]) can be generated from changes occurring at the inputs of individual pins.

The SET task will set the pin selected in CONFIG[n].PSEL to high.

The CLR task will set the pin low.

The effect of the OUT task on the pin is configurable in CONFIG[n].POLARITY, and can either set the pin high, set it low, or toggle it.

The tasks and events are configured using the CONFIG[n] registers. Every set of SET, CLR and OUT[n] tasks and IN[n] events has one CONFIG[n] register associated with it.

As long as a SET[n], CLR[n] and OUT[n] task or an IN[n] event is configured to control a pin **n**, the pin's output value will only be updated by the GPIOTE module. The pin's output value as specified in the GPIO will therefore be ignored as long as the pin is controlled by GPIOTE. Attempting to write a pin as a normal GPIO pin will have no effect. When the GPIOTE is disconnected from a pin, see MODE field in CONFIG[n] register, the associated pin will get the output and configuration values specified in the GPIO module.

When conflicting tasks are triggered simultaneously (i.e. during the same clock cycle) in one channel, the precedence of the tasks will be as described in *Table 31: Task priorities* on page 157.

Table 31: Task priorities

Priority	Task
1	OUT
2	CLR
3	SET



When setting the CONFIG[n] registers, MODE=Disabled does not have the same effect as MODE=Task and POLARITY=None. In the latter case, a CLR or SET task occurring at the exact same time as OUT will end up with no change on the pin, according to the priorities described in the table above.

When a GPIOTE channel is configured to operate on a pin as a task, the initial value of that pin is configured in the OUTINIT field of CONFIG[n].

21.2 Port event

PORT is an event that can be generated from multiple input pins using the GPIO DETECT signal.

The event will be generated on the rising edge of the DETECT signal. See *GPIO* — *General purpose input/output* on page 111 for more information about the DETECT signal.

Putting the system into System ON IDLE while DETECT is high will not cause DETECT to wake the system up again. Make sure to clear all DETECT sources before entering sleep. If the LATCH register is used as a source, if any bit in LATCH is still high after clearing all or part of the register (for instance due to one of the PINx.DETECT signal still high), a new rising edge will be generated on DETECT, see *Pin configuration* on page 111.

Trying to put the system to System OFF while DETECT is high will cause a wakeup from System OFF reset.

This feature is always enabled although the peripheral itself appears to be IDLE, that is, no clocks or other power intensive infrastructure have to be requested to keep this feature enabled. This feature can therefore be used to wake up the CPU from a WFI or WFE type sleep in System ON with all peripherals and the CPU idle, that is, lowest power consumption in System ON mode.

In order to prevent spurious interrupts from the PORT event while configuring the sources, the user shall first disable interrupts on the PORT event (through INTENCLR.PORT), then configure the sources (PIN_CNF[n].SENSE), clear any potential event that could have occurred during configuration (write '1' to EVENTS_PORT), and finally enable interrupts (through INTENSET.PORT).

21.3 Tasks and events pin configuration

Each GPIOTE channel is associated with one physical GPIO pin through the CONFIG.PSEL field.

When Event mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an input, overriding the DIR setting in GPIO. Similarly, when Task mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an output overriding the DIR setting and OUT value in GPIO. When Disabled is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will use its configuration from the PIN[n].CNF registers in GPIO.

Only one GPIOTE channel can be assigned to one physical pin. Failing to do so may result in unpredictable behavior.

21.4 Registers

Table 32: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40006000	GPIOTE	GPIOTE	GPIO Tasks and Events		

Table 33: Register Overview

Register	Offset	Description
TASKS_OUT[0]	0x000	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is configured in
		CONFIG[0].POLARITY.
TASKS_OUT[1]	0x004	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is configured in
		CONFIG[1].POLARITY.



TASKS_OUT[3] 0x008 Task for writing to pin specified in CONFIG[2].PSEL Action on pin is configured in CONFIG[3].POLARITY. TASKS_OUT[4] 0x000 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is configured in CONFIG[3].POLARITY. TASKS_OUT[4] 0x001 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is configured in CONFIG[7].PSEL Action on pin is to set it high. TASKS_OUT[7] 0x012 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[7] 0x038 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[7] 0x038 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_CRITIO 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_CRITIO 0x040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_CRITIO 0x040 Task for writing to pin spec	Register	Offset	Description
TASKS_OUT[4] 0x00C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is configured in CONFIG[3].PSEL Action on pin is configured in CONFIG[4].PSEL Action on pin is configured in CONFIG[4].PSEL Action on pin is configured in CONFIG[4].PSEL Action on pin is configured in CONFIG[6].PSEL Action on pin is to set it high. TASKS_DOT[7] 0x01C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[1] 0x030 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[3] 0x031 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] 0x032 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] 0x043 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] 0x044 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] 0x044 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] 0x044 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_CRE[3] 0x048 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_CRE[4] 0x048 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CRE[4] 0x048 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CRE[5] 0x044 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it how. TASKS_CRE[6] 0x047 Task for writing to pin specified in CONFIG[6].PSEL Action on pin			•
TASKS_OUT[3] bibOC Task for writing to pin specified in CONFIG[3].PSEL Action on pin is configured in CONFIG[3].POLARITY. TASKS_OUT[5] bibO14 Task for writing to pin specified in CONFIG[4].PSEL Action on pin is configured in CONFIG[5].POLARITY. TASKS_OUT[5] bibO14 Task for writing to pin specified in CONFIG[5].PSEL Action on pin is configured in CONFIG[6].PSEL Action on pin is configured in CONFIG[7].PSEL Action on pin is to set it high. TASKS_OUT[7] bibO12 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[1] bibO34 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[1] bibO34 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[8] bibO35 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[8] bibO36 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[8] bibO38 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[8] bibO38 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[8] bibO38 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CER[8] bibO39 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CER[8] bibO39 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CER[8] bibO39 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CER[8] bibO39 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it how. TASKS_CER[8] bibO39 Task for writing to pin specified	1/13/13_001[2]	0,000	
CONFIG[3] POLARITY. TASKS_OUT[6] 0x014 Task for writing to pin specified in CONFIG[4] PSEL Action on pin is configured in CONFIG[6] POLARITY. TASKS_OUT[6] 0x014 Task for writing to pin specified in CONFIG[6] PSEL Action on pin is configured in CONFIG[7] PSEL Action on pin is to set it high. TASKS_SET[0] 0x030 Task for writing to pin specified in CONFIG[6] PSEL Action on pin is to set it high. TASKS_SET[1] 0x038 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it high. TASKS_SET[1] 0x030 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it high. TASKS_SET[1] 0x040 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it high. TASKS_SET[1] 0x040 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it high. TASKS_SET[1] 0x040 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it high. TASKS_SET[1] 0x040 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it high. TASKS_SET[1] 0x040 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it high. TASKS_CLE(1) 0x060 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it high. TASKS_CLE(1) 0x060 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it low. TASKS_CLE(1) 0x060 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it low. TASKS_CLE(1) 0x060 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it low. TASKS_CLE(1) 0x060 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it low. TASKS_CLE(1) 0x060 Tas	TACKE OTILES	0,000	• •
TASKS_OUT[4] Do010 Task for writing to pin specified in CONFIG[4].PSEL Action on pin is configured in CONFIG[4].PSEL Action on pin is configured in CONFIG[5].PSEL Action on pin is configured in CONFIG[5].PSEL Action on pin is configured in CONFIG[6].POLARITY. TASKS_OUT[6] Do10 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is configured in CONFIG[6].POLARITY. TASKS_OUT[7] Do10 Do10 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is configured in CONFIG[7].PSEL Action on pin is configured in CONFIG[7].PSEL Action on pin is configured in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[1] Do30 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[2] Do30 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[3] Do30 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[4] Do40 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[5] Do40 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[6] Do40 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[7] Do40 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[7] Do40 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CLIR[1] Do40 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CLIR[1] Do40 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLIR[1] Do40 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLIR[1] Do40 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLIR[1] Do40 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLIR[1] Do40 Task for	1A3K3_001[5]	OXOOC	
CONFIG[4] POLARITY. TASKS_OUT[5] Ob14 Task for writing to pin specified in CONFIG[5].PSEL Action on pin is configured in CONFIG[5].PSEL Action on pin is configured in CONFIG[6].PSEL Action on pin is configured in CONFIG[7].PSEL Action on pin is configured in CONFIG[7].PSEL Action on pin is configured in CONFIG[7].PSEL Action on pin is to set it high. TASKS_DET[0] Ox930 Task for writing to pin specified in CONFIG[0].PSEL Action on pin is to set it high. TASKS_SET[1] Ox934 Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it high. TASKS_SET[2] Ox938 Task for writing to pin specified in CONFIG[2].PSEL Action on pin is to set it high. TASKS_SET[3] Ox930 Task for writing to pin specified in CONFIG[2].PSEL Action on pin is to set it high. TASKS_SET[3] Ox940 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] Ox944 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] Ox944 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] Ox940 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_CRID] Ox960 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CRID] Ox960 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CRID[3] Ox960 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CRID[3] Ox960 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CRID[3] Ox960 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CRID[3] Ox960 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CRID[3] Ox960 Task for writing to pin specified in CONFIG[3].PSEL Action on pin i	TACKS OUT[4]	0::010	
TASKS_OUT[6] Ox014 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is configured in CONFIG[6].POLARITY. TASKS_OUT[7] Ox01C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is configured in CONFIG[6].POLARITY. TASKS_OUT[7] Ox01C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is configured in CONFIG[7].PDELARITY. TASKS_SET[0] Ox030 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[1] Ox034 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[3] Ox03C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[3] Ox03C Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[3] Ox04C Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[6] Ox04C Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[7] Ox04C Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[7] Ox04C Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_CLE[1] Ox06D Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_CLE[1] Ox06D Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_CLE[1] Ox06D Task for writing to pin specified in CONFIG[9].PSEL Action on pin is to set it how. TASKS_CLE[1] Ox06B Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it how. TASKS_CLE[2] Ox06B Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it how. TASKS_CLE[3] Ox06C Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it how. TASKS_CLE[3] Ox07C Task for writing to pin specified in CONFIG[2].PSEL Action on pin is to set it how. TASKS_CLE[3] Ox07C Task for writing to pin specified in CONFIG[3].PS	TASKS_UUT[4]	0x010	
CONFIGIS]. POLARITY. TASKS_OUT[6] Ox018 Task for writing to pin specified in CONFIGI6]. PSEL. Action on pin is configured in CONFIGI6]. POLARITY. TASKS_OUT[7] Ox01C Task for writing to pin specified in CONFIGI7]. PSEL. Action on pin is configured in CONFIGI7]. POLARITY. TASKS_SET[0] Ox030 Task for writing to pin specified in CONFIGI7]. PSEL. Action on pin is to set it high. TASKS_SET[1] Ox034 Task for writing to pin specified in CONFIGI7]. PSEL. Action on pin is to set it high. TASKS_SET[2] Ox038 Task for writing to pin specified in CONFIGI7]. PSEL. Action on pin is to set it high. TASKS_SET[3] Ox020 Task for writing to pin specified in CONFIGI8]. PSEL. Action on pin is to set it high. TASKS_SET[3] Ox040 Task for writing to pin specified in CONFIGI8]. PSEL. Action on pin is to set it high. TASKS_SET[6] Ox044 Task for writing to pin specified in CONFIGI8]. PSEL. Action on pin is to set it high. TASKS_SET[7] Ox040 Task for writing to pin specified in CONFIGI8]. PSEL. Action on pin is to set it high. TASKS_SET[8] Ox040 Task for writing to pin specified in CONFIGI8]. PSEL. Action on pin is to set it high. TASKS_SET[8] Ox060 Task for writing to pin specified in CONFIGI7]. PSEL. Action on pin is to set it high. TASKS_CLE(1) Ox060 Task for writing to pin specified in CONFIGI7]. PSEL. Action on pin is to set it how. TASKS_CLE(1) Ox060 Task for writing to pin specified in CONFIGI8]. PSEL. Action on pin is to set it how. TASKS_CLE(1) TASKS_CLE(1) Ox060 Task for writing to pin specified in CONFIGI8]. PSEL. Action on pin is to set it how. TASKS_CLE(1) TASKS_CLE(1) Ox060 Task for writing to pin specified in CONFIGI8]. PSEL. Action on pin is to set it how. TASKS_CLE(1) TASKS_CLE(1) Ox070 Task for writing to pin specified in CONFIGI8]. PSEL. Action on pin is to set it how. TASKS_CLE(1) Ox071 Task for writing to pin specified in CONFIGI8]. PSEL. Action on pin is to set it how. TASKS_CLE(1) TASKS_CLE(1) Ox072 Task for writing to pin specified in CONFIGI8]. PSEL. Action o	TACKS OFIE	0::014	
TASKS_OUT[6] Ox018 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is configured in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[0] Ox030 Task for writing to pin specified in CONFIG[0].PSEL Action on pin is to set it high. TASKS_SET[1] Ox038 Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it high. TASKS_SET[3] Ox03C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] Ox04D Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[6] Ox04B Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[7] Ox04C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[7] Ox04C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[7] Ox04C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_CLR[1] Ox06D Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_CLR[1] Ox06D Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox06D Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox06C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox06C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox07C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox10A Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox10A Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASK	TASKS_OUT[5]	0x014	
TASKS_OUT[7] DX01C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is configured in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[1] DX03A Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[2] DX03B Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] DX03C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] DX03C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[8] DX04D Task for writing to pin specified in CONFIG[4].PSEL Action on pin is to set it high. TASKS_SET[8] DX04B Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[8] DX04B Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[8] DX04B Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_CLR[0] DX06C Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it low. TASKS_CLR[1] DX06B Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it low. TASKS_CLR[1] DX06C Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it low. TASKS_CLR[1] DX06C Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it low. TASKS_CLR[1] DX07C TASK for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it low. TASKS_CLR[1] DX07C TASK for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it low. TASKS_CLR[1] DX07C TASK for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it low. TASKS_CLR[1] DX07C TASKS_CLR[2] DX07C TASK for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it low. TASKS_CLR[1] DX07C TASKS_CLR[2] DX07C TASKS_CLR[3] DX07C TASKS_CLR[3] DX07C TASKS_CLR[4] DX07C TASKS_CLR[6] DX07C TASKS_CLR[7] DX17C TASKS_CLR[7] DX17C	TACKS OUTS	0.040	
TASKS_OUT[7] Ox01C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[0] Ox034 Task for writing to pin specified in CONFIG[0].PSEL Action on pin is to set it high. TASKS_SET[1] Ox034 Task for writing to pin specified in CONFIG[0].PSEL Action on pin is to set it high. TASKS_SET[3] Ox03C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] Ox040 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[6] Ox040 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[7] Ox042 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[7] Ox04C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CLR[1] Ox060 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CLR[1] Ox060 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CLR[1] Ox060 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox066 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox06C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox070 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox070 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox071 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox072 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox071 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox072 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] Ox073 T	TASKS_OUT[6]	0x018	
CONFIG[7] POLARITY. TASKS_SET[0] 0x030 Task for writing to pin specified in CONFIG[0].PSEL Action on pin is to set it high. TASKS_SET[1] 0x038 Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it high. TASKS_SET[2] 0x038 Task for writing to pin specified in CONFIG[2].PSEL Action on pin is to set it high. TASKS_SET[3] 0x03C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[4] 0x040 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[6] 0x044 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[7] 0x04C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[7] 0x04C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[7] 0x04C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CLR[1] 0x060 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[2] 0x066 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[2] 0x066 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[6] 0x070 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[6] 0x074 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x100 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[0] 0x110 Event gene	TACKS OF TELET	0.046	• •
TASKS_SET[0] 0x030 Task for writing to pin specified in CONFIG[0].PSEL Action on pin is to set it high. TASKS_SET[1] 0x034 Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it high. TASKS_SET[2] 0x038 Task for writing to pin specified in CONFIG[2].PSEL Action on pin is to set it high. TASKS_SET[3] 0x03C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[4] 0x040 Task for writing to pin specified in CONFIG[4].PSEL Action on pin is to set it high. TASKS_SET[5] 0x044 Task for writing to pin specified in CONFIG[4].PSEL Action on pin is to set it high. TASKS_SET[6] 0x044 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[7] 0x04C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_CLR[0] 0x060 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_CLR[1] 0x066 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[2] 0x068 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[2] 0x060 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x070 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x070 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x070 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x070 Task for writing to pin specified in CONFIG[3].PSEL EVENTS_IN[3] 0x104 Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[3] 0x104 Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[3] 0x104 Event generated from pin specifi	TASKS_OUT[/]	0x01C	
TASKS_SET[3] 0x034 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] 0x038 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] 0x030 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[4] 0x040 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[5] 0x044 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[6] 0x048 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[7] 0x040 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CET[8] 0x040 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[0] 0x060 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[2] 0x068 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x060 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[6] 0x074 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x070 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x070 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x070 Task for writing to pin specified in CONFIG[6].PSEL TASKS_CLR[7] 0x100 Event generated from pin specified in CONFIG[6].PSEL TASKS_CLR[7] 0x100 Event generated from pin specified in CONFIG[6].PSEL TASKS_CLR[7] 0x100 Event generated from pin specified in CONFIG[6].PSEL TASKS_CLR[7] 0x100 Event generated from pin specified in CONFIG[6].PSEL TASKS_CLR[7] 0x100 Event generat	T. 0.40 05T[0]		
TASKS_EST[2] 0x038 Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it high. TASKS_EST[3] 0x03C Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it high. TASKS_EST[4] 0x040 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it high. TASKS_EST[5] 0x044 Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it high. TASKS_EST[7] 0x046 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it high. TASKS_EST[7] 0x04C Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it high. TASKS_CLR[0] 0x060 Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it low. TASKS_CLR[1] 0x066 Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x070 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x070 Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x070 Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. TASKS_CLR[8] 0x078 Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x100 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[1] 0x100 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[8] 0x100 Event generated from pin specified in CONFIG[9].PSEL EVENTS_IN[9] 0x100 Event generated from pin specified in CONFIG[9].PSEL EVENTS_IN[9] 0x101 Event generated from pin specified in CONFIG[9].P	_		
TASKS_EST[3] 0x03C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_EST[4] 0x040 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_EST[5] 0x044 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_EST[6] 0x048 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_EST[7] 0x04C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CLR[0] 0x060 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it low. TASKS_CLR[2] 0x068 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[6] 0x074 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x074 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x072 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x100 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Even	_		
TASKS_SET[4] 0x040 Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it high. TASKS_SET[5] 0x044 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[6] 0x048 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[7] 0x04C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_CLR[1] 0x060 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x066 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[2] 0x068 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[7].PSEL Action on pin is to set it low. EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[3] 0x104 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[3] 0x104 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[3] 0x105 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[6] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL	_		
TASKS_SET[5] 0x044 Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it high. TASKS_SET[6] 0x048 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it high. TASKS_SET[7] 0x04C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_CLR[0] 0x060 Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x068 Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x06C Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it low. TASKS_CLR[1] 0x070 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x074 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x074 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x074 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x070 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x070 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[1] 0x105 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x116 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x116 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x116 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x116 Event generated from pin specifi	_		
TASKS_EST[6] 0x048 Task for writing to pin specified in CONFIG[6]. PSEL Action on pin is to set it high. TASKS_EST[7] 0x04C Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it high. TASKS_CLR[0] 0x060 Task for writing to pin specified in CONFIG[1]. PSEL Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[1]. PSEL Action on pin is to set it low. TASKS_CLR[2] 0x068 Task for writing to pin specified in CONFIG[2]. PSEL Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3]. PSEL Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[3]. PSEL Action on pin is to set it low. TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[5]. PSEL Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6]. PSEL Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[7]. PSEL Action on pin is to set it low. EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[7]. PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[4] 0x10 Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[6] 0x114 Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[8] 0x114 Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[8] 0x114 Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[9] 0x116 Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[9] 0x117 Event generated from pin specified in CONFIG[8]. PSEL EVENTS_IN[8] 0x114 Event generated from pin specified in CONFIG[8]. PSEL E	_		
TASKS_CER[7] 0x04C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_CLR[1] 0x060 Task for writing to pin specified in CONFIG[0].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x068 Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[6] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PS	_		
TASKS_CLR[0] 0x060 Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it low. TASKS_CLR[2] 0x068 Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it low. TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x100 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[7] 0x11C Event generated fro	_		Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it high.
TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it low. TASKS_CLR[2] 0x068 Task for writing to pin specified in CONFIG[2].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[4].PSEL Action on pin is to set it low. TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[5].PSEL Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_PORT 0x17C Event generated from pin specified in CONFIG[6].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTERSET 0x304 Enable interrupt INTERNACR 0x308 Disable interrupt INTERNACR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x516 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	_		
TASKS_CLR[2] 0x068 Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low. TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[7].PSEL. EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_PORT 0x17C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENSET 0x304 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x516 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[0]	0x060	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it low.
TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it low. TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[0].PSEL. EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[3] 0x101 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[6] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_PORT 0x17C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[1]	0x064	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it low.
TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it low. TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[7].PSEL Action on pin is to set it low. EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[6] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[2]	0x068	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it low.
TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[3]	0x06C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low.
TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[4]	0x070	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it low.
TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[5]	0x074	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low.
EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[6]	0x078	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low.
EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[7]	0x07C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low.
EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[0]	0x100	Event generated from pin specified in CONFIG[0].PSEL
EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[1]	0x104	Event generated from pin specified in CONFIG[1].PSEL
EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[2]	0x108	Event generated from pin specified in CONFIG[2].PSEL
EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[3]	0x10C	Event generated from pin specified in CONFIG[3].PSEL
EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[4]	0x110	Event generated from pin specified in CONFIG[4].PSEL
EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[5]	0x114	Event generated from pin specified in CONFIG[5].PSEL
EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[6]	0x118	Event generated from pin specified in CONFIG[6].PSEL
INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[7]	0x11C	Event generated from pin specified in CONFIG[7].PSEL
INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_PORT	0x17C	Event generated from multiple input GPIO pins with SENSE mechanism enabled
CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	INTENSET	0x304	Enable interrupt
CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	INTENCLR	0x308	Disable interrupt
CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	CONFIG[0]	0x510	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	CONFIG[1]	0x514	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	CONFIG[2]	0x518	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	CONFIG[3]	0x51C	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
	CONFIG[4]	0x520	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	CONFIG[5]	0x524	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
• • • • • • • • • • • • • • • • • • • •	CONFIG[6]	0x528	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[7] 0x52C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	CONFIG[7]	0x52C	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

21.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 3	17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	1	HGFEDCBA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description	
		6



Bit n	umbe	er		31 30 29	9 28 27	7 26 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				1				HGFEDCBA
		0000000			0 0	0 (0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Cat	1				See EVENTS_IN[0]
			Set Disabled	0				Enable Read: Disabled
			Enabled	1				Read: Enabled
В	RW	IN1	Lilabieu	1				Write '1' to Enable interrupt for IN[1] event
								See EVENTS_IN[1]
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled
С	RW	IN2						Write '1' to Enable interrupt for IN[2] event
								See EVENTS_IN[2]
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled
D	RW	IN3						Write '1' to Enable interrupt for IN[3] event
								See EVENTS_IN[3]
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled
E	RW	IN4						Write '1' to Enable interrupt for IN[4] event
								See EVENTS_IN[4]
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled
F	RW	IN5						Write '1' to Enable interrupt for IN[5] event
								See EVENTS_IN[5]
			Set	1				Enable
			Disabled	0				Read: Disabled
G	RW	IN6	Enabled	1				Read: Enabled Write '1' to Enable interrupt for IN[6] event
-								
			6.1					See EVENTS_IN[6]
			Set	1				Enable Pool Disabled
			Disabled Enabled	0				Read: Disabled Read: Enabled
Н	RW	IN7	Lilabieu	1				Write '1' to Enable interrupt for IN[7] event
								See EVENTS_IN[7]
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled
I	RW	PORT						Write '1' to Enable interrupt for PORT event
								See EVENTS_PORT
			Set	1				Enable
			Disabled	0				Read: Disabled
			Enabled	1				Read: Enabled

21.4.2 INTENCLR

Address offset: 0x308

Disable interrupt



Bit	numb	er		31 30	29	28 :	27 2	6 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				1						H G F E D C B A
Res	et 0x0	0000000		0 0	0	0	0 () (0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value						Description
Α	RW	INO								Write '1' to Disable interrupt for IN[0] event See EVENTS_IN[0]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
В	RW	IN1								Write '1' to Disable interrupt for IN[1] event
			a.							See EVENTS_IN[1]
			Clear	1						Disable
			Disabled	0						Read: Disabled
_	D\A/	INIO	Enabled	1						Read: Enabled
С	KVV	IN2								Write '1' to Disable interrupt for IN[2] event See EVENTS_IN[2]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
D	RW	IN3								Write '1' to Disable interrupt for IN[3] event
										See EVENTS_IN[3]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Ε	RW	IN4								Write '1' to Disable interrupt for IN[4] event
										See EVENTS_IN[4]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
F	RW	IN5								Write '1' to Disable interrupt for IN[5] event
										See EVENTS_IN[5]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
G	RW	IN6								Write '1' to Disable interrupt for IN[6] event
										See EVENTS_IN[6]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Н	RW	IN7								Write '1' to Disable interrupt for IN[7] event See EVENTS IN[7]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
ı	RW	PORT								Write '1' to Disable interrupt for PORT event
										See EVENTS_PORT
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled

21.4.3 CONFIG[0]

Address offset: 0x510



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		D CC BBBBB A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW MODE		Mode
	Disabled	O Disabled. Pin specified by PSEL will not be acquired by the
		GPIOTE module.
	Event	1 Event mode
		The pin specified by PSEL will be configured as an input and the
		IN[n] event will be generated if operation specified in POLARITY
		occurs on the pin.
	Task	3 Task mode
		The GPIO specified by PSEL will be configured as an output and
		triggering the SET[n], CLR[n] or OUT[n] task will perform the
		operation specified by POLARITY on the pin. When enabled as a
		task the GPIOTE module will acquire the pin and the pin can no
		longer be written as a regular output pin from the GPIO module.
B RW PSEL		[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
		and IN[n] event
C RW POLARITY		When In task mode: Operation to be performed on output
		when OUT[n] task is triggered. When In event mode: Operation
		on input that shall trigger IN[n] event.
	None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no
		IN[n] event generated on pin activity.
	LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate
		IN[n] event when rising edge on pin.
	HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
		IN[n] event when falling edge on pin.
	Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate
D RW OUTINIT		IN[n] when any change on pin. When in task mode: Initial value of the output when the GPIOTE
D WAN OOTHALL		channel is configured. When in event mode: No effect.
	Low	0 Task mode: Initial value of pin before task triggering is low
	High	1 Task mode: Initial value of pin before task triggering is high
	HIGH	1 ask mode. initial value of pin before task triggering is high

21.4.4 CONFIG[1]

Address offset: 0x514

	Ŭ	_		-	-						-	-																						
Bit r	umbe	r		31	30 2	29	28 2	27 :	26 2	5 2	4 2	23 22	2 21	L 20	19	18	3 1	7 1	6 1	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	1	0
Id														D			C	0	2				В	В	В	В	В						Α	А
Rese	et 0x0	0000000		0	0	0	0	0	0 (0) (0 0	0	0	0	0	0) () (0	0	0	0	0	0	0	0 (0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						0	Desc	ript	ion																				
Α	RW	MODE									N	√lod(е																					
			Disabled	0							0	Disab	led	. Pir	ı sp	eci	ifie	d b	y P	SE	Lw	ill n	ot	oe a	ıcqı	uire	d b	y tł	ne					
											C	SPIO	TE	mod	lule	2.																		
			Event	1							Е	ven	t m	ode																				
											Т	he p	oin s	spec	ifie	ed b	oy F	PSE	Lw	/ill	be (con	ıfigı	ırec	l as	an	inp	ut	and	the	е			
											П	N[n]	eve	ent v	will	be	ge	ne	rate	ed	if o	per	atio	n s	pec	ifie	d in	P	OLA	RIT	Υ			
											c	occui	rs o	n th	ер	in.																		
			Task	3							Т	ask	mo	de																				
											Т	he (SPIC) sp	eci	fiec	d by	y P	SEL	wi	ll b	e co	onfi	gur	ed	as a	n o	utp	out a	anc	ı			
											t	rigge	erin	g th	e S	ET[[n],	CL	R[n	n] o	r O	UT	[n]	task	wi	ll p	erfo	rm	the	غ				
											c	per	atio	n sp	eci	ifie	d b	у Р	OL	AR	ITY	on	the	pir	. W	/he	n er	nab	led	as	a			
											t	ask 1	the	GPI	ОТІ	E m	od	ule	wi	II a	cqı	iire	the	e pii	n ar	nd t	he p	oin	can	n)			
											le	onge	er b	e wi	ritte	en a	as a	a re	gu	lar	ou	pu	t pi	n fr	om	the	GP	10	mo	dul	e.			



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			D C C B B B B B A A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
B RW PSEL		[031]	GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
			and IN[n] event
C RW POLARITY			When In task mode: Operation to be performed on output
			when OUT[n] task is triggered. When In event mode: Operation
			on input that shall trigger IN[n] event.
	None	0	Task mode: No effect on pin from OUT[n] task. Event mode: no
			IN[n] event generated on pin activity.
	LoToHi	1	Task mode: Set pin from OUT[n] task. Event mode: Generate
			IN[n] event when rising edge on pin.
	HiToLo	2	Task mode: Clear pin from OUT[n] task. Event mode: Generate
			IN[n] event when falling edge on pin.
	Toggle	3	Task mode: Toggle pin from OUT[n]. Event mode: Generate
			IN[n] when any change on pin.
D RW OUTINIT			When in task mode: Initial value of the output when the GPIOTE
			channel is configured. When in event mode: No effect.
	Low	0	Task mode: Initial value of pin before task triggering is low
	High	1	Task mode: Initial value of pin before task triggering is high

21.4.5 CONFIG[2]

Address offset: 0x518

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
d			D C C B B B B B A A
Reset 0x00000000		0 0 0 0 0 0 0 0	
d RW Field	Value Id	Value	Description
A RW MODE			Mode
	Disabled	0	Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module.
	Event	1	Event mode
			The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin.
	Task	3	Task mode
			The GPIO specified by PSEL will be configured as an output and
			triggering the SET[n], CLR[n] or OUT[n] task will perform the
			operation specified by POLARITY on the pin. When enabled as a
			task the GPIOTE module will acquire the pin and the pin can no
			longer be written as a regular output pin from the GPIO module.
3 RW PSEL		[031]	GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event
C RW POLARITY			When In task mode: Operation to be performed on output
			when OUT[n] task is triggered. When In event mode: Operation
			on input that shall trigger IN[n] event.
	None	0	Task mode: No effect on pin from OUT[n] task. Event mode: no
			IN[n] event generated on pin activity.
	LoToHi	1	Task mode: Set pin from OUT[n] task. Event mode: Generate
			IN[n] event when rising edge on pin.
	HiToLo	2	Task mode: Clear pin from OUT[n] task. Event mode: Generate
			IN[n] event when falling edge on pin.
	Toggle	3	Task mode: Toggle pin from OUT[n]. Event mode: Generate
			IN[n] when any change on pin.



Bit numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 -	4 3	2	1	0
Id														D			С	С				В	В	В	В	В						Α	Α
Reset 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ld RW	Field	Value Id	Va	lue							De	scr	iptio	on																			
D RW	OUTINIT										Wh	nen	in t	tasl	k m	ode	e: In	itia	l va	lue	of	the	out	put	wh	en	the	GF	TOI	E			
											cha	ann	el is	s cc	onfi	gur	ed.	Wh	nen	in e	evei	nt m	ode	e: N	lo e	ffe	ct.						
		Low	0								Tas	sk r	nod	le: I	Initi	al v	alu	e o	f pi	n b	efor	e ta	sk t	rig	geri	ng	is lo	w					
		High	1								Tas	sk r	nod	le: I	Initi	al v	alu	e o	f pi	n b	efor	e ta	sk t	rig	geri	ng	is h	igh					

21.4.6 CONFIG[3]

Address offset: 0x51C

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit	numb	er		3	1 3	29	28	27	26	25	24	23	3 22 2	1 20	19	9 18	17	16	15	14	13	12	11 1	10 9	8	3 7	6	5	4	3	2	1
Id														D			С	С				В	В	ВЕ	3 E	3						Α
Res	et 0x0	0000000		C	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0
Id	RW	Field	Value Id	١	/alu	е						De	escrip	tion																		
Α	RW	MODE										M	ode																			
			Disabled	C)							Di	sable	d. Pi	n s	peci	fiec	l by	PS	EL v	ılli,	not	be a	cqu	ired	by	the					
												GF	PIOTE	mod	dul	e.																
			Event	1								Ev	ent m	ode	•																	
												Th	ie pin	spe	cifi	ed b	y P	SEL	wil	l be	100	nfig	ured	l as	an i	npu	t an	d th	ne			
												IN	[n] ev	ent	wil	l be	ger	nera	itec	lifo	pe	rati	on s	peci	fied	in!	POL	ARI	TY			
												oc	curs	on th	ne p	oin.																
			Task	3	}							Та	sk mo	ode																		
												Th	ie GPI	O sn	eci	ified	bv	PSI	EL w	/ill l	e c	onf	igur	ed a	s aı	า ดน	tpu	t an	d			
													ggerii										_						-			
													eratio	-		_									•				s a			
													sk the																			
												loi	nger b	oe w	ritt	en a	is a	reg	ula	r oı	itpu	ıt pi	n fr	om i	the	GPI	0 m	odu	ıle.			
В	RW	PSEL		[03	1]						GF	PIO nu	ımb	er a	asso	ciat	ed	wit	h SE	T[n], C	LR[n	ı] ar	d C	UT[n] t	asks	5			
												an	d IN[n] ev	/en	t																
С	RW	POLARITY										W	hen II	n tas	k n	nod	e: O	pei	atio	on t	o b	е ре	erfor	me	d oı	n ou	tpu	t				
												wł	hen O	ı]TU	n] t	ask	is tr	igg	ere	d. V	/he	n Ir	eve	ent r	noc	le: C	pe	ratio	on			
												on	inpu	t tha	at s	hall	trig	ger	IN	n] e	eve	nt.										
			None	C)							Та	sk mo	ode:	No	eff	ect	on	pin	froi	n O	UT[n] ta	ask.	Eve	nt r	nod	e: n	10			
												IN	[n] ev	ent	ger	nera	ted	on	pin	act	ivit	у.										
			LoToHi	1	•							Та	sk mo	ode:	Set	t pin	fro	m	רטכ	[[n]	tas	k. E	vent	t mo	de	Ge	nera	ate				
												IN	[n] ev	ent	wh	en r	isin	g e	dge	on	pin											
			HiToLo	2	2							Та	sk mo	ode:	Cle	ear p	in f	ror	n O	UT[n] t	ask.	Eve	nt r	noc	le: G	iene	erat	e			
													[n] ev					-	_		•											
			Toggle	3	3								isk mo				•				[n]	. Ev	ent	mod	le:	Gen	erat	:e				
													[n] w				_		-													
D	RW	OUTINIT											hen ir															PIC	TE			
													annel			-																
			Low	0									sk mo						•							_						
			High	1	-							Та	sk mo	ode:	Ini	tial v	valu	ie o	t pi	n b	efor	e ta	isk t	rigg	erir	ig is	hig	h				

21.4.7 CONFIG[4]

Address offset: 0x520



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		D CC BBBBB A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW MODE		Mode
	Disabled	O Disabled. Pin specified by PSEL will not be acquired by the
		GPIOTE module.
	Event	1 Event mode
		The pin specified by PSEL will be configured as an input and the
		IN[n] event will be generated if operation specified in POLARITY
		occurs on the pin.
	Task	3 Task mode
		The GPIO specified by PSEL will be configured as an output and
		triggering the SET[n], CLR[n] or OUT[n] task will perform the
		operation specified by POLARITY on the pin. When enabled as a
		task the GPIOTE module will acquire the pin and the pin can no
		longer be written as a regular output pin from the GPIO module.
B RW PSEL		[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
		and IN[n] event
C RW POLARITY		When In task mode: Operation to be performed on output
		when OUT[n] task is triggered. When In event mode: Operation
		on input that shall trigger IN[n] event.
	None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no
		IN[n] event generated on pin activity.
	LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate
		IN[n] event when rising edge on pin.
	HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
		IN[n] event when falling edge on pin.
	Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate
D RW OUTINIT		IN[n] when any change on pin. When in task mode: Initial value of the output when the GPIOTE
D WAN OOTHALL		channel is configured. When in event mode: No effect.
	Low	0 Task mode: Initial value of pin before task triggering is low
	High	1 Task mode: Initial value of pin before task triggering is high
	HIGH	1 ask mode. initial value of pin before task triggering is high

21.4.8 CONFIG[5]

Address offset: 0x524

	3			٠	•																														
Bit n	umbe	er		3:	1 30	29	28	3 27	26	25	24	4 23	22	21	20	19	18	3 17	1 10	5 1	5 1	4 1	3 1	12 1	.1 1	0 9	8	3 7	6	5	4	3	2	1	0
Id															D			С	C					В	ВЕ	3 E	E	3						Α	Α
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C) () (0	0 (0 (0	(0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	V	alue	•						De	scr	ipti	on																				
Α	RW	MODE										Mo	ode	è																					
			Disabled	0								Dis	ab	led.	Pin	sp	eci	fie	d b	/ P:	SEL	wi	ll n	ot b	e a	cqui	rec	l by	the	è					
												GP	10	TE n	nod	ule	١.																		
			Event	1								Eve	ent	mo	de																				
												The	e p	in s	pec	ifie	d b	у Р	SEI	. w	ill k	oe c	on	figu	red	as a	an i	npu	t ar	nd t	he				
												IN[[n]	eve	nt v	vill	be	ge	ner	ate	d i	f op	era	atio	n sp	oeci	fied	in I	POL	ARI	ITY				
												oco	cur	s or	the	e p	in.																		
			Task	3								Tas	sk ı	mod	le																				
												The	e G	PIO	spe	ecit	fied	l by	PS	EL	wil	l be	e co	nfig	gure	ed a	s aı	ı ou	tpu	ıt ar	nd				
												trig	gge	ering	th	e S	ET[n],	CLF	R[n]] oi	· 01	JT[n] t	ask	will	pe	rfor	m t	he					
												ор	era	tior	ı sp	eci	fie	d b	/ P()L/	١RI	TY (on t	the	pin	. Wł	nen	ena	able	ed a	s a				
												tas	k t	he (GPIC	OTE	m	od	ıle	wil	l a	qu	ire	the	pin	an	d th	ne pi	in c	an r	าด				
												Ion	ige	r be	wr	itte	en a	as a	re	gul	ar	out	put	pir	fro	m t	he	GPI	0 n	nod	ule.				



Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			D C C B B B B B A A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
B RW PSEL		[031]	GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
			and IN[n] event
C RW POLARI	Υ		When In task mode: Operation to be performed on output
			when OUT[n] task is triggered. When In event mode: Operation
			on input that shall trigger IN[n] event.
	None	0	Task mode: No effect on pin from OUT[n] task. Event mode: no
			IN[n] event generated on pin activity.
	LoToHi	1	Task mode: Set pin from OUT[n] task. Event mode: Generate
			IN[n] event when rising edge on pin.
	HiToLo	2	Task mode: Clear pin from OUT[n] task. Event mode: Generate
			IN[n] event when falling edge on pin.
	Toggle	3	Task mode: Toggle pin from OUT[n]. Event mode: Generate
			IN[n] when any change on pin.
D RW OUTINI			When in task mode: Initial value of the output when the GPIOTE
			channel is configured. When in event mode: No effect.
	Low	0	Task mode: Initial value of pin before task triggering is low
	High	1	Task mode: Initial value of pin before task triggering is high

21.4.9 CONFIG[6]

Address offset: 0x528

Bit num	nbe	r		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 (
Id				D CC BBBBB	A
Reset 0	0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 (
ld R	w	Field	Value Id	Value Description	
A R'	W	MODE		Mode	
			Disabled	O Disabled. Pin specified by PSEL will not be acquired by the	
				GPIOTE module.	
			Event	1 Event mode	
				The pin specified by PSEL will be configured as an input and the	
				IN[n] event will be generated if operation specified in POLARITY	
				occurs on the pin.	
			Task	3 Task mode	
				The COIO and if all to DCCI will be anothered and automated	
				The GPIO specified by PSEL will be configured as an output and	
				triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a	
				task the GPIOTE module will acquire the pin and the pin can no	
				longer be written as a regular output pin from the GPIO module.	
B R'	۱۸/	PSEL		[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks	
<i>D</i> IX		1322		and IN[n] event	
C R	w	POLARITY		When In task mode: Operation to be performed on output	
		. 02		when OUT[n] task is triggered. When In event mode: Operation	
				on input that shall trigger IN[n] event.	
			None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no	
				IN[n] event generated on pin activity.	
			LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate	
				IN[n] event when rising edge on pin.	
			HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate	
				IN[n] event when falling edge on pin.	
			Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate	
				IN[n] when any change on pin.	



Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	.0	9 1	3 7	' 6	5	4	3	2	1	0
Id													D			С	С				В	В	В	ВΙ	3						Α	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0
ld RW Field	Value Id	Va	lue							De	scr	ipti	on																			
D RW OUTINIT										W	hen	in	tasl	c mo	ode	: In	itia	l va	lue	of t	he (out	out	wh	en t	he (SPIC	OTE				
										ch	ann	el i	s cc	nfig	gur	ed.	Wh	ien	in e	ven	t m	ode	: N	o ef	fec							
	Low	0								Ta	sk r	noc	de: I	niti	al v	alu	e o	f pi	n be	efor	e ta	sk t	rigg	erii	ng is	lov	v					
	High	1								Та	sk r	noc	le: I	niti	al v	alu	e o	f pi	n be	efor	e ta	sk t	rigg	erii	ng is	hig	h					

21.4.10 CONFIG[7]

Address offset: 0x52C

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

		<u> </u>									
Bit number	31 30	29 28 27 26 25 24 23	22 21 20 19 18	17 16 15 14 1	.3 12 11 10 9	8 7	6 5	4	3 2	2 1	0
Id			D	СС	ВВВЕ	3 B				Α	Α
Reset 0x00000000	0 0	0 0 0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0	0	0 0	0	0
Id RW Field Valu	ie Id Value	Des	cription								
A RW MODE		Мо	de								
Disa	bled 0	Disa	abled. Pin specif	fied by PSEL wil	ll not be acqu	ired by	the				
		GPI	OTE module.								
Ever	nt 1	Eve	nt mode								
		The	pin specified by	v PSFI will he c	onfigured as	an innut	and t	the			
			n] event will be	•	•	•					
		_	urs on the pin.	Beneratea ii op	serution speci	nea mi	OL/ III				
Task	3		k mode								
. 43.											
			GPIO specified	•	•			nd			
		_	gering the SET[r			•					
		·	ration specified	•							
			k the GPIOTE mo								
	5		ger be written a								
B RW PSEL	[031]		O number assoc	ciated with SET	[n], CLR[n] ar	id OUT[i	n] tasi	KS			
			I IN[n] event								
C RW POLARITY			en In task mode	•	•						
			en OUT[n] task i			noae: O	perat	ion			
	•		input that shall t								
Non	e 0		k mode: No effe	•		Event n	ioae:	no			
LaTe	-11:	_	n] event generat	•	•						
LoTo	oHi 1		k mode: Set pin			ae: Ger	ierate				
HiTo	oLo 2		n] event when ri			da. C		+-			
niic	ilo 2		k mode: Clear pi		='	noue: G	enera	te			
Torr	rlo 2		n] event when fa			lo: Con	rata				
Togg	gle 3		k mode: Toggle n] when any cha	•	iij. Eveiit mot	ie. Gene	ale				
D RW OUTINIT		-		• •	of the cutout	whon th	o CDI	OTE			
D NW OUTINIT			en in task mode		·			OIE			
1	0		nnel is configure								
Low			k mode: Initial v	•	-						
High	1	Tas	k mode: Initial v	raiue oi piii ber	ore task trigg	ering is	ıııgıı				

21.5 Electrical specification

21.5.1 GPIOTE Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{GPIOTE,IN}	Run current with 1 or more GPIOTE active channels in Input		0.1	0.5	μΑ
	mode				



22 PPI — Programmable peripheral interconnect

The Programmable peripheral interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. The PPI allows precise synchronization between peripherals when real-time application constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

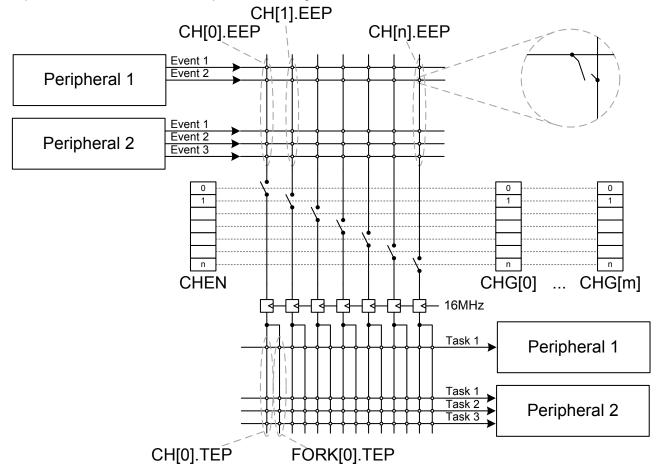


Figure 28: PPI block diagram

The PPI system has, in addition to the fully programmable peripheral interconnections, a set of channels where the event end point (EEP) and task end points (TEP) are fixed in hardware. These fixed channels can be individually enabled, disabled, or added to PPI channel groups in the same way as ordinary PPI channels.

Table 34: Configurable and fixed PPI channels

Instance	Channel	Number of channels	Number of groups
PPI	0-19	20	6
PPI (fixed)	20-31	12	

The PPI provides a mechanism to automatically trigger a task in one peripheral as a result of an event occurring in another peripheral. A task is connected to an event through a PPI channel. The PPI channel is composed of three end point registers, one EEP and two TEPs. A peripheral task is connected to a TEP using the address of the task register associated with the task. Similarly, a peripheral event is connected to an EEP using the address of the event register associated with the event.

On each PPI channel, the signals are synchronized to the 16 MHz clock, to avoid any internal violation of setup and hold timings. As a consequence, events that are synchronous to the 16 MHz clock will be delayed by one clock period, while other asynchronous events will be delayed by up to one 16 MHz clock period.



Note that shortcuts (as defined in the SHORTS register in each peripheral) are not affected by this 16 MHz synchronization, and are therefore not delayed.

Each TEP implements a fork mechanism that enables a second task to be triggered at the same time as the task specified in the TEP is triggered. This second task is configured in the task end point register in the FORK registers groups, e.g. FORK.TEP[0] is associated with PPI channel CH[0].

There are two ways of enabling and disabling PPI channels:

- Enable or disable PPI channels individually using the CHEN, CHENSET, and CHENCLR registers.
- Enable or disable PPI channels in PPI channel groups through the groups' ENABLE and DISABLE tasks.
 Prior to these tasks being triggered, the PPI channel group must be configured to define which PPI channels belongs to which groups.

Note that when a channel belongs to two groups m and n, and CHG[m].EN and CHG[n].DIS occur simultaneously (m and n can be equal or different), EN on that channel has priority.

PPI tasks (for example, CHG[0].EN) can be triggered through the PPI like any other task, which means they can be hooked up to a PPI channel as a TEP. One event can trigger multiple tasks by using multiple channels and one task can be triggered by multiple events in the same way.

22.1 Pre-programmed channels

Some of the PPI channels are pre-programmed. These channels cannot be configured by the CPU, but can be added to groups and enabled and disabled like the general purpose PPI channels. The FORK TEP for these channels are still programmable and can be used by the application.

For a list of pre-programmed PPI channels, see the table below.

Table 35: Pre-programmed channels

Channel	EEP	TEP
20	TIMERO->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
21	TIMERO->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
22	TIMERO->EVENTS_COMPARE[1]	RADIO->TASKS_DISABLE
23	RADIO->EVENTS_BCMATCH	AAR->TASKS_START
24	RADIO->EVENTS_READY	CCM->TASKS_KSGEN
25	RADIO->EVENTS_ADDRESS	CCM->TASKS_CRYPT
26	RADIO->EVENTS_ADDRESS	TIMERO->TASKS_CAPTURE[1]
27	RADIO->EVENTS_END	TIMERO->TASKS_CAPTURE[2]
28	RTCO->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
29	RTC0->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
30	RTCO->EVENTS_COMPARE[0]	TIMERO->TASKS_CLEAR
31	RTCO->EVENTS_COMPARE[0]	TIMERO->TASKS_START

22.2 Registers

Table 36: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001F000	PPI	PPI	Programmable Peripheral Interconnect	

Table 37: Register Overview

Register	Offset	Description
TASKS_CHG[0].EN	0x000	Enable channel group 0
TASKS_CHG[0].DIS	0x004	Disable channel group 0
TASKS_CHG[1].EN	0x008	Enable channel group 1
TASKS_CHG[1].DIS	0x00C	Disable channel group 1
TASKS_CHG[2].EN	0x010	Enable channel group 2
TASKS_CHG[2].DIS	0x014	Disable channel group 2
TASKS_CHG[3].EN	0x018	Enable channel group 3
TASKS_CHG[3].DIS	0x01C	Disable channel group 3
TASKS CHG[4].EN	0x020	Enable channel group 4



Register	Offset	Description
TASKS_CHG[4].DIS	0x024	Disable channel group 4
TASKS_CHG[5].EN	0x028	Enable channel group 5
TASKS_CHG[5].DIS	0x02C	Disable channel group 5
CHEN	0x500	Channel enable register
CHENSET	0x504	Channel enable set register
CHENCLR	0x508	Channel enable clear register
CH[0].EEP	0x510	Channel 0 event end-point
CH[0].TEP	0x514	Channel 0 task end-point
CH[1].EEP	0x518	Channel 1 event end-point
CH[1].TEP	0x51C	Channel 1 task end-point
CH[2].EEP	0x520	Channel 2 event end-point
CH[2].TEP	0x524	Channel 2 task end-point
CH[3].EEP	0x528	Channel 3 event end-point
CH[3].TEP	0x52C	Channel 3 task end-point
CH[4].EEP	0x530	Channel 4 event end-point
CH[4].TEP	0x534	Channel 4 task end-point
CH[5].EEP	0x538	Channel 5 event end-point
CH[5].TEP	0x53C	Channel 5 task end-point
CH[6].EEP	0x540	Channel 6 event end-point
CH[6].TEP	0x544	Channel 6 task end-point
CH[7].EEP	0x548	Channel 7 event end-point
CH[7].TEP	0x54C	Channel 7 task end-point
CH[8].EEP	0x550	Channel 8 event end-point
CH[8].TEP	0x554	Channel 8 task end-point
CH[9].EEP	0x558	Channel 9 event end-point
CH[9].TEP	0x55C	Channel 9 task end-point
CH[10].EEP	0x560	Channel 10 event end-point
CH[10].TEP	0x564	Channel 10 task end-point
CH[11].EEP	0x568	Channel 11 event end-point
CH[11].TEP	0x56C	Channel 11 event end-point Channel 11 task end-point
CH[12].EEP	0x50C 0x570	Channel 12 event end-point
CH[12].TEP	0x570	Channel 12 task end-point
CH[13].EEP	0x574 0x578	Channel 13 event end-point
CH[13].TEP	0x576 0x57C	Channel 13 task end-point
CH[14].EEP	0x580	Channel 14 event end-point
CH[14].TEP	0x580	Channel 14 task end-point
CH[15].EEP	0x584	Channel 15 event end-point
CH[15].TEP	0x58C	Channel 15 task end-point
CH[16].EEP	0x590	Channel 16 event end-point
CH[16].TEP	0x590 0x594	Channel 16 task end-point
CH[17].EEP		·
CH[17].EEP	0x598 0x59C	Channel 17 event end-point Channel 17 task end-point
CH[17].TEP CH[18].EEP	0x59C 0x5A0	Channel 17 task end-point Channel 18 event end-point
CH[18].TEP	0x5A0 0x5A4	Channel 18 task end-point Channel 18 task end-point
CH[19].EEP	0x5A4 0x5A8	Channel 19 event end-point
CH[19].TEP	0x5A6 0x5AC	Channel 19 task end-point Channel 19 task end-point
CHG[0]	0x800	Channel group 1
CHG[1]	0x804	Channel group 3
CHG[2]	0x808	Channel group 2
CHG[3]	0x80C	Channel group 4
CHG[4]	0x810	Channel group 5
CHG[5]	0x814	Channel O task and point
FORK[0].TEP	0x910	Channel 1 task and point
FORK[1].TEP	0x914	Channel 1 task end-point
FORK[2].TEP	0x918	Channel 2 task end-point
FORK[3].TEP	0x91C	Channel 3 task end-point
FORK[4].TEP	0x920	Channel 4 task end-point
FORK[5].TEP	0x924	Channel 5 task end-point



Register	Offset	Description	
FORK[6].TEP	0x928	Channel 6 task end-point	
FORK[7].TEP	0x92C	Channel 7 task end-point	
FORK[8].TEP	0x930	Channel 8 task end-point	
FORK[9].TEP	0x934	Channel 9 task end-point	
FORK[10].TEP	0x938	Channel 10 task end-point	
FORK[11].TEP	0x93C	Channel 11 task end-point	
FORK[12].TEP	0x940	Channel 12 task end-point	
FORK[13].TEP	0x944	Channel 13 task end-point	
FORK[14].TEP	0x948	Channel 14 task end-point	
FORK[15].TEP	0x94C	Channel 15 task end-point	
FORK[16].TEP	0x950	Channel 16 task end-point	
FORK[17].TEP	0x954	Channel 17 task end-point	
FORK[18].TEP	0x958	Channel 18 task end-point	
FORK[19].TEP	0x95C	Channel 19 task end-point	
FORK[20].TEP	0x960	Channel 20 task end-point	
FORK[21].TEP	0x964	Channel 21 task end-point	
FORK[22].TEP	0x968	Channel 22 task end-point	
FORK[23].TEP	0x96C	Channel 23 task end-point	
FORK[24].TEP	0x970	Channel 24 task end-point	
FORK[25].TEP	0x974	Channel 25 task end-point	
FORK[26].TEP	0x978	Channel 26 task end-point	
FORK[27].TEP	0x97C	Channel 27 task end-point	
FORK[28].TEP	0x980	Channel 28 task end-point	
FORK[29].TEP	0x984	Channel 29 task end-point	
FORK[30].TEP	0x988	Channel 30 task end-point	
FORK[31].TEP	0x98C	Channel 31 task end-point	

22.2.1 CHEN

Address offset: 0x500 Channel enable register

	numb	er					28 2																			7	-	_		3 2	_	0
Id				f	е	d	С	b	a Z	Z '	Y X	< W	/ V	' U	ΙT	S	R	Q	Р	0	N	M	L K	J	-1	Н	G	F	ΕI	D C	В	Α
Res	et 0x0	00000000		0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	V	alue						D	escr	ript	ion																		
Α	RW	CH0									E	nabl	le o	r d	isab	le d	har	ne	0 ا													
			Disabled	0							D	isab	ole d	cha	nne	I																
			Enabled	1							E	nabl	le c	har	nnel																	
В	RW	CH1									E	nabl	le o	r d	isab	le d	har	ne	1													
			Disabled	0							D	isab	ole d	cha	nne	I																
			Enabled	1							Ei	nabl	le c	har	nnel																	
С	RW	CH2									E	nabl	le o	r d	isab	le d	har	ne	12													
			Disabled	0							D	isab	ole d	cha	nne	I																
			Enabled	1							E	nabl	le c	har	nnel																	
D	RW	CH3									Ei	nabl	le o	r d	isab	le d	har	nne	13													
			Disabled	0							D	isab	ole d	cha	nne	I																
			Enabled	1							E	nabl	le c	har	nnel																	
Е	RW	CH4									Ei	nabl	le o	r d	isab	le d	har	ne	l 4													
			Disabled	0							D	isab	ole d	cha	nne	I																
			Enabled	1							Ei	nabl	le c	har	nnel																	
F	RW	CH5									Ei	nabl	le o	r di	isab	le d	har	nne	15													
			Disabled	0							D	isab	ole d	cha	nne	I																
			Enabled	1							Ei	nabl	le c	har	nnel																	
G	RW	CH6									E	nabl	le o	r d	isab	le d	har	nne	l 6													
			Disabled	0							D	isab	ole d	cha	nne	I																
			Enabled	1							E	nabl	le c	har	nnel																	
Н	RW	CH7									Ei	nabl	le o	r di	isab	le d	har	nne	17													



Bit r	number			31 30	29 28	27 2	26 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b	a Z	Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00	000000		0 0	0 0	0	0 0	0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
ld	RW F	Field	Value Id	Value					Description
			Disabled	0					Disable channel
			Enabled	1					Enable channel
I	RW (CH8							Enable or disable channel 8
			Disabled	0					Disable channel
			Enabled	1					Enable channel
J	RW (CH9							Enable or disable channel 9
			Disabled	0					Disable channel
			Enabled	1					Enable channel
K	RW (CH10	S. 11.1						Enable or disable channel 10
			Disabled	0					Disable channel
	D)4/ /	01144	Enabled	1					Enable channel
L	RW (CH11	Disabled	0					Enable or disable channel 11
			Disabled	0					Disable channel
	DIA/ /	2114.2	Enabled	1					Enable channel
М	RW (LH12	Disabled	0					Enable or disable channel 12 Disable channel
			Disabled Enabled	0					Disable channel Enable channel
N	RW (^U12	Ellabled	1					Enable or disable channel 13
IN	NVV (CUID	Disabled	0					Disable channel
			Enabled	1					Enable channel
0	RW (^H14	Lilabica	-					Enable or disable channel 14
0			Disabled	0					Disable channel
			Enabled	1					Enable channel
Р	RW (CH15	2.100.00	-					Enable or disable channel 15
•		5.115	Disabled	0					Disable channel
			Enabled	1					Enable channel
Q	RW (CH16							Enable or disable channel 16
-			Disabled	0					Disable channel
			Enabled	1					Enable channel
R	RW (CH17							Enable or disable channel 17
			Disabled	0					Disable channel
			Enabled	1					Enable channel
S	RW (CH18							Enable or disable channel 18
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Т	RW (CH19							Enable or disable channel 19
			Disabled	0					Disable channel
			Enabled	1					Enable channel
U	RW (CH20							Enable or disable channel 20
			Disabled	0					Disable channel
			Enabled	1					Enable channel
V	RW (CH21							Enable or disable channel 21
			Disabled	0					Disable channel
			Enabled	1					Enable channel
W	RW (CH22							Enable or disable channel 22
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Χ	RW (CH23							Enable or disable channel 23
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Υ	RW (CH24							Enable or disable channel 24
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Z	RW (CH25							Enable or disable channel 25
			Disabled	0					Disable channel



Bitı	numbe	er		31 30	29 2	8 27 :	26 2	5 24	1 23	22 2	21 2	20 19	9 1	8 17	16	15	14 1	3 12	2 11	10	9	8	7	6 5	5 4	3	2	1 0
Id				f e	d c	b	a Z	2 Y	Χ	W '	V	U T	- 5	R	Q	Р	0 1	N N	1 L	K	J	1 1	4 (G F	E	D	С	ВА
Res	et 0x0	0000000		0 0	0 0	0	0 0	0	0	0 (0	0 0) (0	0	0	0 (0 0	0	0	0	0 ()	0 0	0	0	0	0 0
Id	RW	Field	Value Id	Value					De	escrip	tio	n																
			Enabled	1					En	able	cha	nne	I															
а	RW	CH26							En	able	or (disak	ole	char	nnel	26												
			Disabled	0					Dis	sable	ch	anne	el															
			Enabled	1					En	able	cha	nne	I															
b	RW	CH27							En	able	or (disak	ole	char	nnel	27												
			Disabled	0					Dis	sable	ch	anne	el															
			Enabled	1					En	able	cha	nne	I															
С	RW	CH28							En	able	or (disak	ole	char	nnel	28												
			Disabled	0					Dis	sable	ch	anne	el															
			Enabled	1					En	able	cha	nne	I															
d	RW	CH29							En	able	or (disak	ole	char	nnel	29												
			Disabled	0					Dis	sable	ch	anne	el															
			Enabled	1					En	able	cha	nne	I															
е	RW	CH30							En	able	or (disak	ole	char	nnel	30												
			Disabled	0					Dis	sable	ch	anne	el															
			Enabled	1					En	able	cha	nne	I															
f	RW	CH31							En	able	or (disab	ole	char	nnel	31												
			Disabled	0					Dis	sable	ch	anne	el															
			Enabled	1					En	able	cha	nne	I															

22.2.2 CHENSET

Address offset: 0x504

Channel enable set register

Read: reads value of CH{i} field in CHEN register.

Bit r	iumbe	er		3:	1 30) 2	9 28	3 2	7 26	5 2	5 24	4 2	23 2	22 2	21 2	20 1	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4 3	3 2	1	0
Id				f	е	C	l c	b	а	Z	<u> </u>	′ >	X١	w v	V	U	Т	S	R	Q	Р	0	N	М	L	K	J	1	Н	G	F	Ε [) C	В	Α
Rese	et 0x0	0000000		0	0	0	0	0	0	(0) (0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	٧	alue	:						D)es	crip	tio	n																			
Α	RW	CH0										С	ha	nne	l O	ena	ble	e se	et re	gis	ter	. W	ritii	ng '	0' h	ıas ı	10 6	effe	ct						
			Disabled	0								R	lea	d: c	har	nne	l di	sab	led																
			Enabled	1								R	lea	d: c	har	ne	l en	nab	led																
			Set	1								٧	Vrit	te: E	Ena	ble	cha	anr	nel																
В	RW	CH1										С	ha	nne	1 1	ena	able	e se	et re	gis	ter	. W	riti	ng '	0' h	ıas ı	10 6	effe	ct						
			Disabled	0								R	lea	d: c	har	nne	l di	sab	led																
			Enabled	1								R	lea	d: c	har	nne	l en	nab	led																
			Set	1								٧	Vrit	te: E	Ena	ble	cha	anr	nel																
С	RW	CH2										C	ha	nne	1 2	ena	ble	e se	et re	gis	ter	. W	riti	ng '	0' h	ıas ı	10 6	effe	ct						
			Disabled	0								R	lea	d: c	har	nne	l di	sab	led																
			Enabled	1								R	lea	d: c	har	nne	l en	nab	led																
			Set	1								٧	Vrit	te: E	Ena	ble	cha	anr	nel																
D	RW	CH3										C	ha	nne	13	ena	ble	e se	et re	gis	ter	. W	ritii	ng '	0' h	ıas ı	10 6	effe	ct						
			Disabled	0								R	lea	d: c	har	nne	l di	sab	led																
			Enabled	1								R	lea	d: c	har	nne	l en	nab	led																
			Set	1								٧	Vrit	te: E	Ena	ble	cha	anr	nel																
Ε	RW	CH4										С	ha	nne	14	ena	ble	e se	et re	gis	ter	. W	riti	ng '	0' h	ıas ı	10 6	effe	ct						
			Disabled	0								R	lea	d: c	har	nne	l di	sab	led																
			Enabled	1								R	lea	d: c	har	nne	l en	nab	led																
			Set	1								٧	Vrit	te: E	Ena	ble	cha	anr	nel																
F	RW	CH5												nne						_	ter	. W	riti	ng '	0' h	ias i	10 6	effe	ct						
			Disabled	0								R	lea	d: c	har	nne	l di	sab	led																
			Enabled	1								R	lea	d: c	har	nne	l en	nab	led																
			Set	1								٧	Vrit	te: E	Ena	ble	cha	anr	nel																



Bitı	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCB
Res	set 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
G	RW CH6	5	Channel 6 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
	DW CUZ	Set	1 Write: Enable channel
Н	RW CH7	Disabled	Channel 7 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
	RW CH8	Set	1 Write: Enable channel
'	KW CH8	Disabled	Channel 8 enable set register. Writing '0' has no effect O Read: channel disabled
		Enabled	1 Read: channel enabled
			1 Write: Enable channel
	RW CH9	Set	
J	KW CH9	Disabled	Channel 9 enable set register. Writing '0' has no effect O Read: channel disabled
		Enabled	1 Read: channel enabled
			1 Write: Enable channel
K	RW CH10	Set	
K	KW CHIO	Disabled	Channel 10 enable set register. Writing '0' has no effect O Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
L	RW CH11	JC1	Channel 11 enable set register. Writing '0' has no effect
•	NW CIIII	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
М	RW CH12	Jet	Channel 12 enable set register. Writing '0' has no effect
	NVV CITIZ	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
N	RW CH13	360	Channel 13 enable set register. Writing '0' has no effect
	6.125	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
0	RW CH14		Channel 14 enable set register. Writing '0' has no effect
_		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Р	RW CH15		Channel 15 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Q	RW CH16		Channel 16 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
R	RW CH17		Channel 17 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
S	RW CH18		Channel 18 enable set register. Writing '0' has no effect
-		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Т	RW CH19	JC.	Channel 19 enable set register. Writing '0' has no effect
•	(111)	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Litablea	- Nead. Chamica Chapica



Bit r	numb	er		31 30 29	9 28 2	7 26 25	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e d	l c k	o a Z	<u> </u>	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et OxC	00000000		0 0 0	0 0	0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Set	1				Write: Enable channel
U	RW	CH20						Channel 20 enable set register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Set	1				Write: Enable channel
٧	RW	CH21						Channel 21 enable set register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Set	1				Write: Enable channel
W	RW	CH22						Channel 22 enable set register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Set	1				Write: Enable channel
Χ	RW	CH23						Channel 23 enable set register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Set	1				Write: Enable channel
Υ	RW	CH24						Channel 24 enable set register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Set	1				Write: Enable channel
Z	RW	CH25						Channel 25 enable set register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Set	1				Write: Enable channel
a	RW	CH26						Channel 26 enable set register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Set	1				Write: Enable channel
b	RW	CH27						Channel 27 enable set register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Set	1				Write: Enable channel
С	RW	CH28						Channel 28 enable set register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Set	1				Write: Enable channel
d	RW	CH29						Channel 29 enable set register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Set	1				Write: Enable channel
e	RW	CH30						Channel 30 enable set register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Set	1				Write: Enable channel
f	RW/	CH31		-				Channel 31 enable set register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Set	1				Write: Enable channel
				-				

22.2.3 CHENCLR

Address offset: 0x508

Channel enable clear register



Read: reads value of CH(i) field in CHEN register.

Bit r	numbe	er		31 30	29 2	28 2	7 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0	0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	:				Description
Α	RW	CH0							Channel 0 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
В	RW	CH1							Channel 1 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
С	RW	CH2							Channel 2 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
D	D\A/	CH3	Cicai	-					Channel 3 enable clear register. Writing '0' has no effect
_	1000	CHS	Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
_	DIA	CUA	Clear	1					Write: disable channel
E	ĸW	CH4	8:-11-1						Channel 4 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
F	RW	CH5							Channel 5 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
G	RW	CH6							Channel 6 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
Н	RW	CH7							Channel 7 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
I	RW	CH8							Channel 8 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
J	RW	CH9							Channel 9 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
K	RW	CH10							Channel 10 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
L	R/v/	CH11	J.Cui	•					Channel 11 enable clear register. Writing '0' has no effect
-	11.44	C.111	Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
	D	CUAD	Clear	1					Write: disable channel
M	ĸW	CH12	8:-11-1						Channel 12 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
N	RW	CH13							Channel 13 enable clear register. Writing '0' has no effect



Bit r	numbe	er		31 30	29 28	27 26	5 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	ΖY	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value				Description
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
0	RW	CH14						Channel 14 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
Р	RW	CH15						Channel 15 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
Q	RW	CH16						Channel 16 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
R	RW	CH17						Channel 17 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
S	RW	CH18						Channel 18 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
Т	RW	CH19						Channel 19 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
U	RW	CH20						Channel 20 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
V	RW	CH21		_				Channel 21 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
	DIA	CU22	Clear	1				Write: disable channel
W	RW	CH22	D' III I	•				Channel 22 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
V	DVA	CU22	Clear	1				Write: disable channel
Х	KVV	CH23	Disabled	0				Channel 23 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
.,	DIA	CUDA	Clear	1				Write: disable channel
Υ	кW	CH24	Disabled	0				Channel 24 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
7	DIA.	CHIZE	Clear	1				Write: disable channel Channel 25 enable clear register. Writing '0' has no effect.
Z	KW	CH25	Disabled	0				Channel 25 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
		CUDG	Clear	1				Write: disable channel
а	RW	CH26	D: 11 1	•				Channel 26 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
b RW CH27	Channel 27 enable clear register. Writing '0' has no effect
Disabled	0 Read: channel disabled
Enabled	1 Read: channel enabled
Clear	1 Write: disable channel
c RW CH28	Channel 28 enable clear register. Writing '0' has no effect
Disabled	0 Read: channel disabled
Enabled	1 Read: channel enabled
Clear	1 Write: disable channel
d RW CH29	Channel 29 enable clear register. Writing '0' has no effect
Disabled	0 Read: channel disabled
Enabled	1 Read: channel enabled
Clear	1 Write: disable channel
e RW CH30	Channel 30 enable clear register. Writing '0' has no effect
Disabled	0 Read: channel disabled
Enabled	1 Read: channel enabled
Clear	1 Write: disable channel
f RW CH31	Channel 31 enable clear register. Writing '0' has no effect
Disabled	0 Read: channel disabled
Enabled	1 Read: channel enabled
Clear	1 Write: disable channel

22.2.4 CH[0].EEP

Address offset: 0x510

Channel 0 event end-point

Bi	t numl	ber	1		31	30	29	28	27	26	25	24	23	22 :	21 :	20 1	.9 1	8 17	7 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	O .
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ,	4 Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A .	A
R	set 0	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	O
Id	RV	N	Field	Value Id	Va	lue							Des	cri	otio	n																			
Α	RV	Ν	EEP										Poi	ntei	r to	eve	nt i	egis	ter	Ac	ept	ts o	ıly a	add	Ires	ses	to	reg	iste	rs					_

from the Event group.

22.2.5 CH[0].TEP

Address offset: 0x514 Channel 0 task end-point

Bit r	umbe	er		31	30	29	28	27	' 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α	A A
Rese	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	TEP										Ро	inte	r tc	ta	sk re	egis	ter	. A	cce	ots	onl	y ac	ddr	ess	es t	o re	egis	ter	S				
												fro	m t	he '	Tas	k gr	our).																

22.2.6 CH[1].EEP

Address offset: 0x518 Channel 1 event end-point



Bitı	umber		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
Α	RW EEP		Pointer to event register. Accepts only addresses to registers
			from the Event group.

22.2.7 CH[1].TEP

Address offset: 0x51C Channel 1 task end-point

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 1	16 1	15 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	TEP										Poi	nte	r to	tas	k re	egis	ter.	Aco	cept	10 2	nly a	ddr	ess	es t	o re	gis	ters	;				
												fro	m tl	he 1	Tasl	c gr	oup																

22.2.8 CH[2].EEP

Address offset: 0x520

Channel 2 event end-point

Bit r	iumbe	er		31	. 30	29	28	27	26	25	24	23 :	22 2	21 2) 19	18	17	16	15 :	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	А Д	A	Α	Α	Α	Α	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	. A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tion	ı																	
Α	RW	EEP										Poir	nter	to e	ven	t re	giste	er. A	Ассе	pts	only	ado	dres	ses	to i	regi	iste	rs				
																	_															

22.2.9 CH[2].TEP

Address offset: 0x524 Channel 2 task end-point

Bit r	iumbe	er		3	1 30	29	9 2	28 2	7 :	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2	1 0
Id				Α	Α	. A	. A	Α,	Д	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α,	А А
Res	et OxC	0000000		0	0	0	(0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	٧	alue	9							Des	cri	ptic	on																			
Α	RW	TEP											Poi	nte	r to	tas	sk r	egis	ster	. Ac	cep	ots (only	ad ad	dre	sse	s to	o re	gist	ers					
													froi	m tl	he	Tasl	k gr	ou	٥.																

22.2.10 CH[3].EEP

Address offset: 0x528

Channel 3 event end-point

and the state of t	
Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW EEP	Pointer to event register. Accepts only addresses to registers

from the Event group.

22.2.11 CH[3].TEP

Address offset: 0x52C Channel 3 task end-point



Bit r	nur	nbe	r		31	. 30	29	28	3 27	7 26	25	24	23	22	21	20 :	19 1	18 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	L 0
Id					Α	Α	Α	Α	А	A	Α	Α	Α	Α	Α	Α	Α.	A A	4 4	A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	A A
Res	et (0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	R	w	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	R	W	TEP										Ро	inte	r to	tas	k re	gist	er.	Acc	ept	on	ly a	ddr	ess	es t	o re	gis	ters					
													fro	m t	he 1	Гask	gro	oup.																

22.2.12 CH[4].EEP

Address offset: 0x530

Channel 4 event end-point

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 1	16 1	15 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	EEP										Poi	nte	r to	ev	ent	reg	iste	r. A	cce	pts	only	ado	dres	ses	to	reg	iste	rs				
												fro	m tl	he l	Eve	nt g	rou	p.															

22.2.13 CH[4].TEP

Address offset: 0x534 Channel 4 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14 :	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	A A
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	pti	on																			
Α	RW	TEP										Ро	inte	r to	ta:	sk r	egis	ster	. Ac	cep	ts c	only	ad	ldre	esse	es t	o re	gis	ters	S				
												fro	m t	he '	Tas	k gr	ou	э.																

22.2.14 CH[5].EEP

Address offset: 0x538

Channel 5 event end-point

Bitı	iumber		31	30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15 :	14 1	13 1	2 11	. 10	9	8	7	6	5	4	3 2	1	0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	А А	Α	Α	Α	Α	Α.	ΑА	A	Α	Α	Α	Α	Α	Α	Α	A A	Α	Α
Res	et 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	DVA/ Field	Value Id	Va	lue							Des	crip	ntio	n																	
	RW Field	value lu	•••									г																			
Α	RW EEP	value lu												ever	it re	gist	er. A	Acce	epts	onl	y ad	dres	sses	to	regi	iste	ers				

22.2.15 CH[5].TEP

Address offset: 0x53C Channel 5 task end-point

Bit r	numbe	er		31	30	29	28	27 :	26 :	25 :	24	23 2	22 2	1 2	0 19	18	3 17	16	15	14	13	12	11 :	LO	9	8	7	6	5 4	4 3	2	1	0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	А А	Α	Α	Α	Α	Α	Α	Α	Α	A.	Α	Α	Α	Α	A A	4 4	A	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tior	1																		
Α	RW	TEP										Poir	nter	to t	task	reg	iste	r. A	cce	pts	only	y ac	ldre	sse	s to	re	gist	ers					

from the Task group.

22.2.16 CH[6].EEP

Address offset: 0x540

Channel 6 event end-point



Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 1	16 1	15 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	EEP										Poi	nte	r to	ev	ent	reg	iste	r. A	cce	pts	only	ado	dres	ses	to	reg	iste	rs				
												fro	m tl	he l	Eve	nt g	rou	p.															

22.2.17 CH[6].TEP

Address offset: 0x544 Channel 6 task end-point

Bitı	umber		31	30	29	28	3 2	7 26	5 2!	5 24	23	22	21	20	19	18	17	16	15 :	14	13 :	12 :	11 1	.0	9	8	7	6	5	4	3	2 :	1 0
Id			Α	Α	Α	Α	Δ	A	Δ	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α,	Δ.	Α	Α	Α	Α	Α	Α	A	Δ ,	А А
Res	et 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW Field	Value Id	Va	lue							De	scr	ipti	on																			
Α	RW TEP										Pc	int	er to	ta	sk r	egis	ter	. Ac	cep	ots o	nly	ad	dre	sse	s to	o re	gis	ters	5				
											fro	m	the	Tas	k gr	oup).																

22.2.18 CH[7].EEP

Address offset: 0x548

Channel 7 event end-point

Bit r	iumb	er		31	30	29	28	27	26	25	24	23	22	21 :	20 1	9 1	8 1	7 1	.6 1	5 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α ,	A A	Δ ,	Δ ,	A A	\ <i>A</i>	. Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	А
Rese	et Ox	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0 (0) (0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																		
Α	RW	EEP										Poi	inte	r to	eve	nt i	regi	ste	r. A	cce	pts	only	ad a	dres	ses	to	reg	iste	rs				
												fro	m tl	h 0 E	von	+ ~.		_															

22.2.19 CH[7].TEP

Address offset: 0x54C Channel 7 task end-point

Bit nu	ımbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 :	L8 1	7 1	6 1	.5 1	4 1	.3 1	.2 :	11 1	LO	9	8	7	6	5	4	3 2	2 1	0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	Δ ,	4 /	Δ ,	۱ ۸	Δ.	Д	Д	Α	Α	Α	Α	Α	Α	Α	A A	A A	A A
Rese	t 0x0	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 () (0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	TEP										Poi	inte	r to	tas	k re	gist	er.	Acc	ept	s o	nly	ad	dre	sse	s to	o re	gist	ters					
												fro	m t	he 1	Task	gr	nun																	

22.2.20 CH[8].EEP

Address offset: 0x550

Channel 8 event end-point

Bitı	numbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16 :	15 :	14 :	13 1	.2 1	1 10	9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ.	Δ Δ	. A	Α	Α	Α	Α	Α	Α .	Α.	A A	٨
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0)
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	EEP										Poi	nte	r to	eve	ent	reg	iste	er. A	Acce	pts	on	ly a	ddre	esse	s to	re	giste	ers					7

from the Event group.

22.2.21 CH[8].TEP

Address offset: 0x554 Channel 8 task end-point



Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 1	16 1	15 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	TEP										Poi	nte	r to	tas	k re	egis	ter.	Aco	cept	10 2	nly a	ddr	ess	es t	o re	gis	ters	;				
												fro	m tl	he 1	Tasl	c gr	oup																

22.2.22 CH[9].EEP

Address offset: 0x558

Channel 9 event end-point

Bit r	iumbe	er		31	. 30	29	28	27	26	25	24	23	22	21 :	20 :	19 1	18 1	7 1	.6 1	5 1	4 13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ ,	Α Α	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	А
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																		
Α	RW	EEP										Poi	nte	r to	eve	ent	regi	ste	r. A	cce	ots o	nly	add	lres:	ses	to	reg	iste	rs				
												fro	m tl	he E	ver	nt g	rou	٥.															

22.2.23 CH[9].TEP

Address offset: 0x55C Channel 9 task end-point

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	8 17	16	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ <i>A</i>	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α.	Α.	Α	А А	A	Α
Res	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	TEP										Poi	ntei	r to	task	re	giste	er. A	Acce	pts	onl	y ac	ldre	esse	s to	re	gist	ers					
												£	41		ask																		

22.2.24 CH[10].EEP

Address offset: 0x560

Channel 10 event end-point

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 1	18 1	17 :	16 :	15 :	L4 1	3 1	.2 1	.1 1	0 9	9 8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	A ,	Δ.	Δ.	Δ ,	Δ Α	\ A	\ A	. A	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)	0	0 (0) (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	EEP										Poi	nte	r to	eve	ent	reg	iste	r. A	Acce	pts	on	ly a	ddr	ess	es t	o re	gist	ers					
												£	m tl			.+ ~																		

22.2.25 CH[10].TEP

Address offset: 0x564

Channel 10 task end-point

Bit number		31	30	29	28	27	' 26	25	24	23	22	21	20	19	18	17 :	16	15 :	14	13 :	12	11	10	9	8	7	6	5	4	3	2	1	C
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A.	Α.	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ld RW Field	Value Id	Va	lue							De	scri	ptic	on																				
A RW TEP										Ро	inte	r to	tas	sk re	egis	ter.	Ac	сер	ts o	only	ad	ldre	esse	s t	o re	gis	ters	5					

from the Task group.

22.2.26 CH[11].EEP

Address offset: 0x568

Channel 11 event end-point



Bit r	umb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15	14 1	.3 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	A	Α /	А А	Α	Α	Α	Α	Α.	Д Д	A	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Res	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	crip	tio	n																	
Α	RW	EEP										Poi	nter	to	even	t re	gist	er. /	Acce	epts	only	y ad	dres	sses	to	reg	iste	rs				
												fro	m th	ie E	vent	gro	up.															

22.2.27 CH[11].TEP

Address offset: 0x56C

Channel 11 task end-point

Bit r	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21 :	20 :	19 1	18 1	7 1	16 1	5 1	4 1	3 12	11	10	9	8	7	6	5	4	3	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α /	Δ ,	A A	Α Α	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α /	A A	АА
Res	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 () (0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							Des	scri	ptio	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	egist	er.	Acc	ept	10 2	nly a	ddr	ess	es t	o re	egis	ters	5				
												froi	m tl	he T	ask	gro	oup.																

22.2.28 CH[12].EEP

Address offset: 0x570

Channel 12 event end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	3 17	16	15	14	13 :	L2 1	.1 1) 9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	А А	Α	Α	Α	Α	Α	Α	Α.	4 <i>A</i>	. Α	. A	. A	Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	EEP										Poi	nter	to	ever	it re	egist	er.	Acc	epts	on	ly a	ddre	esse	s to	re	gist	ers					7
												fror	n th	e F	vent	gra	nıın																

22.2.29 CH[12].TEP

Address offset: 0x574

Channel 12 task end-point

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16 1	L5 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 A	Α	Α	Α .	A A	4 Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	. A	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW/	Field	Value Id	Va	lue							Dag	crip	tion																		
	11.00	riciu	value lu		··uc							Des	,ci ib	LIUI																		
Α		TEP	value lu		···uc								•		task i	regi	ster	. Ac	cep	ts oı	nly a	ddre	esse	s to	o re	gist	ters	5				

22.2.30 CH[13].EEP

Address offset: 0x578

Channel 13 event end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW EEP		Pointer to event register. Accepts only addresses to registers

from the Event group.

22.2.31 CH[13].TEP

Address offset: 0x57C

Channel 13 task end-point



Bit r	umb	er		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	9 18	3 17	16	15	14	13 3	L2 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	А	Α	Α	Α	Α	A A	Α	Α	Α	Α	Α	Α	Α	A A	A A	A A
Res	et Ox(0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 () (0
Id	RW	Field	Value Id	Va	lue							De	scri	otio	n																	
Α	RW	TEP										Poi	nte	r to	task	reg	iste	r. A	cce	pts	only	ado	dres	ses 1	to r	egis	ters	s				
												fro	m tl	ne T	ask	gro	up.															

22.2.32 CH[14].EEP

Address offset: 0x580

Channel 14 event end-point

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 19	9 18	17	16	15	14	13	12 1	.1 1	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 A	. A	Α	Α	Α	Α	Α	A .	4 Δ	. A	Α	Α	Α	Α	Α	Α	A A	4 А
Res	et 0x	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																	
Α	RW	EEP										Poi	nter	to	ever	nt re	gist	er.	Acc	ept	s on	ly a	ddre	esse	s to	re	gist	ers				

22.2.33 CH[14].TEP

Address offset: 0x584

Channel 14 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	.9 1	l8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ,	A A	A /	A A	. Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Α Α	A А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	TEP										Poi	nter	to	tasl	k re	gist	er.	Acc	ept	on	y a	ddre	sse	s to	re	gist	ers	5				
												froi	n th	ne T	ask	gro	oup.																

22.2.34 CH[15].EEP

Address offset: 0x588

Channel 15 event end-point

Bit	number		31 30 29 2	28 27 26	25 2	24 23	22 21	20 19	18 1	7 16	15	14 13	3 12	11 10	9	8	7	6	5	4	3 2	1	0
Id			A A A A	A A A	A	А А	A A	A A	A A	А А	Α	ΑА	А	A A	Α	Α	Α	Α	Α	Α	A A	Α	Α
Res	et 0x00000000		0 0 0 0	0 0 0	0 (0 0	0 0	0 0	0 (0 0	0	0 0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id	DW 5: 11	Value Id	Value			n-																	
	RW Field	value lu	value			De	script	on															
A	RW EEP	value lu	value				•	on o ever	t regi	ster.	Acc	epts	only	addre	sses	s to	reg	iste	ers				

22.2.35 CH[15].TEP

Address offset: 0x58C

Channel 15 task end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16 :	15 1	14 :	13	12	11 :	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	cri	ptic	n																			
Α	RW	TEP										Poi	nte	r to	tas	k re	egis	ter.	Ac	сер	ts c	only	ad	dre	sse	s to	o re	gis	ters	5				

from the Task group.

22.2.36 CH[16].EEP

Address offset: 0x590

Channel 16 event end-point



Bit r	umb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15	14 1	.3 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	A	Α /	А А	Α	Α	Α	Α	Α.	Д Д	A	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Res	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	crip	tio	n																	
Α	RW	EEP										Poi	nter	to	even	t re	gist	er. /	Acce	epts	only	y ad	dres	sses	to	reg	iste	rs				
												fro	m th	ie E	vent	gro	up.															

22.2.37 CH[16].TEP

Address offset: 0x594

Channel 16 task end-point

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15 :	L4 1	3 12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 A	Α	Α	Α	Α	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	4 A	А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio																		
		riciu											,cp	LiUi	•																	
Α		TEP													task	regi	ster	. Ac	сер	ts o	nly a	ddre	esse	s to	re	gist	ters	s				

22.2.38 CH[17].EEP

Address offset: 0x598

Channel 17 event end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	3 17	16	15	14	13 :	L2 1	.1 1) 9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	А А	Α	Α	Α	Α	Α	Α	Α.	4 <i>A</i>	. Α	. A	. A	Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	EEP										Poi	nter	to	ever	it re	egist	er.	Acc	epts	on	ly a	ddre	esse	s to	re	gist	ers					7
												fror	n th	e F	vent	gra	nıın																

22.2.39 CH[17].TEP

Address offset: 0x59C

Channel 17 task end-point

Bit nu	ımbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 :	L8 1	7 1	6 1	.5 1	4 1	.3 1	.2 :	11 1	LO	9	8	7	6	5	4	3 2	2 1	0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	Δ ,	4 /	Δ ,	۱ ۸	Δ.	Д	Д	Α	Α	Α	Α	Α	Α	Α	A A	A A	A A
Rese	t 0x0	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 () (0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	TEP										Poi	inte	r to	tas	k re	gist	er.	Acc	ept	s o	nly	ad	dre	sse	s to	o re	gist	ters					
												fro	m t	he 1	Task	gr	nun																	

22.2.40 CH[18].EEP

Address offset: 0x5A0

Channel 18 event end-point

au I	
Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW EEP	Pointer to event register. Accepts only addresses to registers

from the Event group.

22.2.41 CH[18].TEP

Address offset: 0x5A4
Channel 18 task end-point



Bit r	numbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 :	16 1	15 1	4 1	3 1	2 1:	10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α ,	Δ ,	Δ Δ	. Α	Α	Α	Α	Α	Α	Α	Α	A	A A	. A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							De	cri	otic	n																		
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter.	Ac	cep	ts o	nly	add	ress	es t	o re	gis	ters	5				

from the Task group.

22.2.42 CH[19].EEP

Address offset: 0x5A8

Channel 19 event end-point

Bit r	numb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	7 16	5 15	14	13	12	11	10	9	8	7	6 !	5 4	1 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 4	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 Α	A A	Α	Α	Α
Res	et 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	EEP										Poi	nter	to	eve	nt r	egis	ter	Ac	cept	ts o	nly	add	res	ses	to r	egi	ster	s				Π
												froi	m th	ne E	ven	t gr	oup	١.															

22.2.43 CH[19].TEP

Address offset: 0x5AC Channel 19 task end-point

Bit	numl	per		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15 1	14 1	13 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	A A	Α	Α	Α	Α	Α.	A A	A	Α	Α	Α	Α	Α	Α	Α	АА	. A	Α
Res	et 0	00000000		0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RV	/ Field	Value Id	Va	lue							Des	crip	tior	1																	
Α	R۱۸	/ TEP										Poi	nter	to t	ask	regi	ster	. Ac	cen	ts c	nlv	bbe	ess	es t	o re	egis	ters	s				
	11.0															-0.					,					0						

22.2.44 CHG[0]

Address offset: 0x800 Channel group 0

		• '																															
Bit nu	ımbe	er		31	30	29	28	27	26	25	24	23 2	2 2	1 20	19	18	3 17	16	15	5 14	13	12	11	10	9	8	7	6	5	4 3	3 2	1	0
Id				f	е	d	С	b	а	Z	Υ	X١	N N	/ U	Т	S	R	Q	Р	0	N	М	L	K	J	L	Н	G	F	Ε [) С	В	Α
Reset	0x0	0000000		0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cript	tion																			
Α	RW	СНО										Incl	ıde	or e	xclı	ude	ch	ann	el ()													
			Excluded	0								Excl	ude																				
			Included	1								Incl	ıde																				
В	RW	CH1										Incl	ıde	or e	xclı	ude	ch	ann	el 1	L													
			Excluded	0								Excl	ude																				
			Included	1								Incl	ıde																				
С	RW	CH2										Incl	ıde	or e	xclı	ude	ch	ann	el 2	2													
			Excluded	0								Excl	ude																				
			Included	1								Incl	ıde																				
D	RW	CH3										Incl	ıde	or e	xclı	ude	ch	ann	el 3	3													
			Excluded	0								Excl	ude																				
			Included	1								Incl	ıde																				
E	RW	CH4										Incl	ıde	or e	xclı	ude	ch	ann	el 4	1													
			Excluded	0								Excl	ude																				
			Included	1								Incl	ıde																				
F	RW	CH5										Incl	ıde	or e	xclı	ude	ch	ann	el 5	5													
			Excluded	0								Excl	ude																				
			Included	1								Incl	ıde																				
G	RW	CH6										Incl	ıde	or e	xclı	ude	ch	ann	el 6	5													



Di+ w	مامس	\-		21 20	20.20	27.20	25.24	12 22 24 2	00 10 1	0 17	16 15	14 12	12 11	10 0	0	7 ,	~ F	1	2 2	1 0
Id	iumbe	er						23 22 21 2 X W V I												
	et OxO	0000000						0 0 0 0												
		Field	Value Id	Value				Description												
			Excluded	0				Exclude												
			Included	1				Include												
Н	RW	CH7						Include or	exclud	e chai	nnel 7									
			Excluded	0				Exclude												
			Included	1				Include												
I	RW	CH8						Include or	exclud	e chai	nnel 8									
			Excluded	0				Exclude												
			Included	1				Include												
J	RW	СН9						Include or	exclud	e chai	nnel 9									
			Excluded	0				Exclude												
			Included	1				Include												
K	RW	CH10						Include or	exclud	e chai	nnel 10	0								
			Excluded	0				Exclude												
	Dist	CU11	Included	1				Include												
L	KW	CH11	Evaluded	0				Include or	exclud	e chai	inel 1	Ţ								
			Excluded Included	0				Exclude Include												
М	D\A/	CH12	included	1				Include or	ovelud	o chai	nnal 1	,								
IVI	I VV	CHIZ	Excluded	0				Exclude	exciuu	e ciiai	illei 1.	2								
			Included	1				Include												
N	RW	CH13	o.uucu	_				Include or	exclud	e chai	nnel 1	3								
			Excluded	0				Exclude												
			Included	1				Include												
0	RW	CH14						Include or	exclud	e chai	nnel 1	4								
			Excluded	0				Exclude												
			Included	1				Include												
Р	RW	CH15						Include or	exclud	e chai	nnel 1	5								
			Excluded	0				Exclude												
			Included	1				Include												
Q	RW	CH16						Include or	exclud	e chai	nnel 1	6								
			Excluded	0				Exclude												
			Included	1				Include												
R	RW	CH17						Include or	exclud	e chai	nnel 1	7								
			Excluded	0				Exclude												
	DIA	CUAO	Included	1				Include				_								
S	KVV	CH18	Evaludad	0				Include or	exclud	e cnai	inei 1	5								
			Excluded Included	1				Exclude Include												
Т	RW	CH19	included	_				Include or	exclud	e chai	nnel 1	9								
			Excluded	0				Exclude												
			Included	1				Include												
U	RW	CH20						Include or	exclud	e chai	nnel 20	0								
			Excluded	0				Exclude												
			Included	1				Include												
V	RW	CH21						Include or	exclud	e chai	nnel 2	1								
			Excluded	0				Exclude												
			Included	1				Include												
W	RW	CH22						Include or	exclud	e chai	nnel 2	2								
			Excluded	0				Exclude												
			Included	1				Include												
X	RW	CH23						Include or	exclud	e chai	nnel 2	3								
			Excluded	0				Exclude												
			Included	1				Include												
Υ	кW	CH24	Frielinde d	0				Include or	exclud	e chai	nnel 2	4								
			Excluded	0				Exclude												



numbe	er		31	30	29	28 2	27 26	25	24	23	22 2	1 2	0 19	9 18	3 17	16	15	14 1	.3 1	2 11	10	9	8 7	΄ ε	5	4	3 2	2 1	. 0
			f	е	d	С	b a	Z	Υ	Χ	W١	νı	J T	S	R	Q	Р	0	N N	1 L	K	J	I F	ı	F	Ε	D (СВ	A
et 0x0	0000000		0	0	0	0	0 0	0	0	0	0 (0 (0 0	0	0	0	0	0	0 0	0	0	0	0 0	0	0	0	0 (0	0
RW	Field	Value Id	Va	lue						Des	scrip	tio	n																
		Included	1							Incl	lude																		
RW	CH25									Incl	lude	or	excl	ude	cha	nne	el 25	;											
		Excluded	0							Exc	lude																		
		Included	1							Incl	lude																		
RW	CH26									Incl	lude	or	excl	ude	cha	nne	el 26	j											
		Excluded	0							Exc	lude																		
		Included	1							Incl	lude																		
RW	CH27									Incl	lude	or	excl	ude	cha	nne	el 27	,											
		Excluded	0							Exc	lude																		
		Included	1							Incl	lude																		
RW	CH28									Incl	lude	or	excl	ude	cha	nne	28	3											
		Excluded	0							Exc	lude																		
		Included	1							Incl	lude																		
RW	CH29									Incl	lude	or	excl	ude	cha	nne	29)											
		Excluded	0							Exc	lude																		
		Included	1							Incl	lude																		
RW	CH30									Incl	lude	or	excl	ude	cha	nne	130)											
		Excluded	0							Exc	lude																		
		Included	1							Incl	lude																		
RW	CH31									Incl	lude	or	excl	ude	cha	nne	el 31												
		Excluded	0							Exc	lude																		
		Included	1							Incl	lude																		
	RW RW RW RW	RW CH25 RW CH26 RW CH27 RW CH28 RW CH29 RW CH30	RW CH25 RW CH25 Excluded Included RW CH26 Excluded Included RW CH27 Excluded Included RW CH27 Excluded Included RW CH28 Excluded Included RW CH29 Excluded Included RW CH30 Excluded Included RW CH30 Excluded Included RW CH31 Excluded	Feet 0x0000000000000000000000000000000000	F e et 0x0000000000000000000000000000000000	F E C C C C C C C C C	F e d c c c c c c c c c	F	F	F R C D C D D D D D D D	F e d c b a Z Y X E E E E E E E E E	F e d c b a Z Y X W N N N N N N N N N	F e d c b a Z Y X W V V V V V V V V V	f e d c b a Z Y X W V U T set 0x00000000000000000000000000000000000	f e d c b a Z Y X W V U T S set 0x00000000000000000000000000000000000	F e d c b a Z Y X W V U T S R	F e d c b a Z Y X W V U T S R Q Q Q Q Q Q Q Q Q	F E D C D D D D D D D D	F e d C b a Z Y X W V U T S R Q P O O O O O O O O O	F R R R R R R R R R	Field Value Id V	Field Value Manual Man	Field Value Id Value Id Value Id Value Id Include OF SECONDO	Field Notice 1000000000000000000000000000000000000	Fine bit one bottom one of the bit of the bit of the bit of the bottom one of the bit of	File	Field Value Id Value Id Value Id Value Id Value Id Included Include Included Include	Field Value Id Value Id Value Id Included 1	Field Value Id Value Id Value Id Value Id Included 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

22.2.45 CHG[1]

Address offset: 0x804

Channel group 1

Bit	numbe	er .		31	30	29	28	27 2	6 2	25 24	4 2	3 2	22 2	1 2	20 1	9 1	8 1	7 1	6 1	5 1.	4 1	3 12	11	10	9	8	7	6	5	4 3	2	1	0
Id													w v																				A
Res	et 0x0	0000000											0 0																				
Id	RW	Field	Value Id	Va	lue						D)es	cript	tio	n																		
Α	RW	CH0									lr	nclı	ude	or	excl	ud	e ch	anı	nel	0													
			Excluded	0							Ε	xcl	lude																				
			Included	1							Ir	nclı	ude																				
В	RW	CH1									lr	nclı	ude	or	excl	ud	e ch	anı	nel	1													
			Excluded	0							Ε	xcl	lude																				
			Included	1							lr	nclı	ude																				
С	RW	CH2									lr	nclı	ude	or	excl	ud	e ch	anı	nel	2													
			Excluded	0							Ε	xcl	lude																				
			Included	1							lr	nclı	ude																				
D	RW	CH3									Ir	nclı	ude	or	excl	ud	e ch	anı	nel	3													
			Excluded	0							Ε	xcl	lude																				
			Included	1							lr	nclı	ude																				
Ε	RW	CH4									Ir	nclı	ude	or	excl	ud	e ch	anı	nel	4													
			Excluded	0							Ε	xcl	lude																				
			Included	1							lr	nclı	ude																				
F	RW	CH5									lr	nclı	ude	or	excl	ud	e ch	anı	nel	5													
			Excluded	0							Ε	xcl	lude																				
			Included	1							lr	nclı	ude																				
G	RW	CH6									Ir	nclı	ude	or	excl	ud	e ch	anı	nel	6													
			Excluded	0							Ε	xcl	lude																				
			Included	1							Ir	nclı	ude																				
Н	RW	CH7									Ir	ncli	ude	or	excl	ud	e ch	anı	nel	7													
			Excluded	0							Ε	xcl	lude																				



Bit n	umbe	er		31 30	29 2	28 27	' 26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id				f e	d	c b	a	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B
Rese	et OxO	0000000		0 0	0	0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			Included	1					Include
I	RW	CH8							Include or exclude channel 8
			Excluded	0					Exclude
			Included	1					Include
J	RW	CH9							Include or exclude channel 9
			Excluded	0					Exclude
			Included	1					Include
K	RW	CH10							Include or exclude channel 10
			Excluded	0					Exclude
			Included	1					Include
L	RW	CH11							Include or exclude channel 11
			Excluded	0					Exclude
			Included	1					Include
М	RW	CH12							Include or exclude channel 12
			Excluded	0					Exclude
			Included	1					Include
N	RW	CH13							Include or exclude channel 13
			Excluded	0					Exclude
			Included	1					Include
0	RW	CH14							Include or exclude channel 14
			Excluded	0					Exclude
_			Included	1					Include
Р	RW	CH15	5 1 1 1						Include or exclude channel 15
			Excluded	0					Exclude
_	DVA	CUAC	Included	1					Include
Q	KVV	CH16	Evaludad	0					Include or exclude channel 16
			Excluded Included	1					Exclude Include
R	D\A/	CH17	iliciadea	1					Include or exclude channel 17
IX.	11.00	CHIT	Excluded	0					Exclude
			Included	1					Include
S	R\M/	CH18	inciducu	-					Include or exclude channel 18
3	11.44	CITIO	Excluded	0					Exclude
			Included	1					Include
Т	RW	CH19	meiadea	-					Include or exclude channel 19
·		CITIS	Excluded	0					Exclude
			Included	1					Include
U	RW	CH20	moladed	-					Include or exclude channel 20
-		-	Excluded	0					Exclude
			Included	1					Include
V	RW	CH21							Include or exclude channel 21
			Excluded	0					Exclude
			Included	1					Include
W	RW	CH22							Include or exclude channel 22
			Excluded	0					Exclude
			Included	1					Include
Х	RW	CH23							Include or exclude channel 23
			Excluded	0					Exclude
			Included	1					Include
Υ	RW	CH24							Include or exclude channel 24
			Excluded	0					Exclude
			Included	1					Include
Z	RW	CH25							Include or exclude channel 25
			Excluded	0					Exclude
			Included	1					Include



Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZY	X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
a RW CH26			Include or exclude channel 26
	Excluded	0	Exclude
	Included	1	Include
b RW CH27			Include or exclude channel 27
	Excluded	0	Exclude
	Included	1	Include
c RW CH28			Include or exclude channel 28
	Excluded	0	Exclude
	Included	1	Include
d RW CH29			Include or exclude channel 29
	Excluded	0	Exclude
	Included	1	Include
e RW CH30			Include or exclude channel 30
	Excluded	0	Exclude
	Included	1	Include
f RW CH31			Include or exclude channel 31
	Excluded	0	Exclude
	Included	1	Include

22.2.46 CHG[2]

Address offset: 0x808 Channel group 2

Bit nu	umbe	r		31	30	29	28	27	26	25	24	- 23	3 22	2 2:	1 2	0 1	9 1	.8 1	7 1	.6 1	.5	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (
Id																																			B A
Rese	t 0x0	0000000																																	0 (
Id	RW	Field	Value Id	Va	lue							De	esc	ript	tioi	n																			
Α	RW	СН0										In	clu	de (or (exc	lud	e cl	nan	nel	0														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
В	RW	CH1										In	clu	de (or (exc	lud	e cl	nan	nel	1														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
С	RW	CH2										In	clu	de (or (exc	lud	e cl	nan	nel	2														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
D	RW	CH3										In	clu	de (or (exc	lud	e cl	nan	nel	3														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
Ε	RW	CH4										In	clu	de (or (exc	lud	e cl	nan	nel	4														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
F	RW	CH5										In	clu	de (or (exc	lud	e cl	nan	nel	5														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
G	RW	CH6										In	clu	de (or	exc	lud	e cl	nan	nel	6														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					
Н	RW	CH7												de (or (exc	lud	e cl	nan	nel	7														
			Excluded	0								Ex	clu	ıde																					
			Included	1									clu																						
I	RW	CH8												de (or (exc	lud	e cl	nan	nel	8														
			Excluded	0								Ex	clu	ıde																					
			Included	1								In	clu	de																					



Bit r	numbe	er		31 30	29 28	3 27	26 2	25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									'XWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x0	0000000		0 0	0 0	0	0	0 0	
Id	RW	Field	Value Id	Value					Description
J	RW	CH9							Include or exclude channel 9
			Excluded	0					Exclude
			Included	1					Include
K	RW	CH10							Include or exclude channel 10
			Excluded	0					Exclude
			Included	1					Include
L	RW	CH11							Include or exclude channel 11
			Excluded	0					Exclude
			Included	1					Include
М	RW	CH12							Include or exclude channel 12
			Excluded	0					Exclude
			Included	1					Include
N	RW	CH13							Include or exclude channel 13
			Excluded	0					Exclude
			Included	1					Include
0	RW	CH14							Include or exclude channel 14
			Excluded	0					Exclude
_			Included	1					Include
Р	RW	CH15		_					Include or exclude channel 15
			Excluded	0					Exclude
			Included	1					Include
Q	RW	CH16	5 1 1 1	•					Include or exclude channel 16
			Excluded	0					Exclude
В	D\A/	CU17	Included	1					Include Include or exclude channel 17
R	KVV	CH17	Evaludad	0					Exclude
			Excluded Included	1					Include
S	D\A/	CH18	included	1					Include or exclude channel 18
3	NVV	CHIO	Excluded	0					Exclude
			Included	1					Include
Т	RW	CH19	included	_					Include or exclude channel 19
•		CITES	Excluded	0					Exclude
			Included	1					Include
U	RW	CH20	molacca	-					Include or exclude channel 20
_			Excluded	0					Exclude
			Included	1					Include
V	RW	CH21							Include or exclude channel 21
			Excluded	0					Exclude
			Included	1					Include
W	RW	CH22							Include or exclude channel 22
			Excluded	0					Exclude
			Included	1					Include
Χ	RW	CH23							Include or exclude channel 23
			Excluded	0					Exclude
			Included	1					Include
Υ	RW	CH24							Include or exclude channel 24
			Excluded	0					Exclude
			Included	1					Include
Z	RW	CH25							Include or exclude channel 25
			Excluded	0					Exclude
			Included	1					Include
a	RW	CH26							Include or exclude channel 26
			Excluded	0					Exclude
			Included	1					Include
b	RW	CH27							Include or exclude channel 27



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZY	'XWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Excluded	0	Exclude
	Included	1	Include
c RW CH28			Include or exclude channel 28
	Excluded	0	Exclude
	Included	1	Include
d RW CH29			Include or exclude channel 29
	Excluded	0	Exclude
	Included	1	Include
e RW CH30			Include or exclude channel 30
	Excluded	0	Exclude
	Included	1	Include
f RW CH31			Include or exclude channel 31
	Excluded	0	Exclude
	Included	1	Include

22.2.47 CHG[3]

Address offset: 0x80C

Channel group 3

Bit r	numbe	er		31 30	29	28 2	7 26	25 2	4 2	23 22 21	20 19	9 1	8 17	16	15	14 1	3 1	2 11	10	9	8	7 6	5 5	4	3	2	1 0
Id										x w v																	
	et OxO	0000000								0 0 0																	
Id		Field	Value Id	Value						Descript																	
A		CH0								nclude c		ude	cha	nne	0 اء												
			Excluded	0						xclude																	
			Included	1					1	nclude																	
В	RW	CH1							-1	nclude c	or excl	ude	cha	nne	1 1												
			Excluded	0						xclude																	
			Included	1						nclude																	
С	RW	CH2		=						nclude c	or excl	ude	cha	nne	12												
Ū		52	Excluded	0						xclude	, chei																
			Included	1						nclude																	
D	RW	CH3		_						nclude c	or excl	ude	cha	nne	13												
		3 5	Excluded	0						xclude	, che.				5												
			Included	1						nclude																	
E	RW	CH4	meradea	-						nclude c	or excl	ude	cha	nne	14												
_			Excluded	0						xclude	, chei																
			Included	1						nclude																	
F	RW	CH5		_						nclude c	or excl	ude	cha	nne	15												
·		3 5	Excluded	0						xclude	, che.				5												
			Included	1						nclude																	
G	RW	CH6	moracca	-						nclude c	or excl	ude	cha	nne	16												
Ū		00	Excluded	0						xclude	, chei				0												
			Included	1						nclude																	
Н	RW	CH7		_						nclude c	or excl	ude	cha	nne	17												
••		· · · ·	Excluded	0						xclude	, che.																
			Included	1						nclude																	
	RW	CH8	moracca	-						nclude c	or excl	ude	cha	nne	18												
•			Excluded	0						xclude	. CACI	auc			0												
			Included	1						nclude																	
J	R\M/	CH9	meradeu	•						nclude o	nr excl	ude	cha	nne	19												
,	11.00	Citis	Excluded	0						xclude	, CACI	uuc	CITC														
			Included	1						nclude																	
K	D\A/	CH10	meruucu	1						nclude nclude c	or ovel	uda	cha	nna	110												
K	L/AA	CHILO							1	iiciuue C	n excl	uue	LII	111116	: I T(,											



Bit r	numbe	er		31 30	29 28	27 26	25 24	22 21 20 19 18 17 16	15 14 13	12 11	10 9	8 7	6	5 4	3 2	1 0
Id				f e	d c	b a	Z Y	W V U T S R Q	P O N	M L	K J	ΙH	G	F E	D C	ВА
Res	et OxC	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0	0 0 0	0 0	0 0	0 0	0	0 0	0 0	0 0
Id	RW	Field	Value Id	Value				escription								
			Excluded	0				clude								
			Included	1				clude								
L	RW	CH11						clude or exclude channe	l 11							
			Excluded	0				clude								
			Included	1				clude								
М	RW	CH12		0				clude or exclude channe	l 12							
			Excluded Included	0				clude clude								
N	R\M	CH13	iliciadea	1				clude clude or exclude channe	l 13							
14	11.00	CHIS	Excluded	0				clude	113							
			Included	1				clude								
0	RW	CH14		_				clude or exclude channe	l 14							
			Excluded	0				clude								
			Included	1				clude								
Р	RW	CH15						clude or exclude channe	l 15							
			Excluded	0				clude								
			Included	1				clude								
Q	RW	CH16						clude or exclude channe	l 16							
			Excluded	0				clude								
			Included	1				clude								
R	RW	CH17						clude or exclude channe	l 17							
			Excluded	0				clude								
			Included	1				clude								
S	RW	CH18		_				clude or exclude channe	l 18							
			Excluded	0				clude								
_	DIA	CU10	Included	1				clude clude or exclude channe	110							
Т	KVV	CH19	Excluded	0				clude or exclude channe	119							
			Included	1				clude								
U	RW	CH20	meidded	_				clude or exclude channe	120							
			Excluded	0				clude								
			Included	1				clude								
V	RW	CH21						clude or exclude channe	l 21							
			Excluded	0				clude								
			Included	1				clude								
W	RW	CH22						clude or exclude channe	l 22							
			Excluded	0				clude								
			Included	1				clude								
Χ	RW	CH23						clude or exclude channe	l 23							
			Excluded	0				clude								
			Included	1				clude								
Υ	RW	CH24	Finding	0				clude or exclude channe	1 24							
			Excluded	0				clude								
7	DIA	CHIZE	Included	1				clude	125							
Z	KW	CH25	Excluded	0				clude or exclude channe clude	1 25							
			Included	1				clude clude								
a	RW	CH26	meiaucu	1				clude clude or exclude channe	126							
u			Excluded	0				clude of exclude challine	. =-							
			Included	1				clude								
b	RW	CH27						clude or exclude channe	l 27							
			Excluded	0				clude								
			Included	1				clude								
С	RW	CH28						clude or exclude channe	l 28							
			Excluded	0				clude								



Bit	numbe	er		31	30	29 2	28 2	27 2	26 2	5 2	4 2	3 22	21	20	19	18	17	16	15 :	14 1	.3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id				f	e	d	С	b	a Z	<u>7</u> '	Y X	W	٧	U	Т	S	R	Q	Р	0 1	N M	L	K	J	1	Н	G	F E	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Val	lue						D	escri	ptic	on																		
			Included	1							In	clud	e																			
d	RW	CH29		Include or exclude channel 29 0 Exclude																												
			Excluded																													
			Included	1							In	clud	e																			
e	RW	CH30									In	clud	e oı	ex	cluc	de c	har	ne	I 30													
			Excluded	0							E	clud	le																			
			Included	1							In	clud	e																			
f	RW	CH31									In	clud	e oı	ex	cluc	de c	har	ne	l 31													
			Excluded	0							E	clud	le																			
			Included	1							In	clud	e																			

22.2.48 CHG[4]

Address offset: 0x810 Channel group 4

011	uili	iei group 4																										
Bit	numb	er		31 30	29 2	28 2	7 26	25 2	24 :	23 22 2:	L 20	19 1	L8 1	7 1	5 15	5 14	13	12 3	11 1	0 9	8	7	6	5	4 3	3 2	1	0
Id				f e	d	c k	о а	Z	Υ	x w v	U	Т	S	R C	Q P	0	Ν	М	L k	J	1	Н	G	F	E [) C	В	Α
Res	et 0x(0000000		0 0	0	0 (0	0	0	0 0 0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0
Id	RW	Field	Value Id	Value	•				ı	Descript	ion																	
Α	RW	CH0							ı	Include	or ex	clud	e cl	nanr	el ()												
			Excluded	0					ı	Exclude																		
			Included	1					ı	Include																		
В	RW	CH1							ı	Include	or ex	clud	e cl	nanr	el :	L												
			Excluded	0					- 1	Exclude																		
			Included	1					- 1	Include																		
С	RW	CH2							-	Include	or ex	clud	e cl	nanr	iel 2	2												
			Excluded	0					١	Exclude																		
			Included	1					-	Include																		
D	RW	CH3							- 1	Include	or ex	clud	e cl	nanr	iel 3	3												
			Excluded	0					- 1	Exclude																		
			Included	1					- 1	Include																		
E	RW	CH4								Include	or ex	clud	e cl	nanr	el 4	1												
			Excluded	0						Exclude																		
			Included	1						Include																		
F	RW	CH5								Include	or ex	clud	e cl	nanr	iel 5	5												
			Excluded	0						Exclude																		
	5111	0115	Included	1						Include																		
G	RW	CH6								Include	or ex	clud	e cl	nanr	iel 6	Ó												
			Excluded	0						Exclude																		
Н	DIA	CUZ	Included	1						Include Include		اد ، ، اد	1		-1-	,												
П	KVV	CH7	Excluded	0						Exclude	л ех	ciuu	e ci	Idili	iei .	′												
			Included	1						Include																		
1	R\M	CH8	iliciuded	1						Include	or ev	clud	اء م	nanr	ا م	2												
•	11.00	CHO	Excluded	0						Exclude	JI CA	ciuu	C Ci	iaiii	ici	,												
			Included	1						Include																		
J	RW	CH9		-						Include	or exc	clud	e cl	nanr	el 9)												
			Excluded	0						Exclude																		
			Included	1						Include																		
K	RW	CH10								Include	or ex	clud	e cl	nanr	nel :	LO												
			Excluded	0					ı	Exclude																		
			Included	1					ı	Include																		
L	RW	CH11								Include	or exc	clud	e cl	nanr	el :	l1												
			Excluded	0					ı	Exclude																		



Bit n	umbe	er		31 30	29 2	28 27	26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id				f e	d	c b	a	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B
Rese	et OxO	0000000		0 0	0	0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			Included	1					Include
M	RW	CH12							Include or exclude channel 12
			Excluded	0					Exclude
			Included	1					Include
N	RW	CH13							Include or exclude channel 13
			Excluded	0					Exclude
_			Included	1					Include
0	RW	CH14							Include or exclude channel 14
			Excluded	0					Exclude
	DV4	CUAS	Included	1					Include
Р	KVV	CH15	Evaludad	0					Include or exclude channel 15
			Excluded Included	0					Exclude Include
Q	D\A/	CH16	incidded	1					Include or exclude channel 16
Q	NVV	CHIO	Excluded	0					Exclude of exclude charmer 16
			Included	1					Include
R	D\A/	CH17	iliciadea	1					Include or exclude channel 17
N	NVV	CHIZ	Excluded	0					Exclude of exclude charmer 17
			Included	1					Include
S	RW/	CH18	meidaea	-					Include or exclude channel 18
,		CITIO	Excluded	0					Exclude
			Included	1					Include
Т	RW	CH19		_					Include or exclude channel 19
			Excluded	0					Exclude
			Included	1					Include
U	RW	CH20							Include or exclude channel 20
			Excluded	0					Exclude
			Included	1					Include
٧	RW	CH21							Include or exclude channel 21
			Excluded	0					Exclude
			Included	1					Include
W	RW	CH22							Include or exclude channel 22
			Excluded	0					Exclude
			Included	1					Include
Χ	RW	CH23							Include or exclude channel 23
			Excluded	0					Exclude
			Included	1					Include
Υ	RW	CH24							Include or exclude channel 24
			Excluded	0					Exclude
			Included	1					Include
Z	RW	CH25							Include or exclude channel 25
			Excluded	0					Exclude
			Included	1					Include
а	RW	CH26							Include or exclude channel 26
			Excluded	0					Exclude
			Included	1					Include
b	RW	CH27							Include or exclude channel 27
			Excluded	0					Exclude
			Included	1					Include
С	RW	CH28							Include or exclude channel 28
			Excluded	0					Exclude
		0.100	Included	1					Include
d	RW	CH29	5 1 1 1						Include or exclude channel 29
			Excluded	0					Exclude
			Included	1					Include



Bit	numbe	er		31	30 2	29	28 2	27	26 2	5 2	24 2	3 2	2 21	L 20	19	18	17	16	15 1	.4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				f	e	d	С	b	a Z	7	Υ)	< V	V V	U	Т	S	R	Q	Р	о I	N N	1 L	K	J	1	Н	G	F	Е	D C	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 ()	0 (0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						D	esc	ript	ion																		
е	RW	CH30									lr	nclu	de d	or ex	xclu	de (char	nne	I 30													
			Excluded	0							Е	xclı	ıde																			
			Included	1							Ir	nclu	de																			
f	RW	CH31									lr	nclu	de d	or ex	xclu	de (char	nne	l 31													
			Excluded	0							Е	xclı	ıde																			
			Included	1							Ir	nclu	de																			

22.2.49 CHG[5]

Address offset: 0x814
Channel group 5

Section Sect	Ch	ann	el group 5																										
No No No No No No No No	Bit r	numb	er		31 3	30 2	9 28 2	27 26	25 2	4 2	3 22 2	1 20	19	18	17 1	L6 1	.5 1	4 1	3 12	11	10	9 8	3 7	6	5	4	3	2 :	1 0
No. Field Value Value Description Include or exclude channel O Exclude O Exclude O Exclude O Exclude O O Exclude O O O O O O O O O	Id				f	e d	d c	b a	ΖY	Y >	x w v	v U	Т	S	R	Q I	Р (1 C	I M	L	K	J	Н	G	F	Ε	D	C E	3 A
A RW Propertion End of the process of t	Res	et 0x0	0000000		0	0 (0 0	0 0	0 (0	0 0	0 0	0	0	0	0 (0 (0 (0	0	0	0 (0	0	0	0	0	0 (0 (
B RW RW RH CEN Unded 0 Exclude or exclude channel 1 B RW RW RH CEN Unded 0 Exclude or exclude channel 1 B RW RW RH CEN Unded 0 Exclude or exclude channel 2 CW RW RH CASA Excluded 0 Exclude or exclude channel 2 CW RW RH CHA Excluded 0 Exclude or exclude channel 3 CW RW RH CHA Excluded 0 Description CW RW RH CHA Excluded 0 Description CW RW RH CHA Excluded 0 Description F RW RW RH CHA Excluded 0 Description RW RW RH Excluded 0 Exclude	Id	RW	Field	Value Id	Valu	ıe				D	escrip	tion																	
	Α	RW	CH0							Ir	nclude	or e	xclud	de c	han	nel	0												
B RW b CH1 place Excluded 0 place Excluded C place RW place 1 place Included place C place Excluded place 1 place Include place D place RW place Excluded place 1 place D place Excluded place 1 place Exclude D place Excluded place 1 place Ex				Excluded	0					E	xclude																		
C RW Processed From Processe				Included	1					Ir	nclude																		
	В	RW	CH1							Ir	nclude	or e	xclud	de c	han	nel	1												
C RV CH2 Excluded 0 Exclude D RV CH3 Included 1 Include D RV CH3 Excluded 0 Exclude Included 1 Include or exclude channel 3 Included 1 Include Included 1 Include Excluded 0 Exclude Included 1 Include Included 1 Include Included 2 Exclude Included 1 Include Include 1 Include Include 1 Include or exclude channel 5 Include 1 Include or exclude channel 6 Include 1 Include or exclude channel 7 Include 1 Include or exclude channel 7 Include 1 Include or exclude channel 8 Include 1 Include or exclude channel 8 Include 1 Include or exclude channel 9				Excluded	0					E	xclude																		
				Included	1					Ir	nclude																		
Note	С	RW	CH2							Ir	nclude	or e	xclud	de c	han	nel	2												
D RW CH3 Excluded 0 Exclude E RW CH4 Excluded 0 Exclude E RW CH4 Excluded 0 Exclude E RW CH4 Excluded 0 Exclude F RW CH5 Excluded 0 Exclude G RW CH5 Excluded 0 Exclude G RW CH6 Excluded 0 Exclude G RW CH6 Excluded 0 Exclude G RW CH4 Excluded 0 Exclude G RW CH4 Excluded 0 Exclude G RW CH4 Excluded 0 Exclude G Excluded 0 Exclude Exclude G Excluded 0 Exclude Exclude G Excluded Exclude Exclude G </td <td></td> <td></td> <td></td> <td>Excluded</td> <td>0</td> <td></td> <td></td> <td></td> <td></td> <td>E</td> <td>xclude</td> <td></td>				Excluded	0					E	xclude																		
Excluded 0 Exclude E RW CH4 Excluded 1 Include or exclude channel 4 E RW CH4 Excluded 0 Exclude B Excluded 1 Include F RW CH5 Excluded 0 Exclude G RW CH6 Excluded 0 Exclude G RW CH6 Excluded 0 Exclude G RW CH7 Excluded 0 Exclude G RW CH7 Excluded 0 Exclude G RW CH4 Excluded 0 Exclude G RW CH4 Excluded 0 Exclude G Excluded 0 Exclude Include or exclude channel 8 F Excluded 0 Exclude Include or exclude channel 9 G Excluded 0 Exclude Include or exclude channel 10 G				Included	1					Ir	nclude																		
RW	D	RW	CH3							Ir	nclude	or e	xclu	de c	han	nel	3												
Fig. Ref				Excluded	0					E	xclude																		
Key Excluded 0 Exclude F RW ABS Excluded 0 Include G RW ABS Excluded 0 Exclude G RW ABS Excluded 0 Include G RW ABS Excluded 0 Exclude G RW ABS Excluded 0 Include G RW ABS Include Include G RW ABS Include Include G <				Included	1					Ir	nclude																		
For any series of the control of the	E	RW	CH4							Ir	nclude	or e	xclud	de c	han	nel	4												
Fig. RW Reference Face				Excluded	0					E	xclude																		
Figure F				Included	1					Ir	nclude																		
Record R	F	RW	CH5							Ir	nclude	or e	xclud	de c	han	nel	5												
Figure F				Excluded	0					E	xclude																		
Excluded 0 1 10 10 10 10 10 10 10 10 10 10 10 10				Included	1					Ir	nclude																		
House the second	G	RW	CH6							Ir	nclude	or e	xclud	de c	han	nel	6												
He RW RW RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC				Excluded	0					E	xclude																		
Excluded 0 Exclude 1 Include 1 Include 1 Include 0 Inclu				Included	1					Ir	nclude																		
Included Included Include Include Include Include Include Include Channel 8 Excluded 0 Exclude Exclude Include Include Channel 9 Excluded 0 Include Channel 9 Excluded 0 Exclude Exclude Channel 9 Excluded 0 Exclude Include Include Include Channel 10 Excluded 0 Exclude Include Channel 10 Excluded 0 Exclude Include Channel 10 Excluded 0 Include Include Channel 10 Excluded 0 Exclude Include Channel 10 Excluded 0 Exclude Include Channel 10 Excluded 0 Exclude Include Channel 10 Exclude Channel 10	Н	RW	CH7							Ir	nclude	or e	xclud	de c	han	nel	7												
Include or exclude channel 8 Excluded 0 Exclude Included 1 Include or exclude channel 9 Exclude channel 9 Exclude channel 9 Excluded 0 Exclude channel 9 Excluded 1 Include or exclude channel 9 Excluded 1 Include Included 1 Include Exclude channel 10 Exclude channel 10 Exclude channel 10 Exclude included 1 Include Included 1 Include Included 1 Include Exclude channel 10 Include or exclude channel 11 Excluded 1 Include or exclude channel 11 Exclude or exclude channel 11 Exclude or exclude channel 11 Exclude or exclude channel 12				Excluded	0					E	xclude																		
Excluded 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				Included	1					Ir	nclude																		
Included 1 Include 1 Include 1 Include 1 Include 1 Include 1 Include channel 9 Excluded 0 Exclude 1 Include 1 Include 1 Include Channel 10 Excluded 0 Exclude channel 10 Excluded 0 Exclude Channel 10 Excluded 1 Include Or exclude channel 10 Exclude 1 Include	1	RW	CH8							Ir	nclude	or e	xclud	de c	han	nel	8												
Include or exclude channel 9 Excluded 0 Exclude Included 1 Include or exclude channel 10 Excluded 0 Exclude or exclude channel 10 Excluded 0 Exclude or exclude channel 10 Excluded 1 Include Include or exclude channel 10 Include or exclude channel 11 Include or exclude channel 12				Excluded	0					E	xclude																		
Excluded 0 Exclude Exc				Included	1					Ir	nclude																		
K RW CH10 Excluded 0 Exclude L RW CH11 Included 1 Include L RW CH11 Excluded 0 Exclude Include or exclude channel 11 Include or exclude channel 11 Included 1 Include Include Include Include Include or exclude channel 12 Include or exclude channel 12 Excluded 0 Exclude	J	RW	CH9							Ir	nclude	or e	xclud	de c	han	nel	9												
K RW CH10 Excluded 0 Exclude L RW CH11 Included 1 Include L RW CH11 Excluded 0 Exclude Include 1 Include M RW CH12 Included 1 Include or exclude channel 12 Excluded 0 Exclude Include or exclude channel 12 Excluded 0 Exclude				Excluded	0					E	xclude																		
Excluded 0 Exclude Included 1 Include Include or exclude channel 11 Excluded Excluded 0 Exclude Include Include Include Include Include Include Exclude Include or exclude channel 12 Excluded 0 Exclude				Included	1					Ir	nclude																		
L RW CH11 Excluded 0 Exclude B Excluded 0 Exclude Included 1 Include M RW CH12 Excluded 0 Exclude or exclude channel 12 Excluded 0 Exclude	K	RW	CH10							Ir	nclude	or e	xclud	de c	han	nel	10												
L RW CH11 Excluded 0 Exclude Included 1 Include M RW CH12 Included Include or exclude channel 12 Excluded 0 Exclude				Excluded	0					E	xclude																		
Excluded 0 Exclude Included 1 Include M RW CH12 Include or exclude channel 12 Excluded 0 Exclude				Included	1					Ir	nclude																		
M RW CH12 Included 1 Include Excluded 0 Exclude	L	RW	CH11							Ir	nclude	or e	xclud	de c	han	nel	11												
M RW CH12 Include or exclude channel 12 Excluded 0 Exclude				Excluded	0					E	xclude																		
Excluded 0 Exclude				Included	1					Ir	nclude																		
	М	RW	CH12							Ir	nclude	or e	xclu	de c	han	nel	12												
Included 1 Include				Excluded	0					E	xclude																		
				Included	1					Ir	nclude																		



Bit n	numbe	er		31 30	29 28	27	26.2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
	et 0x0	0000000							0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
N	RW	CH13							Include or exclude channel 13
			Excluded	0					Exclude
			Included	1					Include
0	RW	CH14							Include or exclude channel 14
			Excluded	0					Exclude
			Included	1					Include
Р	RW	CH15							Include or exclude channel 15
			Excluded	0					Exclude
			Included	1					Include
Q	RW	CH16							Include or exclude channel 16
			Excluded	0					Exclude
			Included	1					Include
R	RW	CH17							Include or exclude channel 17
			Excluded	0					Exclude
			Included	1					Include
S	RW	CH18							Include or exclude channel 18
			Excluded	0					Exclude
			Included	1					Include
Т	RW	CH19							Include or exclude channel 19
			Excluded	0					Exclude
			Included	1					Include
U	RW	CH20							Include or exclude channel 20
			Excluded	0					Exclude
			Included	1					Include
V	RW	CH21							Include or exclude channel 21
			Excluded	0					Exclude
			Included	1					Include
W	RW	CH22		_					Include or exclude channel 22
			Excluded	0					Exclude
.,	D14/	CU22	Included	1					Include
Х	RW	CH23	Final radia d	0					Include or exclude channel 23
			Excluded	0					Exclude
V	D\A/	CH24	Included	1					Include
Υ	KVV	CH24	Excluded	0					Include or exclude channel 24 Exclude
			Included	1					Include
Z	D\A/	CH25	iliciadea						Include or exclude channel 25
_	IVVV	CHZS	Excluded	0					Exclude Exclude
			Included	1					Include
a	RW/	CH26	meidaea	_					Include or exclude channel 26
u			Excluded	0					Exclude Exclude
			Included	1					Include
b	RW	CH27		_					Include or exclude channel 27
			Excluded	0					Exclude
			Included	1					Include
С	RW	CH28							Include or exclude channel 28
-		-	Excluded	0					Exclude
			Included	1					Include
d	RW	CH29							Include or exclude channel 29
			Excluded	0					Exclude
			Included	1					Include
e	RW	CH30							Include or exclude channel 30
			Excluded	0					Exclude
			Included	1					Include
f	RW	CH31							Include or exclude channel 31



Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcb	a Z Y X W V U T S F	R Q P O N M L K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description	
Id RW Field	Value Id Excluded	Value 0	Description Exclude	

22.2.50 FORK[0].TEP

Address offset: 0x910 Channel 0 task end-point

Bi	t nı	ımbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	LO	9	8	7	6	5	4	3	2 :	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α	A A	А А
Re	ese	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id		RW	Field	Value Id	Va	lue							De	scri	ptio	on																			
Α		RW	TFP										Poi	nte	r to	ta:	sk re	عوام	ter																

22.2.51 FORK[1].TEP

Address offset: 0x914 Channel 1 task end-point

Bitı	num	bei	r			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id						Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Ĺ
Res	et O	x00	000000			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	RV	٧	Field	Value Id		Va	lue							De	scri	ptic	on																				ı
Α	RV	٧	TEP		Pointer to										tas	sk re	egis	ter																			

22.2.52 FORK[2].TEP

Address offset: 0x918 Channel 2 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17	16	15	14	13 1	12 1	.1 1	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	4 Δ	Α	Α	Α	Α	Α	Α	Α	A A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter															

22.2.53 FORK[3].TEP

Address offset: 0x91C Channel 3 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α,	А А	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				ı
Α	RW	TEP										Poi	nte	er to	ta	sk r	egis	ter																	1

22.2.54 FORK[4].TEP

Address offset: 0x920 Channel 4 task end-point



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$
Id RW Field Value Id	Value Description
A RW TEP	Pointer to task register

22.2.55 FORK[5].TEP

Address offset: 0x924 Channel 5 task end-point

Bit number		31 30	29 2	28 2	27 2	26 2	25 2	24 2	3 2	22 2	1 2	0 19	9 18	3 17	16	15	14	13	12	11 :	LO	9	8	7	6	5	4	3 2	2 1	0
Id		А А	Α	Α	Α	A	Α.	Α	Δ,	A A	Δ ,	4 Α	. A	A	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	A A	A A	A
Reset 0x00000000		0 0	0	0	0	0	0	0	0 (0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id RW Field	Value Id	Value)es	crip	tio	n																		
A RW TEP								F	oin	iter	to 1	task	reg	iste	r															

22.2.56 FORK[6].TEP

Address offset: 0x928 Channel 6 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 1	.3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ ,	A A	A A	Α	Α	Α	Α	Α	Α	A A	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	otic	on																		
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter															

22.2.57 FORK[7].TEP

Address offset: 0x92C Channel 7 task end-point

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (j
Id	RW	Field	Value Id	Va	lue							De	scri	iptio	on																				ı
Α	RW	TEP										Ро	inte	er to	ta	sk r	egi	ster																	7

22.2.58 FORK[8].TEP

Address offset: 0x930 Channel 8 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.59 FORK[9].TEP

Address offset: 0x934 Channel 9 task end-point

Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2 :	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Α Α	А А
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
ld RW Field	Value Id	Va	lue							De	scri	ptic	on																			

A RW TEP Pointer to task register



22.2.60 FORK[10].TEP

Address offset: 0x938

Channel 10 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21	20 :	19 :	18 :	17 :	16 1	15 :	14 1	.3 1	12 1	1 1	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ.	Α ,	4 Α	A	Α	Α	Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otic	n																		
Α	RW	TEP										Poi	nter	r to	tas	k re	egis	ter															

22.2.61 FORK[11].TEP

Address offset: 0x93C

Channel 11 task end-point

Bitı	num	bei	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Ĺ
Res	et O	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	RV	٧	Field	Value Id	Va	lue							De	scri	ptic	on																				ı
Α	RV	٧	TEP										Poi	nte	r to	tas	sk re	egis	ter																	

22.2.62 FORK[12].TEP

Address offset: 0x940

Channel 12 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	17 1	16 1	L5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α.	A .	Δ ,	Δ Α	A A	Δ Δ	Α	Α	Α	Α	Α	Α	Α	Α.	АА
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	egist	ter															

22.2.63 FORK[13].TEP

Address offset: 0x944

Channel 13 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.64 FORK[14].TEP

Address offset: 0x948

Channel 14 task end-point

Bit number		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2 1	1 0	
ld		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	4 A	
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	
ld RW Field	Value Id	Va	lue							De	scri	ptic	on																				
A RW TFP										Pο	inte	r to	ta	sk re	pis	ter																	

22.2.65 FORK[15].TEP

Address offset: 0x94C

Channel 15 task end-point



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW TEP	Pointer to task register

22.2.66 FORK[16].TEP

Address offset: 0x950

Channel 16 task end-point

Bit	nu	mbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	А А
Re	set	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	ı	RW	Field	Value Id	Va	lue							De	scr	ipti	on																			
Α	- 1	RW	TEP										Ро	inte	er to	ta	sk r	egis	ster																

22.2.67 FORK[17].TEP

Address offset: 0x954

Channel 17 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.68 FORK[18].TEP

Address offset: 0x958

Channel 18 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	ı
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	ı
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	on																				l
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter																	1

22.2.69 FORK[19].TEP

Address offset: 0x95C

Channel 19 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.70 FORK[20].TEP

Address offset: 0x960

Channel 20 task end-point

Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 :	.0	9	8	7	6	5	4	3 2	2 1	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ.	A .	Α.	Α	Α	Α	Α	A A	A 4	A A
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 (
ld RW Field	Value Id	Va	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0										on																			

A RW TEP Pointer to task register



22.2.71 FORK[21].TEP

Address offset: 0x964

Channel 21 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	17 :	16 1	15 1	14 1	13 1	.2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α.	Α.	Α.	Α.	Δ,	Δ Δ	Α	Α	Α	Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	gist	ter															

22.2.72 FORK[22].TEP

Address offset: 0x968

Channel 22 task end-point

Bit n	مامسا	0.0		21	20	20	20	27	20	25	24	22	22	21	20	10	10	17	10	1 [11	12	12	11	10	0	0	7	_	г	1	2	.	1 0
DIL II	umb	er		31	30	29	28	21	20	25	24	23	22	21	20	19	10	1/	10	12	14	13	12	11	10	9	٥	/	О	Э	4	3	۷.	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	А А
Rese	t Ox(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	on																			
Α	RW	TEP										Pο	inte	r to	ta:	sk r	egis	ter																

22.2.73 FORK[23].TEP

Address offset: 0x96C

Channel 23 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.74 FORK[24].TEP

Address offset: 0x970

Channel 24 task end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	! 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A		4 A
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter																

22.2.75 FORK[25].TEP

Address offset: 0x974

Channel 25 task end-point

Bit number		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2 1	1 0	
ld		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	4 A	
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	
ld RW Field	Value Id	Va	lue							De	scri	ptic	on																				
A RW TFP										Pο	inte	r to	ta	sk re	pis	ter																	

22.2.76 FORK[26].TEP

Address offset: 0x978

Channel 26 task end-point



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$
Id RW Field Value Id	Value Description
A RW TEP	Pointer to task register

22.2.77 FORK[27].TEP

Address offset: 0x97C

Channel 27 task end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13	12	11 1	0 9) ;	3 7	7 (5 5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	A 4	۱ ۱	A /	١,	Δ Α	A	Α	Α	Α .	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0) (0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	TEP										Poi	inte	r to	ta	sk re	egis	ter																7

22.2.78 FORK[28].TEP

Address offset: 0x980

Channel 28 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 :	21	20 :	19	18	17	16 :	15 :	14 1	13 :	L2 1	11 1	0 9	9 8	3 7	' 6	5 5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Α Α	Α /	A 4	A A	. Δ	A	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0) (0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	crip	otic	n																			
Α	RW	TEP										Poi	ntei	r to	tas	k re	egis	ter																

22.2.79 FORK[29].TEP

Address offset: 0x984

Channel 29 task end-point

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19 1	18 1	17 1	16 1	L5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1)
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α,	A A	Δ ,	Α Α	۸ ۸	A A	Α	Α	Α	Α	Α	Α	Α .	Δ,	A	Δ
Res	et 0x	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 () () (0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Val	ue							Des	cri	otic	n																			
Α	RW	TEP										Poi	nte	r to	tas	k re	gist	ter																7

22.2.80 FORK[30].TEP

Address offset: 0x988

Channel 30 task end-point

Bit num	nber		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 1	16 1	15 1	14 1	13 1	.2 1	.1 10	9	8	7	6	5	4	3	2	1 0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α.	Δ,	4 А	A	Α	Α	Α	Α	Α	Α	Α	АА
Reset 0	x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id R\	W Field	Value Id	Va	lue							De	scri	ptic	on																		
A R\	W TEP										Poi	nte	r to	tas	k re	egis	ter															

22.2.81 FORK[31].TEP

Address offset: 0x98C

Channel 31 task end-point

Bit number	31 30 29	29 28 27 26 25 24 2	23 22 21 20 19 18	8 17 16 15 14 13 12 11 1	10 9 8 7 6 5 4 3 2 1 0
Id	A A A	A A A A A A	A A A A A		A A A A A A A A A
Reset 0x00000000	0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value	ld Value	ı	Description		

A RW TEP Pointer to task register





23 RADIO — 2.4 GHz Radio

The RADIO contains a 2.4 GHz radio receiver and a 2.4 GHz radio transmitter that is compatible with Nordic's proprietary 1 Mbps and 2 Mbps radio modes in addition to 1 Mbps and 2 Mbps *Bluetooth*® low energy mode.

EasyDMA in combination with an automated packet assembler and packet disassembler, and an automated CRC generator and CRC checker, makes it very easy to configure and use the RADIO. See *Figure 29: RADIO block diagram* on page 205 for details.

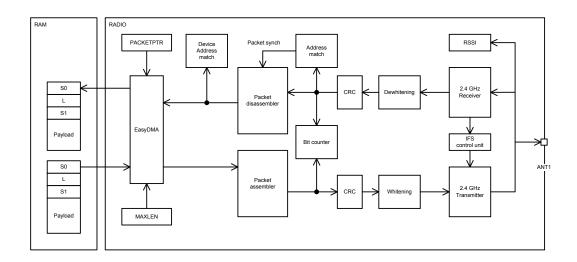


Figure 29: RADIO block diagram

The RADIO includes a Device Address Match unit and an interframe spacing control unit that can be utilized to simplify address white listing and interframe spacing respectively, in *Bluetooth* Smart and similar applications.

The RADIO also includes a Received Signal Strength Indicator (RSSI) and a bit counter. The bit counter generates events when a preconfigured number of bits have been sent or received by the RADIO.

23.1 EasyDMA

The RADIO use EasyDMA for reading and writing of data packets from and to the RAM without CPU involvement.

As illustrated in *Figure 29: RADIO block diagram* on page 205, the RADIO's EasyDMA utilizes the same PACKETPTR for receiving and transmitting packets. The CPU should reconfigure this pointer every time before the RADIO is started via the START task.

The structure of a radio packet is described in detail in *Packet configuration* on page 206. The data that is stored in Data RAM and transported by EasyDMA consists of S0, LENGTH, S1, the payload itself, and a static add-on sent immediately after the payload.

The size of each of the above elements in the frame is configurable (see *Packet configuration* on page 206), and the space occupied in RAM depends on these settings. A size of zero is possible for any of the fields, it is up to the user to make sure that the resulting frame complies with the RF protocol chosen.

For the field sizes defined in bits, the occupation in RAM will always be rounded up to the next full byte size (for instance 3 bit length will allocate 1 byte in RAM, 9 bit length will allocate 2 bytes, etc.).



In addition, the S0INCL field in PCNF0 determines if S0 is present in RAM at all if its length is zero. If present, one byte is allocated in RAM.

The size of S0 is configured through the S0LEN field in PCNF0. The size of LENGTH is configured through the LFLEN field in PCNF0. The size of S1 is configured through the S1LEN field in PCNF0. The size of the payload is configured through the value in RAM corresponding to the LENGTH field. The size of the static add-on to the payload is configured through the STATLEN field in PCNF1.

The MAXLEN field in the PCNF1 register configures the maximum packet payload plus add-on size in number of bytes that can be transmitted or received by the RADIO. This feature can be used to ensure that the RADIO does not overwrite, or read beyond, the RAM assigned to the packet payload. This means that if the packet payload length defined by PCNF1.STATLEN and the LENGTH field in the packet specifies a packet larger than MAXLEN, the payload will be truncated at MAXLEN.

Note that MAXLEN includes the payload and the add-on, but excludes the size occupied by the S0, LENGTH and S1 fields. This has to be taken into account when allocating RAM.

If the payload plus add-on length is specified larger than MAXLEN, the RADIO will still transmit or receive in the same way as before except the payload is now truncated to MAXLEN. The packet's LENGTH field will not be altered when the payload is truncated. The RADIO will calculate CRC as if the packet length is equal to MAXLEN.

If the PACKETPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

The DISABLED event indicates that the EasyDMA has finished accessing the RAM.

23.2 Packet configuration

A Radio packet contains the following fields: PREAMBLE, ADDRESS, S0, LENGTH, S1, PAYLOAD and CRC.

See *Figure 30: On-air packet layout* on page 206. Not shown in the figure is the static payload add-on (the length of which is defined in STATLEN, and which is 0 bytes long in a standard BLE packet), and would be sent between PAYLOAD and CRC. The Radio sends the different fields in the packet in the order they are illustrated below, from left to right. The preamble will be sent least significant bit first on-air.

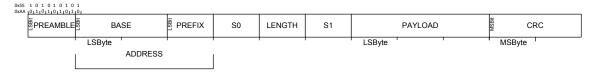


Figure 30: On-air packet layout

For all modes, except for 2 Mbit/s Bluetooth Low Energy mode, the preamble is one byte long. For 2 Mbit/s Bluetooth Low Energy mode the preamble is 2 bytes long. If the first bit of the ADDRESS is 0 the preamble will be set to 0xAA otherwise the PREAMBLE will be set to 0x55.

Radio packets are stored in memory inside instances of a radio packet data structure as illustrated in *Figure 31: In-RAM representation of radio packet, S0, LENGTH and S1 are optional* on page 206. The PREAMBLE, ADDRESS and CRC fields are omitted in this data structure.



Figure 31: In-RAM representation of radio packet, S0, LENGTH and S1 are optional



The byte ordering on air is always Least Significant Byte First for the ADDRESS and PAYLOAD fields and Most Significant Byte First for the CRC field. The ADDRESS fields are always transmitted and received least significant bit first on-air. The CRC field is always transmitted and received Most Significant Bit first. The bit-endian, i.e. which order the bits are sent and received in, of the S0, LENGTH, S1 and PAYLOAD fields can be configured via the ENDIAN in PCNF1.

The S0INCL field in PCNF0 determines if S0 is present in RAM at all if its length is zero. If present, one byte is allocated in RAM.

The sizes of the S0, LENGTH and S1 fields can be individually configured via S0LEN, LFLEN and S1LEN in PCNF0 respectively. If any of these fields are configured to be less than 8 bit long the, the least significant bits of the fields, as seen from the RAM representation, are used.

If S0, LENGTH or S1 are specified with zero length their fields will be omitted in memory, otherwise each field will be represented as a separate byte, regardless of the number of bits in their on-air counterpart.

23.3 Maximum packet length

Independent of the configuration of MAXLEN, the combined length of S0, LENGTH, S1 and PAYLOAD cannot exceed 258 bytes.

23.4 Address configuration

The on-air radio ADDRESS field is composed of two parts, the base address field and the address prefix field.

The size of the base address field is configurable via BALEN in PCNF1. The base address is truncated from LSByte if the BALEN is less than 4. See *Table 38: Definition of logical addresses* on page 207.

The on-air addresses are defined in the BASEn and PREFIXn registers, and it is only when writing these registers the user will have to relate to actual on-air addresses. For other radio address registers such as the TXADDRESS, RXADDRESSES and RXMATCH registers, logical radio addresses ranging from 0 to 7 are being used. The relationship between the on-air radio addresses and the logical addresses is described in *Table 38: Definition of logical addresses* on page 207.

Table 38: Definition of logical addresses

Logical address	Base address	Prefix byte
0	BASE0	PREFIXO.APO
1	BASE1	PREFIXO.AP1
2	BASE1	PREFIXO.AP2
3	BASE1	PREFIXO.AP3
4	BASE1	PREFIX1.AP4
5	BASE1	PREFIX1.AP5
6	BASE1	PREFIX1.AP6
7	BASE1	PREFIX1.AP7

23.5 Data whitening

The RADIO is able to do packet whitening and de-whitening.

See WHITEEN in PCNF1 register for how to enable whitening. When enabled, whitening and de-whitening will be handled by the RADIO automatically as packets are sent and received.

The whitening word is generated using polynomial $g(D) = D^7 + D^4 + 1$, which then is XORed with the data packet that is to be whitened, or de-whitened. See the figure below.



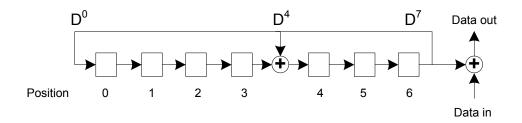


Figure 32: Data whitening and de-whitening

Whitening and de-whitening will be performed over the whole packet (except for the preamble and the address field).

The linear feedback shift register, illustrated in *Figure 32: Data whitening and de-whitening* on page 208 can be initialised via the DATAWHITEIV register.

23.6 CRC

The CRC generator in the RADIO calculates the CRC over the whole packet excluding the preamble. If desirable, the address field can be excluded from the CRC calculation as well

See CRCCNF register for more information.

The CRC polynomial is configurable as illustrated in *Figure 33: CRC generation of an n bit CRC* on page 208 where bit 0 in the CRCPOLY register corresponds to X⁰ and bit 1 corresponds to X¹ etc. See CRCPOLY for more information.

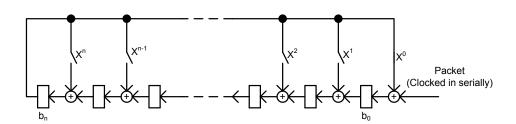


Figure 33: CRC generation of an n bit CRC

As illustrated in *Figure 33: CRC generation of an n bit CRC* on page 208, the CRC is calculated by feeding the packet serially through the CRC generator. Before the packet is clocked through the CRC generator, the CRC generator's latches b_0 through b_n will be initialized with a predefined value specified in the CRCINIT register. When the whole packet is clocked through the CRC generator, latches b_0 through b_n will hold the resulting CRC. This value will be used by the RADIO during both transmission and reception but it is not available to be read by the CPU at any time. A received CRC can however be read by the CPU via the RXCRC register independent of whether or not it has passed the CRC check.

The length (n) of the CRC is configurable, see CRCCNF for more information.

After the whole packet including the CRC has been received, the RADIO will generate a CRCOK event if no CRC errors were detected, or alternatively generate a CRCERROR event if CRC errors were detected.



The status of the CRC check can be read from the CRCSTATUS register after a packet has been received.

23.7 Radio states

The RADIO can enter a number of states.

The RADIO can enter the states described the table below. An overview state diagram for the RADIO is illustrated in *Figure 34: Radio states* on page 209. This figure shows how the tasks and events relate to the RADIO's operation. The RADIO does not prevent a task from being triggered from the wrong state. If a task is triggered from the wrong state, for example if the RXEN task is triggered from the RXDISABLE state, this may lead to incorrect behaviour. As illustrated in *Figure 34: Radio states* on page 209, the PAYLOAD event is always generated even if the payload is zero.

Table 39: RADIO state diagram

State	Description
DISABLED	No operations are going on inside the radio and the power consumption is at a minimum
RXRU	The radio is ramping up and preparing for reception
RXIDLE	The radio is ready for reception to start
RX	Reception has been started and the addresses enabled in the RXADDRESSES register are being monitored
TXRU	The radio is ramping up and preparing for transmission
TXIDLE	The radio is ready for transmission to start
TX	The radio is transmitting a packet
RXDISABLE	The radio is disabling the receiver
TXDISABLE	The radio is disabling the transmitter

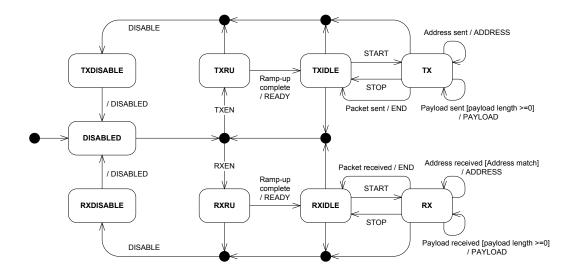


Figure 34: Radio states

23.8 Transmit sequence

Before the RADIO is able to transmit a packet, it must first ramp-up in TX mode.

See TXRU in *Figure 34: Radio states* on page 209 and *Figure 35: Transmit sequence* on page 210. A TXRU ramp-up sequence is initiated when the TXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet transmission can be initiate. A packet transmission is initiated by triggering the START task. As illustrated in *Figure 34: Radio states* on page 209 the START task can first be triggered after the RADIO has entered into the TXIDLE state.

Figure 35: Transmit sequence on page 210 illustrates a single packet transmission where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay caused by CPU execution is expected between READY and START, and between END and DISABLE. As illustrated in Figure 35: Transmit sequence on page 210



the RADIO will by default transmit '1's between READY and START, and between END and DISABLED. What is transmitted can be programmed through the DTX field in the MODECNF0 register.

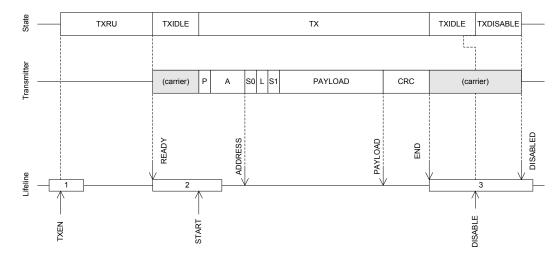


Figure 35: Transmit sequence

A slightly modified version of the transmit sequence from *Figure 35: Transmit sequence* on page 210 is illustrated in *Figure 36: Transmit sequence using shortcuts to avoid delays* on page 210 where the RADIO is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.

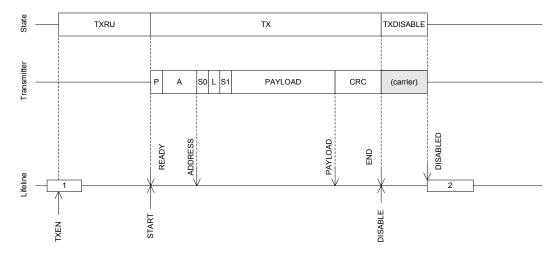


Figure 36: Transmit sequence using shortcuts to avoid delays

The RADIO is able to send multiple packets one after the other without having to disable and re-enable the RADIO between packets, this is illustrated in *Figure 37: Transmission of multiple packets* on page 211.



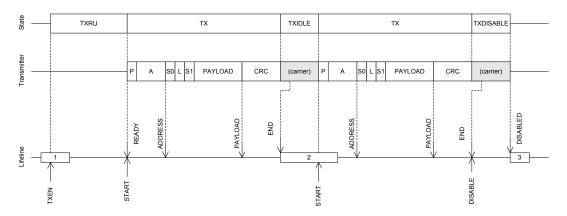


Figure 37: Transmission of multiple packets

23.9 Receive sequence

Before the RADIO is able to receive a packet, it must first ramp up in RX mode

See RXRU in *Figure 34: Radio states* on page 209 and *Figure 38: Receive sequence* on page 211. An RXRU ramp-up sequence is initiated when the RXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet reception can be initiated. A packet reception is initiated by triggering the START task. As illustrated in *Figure 34: Radio states* on page 209 the START task can, first be triggered after the RADIO has entered into the RXIDLE state.

Figure 38: Receive sequence on page 211 illustrates a single packet reception where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay, caused by CPU execution, is expected between READY and START, and between END and DISABLE. As illustrated Figure 38: Receive sequence on page 211 the RADIO will be listening and possibly receiving undefined data, illustrated with an 'X', from START and until a packet with valid preamble (P) is received.

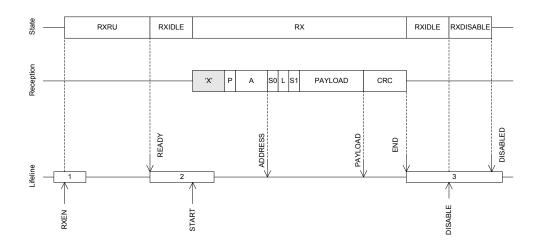


Figure 38: Receive sequence

A slightly modified version of the receive sequence from *Figure 38: Receive sequence* on page 211 is illustrated in *Figure 39: Receive sequence using shortcuts to avoid delays* on page 212 where the the RADIO is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.



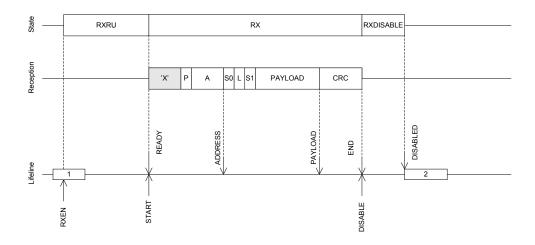


Figure 39: Receive sequence using shortcuts to avoid delays

The RADIO is able to receive multiple packets one after the other without having to disable and re-enable the RADIO between packets, this is illustrated *Figure 40: Reception of multiple packets* on page 212.

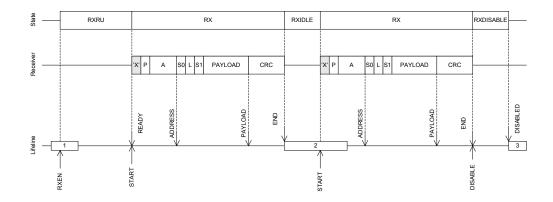


Figure 40: Reception of multiple packets

23.10 Received Signal Strength Indicator (RSSI)

The radio implements a mechanism for measuring the power in the received radio signal. This feature is called Received Signal Strength Indicator (RSSI).

Sampling of the received signal strength is started by using the RSSISTART task. The sample can be read from the RSSISAMPLE register.

The sample period of the RSSI is defined by RSSI_{PERIOD}, see the device product specification for details. The RSSI sample will hold the average received signal strength during this sample period.

For the RSSI sample to be valid the radio has to be enabled in receive mode (RXEN task) and the reception has to be started (READY event followed by START task).

23.11 Interframe spacing

Interframe spacing is the time interval between two consecutive packets.

It is defined as the time, in micro seconds, from the end of the last bit of the previous packet received and to the start of the first bit of the subsequent packet that is transmitted. The RADIO is able to enforce this



interval as specified in the TIFS register as long as TIFS is not specified to be shorter than the RADIO's turnaround time, i.e. the time needed to switch off the receiver, and switch back on the transmitter.

TIFS is only enforced if END_DISABLE and DISABLED_TXEN or END_DISABLE and DISABLED_RXEN shortcuts are enabled. TIFS is only qualified for use in BLE_1MBIT mode, and default ramp-up mode.

23.12 Device address match

The device address match feature is tailored for address white listing in a Bluetooth Smart and similar implementations.

This feature enables on-the-fly device address matching while receiving a packet on air. This feature only works in receive mode and as long as RADIO is configured for little endian, see PCNF1.ENDIAN.

The Device Address match unit assumes that the 48 first bits of the payload is the device address and that bit number 6 in S0 is the TxAdd bit. See the Bluetooth Core Specification for more information about device addresses, TxAdd and whitelisting.

The RADIO is able to listen for eight different device addresses at the same time. These addresses are specified in a DAB/DAP register pair, one pair per address, in addition to a TxAdd bit configured in the DACNF register. The DAB register specifies the 32 least significant bits of the device address, while the DAP register specifies the 16 most significant bits of the device address.

Each of the device addresses can be individually included or excluded from the matching mechanism. This is configured in the DACNF register.

23.13 Bit counter

The RADIO implements a simple counter that can be configured to generate an event after a specific number of bits have been transmitted or received.

By using shortcuts, this counter can be started from different events generated by the RADIO and hence count relative to these.

The bit counter is started by triggering the BCSTART task, and stopped by triggering the BCSTOP task. A BCMATCH event will be generated when the bit counter has counted the number of bits specified in the BCC register. The bit counter will continue to count bits until the DISABLED event is generated or until the BCSTOP task is triggered. The CPU can therefore, after a BCMATCH event, reconfigure the BCC value for new BCMATCH events within the same packet.

The bit counter can only be started after the RADIO has received the ADDRESS event.

The bit counter will stop and reset on BCSTOP, STOP, END and DISABLE tasks.

The figure below illustrates how the bit counter can be used to generate a BCMATCH event in the beginning of the packet payload, and again generate a second BCMATCH event after sending 2 bytes (16 bits) of the payload.



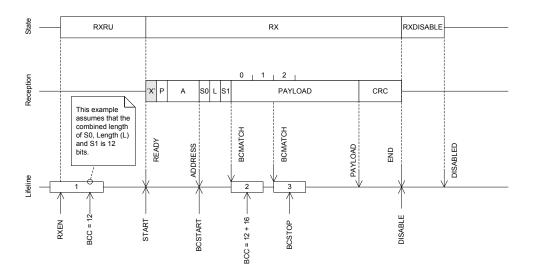


Figure 41: Bit counter example

23.14 Registers

Table 40: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40001000	RADIO	RADIO	2.4 GHz radio		

Table 41: Register Overview

Register	Offset	Description
TASKS_TXEN	0x000	Enable RADIO in TX mode
TASKS RXEN	0x000	Enable RADIO in RX mode
_		
TASKS_START	0x008	Start RADIO
TASKS_STOP	0x00C	Stop RADIO
TASKS_DISABLE	0x010	Disable RADIO
TASKS_RSSISTART	0x014	Start the RSSI and take one single sample of the receive signal strength.
TASKS_RSSISTOP	0x018	Stop the RSSI measurement
TASKS_BCSTART	0x01C	Start the bit counter
TASKS_BCSTOP	0x020	Stop the bit counter
EVENTS_READY	0x100	RADIO has ramped up and is ready to be started
EVENTS_ADDRESS	0x104	Address sent or received
EVENTS_PAYLOAD	0x108	Packet payload sent or received
EVENTS_END	0x10C	Packet sent or received
EVENTS_DISABLED	0x110	RADIO has been disabled
EVENTS_DEVMATCH	0x114	A device address match occurred on the last received packet
EVENTS_DEVMISS	0x118	No device address match occurred on the last received packet
EVENTS_RSSIEND	0x11C	Sampling of receive signal strength complete.
EVENTS_BCMATCH	0x128	Bit counter reached bit count value.
EVENTS_CRCOK	0x130	Packet received with CRC ok
EVENTS_CRCERROR	0x134	Packet received with CRC error
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CRCSTATUS	0x400	CRC status
RXMATCH	0x408	Received address
RXCRC	0x40C	CRC field of previously received packet



Register	Offset	Description	
DAI	0x410	Device address match index	
PACKETPTR	0x504	Packet pointer	
FREQUENCY	0x508	Frequency	
TXPOWER	0x50C	Output power	
MODE	0x510	Data rate and modulation	
PCNF0	0x514	Packet configuration register 0	
PCNF1	0x518	Packet configuration register 1	
BASE0	0x51C	Base address 0	
BASE1	0x520	Base address 1	
PREFIXO	0x524	Prefixes bytes for logical addresses 0-3	
PREFIX1	0x528	Prefixes bytes for logical addresses 4-7	
TXADDRESS	0x52C	Transmit address select	
RXADDRESSES	0x530	Receive address select	
CRCCNF	0x534	CRC configuration	
CRCPOLY	0x538	CRC polynomial	
CRCINIT	0x53C	CRC initial value	
	0x540		Reserved
TIFS	0x544	Inter Frame Spacing in us	
RSSISAMPLE	0x548	RSSI sample	
STATE	0x550	Current radio state	
DATAWHITEIV	0x554	Data whitening initial value	
BCC	0x560	Bit counter compare	
DAB[0]	0x600	Device address base segment 0	
DAB[1]	0x604	Device address base segment 1	
DAB[2]	0x608	Device address base segment 2	
DAB[3]	0x60C	Device address base segment 3	
DAB[4]	0x610	Device address base segment 4	
DAB[5]	0x614	Device address base segment 5	
DAB[6]	0x618	Device address base segment 6	
DAB[7]	0x61C	Device address base segment 7	
DAP[0]	0x620	Device address prefix 0	
DAP[1]	0x624	Device address prefix 1	
DAP[2]	0x628	Device address prefix 2	
DAP[3]	0x62C	Device address prefix 3	
DAP[4]	0x630	Device address prefix 4	
DAP[5]	0x634	Device address prefix 5	
DAP[6]	0x638	Device address prefix 6	
DAP[7]	0x63C	Device address prefix 7	
DACNF	0x640	Device address match configuration	
MODECNF0	0x650	Radio mode configuration register 0	
POWER	0xFFC	Peripheral power control	

23.14.1 SHORTS

Address offset: 0x200

Shortcut register

Bit r	numbe	er		33	1 30	29	2	8 27	7 2	6 2	5 2	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																												Н		G	F	Ε	D	С	ВА
Res	et OxC	0000000		0	0	0	0	0) (0 ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue								Des	scri	ipti	on																			
Α	RW	READY_START										:	Sho	orto	cut l	betv	we	en	RE/	ΝDΥ	eve	ent	and	tS t	AR	T ta	sk								
												:	See	E۱	VEN	TS_	RE	AD	Y aı	nd i	TAS	KS_	STA	ART											
			Disabled	0									Disa	abl	le sł	nort	tcu	t																	
			Enabled	1									Ena	able	e sh	ort	cut	:																	
В	RW	END_DISABLE											Sho	orto	cut l	betv	we	en	ENI) ev	en'	t an	d D	ISA	BLE	E tas	sk								
													See	E١	VEN	TS_	ΕN	ID a	nd	TA.	SKS	_DI	SAE	BLE											



Bit	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				H G F E D C B A
Res	set 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
С	RW DISABLED_TXEN			Shortcut between DISABLED event and TXEN task
				See EVENTS_DISABLED and TASKS_TXEN
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
D	RW DISABLED_RXEN			Shortcut between DISABLED event and RXEN task
				See EVENTS_DISABLED and TASKS_RXEN
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
Ε	RW ADDRESS_RSSISTART			Shortcut between ADDRESS event and RSSISTART task
				See EVENTS_ADDRESS and TASKS_RSSISTART
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
F	RW END_START			Shortcut between END event and START task
				See EVENTS_END and TASKS_START
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
G	RW ADDRESS_BCSTART			Shortcut between ADDRESS event and BCSTART task
				See EVENTS_ADDRESS and TASKS_BCSTART
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
Н	RW DISABLED_RSSISTOP			Shortcut between DISABLED event and RSSISTOP task
				See EVENTS_DISABLED and TASKS_RSSISTOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut

23.14.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			LK I HGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW READY			Write '1' to Enable interrupt for READY event
			See EVENTS_READY
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW ADDRESS			Write '1' to Enable interrupt for ADDRESS event
			See EVENTS_ADDRESS
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW PAYLOAD			Write '1' to Enable interrupt for PAYLOAD event
			See EVENTS_PAYLOAD
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW END			Write '1' to Enable interrupt for END event



Bitı	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				LK I HGFEDCBA
Res	set 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
				See EVENTS_END
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Е	RW DISABLED			Write '1' to Enable interrupt for DISABLED event
				See EVENTS_DISABLED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW DEVMATCH			Write '1' to Enable interrupt for DEVMATCH event
				See EVENTS DEVIMATELY
		Cot	1	See EVENTS_DEVMATCH Enable
		Set Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW DEVMISS	Lilabica	1	Write '1' to Enable interrupt for DEVMISS event
Ü	NW BEVIVISS			
				See EVENTS_DEVMISS
		Set	1	Enable
		Disabled	0	Read: Disabled
	DW DCCIEND	Enabled	1	Read: Enabled
Н	RW RSSIEND			Write '1' to Enable interrupt for RSSIEND event
				See EVENTS_RSSIEND
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
I	RW BCMATCH			Write '1' to Enable interrupt for BCMATCH event
				See EVENTS_BCMATCH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
K	RW CRCOK			Write '1' to Enable interrupt for CRCOK event
				See EVENTS_CRCOK
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
L	RW CRCERROR			Write '1' to Enable interrupt for CRCERROR event
				See EVENTS_CRCERROR
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

23.14.3 INTENCLR

Address offset: 0x308 Disable interrupt

Bit no	umbe	r		31	30	29	28	27	26	25	24	23	22 :	21 2	20 :	19 1	18 :	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	L 0
Id																						L	K		L			Н	G	F	Е	D	С В	3 A
Rese	t 0x0(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			
Α	RW	READY										Wri	te '	1' to	o Di	isab	le i	inte	erru	ıpt	for	RE	AD۱	ev (ent									
												See	EV	EN7	'S_1	REA	DΥ																	
			Clear	1								Disa	ble	:																				
	ld Rese Id	ld Reset 0x00 Id RW	Reset 0x00000000 Id RW Field	Reset 0x000000000 Id RW Field Value Id A RW READY	Reset 0x00000000	Reset 0x00000000 0 0 0 Id RW Field Value Id Value A RW READY	Reset 0x00000000 0 0 0 0 Id RW Field Value Id Value A RW READY	Reset 0x00000000	L Reset 0x00000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0	L K Reset 0x00000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0	L K Reset 0x00000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Reset 0x000000000	Reset 0x000000000	Reset 0x000000000 0 0 0 0 0 0 0 0 0 0 0 0 0	Reset 0x000000000																			



Bitı	numb	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					LK I HGFEDCBA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	ADDRESS			Write '1' to Disable interrupt for ADDRESS event
					See EVENTS_ADDRESS
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	PAYLOAD			Write '1' to Disable interrupt for PAYLOAD event
					See EVENTS_PAYLOAD
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	END			Write '1' to Disable interrupt for END event
					See EVENTS_END
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Ε	RW	DISABLED			Write '1' to Disable interrupt for DISABLED event
					See EVENTS_DISABLED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	DEVMATCH			Write '1' to Disable interrupt for DEVMATCH event
					See EVENTS_DEVMATCH
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	DEVMISS			Write '1' to Disable interrupt for DEVMISS event
					See EVENTS_DEVMISS
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	RSSIEND			Write '1' to Disable interrupt for RSSIEND event
					See EVENTS_RSSIEND
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
I	RW	BCMATCH			Write '1' to Disable interrupt for BCMATCH event
					See EVENTS_BCMATCH
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
K	RW	CRCOK			Write '1' to Disable interrupt for CRCOK event
					See EVENTS_CRCOK
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
L	RW	CRCERROR			Write '1' to Disable interrupt for CRCERROR event
					See EVENTS_CRCERROR
			Clear	1	Disable
			Disabled	0	Read: Disabled



Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16 15	5 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0
Id				L K I	HGFEDCBA
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0000000	00000000
Id RW Field	Value Id	Value	Description		
	Fnabled	1	Read: Enabled		

23.14.4 CRCSTATUS

Address offset: 0x400

CRC status

Bit	numbe	er		31 30	29	28	27	26	25 2	24 2	23 2	2 2	1 20	19	18	17	16	15	14 1	.3 1	2 11	10	9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Value	•						Des	crip	tion																		
Α	R	CRCSTATUS								(CRC	sta	tus	of p	acke	et re	cei	/ed													
			CRCError	0						F	Pack	et r	rece	ived	l wit	th C	RC 6	erro	r												
			CRCOk	1						F	Pack	et r	rece	ived	l wit	th C	RC (ok													

23.14.5 RXMATCH

Address offset: 0x408 Received address

Bitı	numbe	er		31	30	29	28	27	26	25 :	24	23 :	22 :	21 2	20 1	L9 1	8 1	17 1	16 1	15 :	14 :	13 1	2 1	1 10	9	8	7	6	5	4	3	2	1 ()
Id																																Α	Α ,	Ą
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 ()
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			ı
Α	R	RXMATCH										Rec	eive	ed a	ıddı	ress	;																	_

Logical address of which previous packet was received

23.14.6 RXCRC

Address offset: 0x40C

CRC field of previously received packet

Bit r	numbe	er		3	1 30	29	28	8 2	7 26	5 2	5 24	1 23	22	2 21	. 20) 19	18	17	16	15	14	13	12 1	11 1	.0 9	9 1	8	7	6	5	4	3	2	1 0
Id												Α	Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α ,	Δ Α	Α,	Α	Α	Α	Α	Α	Α /	Δ.	4 А
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0	0	0	0	0	0 (0	0 0
ld	RW	Field	Value Id	V	alue	е						De	SC	ripti	ion																			
A	RW R	RXCRC	Value Id	V	alue	е										pre	vio	usly	red	eiv	ed p	oacl	æt											

23.14.7 DAI

Address offset: 0x410

Device address match index

it number	31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
I		A A A
eset 0x00000000	0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
RW Field Value Id	Value	Description
R DAI		Device address match index

Index (n) of device address, see $\mathsf{DAB}[n]$ and $\mathsf{DAP}[n]$, that got an address match.

23.14.8 PACKETPTR

Address offset: 0x504



Packet pointer

Bit	numbe	er		33	1 30	29	9 28	8 27	7 26	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14 1	13 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	A	. Α	A A	A	A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 Α	A A	Α	Α	Α	Α	Α	Α	A	Δ.	АА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	е						De	escr	ipti	on																		
Α	RW	PACKETPTR										Pa	cke	t po	oint	er																	
												Pa	icke	et ac	ddre	ess t	to b	e u	sed	for	the	nex	kt tr	ansr	niss	ion	or						
												re	сер	tion	1. W	/her	n tr	ansı	nit	ting	, th	e pa	cke	t po	inte	d to	by	thi	is				
												ad	ldre	ess v	vill	be t	ran	smi	tte	d ar	nd v	vher	ı re	ceivi	ng,	the	rec	eiv	ed				
												pa	icke	t w	ill b	e w	ritt	en t	o t	his a	addı	ress	. Th	is ac	ldre	ss is	a l	byte	e				
												ali	igne	ed ra	am	add	res	s.															

23.14.9 FREQUENCY

Address offset: 0x508

Frequency

Bit r	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10 !	9	8 7	' 6	5	4	3	2	1 0
Id																											В	Δ	A	Α	Α	Α	А А
Res	et OxO	0000002		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	1 0
Id	RW	Field	Value Id	Va	alue)						De	scri	ipti	on																		
Α	RW	FREQUENCY		[0)10	00]						Ra	dio	cha	nne	el fr	equ	uen	су														
												Fre	equ	enc	y =	240	00 +	FR	EQI	JEN	ICY	(M	Hz)										
В	RW	MAP										Ch	ann	nel r	map	se	lect	ion															
			Default	0								Ch	ann	nel r	map	be	twe	een	24	00 1	ИΗ	Z	250	00 N	lHz								
												Fre	equ	enc	y =	240	00 +	FR	EQI	JEN	ICY	(M	Hz)										
			Low	1								Ch	ann	nel r	map	be	twe	een	23	60 I	ИΗ	Z	246	0 N	lHz								
												Fre	equ	enc	y =	236	60 +	FR	EQI	JEN	ICY	(M	Hz)										

23.14.10 TXPOWER

Address offset: 0x50C

Output power

		•																													
Bitı	numbe	er		31	30 2	29 2	28 27	7 26	25	24	23 2	2 21	1 20	19	18	17	16	15	14 1	13 1	2 1:	1 10	9	8	7	6	5	4 3	3 2	1	0
Id																									Α	Α	Α	A A	A A	Α	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0 0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 (0	0
Id	RW	Field	Value Id	Va	lue						Desc	cript	ion																		
Α	RW	TXPOWER									RADI	Ю о	utpı	ut p	owe	er.															
											Outp	out p	oow	er ir	n nı	ımb	er (of d	Bm,	i.e.	if th	ne va	alue	-20) is	spe	cifie	d			
											the c	outp	ut p	ow	er v	vill k	oe s	et t	o -2	0dB	m.										
			Pos4dBm	0x	04						+4 dI	Bm																			
			Pos3dBm	0x	03						+3 dI	Bm																			
			0dBm	0x	00						0 dB	m																			
			Neg4dBm	0x	FC						-4 dE	Bm																			
			Neg8dBm	0x	F8						-8 dE	Bm																			
			Neg12dBm	0x	F 4						-12 c	dBm																			
			Neg16dBm	0x	FO						-16 c	dBm																			
			Neg20dBm	0x	EC						-20 c	dBm																			
			Neg30dBm	0x	D8						-40 c	dBm																D	epre	ecat	ed
			Neg40dBm	0x	D8						-40 c	dBm																			
			•																									L	cpi	cai	eu

23.14.11 MODE

Address offset: 0x510

Data rate and modulation



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3	2 1 0
Id		A	A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0
Id RW Field	Value Id	Value Description	
A RW MODE		Radio data rate and modulation setting. The radio supports	
		Frequency-shift Keying (FSK) modulation.	
	Nrf_1Mbit	0 1 Mbit/s Nordic proprietary radio mode	
	Nrf_2Mbit	1 2 Mbit/s Nordic proprietary radio mode	
	Nrf_250Kbit	2 250 kbit/s Nordic proprietary radio mode De	eprecated
	Ble_1Mbit	3 1 Mbit/s Bluetooth Low Energy	
	Ble_2Mbit	4 2 Mbit/s Bluetooth Low Energy	

23.14.12 PCNF0

Address offset: 0x514

Packet configuration register 0

Bit n	umbe	er		31	30 2	9 :	28 2	7 2	26 2	5 2	4 23	3 22	21	20	19	18	17	16 1	15 1	4 1	3 12	11	10	9	8	7	6	5 4	3	2	1 0
Id										G	ì			F	Ε	Ε	Ε	Е							С				Α	Α	A A
Rese	et 0x0	0000000		0	0	0	0 (0	0 (0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						D	escri	ptio	n																	
Α	RW	LFLEN									Le	ength	n on	air	of I	LEN	GT	H fie	eld i	n nı	ımb	er o	f bit	s.							
С	RW	SOLEN									Le	ength	n on	air	of S	50 f	ielo	lin	nun	nber	of l	yte	s.								
E	RW	S1LEN									Le	ength	n on	air	of S	51 f	ielo	lin	nun	nber	of l	its.									
F	RW	S1INCL									In	clud	e or	ex	clud	le S	1 fi	eld	in R	AM											
			Automatic	0							In	clud	e S1	fie	ld i	n R	٩M	onl	y if	S1L	N >	0									
			Include	1							Al	way	s inc	luc	le S	1 fi	eld	in R	ΑM	ind	epe	nde	nt o	f S1	LEN						
G	RW	PLEN									Le	ength	of	pre	am	ble	on	air.	Dec	isio	n pc	int:	TAS	KS.	_ST/	ART	tas	k			
			8bit	0							8-	bit p	rea	mb	le																
			16bit	1							16	5-bit	pre	am	ble																

23.14.13 PCNF1

Address offset: 0x518

Packet configuration register 1

Rit r	umbe	or		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	Idilibe	-1		E D	
	t OxO	0000000		0 0 0 0 0 0 0 0	
Id		Field	Value Id	Value	Description
Α	RW	MAXLEN		[0255]	Maximum length of packet payload. If the packet payload is
					larger than MAXLEN, the radio will truncate the payload to
					MAXLEN.
В	RW	STATLEN		[0255]	Static length in number of bytes
					The static length responsible is added to the total length of the
					The static length parameter is added to the total length of the
					payload when sending and receiving packets, e.g. if the static
					length is set to N the radio will receive or send N bytes more
					than what is defined in the LENGTH field of the packet.
С	RW	BALEN		[24]	Base address length in number of bytes
					The address field is composed of the base address and the one
					byte long address prefix, e.g. set BALEN=2 to get a total address
					of 3 bytes.
D	RW	ENDIAN			On air endianness of packet, this applies to the SO, LENGTH, S1
					and the PAYLOAD fields.
			Little	0	Least Significant bit on air first
			Big	1	Most significant bit on air first
Е	RW	WHITEEN			Enable or disable packet whitening
			Disabled	0	Disable



	value lu	value	Description				
Id RW Field	Value Id	Value	Description				
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0	0 0 0 0	0 0 0 0 0	0 0 0 0 0 0 0
Id		E C)	CCCI	в в в в	B B B B A	A A A A A A A
Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19	18 17 16 1	15 14 13 12	11 10 9 8 7	7 6 5 4 3 2 1 0

23.14.14 BASE0

Address offset: 0x51C

Base address 0

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 :	21	20 :	19 :	18 :	17 :	16 1	15 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α ,	۸ ۸	A A	Δ Δ	Α	Α	Α	Α	Α	Α	Α	A A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	scrip	otic	n																		
Α	RW	BASE0										Bas	e a	ddr	ess	0																	

Radio base address 0.

23.14.15 BASE1

Address offset: 0x520

Base address 1

	Bit n	umbe	er		31	30	29 2	28 2	27 2	26 2	25 2	24 2	23 2	22 2	21 2	20 1	9 1	8 17	16	15	14	13	12 :	11 1	0 9	9 8	3 7	6	5	4	3	2	1 0
	Id				Α	Α	Α	Α	Α.	Α.	Α.	A	A	Α	Α	A A	Α Α	А А	Α	Α	Α	Α	Α	Α /	Α ,	4 <i>A</i>	A	Α	Α	Α	Α .	Α.	АА
	Rese	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0	0 0
	Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
ľ	Α	RW	BASE1									E	3ase	e ac	ddre	ess :	L																

Radio base address 1.

23.14.16 PREFIX0

Address offset: 0x524

Prefixes bytes for logical addresses 0-3

Bitı	numbe	r		31	. 30	29	28	3 27	26	5 25	24	23	22	21	20	19	18	17	16	15 :	14 1	13 1	L2 1	1 1	0 9	9	8	7	6	5	4	3	2	1 ()
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	В	В	В	В	3 I	3 E	3	В	А	Α	Α	Α	Α .	Δ,	A A	4
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0	0	0 (0 0)
Id	RW	Field	Value Id	Va	lue	:						De	scri	ptic	on																				
Α	RW	AP0										Ad	dre	ss p	ref	ix 0																			_
В	RW	AP1										Ad	dre	ss p	ref	ix 1																			
С	RW	AP2										Ad	dre	ss p	ref	ix 2																			
D	RW	AP3										Ad	dre	ss p	ref	ix 3																			

23.14.17 PREFIX1

Address offset: 0x528

Prefixes bytes for logical addresses 4-7

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14 1	13 1	12 1	.1 1	.0 9	9	8	7	6	5	4	3	2 :	1 0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	В	В	В	В	ВІ	ВІ	В	В	Α	Α	Α	Α	A	Δ ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	scrip	otic	on																			
Α	RW	AP4										Ado	dres	s p	refi	x 4.																		
В	RW	AP5										Add	dres	s p	refi	x 5.																		
С	RW	AP6										Add	dres	s p	refi	x 6.																		
D	RW	AP7										Add	dres	s p	refi	x 7.																		



23.14.18 TXADDRESS

Address offset: 0x52C

Transmit address select

Bitı	numbe	er		31	30	29 2	28 2	7 26	25	24	23	22 2	21 2	20 1	9 18	3 17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3	2	1 0	ı
Id																														Α.	А А	ı
Res	et 0x0	0000000		0	0	0	0 (0	0	0	0	0	0 (0 (0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	ı
Id	RW	Field	Value Id	Val	lue						De	scrip	tio	n																		l
Α	RW	TXADDRESS									Tra	nsm	it a	ddr	ess s	sele	ct															١

Logical address to be used when transmitting a packet.

23.14.19 RXADDRESSES

Address offset: 0x530 Receive address select

	numbe	er -		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					HGFEDCBA
Res		0000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value	Description
Α	RW	ADDR0			Enable or disable reception on logical address 0.
			Disabled	0	Disable
			Enabled	1	Enable
В	RW	ADDR1			Enable or disable reception on logical address 1.
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	ADDR2			Enable or disable reception on logical address 2.
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	ADDR3			Enable or disable reception on logical address 3.
			Disabled	0	Disable
			Enabled	1	Enable
Е	RW	ADDR4			Enable or disable reception on logical address 4.
			Disabled	0	Disable
			Enabled	1	Enable
F	RW	ADDR5			Enable or disable reception on logical address 5.
			Disabled	0	Disable
			Enabled	1	Enable
G	RW	ADDR6			Enable or disable reception on logical address 6.
			Disabled	0	Disable
			Enabled	1	Enable
Н	RW	ADDR7			Enable or disable reception on logical address 7.
			Disabled	0	Disable
			Enabled	1	Enable

23.14.20 CRCCNF

Address offset: 0x534 CRC configuration

31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	B A A
0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Value	Description
[13]	CRC length in number of bytes.
0	CRC length is zero and CRC calculation is disabled
1	CRC length is one byte and CRC calculation is enabled
2	CRC length is two bytes and CRC calculation is enabled
	0 0 0 0 0 0 0 0 Value



Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B A A
Reset 0x00000000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
	Three	3	CRC length is three bytes and CRC calculation is enabled
B RW SKIPADDR			Include or exclude packet address field out of CRC calculation.
	Include	0	CRC calculation includes address field
	Skip	1	CRC calculation does not include address field. The CRC
			calculation will start at the first byte after the address.

23.14.21 CRCPOLY

Address offset: 0x538

CRC polynomial

Bit r	numbe	er		31	. 30	29	28	27	26 2	25 2	24 :	23 2	22 2	21 2	20 :	19 1	18 3	17 1	6 1	5 1	4 1	3 12	11	10	9	8	7	6	5	4	3	2	1 0
Id												Α	Α .	Α.	Α	Α.	Α	A A	A A	Δ ,	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A.	А А
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	tio	n																		
Α	RW	CRCPOLY									(CRC	ро	lynd	om	ial																	
											ı	Eacl	h te	rm	in t	he	CR	Сро	lyn	om	ial is	ma	рре	d to	o a l	bit i	n tl	his					
												regi	ister	r wł	hich	n ind	dex	cor	res	por	ıds t	o th	e te	rm'	s ex	noqx	nen	nt. T	he				
											1	leas	st sig	gnif	fica	nt t	ern	n/bit	t is	har	d-w	ired	inte	erna	ally	to 1	., aı	nd b	oit				
												nun	nbe	r 0	of t	he	reg	ister	r co	nte	nt is	s igr	ore	d by	/ th	e ha	ard	war	e.				
												The	foll	low	ing	exa	amp	ole is	s fo	r aı	1 8 t	it C	RC p	ooly	nor	nial	: x8	3 + >	(7 +	+			
											,	x3 +	- x2	+ 1	. = 1	10	000	110	1.														

23.14.22 CRCINIT

Address offset: 0x53C

CRC initial value

Bitı	numbe	er		31	30	29	28	27	26	25 :	24	23 :	22	21	20	19	18	17	16	15 :	14 :	L3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	۸ ۸	4 A	A	Α	Α	Α	Α	Α	Α ,	Δ.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	on																		
Α	RW	CRCINIT										CRC	in	itia	l va	lue																	

Initial value for CRC calculation.

bit of the subsequent packet.

23.14.23 TIFS

Address offset: 0x544

Inter Frame Spacing in us

Bit	numbe	er		31	L 30	29	28	3 27	26	25	24	23	22	21	20	19	18	3 1	7 1	6 1	15 :	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													Α	Α	Α	Α	Α	Α	Α	Α
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																					
Α	RW	TIFS										Inte	er F	ran	ne :	Spa	cin	ıg i	n u	S																
												Inte				•																ve				
												pac	cke	ts. I	t is	dei	tine	ed	as t	he	tir	ne,	ın	mi	cro	sec	one	ds, t	ror	n tr	ne					
												end	to b	fthe	e la	st b	oit (of t	the	pr	evi	ou:	5 ра	ack	et t	o th	ne s	tart	of	the	e fir	st				

23.14.24 RSSISAMPLE

Address offset: 0x548

RSSI sample



Bit r	iumbe	r		31 3	0 29	28	27	26 2	5 2	24 2	3 2	2 21	1 20	19	18	17	16	15 1	.4 1	3 12	2 11	. 10	9	8 7	6	5	4	3	2	1 0	
Id																									Α	A	Α	Α	Α	A A	
Res	et 0x0	0000000		0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	Valu	e					C	esc	ript	tion																		
Α	R	RSSISAMPLE		[01	27]					R	SSI	sam	nple																		
										v	alue alue	e wh	hile	the Il re	act ceiv	ual i	ece	eive al s	d sig	gnal gth	stre	engtl	ı is i	ad as a neg as f	gativ	ve	ive				

23.14.25 STATE

Address offset: 0x550 Current radio state

Bit number		31	30	29	28 2	7 2	26 2	5 24	23	22 2	21 2	0 1	9 1	8 17	16	5 1	5 1	4 1	.3	12 :	11 1	.0	9	8	7	6	5	4	3 2	! 1	. 0
Id																													ΑА	. 4	A A
Reset 0x00000000		0	0	0	0	0 (0 (0 0	0	0	0 () (0	0	0	C)	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
ld RW Field	Value Id	Va	lue						De	scrip	tior	1																			
A R STATE									Cur	rent	rac	lio s	stat	e																	,
	Disabled	0							RAI	DIO	is in	the	e Dis	sabl	ed	sta	ite														
	RxRu	1							RAI	DIO	is in	the	RX	RU	sta	te															
	RxIdle	2							RAI	DIO	is in	the	RX	IDL	E st	ate	ē														
	Rx	3							RAI	DIO	is in	the	RX	sta	te																
	RxDisable	4							RAI	DIO	is in	the	RX	DIS	ABL	.ED	st	ate													
	TxRu	9							RAI	DIO	is in	the	e TX	RU	stat	e															
	TxIdle	10							RAI	DIO	is in	the	e TX	IDLI	E st	ate	9														
	Tx	11							RAI	DIO	is in	the	e TX	sta	te																
	TxDisable	12							RAI	DIO	is in	the	e TX	DIS	ABL	ED	st	ate													
A K SIAIE	RxRu RxIdle Rx RxDisable TxRu TxIdle	1 2 3 4 9 10							RAI RAI RAI RAI RAI RAI	DIO DIO DIO DIO DIO DIO	is in	the the the the the the	Dise RX RX RX RX RX TX TX	sabl RU IDL sta DIS RU IDLI	star E st te ABI star E st	te ate ED	e) st														

23.14.26 DATAWHITEIV

Address offset: 0x554

Data whitening initial value

Bit r	umbe	r		31	. 30	29	28	3 27	' 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																													Α	Α	Α	Α	Α	А А
Rese	t 0x0	0000040		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptio	on																			
Α	RW	DATAWHITEIV										Dat	a w	vhit	eni	ing	init	ial	valu	ıe.	Bit (5 is	har	d-w	/ire	d to	'1',	wr	itin	g '()'			
											1	to i	t ha	as n	no e	effe	ct,	and	l it v	will	alw	ays	be	rea	d b	ack	and	l us	ed	by				
											1	the	de	vice	e as	s '1	١.																	
												Bit	0 c	orre	esp	on	ds t	o P	osit	ion	6 o	f th	ie L	SFR	, Bit	1 t	o P	osit	ion	5,				
												etc.																						

23.14.27 BCC

Address offset: 0x560 Bit counter compare

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 1	.6 1	5 14	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Δ ,	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	ΑА	Α	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
Α	RW	всс										Bit	cou	ınte	er co	omp	are	:															

Bit counter compare register



23.14.28 DAB[0]

Address offset: 0x600

Device address base segment 0

Bit r	numbe	r		31	30	29	28	27	26	25	24	23	22 :	21 :	20 1	19 :	18 1	.7 1	6 1	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ ,	4 Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	ΑА	Α Δ	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																		
Α	RW	DAB										Dev	ice	ado	dres	ss b	ase	seg	mei	nt 0													

23.14.29 DAB[1]

Address offset: 0x604

Device address base segment 1

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW DAB		Device address base segment 1

23.14.30 DAB[2]

Address offset: 0x608

Device address base segment 2

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	A A
Re	et 0x(0000000		0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	DAB										Dev	/ice	ado	lres	s ba	se s	egn	nen	t 2													

23.14.31 DAB[3]

Address offset: 0x60C

Device address base segment 3

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW DAB		Device address base segment 3

23.14.32 DAB[4]

Address offset: 0x610

Device address base segment 4

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 1	8 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description	

A RW DAB Device address base segment 4

23.14.33 DAB[5]

Address offset: 0x614

Device address base segment 5



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 3	17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A	A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field Value Id	Value Description	
A RW DAB	Device address base	segment 5

23.14.34 DAB[6]

Address offset: 0x618

Device address base segment 6

Bit r	numbe	r		31	30	29	28 :	27 2	26 2	25 :	24	23 :	22 2	21 2	20 1	9 1	8 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	A /	Α Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	DAB										Dev	ice	ado	lres:	s ba	ise s	egr	nen	t 6													

23.14.35 DAB[7]

Address offset: 0x61C

Device address base segment 7

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 1	16 :	15 1	L4 1	L3 1	12 :	l1 1	.0	9 .	8 7	7	6	5	4	3 2	! 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	A ,	Δ,	Δ.	Δ ,	Д	Α	Α	Α	A A		A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0 0) (0
Id	RW	Field	Value Id	Va	lue							Des	scri	otic	n																			
Α	RW	DAB										Dev	vice	ad	dre	ss b	ase	se	gme	ent	7													

23.14.36 DAP[0]

Address offset: 0x620 Device address prefix 0

Bitı	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id																				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (,
Id	RW	Field	Value Id	Va	alue							De	cri	ptic	on																				ı
Α	RW	DAP										Dev	/ice	ad	dre	ess	pre	fix ()																-

23.14.37 DAP[1]

Address offset: 0x624

Device address prefix 1

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17	16 15 14 13 12 1	11 10 9 8	7 6 5 4 3 2 1	0
Id				AAAA	AAAA	A A A A A A	Α
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0	0
Id RW Field	Value Id	Value	Description				
A RW DAP			Device address prefix 1				

23.14.38 DAP[2]

Address offset: 0x628

Device address prefix 2

Bit	nun	nbe	r			31	. 30	29	28 2	7 26	5 25	24	23 :	22 :	21 2	20 1	.9 1	3 17	16	15	14	13	12 1	11 10	9	8	7	6	5	4	3	2 1	1 0
Id																				Α	Α	Α	Α.	ΑА	A	Α	Α	Α	Α	Α	Α	A A	A A
Re	set (0x0	0000000			0	0	0	0 (0	0	0	0	0	0 (0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	R	w	Field		Value Id	Va	lue						Des	crip	otio	n																	
_	_												_					٠.	_														



23.14.39 DAP[3]

Address offset: 0x62C Device address prefix 3

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 1	16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id				A A A A A A	A A A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A RW DAP			Device address prefix 3		

23.14.40 DAP[4]

Address offset: 0x630 Device address prefix 4

Bit r	numbe	er		31	30 2	9 :	28 2	7 26	5 25	24	1 23	22	21	20	19 1	L8 1	17 1	.6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2 1	1 0
Id																		A	A A	4 A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	А А
Res	et 0x0	0000000		0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 (0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						De	escr	iptic	on																		
Α	RW	DAP									De	evic	e ad	dre	ss p	refi	x 4															

23.14.41 DAP[5]

Address offset: 0x634

Device address prefix 5

Bitı	numbe	er		31	30 2	9 :	28 2	7 26	5 25	5 24	23	22	21	20	19 :	18 1	.7 1	6 1	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																		Д	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	АА
Res	et 0x0	0000000		0	0 ()	0 (0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue						De	scri	ptic	on																		
Α	RW	DAP									De	vice	ad	dre	ss p	refi	x 5															

23.14.42 DAP[6]

Address offset: 0x638

Device address prefix 6

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Id		A A A A A A A A A A A A A A A A A A A	АА
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
ld RW Field	Value Id	Value Description	
A RW DAP		Device address prefix 6	

23.14.43 DAP[7]

Address offset: 0x63C

Device address prefix 7

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 1	16 15 14 13 12 11 1	.0 9 8 7 6 5 4 3 2 1 0
Id				AAAAAA	A A A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0000000	0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A RW DAP			Device address prefix 7		

23.14.44 DACNF

Address offset: 0x640

Device address match configuration



Bit	number			31 30 2	29 28	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
Id								P O N M L K J I H G F E D C B /
Res	et 0x000	000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW F	Field	Value Id	Value				Description
Α	RW E	ENA0						Enable or disable device address matching using device address
								0
			Disabled	0				Disabled
			Enabled	1				Enabled
В	RW E	ENA1						Enable or disable device address matching using device address
								1
			Disabled	0				Disabled
			Enabled	1				Enabled
С	RW E	ENA2						Enable or disable device address matching using device address
								2
			Disabled	0				Disabled
			Enabled	1				Enabled
D	RW E	ENA3						Enable or disable device address matching using device address
								3
			Disabled	0				Disabled
			Enabled	1				Enabled
Ε	RW E	ENA4						Enable or disable device address matching using device address
								4
			Disabled	0				Disabled
			Enabled	1				Enabled
F	RW E	ENA5						Enable or disable device address matching using device address
								5
			Disabled	0				Disabled
			Enabled	1				Enabled
G	RW E	ENA6						Enable or disable device address matching using device address
								6
			Disabled	0				Disabled
			Enabled	1				Enabled
Н	RW E	ENA7						Enable or disable device address matching using device address
								7
			Disabled	0				Disabled
			Enabled	1				Enabled
1		TXADD0						TxAdd for device address 0
J		TXADD1						TxAdd for device address 1
K		TXADD2						TxAdd for device address 2
L		TXADD3						TxAdd for device address 3
M		TXADD4						TxAdd for device address 4
N		TXADD5						TxAdd for device address 5
0		TXADD6						TxAdd for device address 6
Р	K VV I	TXADD7						TxAdd for device address 7

23.14.45 MODECNF0

Address offset: 0x650

Radio mode configuration register 0

Bit	nun	nbe	r		31	. 30	29	28	27 :	26 :	25 2	24 2	23 2	2 21	. 20	19	18	17	16	15	14 :	L3 1	2 1:	l 10	9	8	7	6	5	4	3	2	1 0
Id																									С	С							Α
Res	et (0x0(0000200		0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	0	1	0	0	0	0	0	0	0 (0 0
Id	R	w	Field	Value Id	Va	lue						ı	Desc	ript	ion																		
Α	R	W	RU									ı	Radi	o rai	mp-	up t	ime	е															
				Default	0							[Defa	ult r	am	p-up	tir	ne (tRX	EN)), cc	mp	atib	e wi	th f	irm	war	e					
												١	writt	en f	or r	nRF5	1																
				Fast	1							F	ast	ram	p-u	p (tl	RXE	N,F	AST), se	ee e	lect	rica	spe	cific	atio	on f	or r	nor	e			
												i	nfor	mat	ion																		



	31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
		C C A
	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0
Value Id	Value	Description
		Default TX value
		Specifies what the RADIO will transmit when it is not started, i.e. between:
		RADIO.EVENTS_READY and RADIO.TASKS_START
		RADIO.EVENTS_END and RADIO.TASKS_START
		RADIO.EVENTS_END and RADIO.EVENTS_DISABLED
B1	0	Transmit '1'
В0	1	Transmit '0'
Center	2	Transmit center frequency
		When tuning the crystal for centre frequency, the RADIO must
		be set in DTX = Center mode to be able to achieve the expected
		accuracy.
	B1 B0	B1 0 B0 1

23.14.46 POWER

Address offset: 0xFFC
Peripheral power control

Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				А
Res	et 0x00000001		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW POWER			Peripheral power control. The peripheral and its registers will be
				reset to its initial state by switching the peripheral off and then
				back on again.
		Disabled	0	Peripheral is powered off
		Enabled	1	Peripheral is powered on

23.15 Electrical specification

23.15.1 General Radio Characteristics

Symbol	Description	Min.	Тур.	Max.	Units
f_{OP}	Operating frequencies	2360		2500	MHz
f _{PLL,PROG,RES}	PLL programming resolution		2		kHz
f _{PLL,CH,SP}	PLL channel spacing		1		MHz
f _{DELTA,1M}	Frequency deviation @ 1 Msps		±170		kHz
f _{DELTA,BLE,1M}	Frequency deviation @ BLE 1Msps		±250		kHz
f _{DELTA,2M}	Frequency deviation @ 2 Msps		±320		kHz
f _{DELTA,BLE,2M}	Frequency deviation @ BLE 2 Msps		±500		kHz
fsk _{SPS}	On-the-air data rate	1		2	Msps

23.15.2 Radio current consumption (Transmitter)

Symbol	Description	Min.	Тур.	Max.	Units
I _{TX,PLUS4dBM,DCDC}	TX only run current (DCDC, 3V) P _{RF} =+4 dBm		7.5		mA
I _{TX,PLUS4dBM}	TX only run current P _{RF} = +4 dBm		16.6		mA
I _{TX,0dBM,DCDC}	TX only run current (DCDC, 3V)P _{RF} = 0dBm		5.3		mA
I _{TX,0dBM}	TX only run current P _{RF} = 0dBm		11.6		mA
I _{TX,MINUS4dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -4dBm		4.2		mA
I _{TX,MINUS4dBM}	TX only run current P _{RF} = -4 dBm		9.3		mA
I _{TX,MINUS8dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -8 dBm		3.8		mA



Symbol	Description	Min.	Тур.	Max.	Units
I _{TX,MINUS8dBM}	TX only run current P _{RF} = -8 dBm		8.4		mA
I _{TX,MINUS12dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -12 dBm		3.5		mA
I _{TX,MINUS12dBM}	TX only run current P _{RF} = -12 dBm		7.7		mA
I _{TX,MINUS16dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -16 dBm		3.3		mA
I _{TX,MINUS16dBM}	TX only run current P _{RF} = -16 dBm		7.3		mA
I _{TX,MINUS20dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -20 dBm		3.2		mA
I _{TX,MINUS20dBM}	TX only run current P _{RF} = -20 dBm		7.0		mA
I _{TX,MINUS40dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -40 dBm		2.7		mA
I _{TX,MINUS40dBM}	TX only run current P _{RF} = -40 dBm		5.9		mA
I _{START,TX,DCDC}	TX start-up current DCDC, 3V, P _{RF} = 4 dBm		4.0		mA
I _{START,TX}	TX start-up current, P _{RF} = 4 dBm		8.8		mA

23.15.3 Radio current consumption (Receiver)

Symbol	Description	Min.	Тур.	Max.	Units
I _{RX,1M,DCDC}	RX only run current (DCDC, 3V) 1Msps / 1Msps BLE		5.4		mA
I _{RX,1M}	RX only run current 1Msps / 1Msps BLE		11.7		mA
I _{RX,2M,DCDC}	RX only run current (DCDC, 3V) 2Msps / 2Msps BLE		5.8		mA
I _{RX,2M}	RX only run current 2Msps / 2Msps BLE		12.9		mA
I _{START,RX,DCDC}	RX start-up current (DCDC 3V)		3.5		mA
I _{START,RX,LDO}	RX start-up current (LDO 3V)		7.5		mA

23.15.4 Transmitter specification

Symbol	Description	Min.	Тур.	Max.	Units
P _{RF}	Maximum output power		4	6	dBm
P _{RFC}	RF power control range		24		dB
P _{RFCR}	RF power accuracy			±4	dB
P _{RF1,1}	1st Adjacent Channel Transmit Power 1 MHz (1 Msps Nordic		-25		dBc
	proprietary mode)				
P _{RF2,1}	2nd Adjacent Channel Transmit Power 2 MHz (1 Msps Nordic		-50		dBc
··· -/-	proprietary mode)				
P _{RF1,2}	1st Adjacent Channel Transmit Power 2 MHz (2 Msps Nordic		-25		dBc
	proprietary mode)				
P _{RF2,2}	2nd Adjacent Channel Transmit Power 4 MHz (2 Msps Nordic		-50		dBc
	proprietary mode)				
P _{RF1,2,BLE}	1st Adjacent Channel Transmit Power 2 MHz (2 Msps BLE mode)		-20		dBc
P _{RF2,2,BLE}	2nd Adjacent Channel Transmit Power 4 MHz (2 Msps BLE		-50		dBc
	mode)				

23.15.5 Receiver operation

Symbol	Description	Min.	Тур.	Max.	Units
P _{RX,MAX}	Maximum received signal strength at < 0.1% BER		0		dBm
P _{SENS,IT,1M}	Sensitivity, 1Msps nRF mode ¹⁶		-93		dBm
P _{SENS,IT,SP,1M,BLE}	Sensitivity, 1Msps BLE ideal transmitter, <=37 bytes BER=1E-3 ¹⁷		-96		dBm
P _{SENS,IT,LP,1M,BLE}	Sensitivity, 1Msps BLE ideal transmitter >=128 bytes BER=1E-4 18		-95		dBm
P _{SENS,IT,2M}	Sensitivity, 2Msps nRF mode ¹⁹		-89		dBm

¹⁶ Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

As defined in the Bluetooth Core Specification v4.0 Volume 6: Core System Package (Low Energy Controller Volume)

¹⁸ Equivalent BER limit < 10E-04

Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.



Symbol	Description	Min.	Тур.	Max.	Units
P _{SENS,IT,SP,2M,BLE}	Sensitivity, 2Msps BLE ideal transmitter, Packet length		-93		dBm
	<=37bytes				
P _{SENS,DT,SP,2M,BLE}	Sensitivity, 2Msps BLE dirty transmitter, Packet length		-93		dBm
	<=37bytes				
P _{SENS,IT,LP,2M,BLE}	Sensitivity, 2Msps BLE ideal transmitter >= 128bytes		-92		dBm
P _{SENS,DT,LP,2M,BLE}	Sensitivity, 2Msps BLE dirty transmitter, Packet length >=		-92		dBm
	128bytes				

23.15.6 RX selectivity

RX selectivity with equal modulation on interfering signal²⁰

Symbol	Description	Min.	Тур.	Max.	Units
C/I _{1M,co-channel}	1Msps mode, Co-Channel interference		9		dB
C/I _{1M,-1MHz}	1 Msps mode, Adjacent (-1 MHz) interference		-2		dB
C/I _{1M,+1MHz}	1 Msps mode, Adjacent (+1 MHz) interference		-10		dB
C/I _{1M,-2MHz}	1 Msps mode, Adjacent (-2 MHz) interference		-19		dB
C/I _{1M,+2MHz}	1 Msps mode, Adjacent (+2 MHz) interference		-42		dB
C/I _{1M,-3MHz}	1 Msps mode, Adjacent (-3 MHz) interference		-38		dB
C/I _{1M,+3MHz}	1 Msps mode, Adjacent (+3 MHz) interference		-48		dB
C/I _{1M,±6MHz}	1 Msps mode, Adjacent (≥6 MHz) interference		-50		dB
C/I _{1MBLE,co-channel}	1 Msps BLE mode, Co-Channel interference		6		dB
C/I _{1MBLE,-1MHz}	1 Msps BLE mode, Adjacent (-1 MHz) interference		-2		dB
C/I _{1MBLE,+1MHz}	1 Msps BLE mode, Adjacent (+1 MHz) interference		-9		dB
C/I _{1MBLE,-2MHz}	1 Msps BLE mode, Adjacent (-2 MHz) interference		-22		dB
C/I _{1MBLE,+2MHz}	1 Msps BLE mode, Adjacent (+2 MHz) interference		-46		dB
C/I _{1MBLE,>3MHz}	1 Msps BLE mode, Adjacent (≥3 MHz) interference		-50		dB
C/I _{1MBLE,image}	Image frequency Interference		-22		dB
C/I _{1MBLE,image,1MHz}	Adjacent (1 MHz) interference to in-band image frequency		-35		dB
C/I _{2M,co-channel}	2Msps mode, Co-Channel interference		10		dB
C/I _{2M,-2MHz}	2 Msps mode, Adjacent (-2 MHz) interference		6		dB
C/I _{2M,+2MHz}	2 Msps mode, Adjacent (+2 MHz) interference		-14		dB
C/I _{2M,-4MHz}	2 Msps mode, Adjacent (-4 MHz) interference		-20		dB
C/I _{2M,+4MHz}	2 Msps mode, Adjacent (+4 MHz) interference		-44		dB
C/I _{2M,-6MHz}	2 Msps mode, Adjacent (-6 MHz) interference		-42		dB
C/I _{2M,+6MHz}	2 Msps mode, Adjacent (+6 MHz) interference		-47		dB
C/I _{2M,≥12MHz}	2 Msps mode, Adjacent (≥12 MHz) interference		-52		dB
C/I _{2MBLE,co-channel}	2 Msps BLE mode, Co-Channel interference		7		dB
C/I _{2MBLE,±2MHz}	2 Msps BLE mode, Adjacent (±2 MHz) interference		0		dB
C/I _{2MBLE,±4MHz}	2 Msps BLE mode, Adjacent (±4 MHz) interference		-47		dB
C/I _{2MBLE,≥6MHz}	2 Msps BLE mode, Adjacent (≥6 MHz) interference		-49		dB
C/I _{2MBLE,image}	Image frequency Interference		-21		dB
C/I _{2MBLE,image, 2MHz}	Adjacent (2 MHz) interference to in-band image frequency		-36		dB

23.15.7 RX intermodulation

RX intermodulation²¹

Symbol	Description	Min.	Тур.	Max.	Units
P _{IMD,1M}	IMD performance, 1 Msps (3 MHz, 4 MHz, and 5 MHz offset)		-33		dBm
P _{IMD,1M,BLE}	IMD performance, BLE 1 Msps (3 MHz, 4 MHz, and 5 MHz		-30		dBm
	offset)				
P _{IMD,2M}	IMD performance, 2 Msps (6 MHz, 8 MHz, and 10 MHz offset)		-33		dBm

Wanted signal level at PIN = -67 dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented

Wanted signal level at PIN = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is not modulated, the other interferer is modulated equal with the wanted signal. The input power of the interferers where the sensitivity equals BER = 0.1% is presented.



Symbol	Description	Min.	Тур.	Max.	Units
P _{IMD,2M,BLE}	IMD performance, BLE 2 Msps (6 MHz, 8 MHz, and 10 MHz		-32		dBm
	offset)				

23.15.8 Radio timing

Symbol	Description	Min.	Тур.	Max.	Units
t _{TXEN}	Time between TXEN task and READY event after channel		140		us
	FREQUENCY configured				
t _{TXEN,FAST}	Time between TXEN task and READY event after channel		40		us
	FREQUENCY configured (Fast Mode)				
t _{TXDISABLE}	Time between DISABLE task and DISABLED event when the		6		us
	radio was in TX and mode is set to 1Msps				
t _{TXDISABLE,2M}	Time between DISABLE task and DISABLED event when the		4		us
	radio was in TX and mode is set to 2Msps				
t _{RXEN}	Time between the RXEN task and READY event after channel		140		us
	FREQUENCY configured in default mode				
t _{RXEN,FAST}	Time between the RXEN task and READY event after channel		40		us
	FREQUENCY configured in fast mode				
t _{SWITCH}	The minimum time taken to switch from RX to TX or TX to RX		20		us
	(channel FREQUENCY unchanged)				
t _{RXDISABLE}	Time between DISABLE task and DISABLED event when the		0		us
	radio was in RX				
t _{TXCHAIN}	TX chain delay		0.6		us
t _{RXCHAIN}	RX chain delay		9.4		us
t _{RXCHAIN,2M}	RX chain delay in 2Msps mode		5		us

23.15.9 Received Signal Strength Indicator (RSSI) specifications

Symbol	Description	Min.	Тур.	Max.	Units
RSSI _{ACC}	RSSI Accuracy Valid range -90 to -20 dBm		±2		dB
RSSI _{RESOLUTION}	RSSI resolution		1		dB
RSSI _{PERIOD}	Sample period		0.25		us

23.15.10 Jitter

Symbol	Description	Min.	Тур.	Max.	Units
t _{DISABLEDJITTER}	Jitter on DISABLED event relative to END event when shortcut		0.25		us
	between END and DISABLE is enabled.				
t _{READYJITTER}	Jitter on READY event relative to TXEN and RXEN task.		0.25		us

23.15.11 Delay when disabling the RADIO

Symbol	Description	Min.	Тур.	Max.	Units
t _{TXDISABLE,1M}	Disable delay from TX.		6		us
	Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit				
	and MODE = Ble_1Mbit				
t _{RXDISABLE,1M}	Disable delay from RX.		0		us
	Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit				
	and MODE = Ble_1Mbit				



24 TIMER — Timer/counter

The TIMER can operate in two modes: timer and counter.

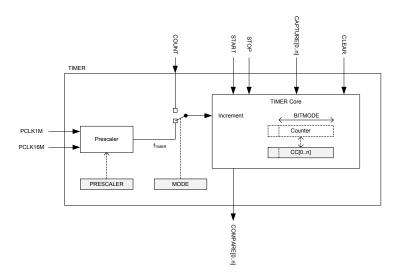


Figure 42: Block schematic for timer/counter

The timer/counter runs on the high-frequency clock source (HFCLK) and includes a four-bit (1/2X) prescaler that can divide the timer input clock from the HFCLK controller. Clock source selection between PCLK16M and PCLK1M is automatic according to TIMER base frequency set by the prescaler. The TIMER base frequency is always given as 16 MHz divided by the prescaler value.

The PPI system allows a TIMER event to trigger a task of any other system peripheral of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

The TIMER can operate in two modes, Timer mode and Counter mode. In both modes, the TIMER is started by triggering the START task, and stopped by triggering the STOP task. After the timer is stopped the timer can resume timing/counting by triggering the START task again. When timing/counting is resumed, the timer will continue from the value it had prior to being stopped.

In Timer mode, the TIMER's internal Counter register is incremented by one for every tick of the timer frequency f_{TIMER} as illustrated in *Figure 42: Block schematic for timer/counter* on page 234. The timer frequency is derived from PCLK16M as shown below, using the values specified in the PRESCALER register:

```
f_{\text{TIMER}} = 16 \text{ MHz} / (2^{\text{PRESCALER}})
```

When $f_{TIMER} \le 1$ MHz the TIMER will use PCLK1M instead of PCLK16M for reduced power consumption.

In counter mode, the TIMER's internal Counter register is incremented by one each time the COUNT task is triggered, that is, the timer frequency and the prescaler are not utilized in counter mode. Similarly, the COUNT task has no effect in Timer mode.

The TIMER's maximum value is configured by changing the bit-width of the timer in the *BITMODE* on page 239 register.

PRESCALER on page 239 and the *BITMODE* on page 239 must only be updated when the timer is stopped. If these registers are updated while the TIMER is started then this may result in unpredictable behavior.



When the timer is incremented beyond its maximum value the Counter register will overflow and the TIMER will automatically start over from zero.

The Counter register can be cleared, that is, its internal value set to zero explicitly, by triggering the CLEAR task.

The TIMER implements multiple capture/compare registers.

Independent of prescaler setting the accuracy of the TIMER is equivalent to one tick of the timer frequency f_{TIMER} as illustrated in *Figure 42: Block schematic for timer/counter* on page 234.

24.1 Capture

The TIMER implements one capture task for every available capture/compare register.

Every time the CAPTURE[n] task is triggered, the Counter value is copied to the CC[n] register.

24.2 Compare

The TIMER implements one COMPARE event for every available capture/compare register.

A COMPARE event is generated when the Counter is incremented and then becomes equal to the value specified in one of the capture compare registers. When the Counter value becomes equal to the value specified in a capture compare register CC[n], the corresponding compare event COMPARE[n] is generated.

BITMODE on page 239 specifies how many bits of the Counter register and the capture/compare register that are used when the comparison is performed. Other bits will be ignored.

24.3 Task delays

After the TIMER is started, the CLEAR task, COUNT task and the STOP task will guarantee to take effect within one clock cycle of the PCLK16M.

24.4 Task priority

If the START task and the STOP task are triggered at the same time, that is, within the same period of PCLK16M, the STOP task will be prioritized.

24.5 Registers

Table 42: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40008000	TIMER	TIMER0	Timer 0	This timer instance has 4 CC registers
				(CC[03])
0x40009000	TIMER	TIMER1	Timer 1	This timer instance has 4 CC registers
				(CC[03])
0x4000A000	TIMER	TIMER2	Timer 2	This timer instance has 4 CC registers
				(CC[03])
0x4001A000	TIMER	TIMER3	Timer 3	This timer instance has 6 CC registers
				(CC[05])
0x4001B000	TIMER	TIMER4	Timer 4	This timer instance has 6 CC registers
				(CC[05])

Table 43: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start Timer



Register	Offset	Description	
TASKS_STOP	0x004	Stop Timer	
TASKS_COUNT	0x008	Increment Timer (Counter mode only)	
TASKS_CLEAR	0x00C	Clear time	
TASKS_SHUTDOWN	0x010	Shut down timer	Deprecated
TASKS_CAPTURE[0]	0x040	Capture Timer value to CC[0] register	
TASKS_CAPTURE[1]	0x044	Capture Timer value to CC[1] register	
TASKS_CAPTURE[2]	0x048	Capture Timer value to CC[2] register	
TASKS_CAPTURE[3]	0x04C	Capture Timer value to CC[3] register	
TASKS_CAPTURE[4]	0x050	Capture Timer value to CC[4] register	
TASKS_CAPTURE[5]	0x054	Capture Timer value to CC[5] register	
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match	
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match	
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match	
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match	
EVENTS_COMPARE[4]	0x150	Compare event on CC[4] match	
EVENTS_COMPARE[5]	0x154	Compare event on CC[5] match	
SHORTS	0x200	Shortcut register	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
MODE	0x504	Timer mode selection	
BITMODE	0x508	Configure the number of bits used by the TIMER	
PRESCALER	0x510	Timer prescaler register	
CC[0]	0x540	Capture/Compare register 0	
CC[1]	0x544	Capture/Compare register 1	
CC[2]	0x548	Capture/Compare register 2	
CC[3]	0x54C	Capture/Compare register 3	
CC[4]	0x550	Capture/Compare register 4	
CC[5]	0x554	Capture/Compare register 5	

24.5.1 SHORTS

Address offset: 0x200 Shortcut register

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					LKJIHG FEDCBA
Rese	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	COMPAREO_CLEAR			Shortcut between COMPARE[0] event and CLEAR task
					See EVENTS_COMPARE[0] and TASKS_CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
В	RW	COMPARE1 CLEAR			Shortcut between COMPARE[1] event and CLEAR task
		_			Car EVENTS COMPAREIAL and TASKS CLEAR
			a		See EVENTS_COMPARE[1] and TASKS_CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
С	RW	COMPARE2_CLEAR			Shortcut between COMPARE[2] event and CLEAR task
					See EVENTS_COMPARE[2] and TASKS_CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
D	RW	COMPARE3_CLEAR			Shortcut between COMPARE[3] event and CLEAR task
					See EVENTS COMPARE[3] and TASKS CLEAR
			Disabled	0	Disable shortcut
_	DIA:	COLADADEA CLEAD	Enabled	1	Enable shortcut
Ε	RW	COMPARE4_CLEAR			Shortcut between COMPARE[4] event and CLEAR task
					See EVENTS_COMPARE[4] and TASKS_CLEAR



Bit	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				L K J I H G F E D C B A
Res	set 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
F	RW COMPARE5_CLEAR			Shortcut between COMPARE[5] event and CLEAR task
				See EVENTS_COMPARE[5] and TASKS_CLEAR
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
G	RW COMPAREO_STOP			Shortcut between COMPARE[0] event and STOP task
				See EVENTS_COMPARE[0] and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
Н	RW COMPARE1_STOP			Shortcut between COMPARE[1] event and STOP task
				See EVENTS_COMPARE[1] and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
ī	RW COMPARE2_STOP			Shortcut between COMPARE[2] event and STOP task
				See EVENTS_COMPARE[2] and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
J	RW COMPARE3_STOP			Shortcut between COMPARE[3] event and STOP task
	_			
		Disabled	0	See EVENTS_COMPARE[3] and TASKS_STOP Disable shortcut
		Enabled	1	Enable shortcut
K	RW COMPARE4_STOP	Lilabica	-	Shortcut between COMPARE[4] event and STOP task
		Disabled	0	See EVENTS_COMPARE[4] and TASKS_STOP
		Disabled Enabled	0 1	Disable shortcut Enable shortcut
L	RW COMPARES_STOP	Liidulcu	*	Shortcut between COMPARE[5] event and STOP task
_	W COMI ANES_STOP			
				See EVENTS_COMPARE[5] and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut

24.5.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	numbe	r		31	30	29	28 2	27 :	26 2	5 2	24 2	23 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id													F	Ε	D	С	В	Α															
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						ı	Descr	ipti	on																			
Α	RW	COMPARE0									١	Write	'1'	to E	nal	ble	int	erru	ıpt	for	CO	MF	ARI	E[0]	eve	ent							
											9	See <i>E</i>	VΕN	ITS_	co	MF	PAR	E[0	1														
			Set	1							1	Enabl	e																				
			Disabled	0							F	Read	Dis	abl	ed																		
			Enabled	1							ı	Read:	Ena	able	ed																		
В	RW	COMPARE1									١	Write	'1'	to E	nal	ble	int	erru	ıpt	for	CO	MF	ARI	E[1]	eve	ent							
											9	See <i>E</i>	VΕN	ITS_	co	MF	PAR	E[1	1														
			Set	1							1	Enabl	e																				
			Disabled	0							F	Read:	Dis	abl	ed																		
			Enabled	1							F	Read:	Ena	able	ed																		
С	RW	COMPARE2									١	Write	'1'	to E	nal	ble	int	erru	ıpt	for	CO	MF	ARI	E[2]	eve	ent							



Bit no	umber			31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					F E D C B A
Rese	t 0x000	000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW F	ield	Value Id	Value	Description
					See EVENTS_COMPARE[2]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW C	COMPARE3			Write '1' to Enable interrupt for COMPARE[3] event
					See EVENTS_COMPARE[3]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW C	COMPARE4			Write '1' to Enable interrupt for COMPARE[4] event
					See EVENTS_COMPARE[4]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW C	COMPARE5	Enabled	-	Write '1' to Enable interrupt for COMPARE[5] event
·		JOINI AIRES			· · · · · ·
					See EVENTS_COMPARE[5]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

24.5.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit n	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					FEDCBA
Rese	et 0x0	0000000		0 0 0 0 0 0 0 0	
Id	RW	Field	Value Id	Value	Description
Α	RW	COMPARE0			Write '1' to Disable interrupt for COMPARE[0] event
					See EVENTS_COMPARE[0]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	COMPARE1			Write '1' to Disable interrupt for COMPARE[1] event
					See EVENTS_COMPARE[1]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	COMPARE2			Write '1' to Disable interrupt for COMPARE[2] event
					See EVENTS_COMPARE[2]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	COMPARE3			Write '1' to Disable interrupt for COMPARE[3] event
					Con EVENTS COMPARE[3]
			Clear	1	See EVENTS_COMPARE[3] Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW	COMPARE4		-	Write '1' to Disable interrupt for COMPARE[4] event
					See EVENTS_COMPARE[4]
			Clear	1	Disable



Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
F RW COMPARE5			Write '1' to Disable interrupt for COMPARE[5] event
			See EVENTS_COMPARE[5]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

24.5.4 MODE

Address offset: 0x504 Timer mode selection

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 1	18 1	17	16	15	14 :	13 :	12 1	l1 1	.0 9	9 ;	3 7	7 (5 5	5 4	4 3	3 2	1	0
Id																																	Α	А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0) () () (0 (0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	MODE										Tim	ner	mo	de																			
			Timer	0								Sel	ect	Tim	er i	noc	de																	
			Counter	1								Sel	ect	Cou	ınte	r m	ode	e													D	epr	eca	ted
			LowPowerCounter	2								Sel	ect	Lov	/ Pc	we	r Co	oun	ter	mo	de													

24.5.5 BITMODE

Address offset: 0x508

Configure the number of bits used by the TIMER

Bit	numbe	er		31	. 30	29	28	3 27	7 26	5 2	5 2	4 2	23 2	22 2	21 :	20	19	18	17	16	15	5 14	1 13	3 12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							0	Des	crip	otio	n																				
Α	RW	BITMODE										Т	Γim	er b	oit v	wid	lth																			
			16Bit	0								1	16 b	it t	ime	er b	oit v	wid	lth																	
			08Bit	1								8	3 bi	t tir	nei	bit	t w	idt	h																	
			24Bit	2								2	24 b	it t	ime	er b	oit v	wid	lth																	
			32Bit	3								3	32 b	it t	ime	er b	oit v	wid	lth																	

24.5.6 PRESCALER

Address offset: 0x510
Timer prescaler register

Bit	numbe	r		31	30	29 2	28 2	7 26	25	24	23	22	21 :	20 1	19 1	l8 1	7 16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3	2 1	1 0	
Id																													Α /	Α Α	А А	
Res	et 0x0	000004		0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0	0	0 :	L (0 0	
Id	RW	Field	Value Id	Val	lue						Des	scrip	otio	n																		
Α	RW	PRESCALER		[0	.9]						Pre	sca	ler v	valu	ie																	

24.5.7 CC[0]

Address offset: 0x540

Capture/Compare register 0



Bit	numbe	er		31	L 30	29	28	27	26	25	24	23	22 2	1 20	19	18	17	16	15	14 1	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	Α	Α	Α	Α	Α	Α	Α,	4 <i>A</i>	A A	Α	Α	Α	Α	Α	Α /	Α Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	alue							Des	crip	tion																		
Α	RW	CC										Cap	ture	/Co	mpa	re ۱	/alu	e														
												Onl	y the	e nu	mbe	er of	f bit	s ir	dic	ated	by	BIT	MO	DE v	vill l	be u	ısed	l by				
												the	TIM	FR							·							ŕ				

24.5.8 CC[1]

Address offset: 0x544

Capture/Compare register 1

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	9 18	3 17	7 16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 A	. A	Α	Α	Α	Α	ДД	Α	Α	Α	Α	Α	Α	Α	Α /	4 Α	A
Res	et 0x(0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																	
Α	RW	CC										Cap	otur	e/C	omp	are	val	ue														
												On	ly th	ne n	umb	oer o	of b	its i	ndic	ate	d by	BITI	MOE	DE w	/ill k	oe u	ised	d by	,			
												the	TIN	ИER																		

24.5.9 CC[2]

Address offset: 0x548

Capture/Compare register 2

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	9 1	8 1	7 16	5 15	14	13	12	11 :	10	9	8 7	7 6	5 5	4	3	2	1 0	l
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α,	4 Α	. Δ	A	Α	Α	Α	Α	Α	Α	A .	A A	A /	Α Α	A	Α	Α	А А	l
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0 0	l
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																		l
Α	RW	СС										Ca	otur	e/C	om	oare	val	lue															١
												On	ly th	ne n	uml	ber	of b	its i	ndi	cate	d b	y BI	TM	ODE	wi	ll be	us	ed b	ру				
												the	TIN	ИER																			

24.5.10 CC[3]

Address offset: 0x54C

Capture/Compare register 3

Bit	num	nber	r		31	. 30	29	28	3 27	7 2	6 25	5 2	4 23	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α	Α	. 4	A A	. 4	A A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	4 А
Res	et 0)x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	R۱	w	Field	Value Id	Va	lue							D	esc	ripti	on																			
Α	R۱	W	СС										Ca	aptı	ıre/	Con	npa	re v	alu	e															
													0	nly	the	nur	nbe	r of	bit	s ir	ndic	ate	d b	у В	ITN	10D	Εw	vill l	oe ι	ıseo	d by	/			
														_	IME	_																			

24.5.11 CC[4]

Address offset: 0x550

Capture/Compare register 4

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW CC	Capture/Compare value



Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 10 1d A A A A A A A A A A A A A A A A A A
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Only the number of bits indicated by BITMODE will be used by the TIMER.

24.5.12 CC[5]

Address offset: 0x554

Capture/Compare register 5

Bit nu	ımbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 /	А А
Rese	t 0x0(000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	pti	on																			
Α	RW	СС										Ca	ptu	re/0	Con	npai	re v	alu	e															

Only the number of bits indicated by BITMODE will be used by the TIMER.

24.6 Electrical specification

24.6.1 Timers Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{TIMER_1M}	Run current with 1 MHz clock input (PCLK1M)	3	5	8	μΑ
I _{TIMER_16M}	Run current with 16 MHz clock input (PCLK16M)	50	70	120	μΑ
t _{TIMER,START}	Time from START task is given until timer starts counting		0.25		μs



25 RTC — Real-time counter

The Real-time counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK).

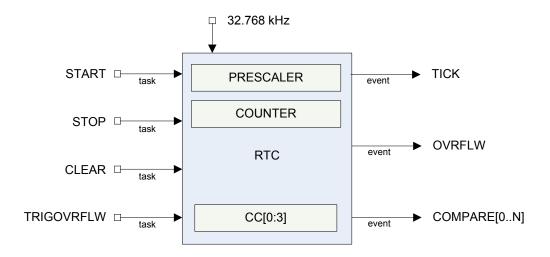


Figure 43: RTC block schematic

The RTC module features a 24-bit COUNTER, a 12-bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

25.1 Clock source

The RTC will run off the LFCLK.

The COUNTER resolution will therefore be $30.517 \,\mu s$. Depending on the source, the RTC is able to run while the HFCLK is OFF and PCLK16M is not available.

The software has to explicitely start LFCLK before using the RTC.

See CLOCK — Clock control on page 101 for more information about clock sources.

25.2 Resolution versus overflow and the PRESCALER

Counter increment frequency:

```
f_{RTC} [kHz] = 32.768 / (PRESCALER + 1 )
```

The PRESCALER register is read/write when the RTC is stopped. The PRESCALER register is read-only once the RTC is STARTed. Writing to the PRESCALER register when the RTC is started has no effect.

The PRESCALER is restarted on START, CLEAR and TRIGOVRFLW, that is, the prescaler value is latched to an internal register (<<PRESC>>) on these tasks.

Examples:

1. Desired COUNTER frequency 100 Hz (10 ms counter period)

 $f_{RTC} = 99.9 \text{ Hz}$



10009.576 µs counter period

2. Desired COUNTER frequency 8 Hz (125 ms counter period)

PRESCALER = round(32.768 kHz / 8 Hz) - 1 = 4095

 $f_{RTC} = 8 Hz$

125 ms counter period

Table 44: RTC resolution versus overflow

Prescaler	Counter resolution	Overflow
0	30.517 μs	512 seconds
28-1	7812.5 μs	131072 seconds
2 ¹² -1	125 ms	582.542 hours

25.3 COUNTER register

The COUNTER increments on LFCLK when the internal PRESCALER register (<<PRESC>>) is 0x00. <<PRESC>> is reloaded from the PRESCALER register. If enabled, the TICK event occurs on each increment of the COUNTER. The TICK event is disabled by default.

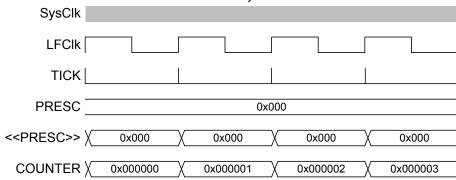


Figure 44: Timing diagram - COUNTER_PRESCALER_0

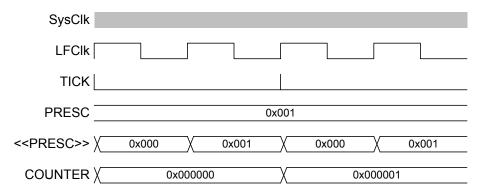


Figure 45: Timing diagram - COUNTER_PRESCALER_1

25.4 Overflow features

The TRIGOVRFLW task sets the COUNTER value to 0xFFFFF0 to allow SW test of the overflow condition.

OVRFLW occurs when COUNTER overflows from 0xFFFFFF to 0.

Important: The OVRFLW event is disabled by default.

25.5 TICK event

The TICK event enables low power "tick-less" RTOS implementation as it optionally provides a regular interrupt source for a RTOS without the need to use the ARM® SysTick feature.



Using the RTC TICK event rather than the SysTick allows the CPU to be powered down while still keeping RTOS scheduling active.

Important: The TICK event is disabled by default.

25.6 Event control feature

To optimize RTC power consumption, events in the RTC can be individually disabled to prevent PCLK16M and HFCLK being requested when those events are triggered. This is managed using the EVTEN register.

For example, if the TICK event is not required for an application, this event should be disabled as it is frequently occurring and may increase power consumption if HFCLK otherwise could be powered down for long durations.

This means that the RTC implements a slightly different task and event system compared to the standard system described in *Peripheral interface* on page 68. The RTC task and event system is illustrated in *Figure 46: Tasks, events and interrupts in the RTC* on page 244.

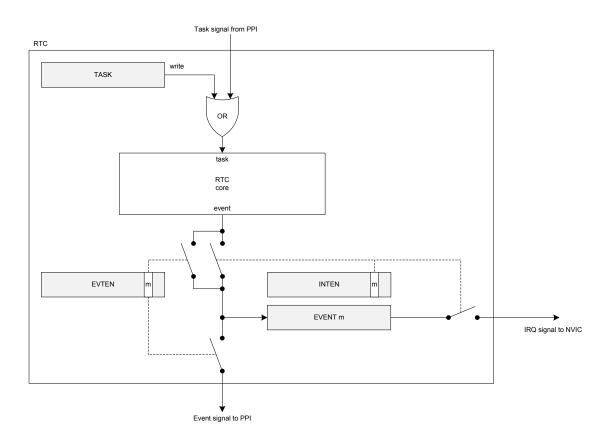


Figure 46: Tasks, events and interrupts in the RTC

25.7 Compare feature

There are a number of Compare registers.

For more information, see *Registers* on page 248.

When setting a compare register, the following behavior of the RTC compare event should be noted:

If a CC register value is 0 when a CLEAR task is set, this will not trigger a COMPARE event.



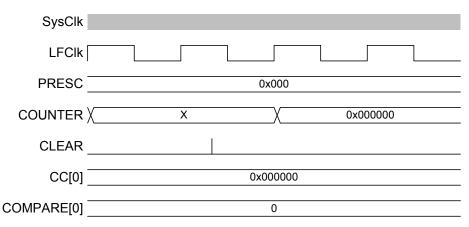


Figure 47: Timing diagram - COMPARE_CLEAR

 If a CC register is N and the COUNTER value is N when the START task is set, this will not trigger a COMPARE event.

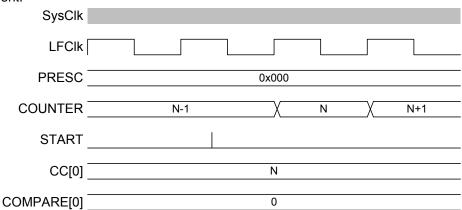


Figure 48: Timing diagram - COMPARE_START

• COMPARE occurs when a CC register is N and the COUNTER value transitions from N-1 to N.

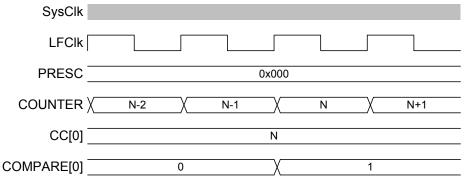


Figure 49: Timing diagram - COMPARE

• If the COUNTER is N, writing N+2 to a CC register is guaranteed to trigger a COMPARE event at N+2.



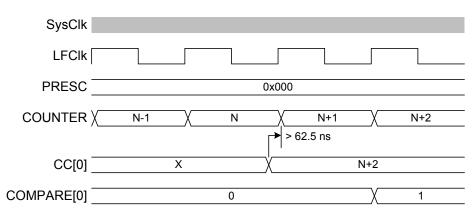


Figure 50: Timing diagram - COMPARE_N+2

• If the COUNTER is N, writing N or N+1 to a CC register may not trigger a COMPARE event.

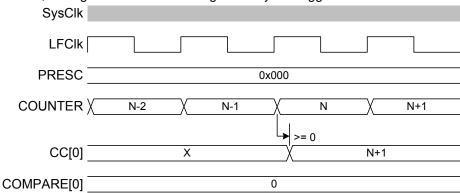


Figure 51: Timing diagram - COMPARE_N+1

• If the COUNTER is N and the current CC register value is N+1 or N+2 when a new CC value is written, a match may trigger on the previous CC value before the new value takes effect. If the current CC value greater than N+2 when the new value is written, there will be no event due to the old value.

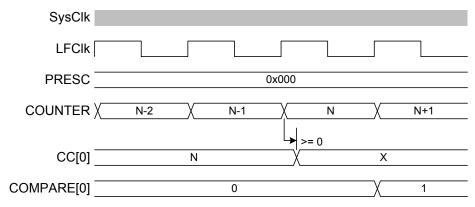


Figure 52: Timing diagram - COMPARE_N-1

25.8 TASK and EVENT jitter/delay

Jitter or delay in the RTC is due to the peripheral clock being a low frequency clock (LFCLK) which is not synchronous to the faster PCLK16M.

Registers in the peripheral interface, part of the PCLK16M domain, have a set of mirrored registers in the LFCLK domain. For example, the COUNTER value accessible from the CPU is in the PCLK16M domain and is latched on read from an internal register called COUNTER in the LFCLK domain. COUNTER is the register which is actually modified each time the RTC ticks. These registers must be synchronised between clock domains (PCLK16M and LFCLK).

The following is a summary of the jitter introduced on tasks and events. Figures illustrating jitter follow.



Table 45: RTC jitter magnitudes on tasks

 Task
 Delay

 CLEAR, STOP, START, TRIGOVRFLOW
 +15 to 46 μs

Table 46: RTC jitter magnitudes on events



1. CLEAR and STOP (and TRIGOVRFLW; not shown) will be delayed as long as it takes for the peripheral to clock a falling edge and rising of the LFCLK. This is between 15.2585 μ s and 45.7755 μ s – rounded to 15 μ s and 46 μ s for the remainder of the section.

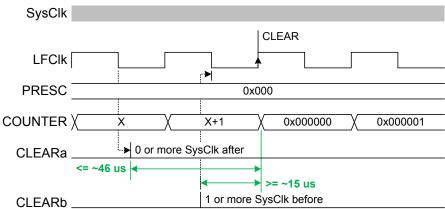


Figure 53: Timing diagram - DELAY_CLEAR

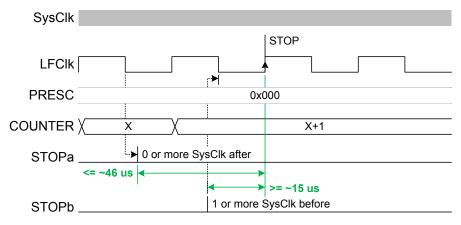


Figure 54: Timing diagram - DELAY_STOP

2. The START task will start the RTC. Assuming that the LFCLK was previously running and stable, the first increment of COUNTER (and instance of TICK event) will be typically after 30.5 μs +/-15 μs. In some cases, in particular if the RTC is STARTed before the LFCLK is running, that timing can be up to ~250 μs. The software should therefore wait for the first TICK if it has to make sure the RTC is running. Sending a TRIGOVRFLW task sets the COUNTER to a value close to overflow. However, since the update of COUNTER relies on a stable LFCLK, sending this task while LFCLK is not running will start LFCLK, but the update will then be delayed by the same amount of time of up to ~250 us. The figures show the smallest and largest delays to on the START task which appears as a +/-15 μs jitter on the first COUNTER increment.

Note: 32.768 kHz clock jitter is additional to the numbers provided above.

²² Assumes RTC runs continuously between these events.



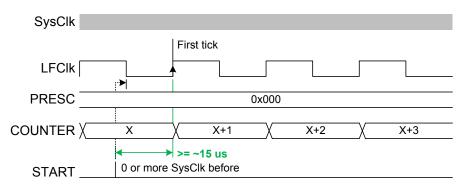


Figure 55: Timing diagram - JITTER_START-

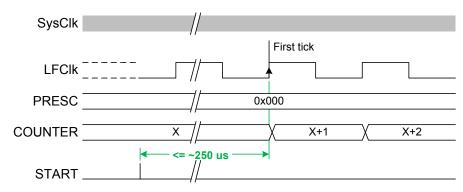


Figure 56: Timing diagram - JITTER_START+

25.9 Reading the COUNTER register

To read the COUNTER register, the internal <<COUNTER>> value is sampled.

To ensure that the <<COUNTER>> is safely sampled (considering an LFCLK transition may occur during a read), the CPU and core memory bus are halted for three cycles by lowering the core PREADY signal. The Read takes the CPU 2 cycles in addition resulting in the COUNTER register read taking a fixed five PCLK16M clock cycles.

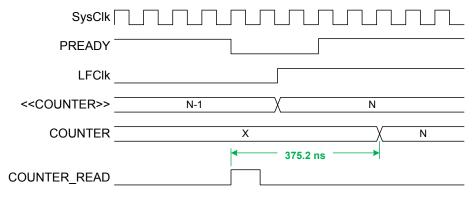


Figure 57: Timing diagram - COUNTER_READ

25.10 Registers

Table 47: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000B000	RTC	RTC0	Real-time counter 0	CC[02] implemented, CC[3] not
				implemented
0x40011000	RTC	RTC1	Real-time counter 1	CC[03] implemented



Base address	Peripheral	Instance	Description	Configuration
0x40024000	RTC	RTC2	Real-time counter 2	CC[03] implemented

Table 48: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start RTC COUNTER
TASKS_STOP	0x004	Stop RTC COUNTER
TASKS_CLEAR	0x008	Clear RTC COUNTER
TASKS_TRIGOVRFLW	0x00C	Set COUNTER to 0xFFFFF0
EVENTS_TICK	0x100	Event on COUNTER increment
EVENTS_OVRFLW	0x104	Event on COUNTER overflow
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
EVTEN	0x340	Enable or disable event routing
EVTENSET	0x344	Enable event routing
EVTENCLR	0x348	Disable event routing
COUNTER	0x504	Current COUNTER value
PRESCALER	0x508	12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)). Must be written when RTC is
		stopped
CC[0]	0x540	Compare register 0
CC[1]	0x544	Compare register 1
CC[2]	0x548	Compare register 2
CC[3]	0x54C	Compare register 3

25.10.1 INTENSET

Address offset: 0x304

Enable interrupt

		, intorrupt			
Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	TICK			Write '1' to Enable interrupt for TICK event
					See EVENTS_TICK
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	OVRFLW			Write '1' to Enable interrupt for OVRFLW event
					See EVENTS_OVRFLW
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	COMPARE0			Write '1' to Enable interrupt for COMPARE[0] event
					See EVENTS_COMPARE[0]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	COMPARE1			Write '1' to Enable interrupt for COMPARE[1] event
					See EVENTS_COMPARE[1]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled



Bit r	numbe	r		31	30 2	9 2	8 27	7 20	5 25	24	23 2	22 2	21 2	0 1	9 1	18 1	17 1	16	15 1	.4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	1	. 0
Id														F	FI	E	D	С													В	ВА
Res	et 0x0	0000000		0	0 () (0 0	0	0	0	0	0	0 () (0 (0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	otior	1																		
Ε	RW	COMPARE2									Writ	e '	1' to	En	abl	e ir	nter	rru	ot fo	or Co	IMC	PAR	E[2]	ev	ent							
											See	EV	ENT.	s_c	ON	1P.A	\RE	[2]														
			Set	1							Enal	ble																				
			Disabled	0							Rea	d: [Disal	oled	b																	
			Enabled	1							Rea	d: E	nab	led	ı																	
F	RW	COMPARE3									Writ	e '	1' to	En	abl	e ir	ntei	rru	ot fo	or Co	IMC	PAR	E[3]	ev	ent							
											See	EV	ENT.	s_c	ON	1P.A	NRE,	[3]														
			Set	1							Enal	ble																				
			Disabled	0							Rea	d: [Disal	oled	b																	
			Enabled	1							Rea	d: E	Enab	led	1																	

25.10.2 INTENCLR

Address offset: 0x308

Dis	sabl	e interrupt																														
Bitı	numb	er		31 30	29	9 28	3 27	26	25	24	23	22 2	21 20	0 19	18	17	16	15	14	13	12	11	10	9	8	7	6 !	5 4	4 3	2	1	0
Id														F	Ε	D	С														В	Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0 (0	0	0	0
Id	RW	Field	Value Id	Value	2					ı	Des	scrip	tion	ı																		
Α	RW	TICK								,	Wr	rite '1	1' to	Disa	able	inte	errı	upt	for	TIC	K e	/en	t									
												e <i>EVE</i>		_TIC	CK																	
			Clear	1						١	Dis	able																				
			Disabled	0						١	Rea	ad: D	isab	led																		
			Enabled	1						١	Rea	ad: E	nab	led																		
В	RW	OVRFLW								,	Wr	rite '1	1' to	Disa	able	inte	errı	upt	for	OV	RFL	W e	ever	nt								
										:	See	e <i>EVE</i>	ENTS	_ <i>o</i> v	/RFI	LW																
			Clear	1						١	Dis	able																				
			Disabled	0						١	Rea	ad: D	isab	led																		
			Enabled	1						١	Rea	ad: E	nab	led																		
С	RW	COMPARE0								١	Wr	rite '1	1' to	Disa	able	inte	errı	upt	for	СО	MP	ARE	[0]	eve	ent							
											See	e <i>EVE</i>	ENTS	_co	OMF	PARI	[0]	1														
			Clear	1						1	Dis	able																				
			Disabled	0						١	Rea	ad: D	isab	led																		
			Enabled	1						ı	Rea	ad: E	nab	led																		
D	RW	COMPARE1										rite '1							for	CO	MP	ARE	[1]	eve	ent							
										:	See	e <i>EVE</i>	ENTS	_ <i>co</i>	OMF	PARI	[1]	1														
			Clear	1						ı	Dis	able																				
			Disabled	0						ı	Rea	ad: D	isab	led																		
			Enabled	1						١	Rea	ad: E	nab	led																		
Ε	RW	COMPARE2								,	Wr	rite '1	1' to	Disa	able	inte	errı	upt	for	CO	MP	ARE	[2]	eve	ent							
											See	e <i>EVE</i>	ENTS	_co	OMF	PARI	E[2]	1														
			Clear	1						١	Dis	able																				
			Disabled	0						- 1	Rea	ad: D	isab	led																		
			Enabled	1							Rea	ad: E	nab	led																		
F	RW	COMPARE3								١	Wr	rite '1	1' to	Disa	able	inte	erri	upt	for	СО	MP	ARE	[3]	eve	ent							
										:	See	e <i>EVE</i>	ENTS	_cc	OMF	PARI	E[3]	1														
			Clear	1						- 1	Dis	able																				
			Disabled	0						ı	Rea	ad: D	isab	led																		
			Enabled	1						- 1	Rea	ad: E	nab	led																		



25.10.3 EVTEN

Address offset: 0x340

Enable or disable event routing

Reset 0x00000000000000000000000000000000000	Bit	numbe	er		31 30	29	28 27	7 26	25 :	24 2:	3 22	2 21 :	20	19	18 -	17	16	15	14	13	12 .	11 1	0 9	8	7	6	5	4	3 2) 1	0
Reset UNDOOOOOOOOOOOOOOOOOOOOOOOOOOOOOOOOOOOO	Id		•		31 30		20 2,				<i>-</i>								- '					Ŭ	•	Ŭ	J		٠.		
RW TICK Disabled 0 Disable Enable Compared		et 0x0	0000000		0 0	0	0 0	0	0	0 0	0	0	0					0	0	0	0	0 (0	0	0	0	0	0	0 (
See EVENTS_TICK Disabled 0 Disable Enabled 1 Enable RW OVRFLW Enabled 0 Disable Enabled 0 Disable Enable or disable event routing for OVRFLW event See EVENTS_OVRFLW Disabled 0 Disable Enable or disable event routing for COMPARE[0] event See EVENTS_COMPARE[0] Disabled 0 Disable Enable or disable event routing for COMPARE[1] event See EVENTS_COMPARE[1] Disabled 0 Disable Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled 0 Disable Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled 0 Disable Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled 0 Disable Enable or disable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disabled 0 Disable Enable or disable event routing for COMPARE[3] event	Id	RW	Field	Value Id	Value					D	esci	riptio	n																		
Disabled 0 Disable Enable 1 Enable Enable 1 Enable Disable event routing for OVRFLW event Enable or disable event routing for OVRFLW event Enable Disable Enable Disable Enable Disable Enable O Disable Enable Enable Enable Enable Enable Enable Enable Disable Enable En	Α	RW	TICK													ent	ro	utin	ng f	or T	ICK	eve	nt								
RW OVRFLW Disabled 1				Disabled	0								_		•																
RW OVRFLW Disabled Enabled Enable					1																										
See EVENTS_OVRFLW Disabled 0 Disable Enabled 1 Enable C RW COMPARE0 Disabled 0 Disable Enable or disable event routing for COMPARE[0] event See EVENTS_COMPARE[0] Disabled 0 Disable Enable or disable event routing for COMPARE[1] event See EVENTS_COMPARE[1] Disabled 0 Disable Enable or disable event routing for COMPARE[2] event Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled 0 Disable Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled 0 Disable Enable or disable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disabled 0 Disable Enable or disable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disabled 0 Disable	В	RW	OVRFLW							Er	nab	le or	dis	able	ev	ent	ro	utir	ng f	or C	VR	FLW	eve	ent							
Disabled 0 Disable Enabled 1 Enable C RW COMPAREO Disabled 0 Enable or disable event routing for COMPARE[0] event See EVENTS_COMPARE[0] Disabled 0 Disable Enable or disable event routing for COMPARE[0] event See EVENTS_COMPARE[0] Disabled 1 Enable or disable event routing for COMPARE[1] event See EVENTS_COMPARE[1] Disabled 0 Disable Enable event routing for COMPARE[2] event Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled 0 Disable Enable or disable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disabled 0 Disable Enable or disable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disabled 0 Disable																			•												
Enabled 1 Enable C RW COMPAREO Disabled 0 Disable Enable or disable event routing for COMPARE[0] event See EVENTS_COMPARE[0] Disabled 1 Enable Enable or disable event routing for COMPARE[1] event See EVENTS_COMPARE[1] Disabled 0 Disable Enable enabled 1 Enable Enable event routing for COMPARE[1] event See EVENTS_COMPARE[1] Disabled 1 Enable Enable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled 0 Disable Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled 1 Enable Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled 0 Disable Enable or disable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disabled 0 Disable				Disabled	0								15_	UVI	(FL)	vv															
Enable or disable event routing for COMPARE[0] event See EVENTS_COMPARE[0] Disabled Enabled Disabled Enabled Disabled Enable or disable event routing for COMPARE[1] event See EVENTS_COMPARE[1] Disabled Enabled Disable Enable Disable Enable Enable Disable Enable Disable Enable Disable																															
See EVENTS_COMPARE[0] Disabled Enabled 1 Enable Enable or disable event routing for COMPARE[1] event See EVENTS_COMPARE[1] Disabled Enabled 1 Enable Enable Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled Enable Enable Enable Enable Enable Enable Enable Enable Disable Disable Disabled Disable Disable Disable Disabled Disable	C	D\A/	COMPARIO	Enabled	1								di.	abla					f	~ · ·	-01	4DAI	יבנס	1	+						
Disabled 0 Disable Enabled 1 Enable COMPARE1 Disabled 0 Disable event routing for COMPARE[1] event See EVENTS_COMPARE[1] Disabled 0 Disable Enable or disable event routing for COMPARE[1] event See EVENTS_COMPARE[1] Enable or disable event routing for COMPARE[2] event Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled 0 Disable Enable Enable or disable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disabled 0 Disable	C	KVV	COMPAREO							EI	пар	ie or	uis	dDIE	ev	rent	10	utii	ıg ı	or C	.Oiv	IPAI	ELO	j ev	ent						
Enabled 1 Enable COMPARE1 Enable or disable event routing for COMPARE[1] event See EVENTS_COMPARE[1] Disabled 0 Disable Enable or disable event routing for COMPARE[1] event See EVENTS_COMPARE[1] Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled 0 Disable Enable Enable Enable Enable Enable Enable Enable Enable Disable Enable Disable Disable Disable Disable Disable Disable Disable Disable Disable										Se	ee E	VENT	TS_	COI	ЛΡΑ	ARE	[0]														
Enable or disable event routing for COMPARE[1] event See EVENTS_COMPARE[1] Disabled Enabled Enable Enable or disable event routing for COMPARE[1] event See EVENTS_COMPARE[1] Enable Enable Enable Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled Enable Enable Enable Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[3] Enable or disable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disabled Disable				Disabled	0					Di	isab	ole																			
See EVENTS_COMPARE[1] Disabled Enabled 1 Enable Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled Disabled Enabled 1 Enable Enable Enable Enable Enable Disable Enable Disable Enable Disable Disable Disable Disable Disable Disable Disable Disable Disable				Enabled	1					Er	nab	le																			
Disabled 0 Disable Enabled 1 Enable ENW COMPARE2 Enabled 0 Enable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled 0 Disable Enabled 1 Enable Enable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disabled 0 Disable Enable or disable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disabled 0 Disable	D	RW	COMPARE1							Er	nab	le or	dis	able	ev	ent	ro	utin	ng f	or C	ON	1PAF	RE[1] ev	ent						
Enabled 1 Enable RW COMPARE2 Enabled 5 Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled 0 Disable Enable Enable event routing for COMPARE[3] event Enable or disable event routing for COMPARE[3] event Enable or disable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disabled 0 Disable										Se	ee E	VENT	TS_	COI	ЛΡΑ	ARE	[1]														
Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[2] Disabled Enabled 1 Enable Enable or disable event routing for COMPARE[2] event See EVENTS_COMPARE[3] Disable Disable Disable Disable				Disabled	0					Di	isab	ole																			
See EVENTS_COMPARE[2] Disabled Enabled 1 Enable Enable or disable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disabled 0 Disable				Enabled	1					Er	nab	le																			
Disabled 0 Disable Enabled 1 Enable F RW COMPARE3 Figure 1	Ε	RW	COMPARE2							Er	nab	le or	dis	able	ev	ent	ro	utir	ng f	or C	ON	1PAF	RE[2] ev	ent						
Disabled 0 Disable Enabled 1 Enable F RW COMPARE3 Figure 1										Se	عم F	VENT	TC	COL	ЛD	ΔRF	[2]														
Enabled 1 Enable F RW COMPARE3 Enable or disable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disabled 0 Disable				Disabled	0									.001	,,,	7/12	[=]														
Enable or disable event routing for COMPARE[3] event See EVENTS_COMPARE[3] Disable Disable																															
See EVENTS_COMPARE[3] Disabled 0 Disable	F	RW/	COMPARE3	Lilabica	_								dis	ahle	ev	ent/	ro	ıtir	nσ f	or C	O.V.	ΛΡΔΕ	F[3	l ev	ent						
Disabled 0 Disable			55 / IIIE5																.6 '	٥. د		, (1	[3	,	2110						
													TS_	COI	ЛΡΑ	ARE	[3]														
Enabled 1 Enable																															
				Enabled	1					Er	nab	le																			

25.10.4 EVTENSET

Address offset: 0x344 Enable event routing

Bit r	iumbe	r		31	30 29	9 28	27	26 25	5 24	1 23 2	22 2	21 20	19	9 18	3 17	16	15	14	13 1	2 11	10	9	8	7	6 5	5 4	3	2	1 0
Id													F	E	D	С													ВА
Res	et 0x0	0000000		0	0 0	0	0	0 0	0	0 (0 (0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0 0	0	0	0 0
Id	RW	Field	Value Id	Val	lue					Desc	crip	tion																	
Α	RW	TICK								Writ	e '1	1' to	Ena	able	eve	ent	rou	ting	for T	ГІСК	eve	nt							
										See	EVE	ENTS	TI	ICK															
			Set	1						Enab	ble																		
			Disabled	0						Read	d: D	Disab	led	l															
			Enabled	1						Read	d: E	nabl	ed																
В	RW	OVRFLW								Writ	e '1	1' to	Ena	able	eve	ent	rou	ting	for (OVR	FLW	eve	ent						
										See	EVE	ENTS	_0	VRF	LW														
			Set	1						Enab	ble																		
			Disabled	0						Read	d: D	Disab	led	l															
			Enabled	1						Read	d: E	nabl	ed																
С	RW	COMPARE0								Writ	e '1	1' to	Ena	able	eve	ent	rou	ting	for (COM	PAR	E[0] eve	ent					
										See	EVE	ENTS	_C	ОМ	PAR	E[0]	1												
			Set	1						Enab	ble																		



Bit number		31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			F E D C
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW COMPARE1			Write '1' to Enable event routing for COMPARE[1] event
			See EVENTS_COMPARE[1]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW COMPARE2			Write '1' to Enable event routing for COMPARE[2] event
			See EVENTS_COMPARE[2]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
F RW COMPARE3			Write '1' to Enable event routing for COMPARE[3] event
			See EVENTS_COMPARE[3]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

25.10.5 EVTENCLR

Address offset: 0x348 Disable event routing

		r		31 30	29	28 2	7 2	26 25	5 24	23	22	2 21 :	20	19	18	17	16	15	14	13	12	11 1	.0 9	8 (7	6	5	4	3	2	1 0
Id														F	Ε	D	С													1	ВА
Rese	t 0x0	0000000		0 0	0	0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 0
ld	RW	Field	Value Id	Value						De	esci	riptio	n																		
A	RW	TICK								W	rite	e '1' t	0 [Disa	ble	ev	ent	rou	utin	g fo	r TIO	CK e	ven	t							
										Se	e E	VEN	TS_	TIC	K																
			Clear	1						Dis	sab	ole																			
			Disabled	0						Re	ad	: Disa	abl	ed																	
			Enabled	1						Re	ad	: Ena	ble	ed																	
В	RW	OVRFLW								Wr	rite	e '1' t	0 [Disa	ble	ev	ent	rou	utin	g fo	r 0\	/RFI	.W 6	ever	it						
										Se	e E	VEN	TS_	_Ov	'RFL	LW															
			Clear	1						Dis	sab	ole																			
			Disabled	0						Re	ad	: Disa	bl	ed																	
			Enabled	1						Re	ad	: Ena	ble	ed																	
С	RW	COMPARE0								Wr	rite	e '1' t	0 [Disa	ble	ev	ent	rou	utin	g fo	r CC	MP	ARE	[0]	evei	nt					
										Se	e E	VEN	TS_	_co	MP	PAR	E[0]													
			Clear	1						Dis	sab	ole																			
			Disabled	0						Re	ad	: Disa	abl	ed																	
			Enabled	1						Re	ead	: Ena	ble	ed																	
D	RW	COMPARE1								Wr	rite	e '1' t	0 [Disa	ble	ev	ent	rou	utin	g fo	r CC	MP	ARE	[1]	evei	nt					
										Se	e E	VEN	TS_	_co	MP	PAR	E[1]													
			Clear	1						Dis	sab	ole																			
			Disabled	0						Re	ad	: Disa	bl	ed																	
			Enabled	1						Re	ead	: Ena	ble	ed																	
E	RW	COMPARE2								W	rite	e '1' t	0 [Disa	ble	ev	ent	rou	utin	g fo	r CC	MP	ARE	[2]	evei	nt					
										Se	e E	VEN	TS_	_co	MP	PAR	E[2	1													
			Clear	1						Dis	sab	ole																			
			Disabled	0						Re	ad	: Disa	abl	ed																	
			Enabled	1						Re	ad	: Ena	ble	ed																	



Bit	numbe	er		3:	1 30	29	28	8 27	7 2	6 2	5 2	24 2	23	22	21	20	19	9 18	8 1	.7 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	F	Е	. 1	D	С															В	Α
Res	et 0x0	0000000		0	0	0	0	0	(0 () (0	0	0	0	0	0	0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	V	'alue)							Des	cri	pti	on																					
F	RW	COMPARE3										١	۷ri	ite	'1'	to I	Dis	abl	e e	eve	nt	rou	tin	g fo	or C	O۱	1PA	RE[3] 6	eve	nt						
												5	See	E١	/EN	TS_	_C(ЭМ	PA	RE	[3]																
			Clear	1								[Disa	abl	e																						
			Disabled	0								F	Rea	ıd:	Dis	abl	ed																				
			Enabled	1								F	Rea	ıd:	Ena	able	ed																				

25.10.6 COUNTER

Address offset: 0x504

Current COUNTER value

Bit	numb	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A	A A A A A A A A A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description	
Α	R	COUNTER		Counter value	

25.10.7 PRESCALER

Address offset: 0x508

12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)). Must be written when RTC is stopped

Bit	numbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	.0 9	9	8	7	6	5	4	3	2 :	1 0
Id																								Α	Δ ,	4	A	Α	Α	Α	Α	Α,	Δ ,	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																			
Α	RW	PRESCALER										Pre	sca	ler	valı	ue																		

25.10.8 CC[0]

Address offset: 0x540 Compare register 0

Bit nu	ımbe	r		31	L 30	29	2	8 2	7 2	6 2	5 2	24 2	3 :	22 :	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1)
Id													Д	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A	A
Reset	t 0x0	0000000		0	0	0	0) () () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	Va	alu	е							es	crip	otic	n																				
Α	RW	COMPARE										(on	npa	re v	valı	ue																			

25.10.9 CC[1]

Address offset: 0x544 Compare register 1

Bit r	numbe	er		31 30 29 28 27	26 25 24 2	3 22 21	. 20 1	9 18 :	17 16	5 15 3	L4 13	12	11 10	9	8	7	6	5	4 3	3 2	1 0
Id					A	. A A	A A	A	A A	Α	А А	Α	A A	Α	Α	Α	Α	Α	A A	4 A	АА
Res	et 0x0	0000000		0 0 0 0 0	0 0 0 0	0 0	0 0	0	0 0	0	0 0	0	0 0	0	0	0	0	0	0 (0 0	0 0
Id	RW	Field	Value Id	Value	D	escript	ion														
Α	RW	COMPARE			C	ompare	value														

25.10.10 CC[2]

Address offset: 0x548 Compare register 2



Bit r	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue	•						Des	cri	ptic	on																			
Α	RW	COMPARE										Cor	npa	are	valı	ue																		

25.10.11 CC[3]

Address offset: 0x54C Compare register 3

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ <i>A</i>	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																			
Α	RW	COMPARE										Со	mp	are	va	ue																		

25.11 Electrical specification

25.11.1 RTC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
Іртс	Run current Real Time Counter (LECLK source)		0.1		пА



26 RNG — Random number generator

The Random number generator (RNG) generates true non-deterministic random numbers based on internal thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

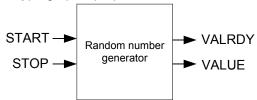


Figure 58: Random number generator

The RNG is started by triggering the START task and stopped by triggering the STOP task. When started, new random numbers are generated continuously and written to the VALUE register when ready. A VALRDY event is generated for every new random number that is written to the VALUE register. This means that after a VALRDY event is generated the CPU has the time until the next VALRDY event to read out the random number from the VALUE register before it is overwritten by a new random number.

26.1 Bias correction

A bias correction algorithm is employed on the internal bit stream to remove any bias toward '1' or '0'. The bits are then queued into an eight-bit register for parallel readout from the VALUE register.

It is possible to enable bias correction in the CONFIG register. This will result in slower value generation, but will ensure a statistically uniform distribution of the random values.

26.2 Speed

The time needed to generate one random byte of data is unpredictable, and may vary from one byte to the next. This is especially true when bias correction is enabled.

26.3 Registers

Table 49: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000D000	RNG	RNG	Random number generator	

Table 50: Register Overview

Register	Offset	Description
TASKS_START	0x000	Task starting the random number generator
TASKS_STOP	0x004	Task stopping the random number generator
EVENTS_VALRDY	0x100	Event being generated for every new random number written to the VALUE register
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CONFIG	0x504	Configuration register
VALUE	0x508	Output random number

26.3.1 SHORTS

Address offset: 0x200 Shortcut register



В	t nu	ımbe	r		31	1 30	29	28	3 27	7 26	25	24	23	22	21	20	19 1	18 :	17 1	6 1	.5 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																																		Α
R	eset	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 () (0	0	0	0	0	0	0	0	0	0 (0	0
Id	l	RW	Field	Value Id	Va	alue							De	scri	ptic	n																		
Α		RW	VALRDY_STOP										Sh	orto	ut b	etv	vee	n V	ALR	DY	eve	nt a	nd :	STO	P ta	sk								
													Se	e <i>EV</i>	/EN	TS_	VAL	RD	Y an	d 7.	ASK	:S_S	TOF	•										
				Disabled	0								Dis	abl	e sh	ort	cut																	
				Enabled	1								En	able	sho	orto	cut																	

26.3.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31 3	0 29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2	1 0
Id																																	Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) (0 (0 0
Id	RW	Field	Value Id	Valu	e						De	scr	ipti	on																			
Α	RW	VALRDY									Wı	rite	'1'	to E	nab	le i	nte	rru	pt f	or \	/AL	RD	Y ev	ent									
											Se	e <i>E</i>	VEN	TS_	VAL	.RD	Υ																
			Set	1							En	abl	e																				
			Disabled	0							Re	ad:	Dis	able	ed																		
			Enabled	1							Re	ad:	Ena	ble	d																		

26.3.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	iumbe	r		31	. 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 1	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																																	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	VALRDY										Wr	ite	'1' t	to D	Disa	ble	int	erru	ıpt	for	VAI	.RD	Y ev	ent								
												See	e EV	/EN	TS_	VA.	LRE	ŊΥ															
			Clear	1								Dis	able	e																			
			Disabled	0								Rea	ad:	Disa	able	ed																	
			Enabled	1								Rea	ad:	Ena	ble	d																	

26.3.4 CONFIG

Address offset: 0x504 Configuration register

Bit	numbe	r		3:	1 30	29	28	3 27	7 26	5 25	5 24	23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	•						De	escr	ipti	on																			
Α	RW	DERCEN										Bia	as c	orre	ecti	on																		
			Disabled	0								Di	sab	led																				
			Enabled	1								En	abl	ed																				

26.3.5 VALUE

Address offset: 0x508

Output random number



Bit number		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A R VALUE		[0255]	Generated random number

26.4 Electrical specification

26.4.1 RNG Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{RNG}	Run current, CPU sleeping.		500		μΑ
t _{RNG,START}	Time from setting the START task to generation begins. This is		128		μs
	a one-time delay on START signal and does not apply between				
	samples.				
t _{RNG,RAW}	Run time per byte without bias correction. Uniform distribution		30		μs
	of 0 and 1 is not guaranteed.				
t _{RNG,BC}	Run time per byte with bias correction. Uniform distribution		120		μs
	of 0 and 1 is guaranteed. Time to generate a byte cannot be				
	guaranteed.				



27 TEMP — Temperature sensor

The temperature sensor measures die temperature over the temperature range of the device. Linearity compensation can be implemented if required by the application.

Listed here are the main features for TEMP:

- Temperature range is greater than or equal to operating temperature of the device
- Resolution is 0.25 degrees

TEMP is started by triggering the START task.

When the temperature measurement is completed, a DATARDY event will be generated and the result of the measurement can be read from the TEMP register.

To achieve the measurement accuracy stated in the electrical specification, the crystal oscillator must be selected as the HFCLK source, see *CLOCK* — *Clock control* on page 101 for more information.

When the temperature measurement is completed, TEMP analog electronics power down to save power.

TEMP only supports one-shot operation, meaning that every TEMP measurement has to be explicitly started using the START task.

27.1 Registers

Table 51: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000C000	TEMP	TEMP	Temperature sensor	

Table 52: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start temperature measurement
TASKS_STOP	0x004	Stop temperature measurement
EVENTS_DATARDY	0x100	Temperature measurement complete, data ready
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
TEMP	0x508	Temperature in °C (0.25° steps)
A0	0x520	Slope of 1st piece wise linear function
A1	0x524	Slope of 2nd piece wise linear function
A2	0x528	Slope of 3rd piece wise linear function
A3	0x52C	Slope of 4th piece wise linear function
A4	0x530	Slope of 5th piece wise linear function
A5	0x534	Slope of 6th piece wise linear function
B0	0x540	y-intercept of 1st piece wise linear function
B1	0x544	y-intercept of 2nd piece wise linear function
B2	0x548	y-intercept of 3rd piece wise linear function
В3	0x54C	y-intercept of 4th piece wise linear function
B4	0x550	y-intercept of 5th piece wise linear function
B5	0x554	y-intercept of 6th piece wise linear function
то	0x560	End point of 1st piece wise linear function
T1	0x564	End point of 2nd piece wise linear function
T2	0x568	End point of 3rd piece wise linear function
<i>T3</i>	0x56C	End point of 4th piece wise linear function
T4	0x570	End point of 5th piece wise linear function



27.1.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	numbe	er		31	1 30	29	2	8 2	7 2	26 :	25	24	23	22	21	L 20	1	9 1	8 :	17	16	15	14	13	3 12	2 1:	1 1	9	8	7	6	5	4	3	2	1	0
Id																																					Α
Res	et 0x0	0000000		0	0	0	C	0)	0	0	0	0	0	0	0	C) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	:							De	scr	ipt	ion																					
Α	RW	DATARDY											Wı	rite	'1'	to	En	abl	e ii	nte	rru	pt	for	DΑ	TΑ	RD	Y e	ent/	t								
													Se	e <i>E</i>	VEI	NTS	_D	AT.	4R	DΥ																	
			Set	1									En	abl	e																						
			Disabled	0									Re	ad:	Di	sab	led	ł																			
			Enabled	1									Re	ad:	En	abl	ed																				

27.1.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bitı	numbe	er		31	30	29	28	3 27	7 26	5 25	5 24	4 2	3 2	22	21	20	19	18	3 1	.7 1	.6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																					Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0) (0 (0	0	0	0	0	(0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							C	es	crip	ptio	on																					
Α	RW	DATARDY										٧	Vrit	e '	1'1	to [Disa	able	e iı	nte	rru	pt	for	DA	TAI	RDY	ev	ent									
												S	ee	EV	ΈN	TS_	DA	4 <i>T</i> /	\RL	ΟY																	
			Clear	1								C	isa	ble	ē																						
			Disabled	0								R	lead	d: [Dis	abl	ed																				
			Enabled	1								R	lead	d: E	Ena	able	ed																				

27.1.3 TEMP

Address offset: 0x508

Temperature in °C (0.25° steps)

Bit	numbe	er		31	30	29	28	27	26 2	25 2	4 2	3 22	2 21	20	19	18	17	16	15	14	13 1	2 11	1 10	9	8	7	6	5 4	1 3	2	1	0
Id				Α	Α	Α	Α	Α	Α .	A A	4 Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	А	Α	Α	Α	Α.	A A	Α Α	A	Α	Α
Re	et 0x0	0000000		0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0) 0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	ripti	on																		
Α	R	TEMP									Te	emp	era	tur	e in	°C	(0.2	!5° s	step	s)												
													lt of olem		•							. Die	tem	ipei	ratu	re ii	n °C	, 2's	5			
											D	ecis	ion	poi	nt: l	DA1	TAR	DY														

27.1.4 A0

Address offset: 0x520

Slope of 1st piece wise linear function

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11	10 9 8 7 6 5 4 3 2 1 0
Id			Α	A A A A A A A A A A
Reset 0x00000320		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 0 0 1 0 0 0 0 0
ld RW Field	Value Id	Value	Description	
A RW A0			Slope of 1st piece wise linear function	

27.1.5 A1

Address offset: 0x524



Slope of 2nd piece wise linear function

Bit	numb	er		31 30	29	28 2	7 26	25	24	23 :	22 2	1 2	0 19	9 18	17	16	15	14	13 1	2 11	. 10	9	8	7	6	5 4	4 3	2	1	0
Id																				Α	Α	Α	Α	Α	Α	A	4 А	Α	Α	Α
Re	set 0x0	00000343		0 0	0	0 (0 0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0	0	1	1	0	1	0	0 0	0	1	1
Id	RW	Field	Value Id	Value						Des	crip	tior	1																	
Α	RW	A1								Slor	oe of	f 2n	d pi	ece	wis	e lii	neai	r fur	nctic	n										

27.1.6 A2

Address offset: 0x528

Slope of 3rd piece wise linear function

Bitı	numbe	er		31	30 2	9	28	27 :	26	25	24	23 2	22 2	21 2	20 1	.9 1	8 1	7 1	6 15	5 14	1 13	3 12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id																							Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	4 A
Res	et 0x0	000035D		0	0	0	0	0	0	0	0	0	0 (0 (0	0 () (0	0	0	0	0	0	0	1	1	0	1	0	1	1	1 (0 1
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	A2									:	Slop	e o	f 3r	d p	iece	wi	se l	inea	ır fu	ınct	ion											

27.1.7 A3

Address offset: 0x52C

Slope of 4th piece wise linear function

Bitı	numb	er		31	30 2	9 :	28 27	7 26	25	24	23 :	22 2	21 2	20 1	9 1	8 17	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id																						Α	Α	Α	Α	Α	Α	Α	Α.	A A	A A	А
Res	et 0x0	0000400		0	0)	0 0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	1	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	tio	n																		
Α	RW	A3									Slot	oe o	f 4t	h n	iece	wis	se li	nea	r fu	ncti	ion											

27.1.8 A4

Address offset: 0x530

Slope of 5th piece wise linear function

Di	t nı	ım	har					21	20 ·	o -	າວາ	7 26	25	24	22 °	י י	1 2/	10	10	17	16	10	11.	10 1	2 11	10	0	0	7	6	С	1	2	· ·	1 0
ы	L III	ullii	bei					31	. 30 2	. כ	20 2	20	23	24	23 2	-2 2	1 21	J 15	10	1/	10	13	14.	19 1	2 11	. 10	9	0	/	U	J	4	3	۷.	1 0
Id																									Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	А А
Re	ese	t 0	x00	00047F				0	0	0	0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	1	0	0	0	1	1	1	1	1 :	1 1
Id		RV	V	Field		Value Id		Va	lue						Des	crip	tion	ı																	
Α	ld RW Field Value Id Value A RW A4												Slop	e of	f 5th	n pie	ce	wise	lin	ear	fun	ctio	n												

27.1.9 A5

Address offset: 0x534

Slope of 6th piece wise linear function

Bit number		31 30 29 28 27 26	$25\ 24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ \ 9$	8 7 6 5 4 3 2 1 0
Id			A A A	A A A A A A A A
Reset 0x0000037B		0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	1 0 1 1 1 1 0 1 1
ld RW Field	Value Id	Value	Description	
A RW A5			Slope of 6th piece wise linear function	

27.1.10 B0

Address offset: 0x540

y-intercept of 1st piece wise linear function



Bitı	numbe	er		31	30 2	9 2	28 2	27 26	5 25	5 24	23	22	21	20 :	19 1	l8 1	7 1	6 1	5 14	13	12	11	10	9	8	7	6	5	4	3 :	2 1	L 0
Id																				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 Α	A A
Res	et 0x0	0003FCC		0	0	0	0	0	0	0	0 (0	0	0	1	1	1	1	1	1	1	1	0	0	1 :	1 (0					
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																												
Α	RW	В0		Value Description y-intercept of 1st piece wise linear function																												

27.1.11 B1

Address offset: 0x544

y-intercept of 2nd piece wise linear function

Bit n	umbe	er		31	30 2	9 2	28 2	7 26	25	24	23	22 :	21 2	20 1	9 1	8 1	7 10	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id																				Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 A	Α	Α
Rese	t 0x0	0003F98		0 0 0 0 0 0 0 0 0 0											0 () (0	0	0	1	1	1	1	1	1	1	0	0	1	1 0	0	0
Id	RW	Field	Value Id	Val	ue						Des	crip	otio	n																		
Α	RW	B1		Value Id Value Description y-intercept of 2nd piece wise linear function																												

27.1.12 B2

Address offset: 0x548

y-intercept of 3rd piece wise linear function

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id				A A A A A	A A A A A A A A
Reset 0x00003F98		0 0 0 0 0	0 0 0 0 0 0 0 0 0	000011111	1 1 0 0 1 1 0 0 0
Id RW Field	Value Id	Value	Description		
A RW B2			y-intercept of 3rd pie	ece wise linear function	

27.1.13 B3

Address offset: 0x54C

y-intercept of 4th piece wise linear function

Bit r	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	! 1	1 0
Id																						Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A		4 A
Res	et 0x0	0000012		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0 0) 1	1 0
Id	RW	Field	Value Id	Va	alue							Des	cri	otic	n																			
Α	RW	В3										y-ir	iter	сер	t o	f 4t	h p	iece	e w	ise l	ine	ar f	unc	tio	n									

27.1.14 B4

Address offset: 0x550

y-intercept of 5th piece wise linear function

Bit number		31 3	0 29	28	27 2	26 2	5 2	4 2	3 22	2 21	20	19	18	17	16	15	14 :	13 :	12 1	.1 1	0 9	9 8	3 7	6	5	4	3	2	1)
Id																		Α	Α.	Δ ,	A A	A A	A A	. A	A	Α	Α	Α	Α	Δ
Reset 0x0000006A		0 (0 0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	1	1	0	1	0	1	0
ld RW Field	Value Id	Valu	e					D	esc	ripti	ion																			
A RW B4								у-	inte	erce	pt (of 5	th p	iece	e wi	ise I	ine	ar f	unc	tion										7

27.1.15 B5

Address offset: 0x554

y-intercept of 6th piece wise linear function

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id				$A \; A \; A \; A \; A \; A$	A A A A A A A A
Reset 0x00003DD0		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 1 1 1 1 0	1 1 1 0 1 0 0 0 0
Id RW Field	Value Id	Value	Description		
A RW B5			y-intercept of 6th pied	ce wise linear function	

y-intercept of 6th piece wise linear function



27.1.16 TO

Address offset: 0x560

End point of 1st piece wise linear function

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 1	19 18 17 16	5 15 14 13	3 12 11 10	9 8	7	6	5 4	3	2 1	0
Id								Α	Α	ΑА	Α.	A A	Α
Reset 0x000000E2		0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0	0 0 0	0 0 0	0 0	1	1	1 0	0	0 1	0
Id RW Field	Value Id	Value	Description										
A RW TO			End point of 1	st piece wi	se linear f	unction							

27.1.17 T1

Address offset: 0x564

End point of 2nd piece wise linear function

Bit r	numbe	er		31	30 2	9 2	28 2	27 2	26 2	25 2	24	23 :	22	21 2	20 1	9 1	8 1	7 1	.6 1	15 1	14 1	L3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0	ĺ
Id																											Α	Α	Α	Α	Α	Α	А А	l
Res	et 0x0	0000000		0 0 0									0	0	0	0 (0	0 (0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	ı
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																			l
Α	RW	T1	Value Id Value Description End point of 2nd piece wise linear function																															

27.1.18 T2

Address offset: 0x568

End point of 3rd piece wise linear function

Bit	numbe	er		31	30 2	9 :	28	27 2	26 2	25 2	24 :	23 :	22 2	21 2	20 1	9 1	8 1	17 1	6 1	5 1	4 1	3 1	2 1:	10	9	8	7	6	5	4	3	2	1 0	ı
Id																											Α	Α	Α	Α	A	Δ,	А А	
Res	et 0x0	0000014		0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0 (0 (0 (0	0	0	0	0	0	0	0	1	0	1 (0 0	
Id	RW	Field	Value Id	Va	lue						1	Des	crip	tio	n																			ı
Α	RW	T2									- 1	End	poi	int	of 3	rd p	oied	e v	/ise	lin	ear	fun	ctio	n										1

27.1.19 T3

Address offset: 0x56C

End point of 4th piece wise linear function

Bit r	umbe	r		31	30	29 2	28 2	7 26	25	24	23	22 2	21 2	0 1	9 18	3 17	16	15	14 1	3 12	11	10	9	8	7 (5 5	4	3	2	1 0
Id																									4 /	4 A	Α	Α .	A .	А А
Rese	et 0x00	0000019		0	0	0	0 (0	0	0	0	0	0 (0 (0	0	0	0	0 (0	0	0	0	0) (0 0	1	1	0	0 1
Id	RW	Field	Value Id	Val	lue						Des	crip	tio	n																
Α	RW	T3									End	ро	int o	of 41	th p	iece	wis	e lir	ear	func	tion	1								

27.1.20 T4

Address offset: 0x570

End point of 5th piece wise linear function

Bit number	31	1 30 29 28 27	26 25	24 23	3 22 2	1 20	19 1	8 17	16	15 14	1 13	12 13	10	9	8 7	6	5	4	3 2	1	0
Id															Α	Α	Α	A	A А	Α	Α
Reset 0x00000050	0	0 0 0 0	0 0	0 0	0 (0 0	0 (0 0	0	0 0	0	0 0	0	0	0 0	1	0	1 (0 0	0	0
ld RW Field V	alue Id Va	alue		De	escrip	tion															
A RW T4				Er	ıd poi	nt of	5th p	iece	wise	e line	ar fu	ınctio	n								



27.2 Electrical specification

27.2.1 Temperature Sensor Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{TEMP}	Time required for temperature measurement		36		μs
T _{TEMP,RANGE}	Temperature sensor range	-40		85	°C
T _{TEMP,ACC}	Temperature sensor accuracy	-5		5	°C
T _{TEMP,RES}	Temperature sensor resolution		0.25		°C
T _{TEMP,STB}	Sample to sample stability at constant device temperature		+/-0.25		°C
T _{TEMP,OFFST}	Sample offset at 25°C	-2.5		2.5	°C



28 ECB — AES electronic codebook mode encryption

The AES electronic codebook mode encryption (ECB) can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. The ECB encryption block supports 128 bit AES encryption (encryption only, not decryption).

AES ECB operates with EasyDMA access to system Data RAM for in-place operations on cleartext and ciphertext during encryption. ECB uses the same AES core as the CCM and AAR blocks and is an asynchronous operation which may not complete if the AES core is busy.

AES ECB features:

- 128 bit AES encryption
- · Supports standard AES ECB block encryption
- Memory pointer support
- · DMA data transfer

AES ECB performs a 128 bit AES block encrypt. At the STARTECB task, data and key is loaded into the algorithm by EasyDMA. When output data has been written back to memory, the ENDECB event is triggered.

AES ECB can be stopped by triggering the STOPECB task.

28.1 Shared resources

The ECB, CCM, and AAR share the same AES module. The ECB will always have lowest priority and if there is a sharing conflict during encryption, the ECB operation will be aborted and an ERRORECB event will be generated.

28.2 EasyDMA

The ECB implements an EasyDMA mechanism for reading and writing to the Data RAM. This DMA cannot access the program memory or any other parts of the memory area except RAM.

If the ECBDATAPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

The EasyDMA will have finished accessing the Data RAM when the ENDECB or ERRORECB is generated.

28.3 ECB data structure

Input to the block encrypt and output from the block encrypt are stored in the same data structure. ECBDATAPTR should point to this data structure before STARTECB is initiated.

Table 53: ECB data structure overview

Property	Address offset	Description
KEY	0	16 byte AES key
CLEARTEXT	16	16 byte AES cleartext input block
CIPHERTEXT	32	16 byte AES ciphertext output block



28.4 Registers

Table 54: Instances

Base address	Peripheral	Instance	Description	Configuration			
0x4000E000	ECB	ECB	AES Electronic Code Book (ECB) mode				
			block encryption				

Table 55: Register Overview

Register	Offset	Description
TASKS_STARTECB	0x000	Start ECB block encrypt
TASKS_STOPECB	0x004	Abort a possible executing ECB operation
EVENTS_ENDECB	0x100	ECB block encrypt complete
EVENTS_ERRORECB	0x104	ECB block encrypt aborted because of a STOPECB task or due to an error
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ECBDATAPTR	0x504	ECB block encrypt memory pointers

28.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit n	umbe	r		31	30 :	29 2	28 2	7 2	6 2	5 24	4 2	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id																																В	Α
Rese	t 0x0	0000000		0	0	0	0 (0 (0 0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Val	ue						D	escr	ipti	on																			
Α	RW	ENDECB									V	√rite	'1'	to E	Ena	ble	inte	erru	pt	for	ENI	DEC	Ве	ven	t								
											S	ee <i>E</i>	VΕN	ITS_	EΝ	DE	СВ																
			Set	1							Е	nabl	e																				
			Disabled	0							R	ead:	Dis	abl	ed																		
			Enabled	1							R	ead:	Ena	able	ed																		
В	RW	ERRORECB									V	√rite	'1'	to E	Ena	ble	inte	erru	pt	for	ERF	ROR	ECE	3 ev	ent	t							
											S	ee <i>E</i> '	VΕN	ITS_	_ER	ROI	REC	В															
			Set	1							E	nabl	e																				
			Disabled	0							R	ead:	Dis	abl	ed																		
			Enabled	1							R	ead:	Ena	able	ed																		

28.4.2 INTENCLR

Address offset: 0x308 Disable interrupt

Bit	numbe	r		31	. 30 2	9 2	28 2	7 2	6 25	5 24	23	22	21 2	0 1	19 1	8 1	.7 1	6 1	5 1	4 1	3 1	2 1	1 1	0 9	8	7	6	5	4	3 2	1	0
Id																															В	Α
Res	et 0x0	0000000		0	0	0	0 0) (0	0	0	0	0 ()	0 () (0 () () (0) (0) (0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						De	scri	ption	1																		
Α	RW	ENDECB									Wr	rite '	'1' to	Di	sab	le i	nter	rup	ot fo	or E	ND	ECE	ev	ent								
											See	e <i>EV</i>	ENT.	S_E	ND	ECE	3															
			Clear	1							Dis	able	e																			
			Disabled	0							Rea	ad: I	Disal	ole	d																	
			Enabled	1							Rea	ad: I	Enab	led	ł																	
В	RW	ERRORECB									Wr	rite '	'1' to	Di	sab	le i	nter	rup	ot fo	or E	RRO	ORE	СВ	eve	nt							
											See	e <i>EV</i>	ENT.	S_E	RR	ORE	СВ															
			Clear	1							Dis	able	е																			
			Disabled	0							Rea	ad: I	Disal	ole	d																	

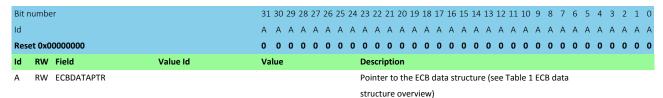


Bit number	31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		B A
Reset 0x00000000	0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field Value Id	Value	Description
Enabled	1	Read: Enabled

28.4.3 ECBDATAPTR

Address offset: 0x504

ECB block encrypt memory pointers



28.5 Electrical specification

28.5.1 ECB Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{FCB}	Run time per 16 byte block in all modes		6		μs



29 CCM — AES CCM mode encryption

Cipher block chaining - message authentication code (CCM) mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer. CCM combines counter mode encryption and CBC-MAC authentication. The CCM terminology "Message authentication code (MAC)" is called the "Message integrity check (MIC)" in 'Bluetooth terminology and also in this document.

The CCM block generates an encrypted keystream that is applied to input data using the XOR operation and generates the 4 byte MIC field in one operation. The CCM and radio can be configured to work synchronously. The CCM will encrypt in time for transmission and decrypt after receiving bytes into memory from the Radio. All operations can complete within the packet RX or TX time. CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF *RFC3610*, and depends on the AES-128 block cipher. A description of the CCM algorithm can also be found in *NIST Special Publication 800-38C*. The *Bluetooth* specification describes the configuration of counter mode blocks and encryption blocks to implement compliant encryption for BLE.

The CCM block uses EasyDMA to load key, counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

The AES CCM supports three operations: key-stream generation, packet encryption, and packet decryption. All these operations are done in compliance with the *Bluetooth* specification. ²³A new key-stream must be generated before a new packet encryption or packet decryption operation can be started.

A key-stream is generated by triggering the KSGEN task. An ENDKSGEN event will be generated when the new key-stream has been generated. The key-stream will be stored in the AES CCM's temporary memory area, specified by the SCRATCHPTR, where it will be used in subsequent encryption and decryption operations.

Encryption is started by triggering the CRYPT task with the MODE register set to ENCRYPTION. Similarly, decryption is started by triggering the same task with MODE set to DECRYPTION. An ENDCRYPT event will be generated when packet encryption is completed as well as when packet decryption is completed, see *Figure 59: Key-stream generation followed by encryption or decryption. The shortcut is optional.* on page 267.

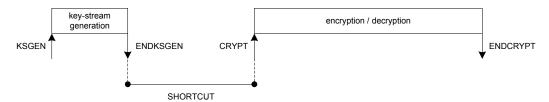


Figure 59: Key-stream generation followed by encryption or decryption. The shortcut is optional.

Key-stream generation, packet encryption, and packet decryption operations utilize the configuration specified in the data structure pointed to by the CNFPTR pointer. It is necessary to configure this pointer and its underlying data structure, and the MODE register before the KSGEN task is triggered. It is also necessary to configure the INPTR pointer and the OUTPTR pointer before the CRYPT task is triggered.

If a shortcut is used between ENDKSGEN event and CRYPT task, the INPTR pointer and the OUTPTR pointer must be configured before the KSGEN task is triggered.

The AES CCM supports different packet lengths, this is configured via the PACKETLENGTH field in the MODE register.

Bluetooth AES CCM 128 bit block encryption, see Bluetooth Core specification Version 4.0.



29.1 Shared resources

The CCM shares registers and other resources with other peripherals that have the same ID as the CCM. The user must therefore disable all peripherals that have the same ID as the CCM before the CCM can be configured and used.

Disabling a peripheral that have the same ID as the CCM will not reset any of the registers that are shared with the CCM. It is therefore important to configure all relevant CCM registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 24 for details on peripherals and their IDs.

29.2 Encryption

During packet encryption, the AES CCM will read the unencrypted packet located in RAM at the address specified in the INPTR pointer, encrypt the packet and append a four byte long Message Integrity Check (MIC) field to the packet.

The AES CCM will also modify the length field of the packet to adjust for the appended MIC field, that is, add four bytes to the length, and store the resulting packet back into RAM at the address specified in the OUTPTR pointer, see *Figure 60: Encryption* on page 268.

Empty packets (length field is set to 0) will not be encrypted but instead moved unmodified through the AES CCM.

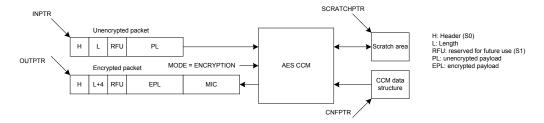


Figure 60: Encryption

29.3 Decryption

During packet decryption, the AES CCM will read the encrypted packet located in RAM at the address specified in the INPTR pointer, decrypt the packet, authenticate the packet's MIC field and generate the appropriate MIC status.

The AES CCM will also modify the length field of the packet to adjust for the MIC field, that is, subtract four bytes from the length, and then store the decrypted packet into RAM at the address pointed to by the OUTPTR pointer, see *Figure 61: Decryption* on page 269.

The CCM is only able to decrypt packets that are at least 5 bytes long, that is, 1 byte or more encrypted payload (EPL) and 4 bytes of MIC. The CCM will therefore generate a MIC error for packets where the length field is set to 1, 2, 3 or 4.

Empty packets (length field is set to 0) will not be decrypted but instead moved unmodified through the AES CCM, these packets will always pass the MIC check.



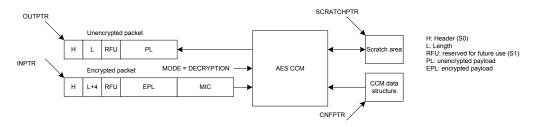


Figure 61: Decryption

29.4 AES CCM and RADIO concurrent operation

The AES CCM is designed to run in parallel with the RADIO to enable on-the-fly encryption and decryption of RADIO packets without CPU involvement. To facilitate this, the RADIO has to be configured with specific settings.

Table 56: Radio configuration settings

Radio parameter	Value	Description
PCNF0.S0LEN	1	Length of HEADER field in: <i>Table 58: Data structure for unencrypted packet</i> on page 271 and <i>Table 59: Data structure for encrypted packet</i> on page 271.
PCNF0.LFLEN	5 or 8	Length of LENGTH field in: <i>Table 58: Data structure for unencrypted packet</i> on page 271 and <i>Table 59: Data structure for encrypted packet</i> on page 271.
PCNF0.S1LEN	3 or 0	Length of the RFU field in: Table 58: Data structure for unencrypted packet on page 271 and Table 59: Data structure for encrypted packet on page 271. The combined length of LENGTH and RFU must always be 8 bit.
PCNF0.S1	Include	Always include the S1 field (RFU field) in RAM to secure that the same data structure can be used for PCNF0.S1LEN = 3 and PCNF0.S1LEN = 0: Table 58: Data structure for unencrypted packet on page 271 and Table 59: Data structure for encrypted packet on page 271.
MODE	Ble_1Mbit	Data rate. Must match CCM->MODE.DATARATE
PCNF1.BALEN	3	Length of address (32 bit)
CRCCNF.LEN	3	Length of CRC (24 bit)

29.5 Encrypting packets on-the-fly in radio transmit mode

When the AES CCM is encrypting a packet on-the-fly at the same time as the RADIO is transmitting it, the RADIO must read the encrypted packet from the same memory location as the AES CCM is writing to.

The OUTPTR pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the RADIO, see *Figure 62: Configuration of on-the-fly encryption* on page 269.

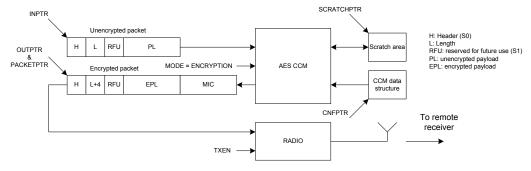


Figure 62: Configuration of on-the-fly encryption

In order to match the RADIO's timing, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered, in addition the shortcut between the ENDKSGEN event and the CRYPT task must be enabled. This use-case is illustrated in *Figure 63: On-the-fly encryption using a PPI connection* on page 270 using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM.



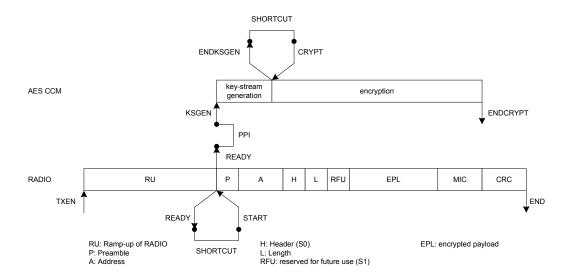


Figure 63: On-the-fly encryption using a PPI connection

29.6 Decrypting packets on-the-fly in radio receive mode

When the AES CCM is decrypting a packet on-the-fly at the same time as the RADIO is receiving it, the AES CCM must read the encrypted packet from the same memory location as the RADIO is writing to.

The INPTR pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the RADIO, see *Figure 64: Configuration of on-the-fly decryption* on page 270.

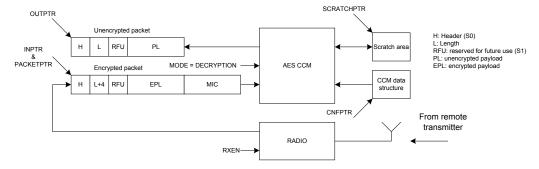


Figure 64: Configuration of on-the-fly decryption

In order to match the RADIO's timing, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered. In addition, the CRYPT task must be triggered no earlier than when the ADDRESS event is generated by the RADIO.

If the CRYPT task is triggered exactly at the same time as the ADDRESS event is generated by the RADIO, the AES CCM will guarantee that the decryption is completed no later than when the END event in the RADIO is generated.

This use-case is illustrated in *Figure 65: On-the-fly decryption using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM* on page 271 using a PPI connection between the ADDRESS event in the RADIO and the CRYPT task in the AES CCM. The KSGEN task is triggered from the READY event in the RADIO through a PPI connection.



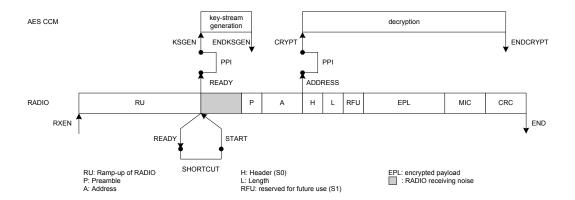


Figure 65: On-the-fly decryption using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM

29.7 CCM data structure

The CCM data structure is located in Data RAM at the memory location specified by the CNFPTR pointer register.

Table 57: CCM data structure overview

Property	Address offset	Description
KEY	0	16 byte AES key
PKTCTR	16	Octet0 (LSO) of packet counter
	17	Octet1 of packet counter
	18	Octet2 of packet counter
	19	Octet3 of packet counter
	20	Bit 6 – Bit 0: Octet4 (7 most significant bits of packet counter, with Bit 6 being the most significant
		bit) Bit7: Ignored
	21	Ignored
	22	Ignored
	23	Ignored
	24	Bit 0: Direction bit Bit 7 – Bit 1: Zero padded
IV	25	8 byte initialization vector (IV) Octet0 (LSO) of IV, Octet1 of IV,, Octet7 (MSO) of IV

The NONCE vector (as specified by the *Bluetooth* Core Specification) will be generated by hardware based on the information specified in the CCM data structure from *Table 57: CCM data structure overview* on page 271.

Table 58: Data structure for unencrypted packet

Property	Address offset	Description
HEADER	0	Packet Header
LENGTH	1	Number of bytes in unencrypted payload
RFU	2	Reserved Future Use
PAYLOAD	3	Unencrypted payload

Table 59: Data structure for encrypted packet

Property	Address offset	Description
HEADER	0	Packet Header
LENGTH	1	Number of bytes in encrypted payload including length of MIC
		Important: LENGTH will be 0 for empty packets since the MIC is not added to empty
		packets
RFU	2	Reserved Future Use
PAYLOAD	3	Encrypted payload
MIC	3 + payload length	ENCRYPT: 4 bytes encrypted MIC



Property	Address offset	Description

Important: MIC is not added to empty packets

29.8 EasyDMA and ERROR event

The CCM implements an EasyDMA mechanism for reading and writing to the RAM.

In some scenarios where the CPU and other DMA enabled peripherals are accessing the RAM at the same time, the CCM DMA could experience some bus conflicts which may also result in an error during encryption. If this happens, the ERROR event will be generated.

The EasyDMA will have finished accessing the RAM when the ENDKSGEN and ENDCRYPT events are generated.

If the CNFPTR, SCRATCHPTR, INPTR and the OUTPTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

29.9 Registers

Table 60: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000F000	CCM	CCM	AES CCM Mode Encryption	

Table 61: Register Overview

Register	Offset	Description
TASKS_KSGEN	0x000	Start generation of key-stream. This operation will stop by itself when completed.
TASKS_CRYPT	0x004	Start encryption/decryption. This operation will stop by itself when completed.
TASKS_STOP	0x008	Stop encryption/decryption
EVENTS_ENDKSGEN	0x100	Key-stream generation complete
EVENTS_ENDCRYPT	0x104	Encrypt/decrypt complete
EVENTS_ERROR	0x108	CCM error event
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
MICSTATUS	0x400	MIC check result
ENABLE	0x500	Enable
MODE	0x504	Operation mode
CNFPTR	0x508	Pointer to data structure holding AES key and NONCE vector
INPTR	0x50C	Input pointer
OUTPTR	0x510	Output pointer
SCRATCHPTR	0x514	Pointer to data area used for temporary storage

29.9.1 SHORTS

Address offset: 0x200

Shortcut register

Bit	numbe	er		31	30	29	28 :	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	on																				
Α	RW	ENDKSGEN_CRYPT										Sho	rtc	ut l	bet	wee	en E	ENE	OKS	GEI	۷e	ven	t ar	d C	RYP	T ta	isk								
												See	EV	/EN	TS_	EN	DK	SGE	N a	nd	TA.	SKS	_CF	ΥP	г										
			Disabled	0								Disa	able	e sh	nort	tcut	t																		
			Enabled	1								Ena	ble	sh	ort	cut																			



29.9.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					СВА
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
Α	RW	ENDKSGEN			Write '1' to Enable interrupt for ENDKSGEN event
					See EVENTS_ENDKSGEN
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	ENDCRYPT			Write '1' to Enable interrupt for ENDCRYPT event
					See EVENTS_ENDCRYPT
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	ERROR			Write '1' to Enable interrupt for ERROR event
					See EVENTS_ERROR
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

29.9.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				СВА
Res	et 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW ENDKSGEN			Write '1' to Disable interrupt for ENDKSGEN event
				See EVENTS_ENDKSGEN
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW ENDCRYPT			Write '1' to Disable interrupt for ENDCRYPT event
				See EVENTS_ENDCRYPT
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW ERROR			Write '1' to Disable interrupt for ERROR event
				See EVENTS_ERROR
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

29.9.4 MICSTATUS

Address offset: 0x400 MIC check result



Bit	numbe	r		31	1 30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 1	8 1	7 16	15	14	13 1	12 1	.1 10	9	8	7	6	5	4	3 2	2 1	1 0
Id																																Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0 0	0 0
Id	RW	Field	Value Id	Va	alue							Des	crip	otio	n																	
Α	R	MICSTATUS										The	res	ult	of t	he I	MIC	che	ck p	erf	orm	ed c	lurin	g th	ie p	revi	ous	5				
												dec	ryp	tion	ор	erat	tion															
			CheckFailed	0								MIC	C ch	eck	fail	ed																
			CheckPassed	1								MIC	C ch	eck	pas	sed	l															

29.9.5 ENABLE

Address offset: 0x500

Enable

Bit	nur	mbei	•		3	31 3	30 2	29 2	28 :	27	26	25	24	23	22	21	20	19	18	3 17	7 16	5 15	5 14	4 1	3 1	.2 1	11 :	10	9	8	7	6	5	4	3	2 1	1 0
Id																																				A	A A
Re	set	0x00	000000		(0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	() (0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	R	RW	Field	Value Id	١	Valu	ıe							De	scr	ipt	on																				
Α	R	RW	ENABLE											En	abl	e o	r di:	sab	le (CCN	1																
				Disabled	(0								Di	sab	le																					
				Enabled	2	2								En	abl	e																					

29.9.6 MODE

Address offset: 0x504

Operation mode

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		C B A
Reset 0x00000001		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW MODE		The mode of operation to be used
	Encryption	0 AES CCM packet encryption mode
	Decryption	1 AES CCM packet decryption mode
B RW DATARATE		Data rate that the CCM shall run in synch with
	1Mbit	0 In synch with 1 Mbit data rate
	2Mbit	1 In synch with 2 Mbit data rate
C RW LENGTH		Packet length configuration
	Default	O Default length. Effective length of LENGTH field is 5-bit
	Extended	1 Extended length. Effective length of LENGTH field is 8-bit

29.9.7 CNFPTR

Address offset: 0x508

Pointer to data structure holding AES key and NONCE vector

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20 1	9 1	.8 1	7 16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2 1	1 0	
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α ,	ДД	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	A A	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	CNFPTR										Poi	nte	r to	the	dat	ta st	ruct	ure	hol	din	g th	e A	ES I	кеу	an	d th	ne C	CIV	1				
												NO	NCE	- ve	cto	· (se	e Ta	hle	1 C	СМ	dat	a st	ruc	tura	۰ ۵۱	/er	viev	۸/۱						

29.9.8 INPTR

Address offset: 0x50C

Input pointer



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value Description
A RW INPTR	Input pointer

29.9.9 OUTPTR

Address offset: 0x510

Output pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW OUTPTR		Output pointer

29.9.10 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

Bit	numb	er		31	L 30	29	28	27	26	25 :	24	23 :	22 2	1 2	0 19	18	17	16	15 1	14 13	3 12	11	10	9	8	7	6	5	4	3 :	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 <i>A</i>	A	Α	Α	Α	Α	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	۱ ۸	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 () (0 (
Id	RW	Field	Value Id	Va	alue							Des	crip	tion	1																	
Α	RW	SCRATCHPTR										duri dec The	ring l crypt	key- ion. atch	strea	am į	gene use	erat	ion	used , MIC	gei	nera	tior	n ar	nd e	ncr	ypt		1/			
												A sp	pace	of 4	43 by	/tes	, or	(16	+ N	Cryp IAXF RAN	ACI		IZE)) by	rtes,	wl	hate	eve	r			



30 AAR — Accelerated address resolver

Accelerated address resolver is a cryptographic support function for implementing the "Resolvable Private Address Resolution Procedure" described in the *Bluetooth Core specification* v4.0. "Resolvable private address generation" should be achieved using ECB and is not supported by AAR.

The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address. The AAR block enables real-time address resolution on incoming packets when configured as described in this chapter. This allows real-time packet filtering (whitelisting) using a list of known shared keys (Identity Resolving Keys (IRK) in *Bluetooth*).

30.1 Shared resources

The AAR shares registers and other resources with the peripherals that have the same ID as the AAR. The user must therefore disable all peripherals that have the same ID as the AAR before the AAR can be configured and used.

Disabling a peripheral that have the same ID as the AAR will not reset any of the registers that are shared with the AAR. It is therefore important to configure all relevant AAR registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 24 for details on peripherals and their IDs.

30.2 EasyDMA

The AAR implements EasyDMA for reading and writing to the RAM. The EasyDMA will have finished accessing the RAM when the END, RESOLVED, and NOTRESOLVED events are generated.

If the IRKPTR, ADDRPTR and the SCRATCHPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

30.3 Resolving a resolvable address

As per Bluetooth specification, a private resolvable address is composed of six bytes.

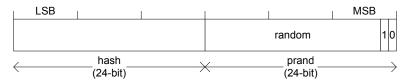


Figure 66: Resolvable address

To resolve an address the ADDRPTR register must point to the start of packet. The resolver is started by triggering the START task. A RESOLVED event is generated when the AAR manages to resolve the address using one of the Identity Resolving Keys (IRK) found in the IRK data structure. The AAR will use the IRK specified in the register IRK0 to IRK15 starting from IRK0. How many to be used is specified by the NIRK register. The AAR module will generate a NOTRESOLVED event if it is not able to resolve the address using the specified list of IRKs.

The AAR will go through the list of available IRKs in the IRK data structure and for each IRK try to resolve the address according to the Resolvable Private Address Resolution Procedure described in the *Bluetooth* Specification²⁴. The time it takes to resolve an address may vary depending on where in the list the

Bluetooth Specification Version 4.0 [Vol 3] chapter 10.8.2.3.



resolvable address is located. The resolution time will also be affected by RAM accesses performed by other peripherals and the CPU. See the *Electrical specifications* for more information about resolution time.

The AAR will only do a comparison of the received address to those programmed in the module. And not check what type of address it actually is.

The AAR will stop as soon as it has managed to resolve the address, or after trying to resolve the address using NIRK number of IRKs from the IRK data structure. The AAR will generate an END event after it has stopped.

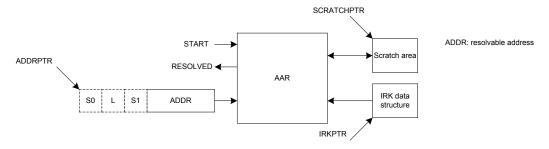


Figure 67: Address resolution with packet preloaded into RAM

30.4 Use case example for chaining RADIO packet reception with address resolution using AAR

The AAR may be started as soon as the 6 bytes required by the AAR have been received by the RADIO and stored in RAM. The ADDRPTR pointer must point to the start of packet.

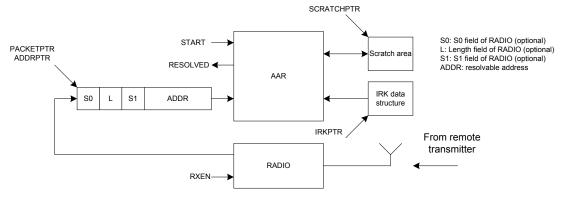


Figure 68: Address resolution with packet loaded into RAM by the RADIO

30.5 IRK data structure

The IRK data structure is located in RAM at the memory location specified by the CNFPTR pointer register.

Table 62: IRK data structure overview

Property	Address offset	Description
IRKO	0	IRK number 0 (16 - byte)
IRK1	16	IRK number 1 (16 - byte)
	**	
IRK15	240	IRK number 15 (16 - byte)



30.6 Registers

Table 63: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000F000	AAR	AAR	Acelerated Address Resolver	

Table 64: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start resolving addresses based on IRKs specified in the IRK data structure
TASKS_STOP	0x008	Stop resolving addresses
EVENTS_END	0x100	Address resolution procedure complete
EVENTS_RESOLVED	0x104	Address resolved
EVENTS_NOTRESOLVED	0x108	Address not resolved
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STATUS	0x400	Resolution status
ENABLE	0x500	Enable AAR
NIRK	0x504	Number of IRKs
IRKPTR	0x508	Pointer to IRK data structure
ADDRPTR	0x510	Pointer to the resolvable address
SCRATCHPTR	0x514	Pointer to data area used for temporary storage

30.6.1 INTENSET

Address offset: 0x304

Enable interrupt

Bitı	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C B A
Res	et 0x00000000		0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW Field	Value Id	Value	Description
Α	RW END			Write '1' to Enable interrupt for END event
				See EVENTS_END
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW RESOLVED			Write '1' to Enable interrupt for RESOLVED event
				See EVENTS_RESOLVED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW NOTRESOLVED			Write '1' to Enable interrupt for NOTRESOLVED event
				See EVENTS_NOTRESOLVED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

30.6.2 INTENCLR

Address offset: 0x308 Disable interrupt



Bit	numbe	er		31	30	29	28 2	27 2	26 25	5 24	23 2	2 2	1 20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5 4	3	2	1 0
Id																													С	ВА
Res	et 0x0	0000000		0	0	0	0 (0	0 0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0 0
Id	RW	Field	Value Id	Va	lue						Des	cript	tion																	
Α	RW	END									Writ	e '1'	' to I	Disa	ble	int	erru	ıpt	for	END	eve	nt								
											See	EVE	NTS_	_EN	D															
			Clear	1							Disa	ble																		
			Disabled	0							Read	d: Di	isabl	led																
			Enabled	1							Read	d: Er	nable	ed																
В	RW	RESOLVED									Writ	e '1'	' to I	Disa	ble	inte	erru	ıpt	for	RES	OLV	ED e	ven	t						
											See	EVE	NTS_	_RE	SOL	VEL)													
			Clear	1							Disa	ble																		
			Disabled	0							Read	d: Di	isabl	led																
			Enabled	1							Read	d: Er	nable	ed																
С	RW	NOTRESOLVED									Writ	e '1'	' to I	Disa	ble	int	erru	ıpt	for	NOT	RES	OLV	ED (ever	nt					
											See	EVE	NTS_	_NC	TRI	ESO	LVE	D												
			Clear	1							Disa	ble																		
			Disabled	0							Read	d: Di	isabl	led																
			Enabled	1							Read	d: Er	nable	ed																

30.6.3 STATUS

Address offset: 0x400

Resolution status

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ААА
Reset 0x00000000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
A R STATUS		[015]	The IRK that was used last time an address was resolved

30.6.4 ENABLE

Address offset: 0x500

Enable AAR

Bit	numb	er		31 30	29	28 2	27 2	26 2	5 24	23	22	21 2	0 1	9 18	3 17	16	15	14	13 1	L2 1	1 10	9	8	7	6	5	4 3	2	1	0
Id																													Α	Α
Res	et 0x	0000000		0 0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Value						De	scrip	otio	n																	
Α	RW	ENABLE								En	able	or (lisal	ole A	AAR															
			Disabled	0						Dis	sable	è																		
			Enabled	3						En	able																			

30.6.5 NIRK

Address offset: 0x504

Number of IRKs

Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ААААА
Reset 0x00000001		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
A RW NIRK		[116]	Number of Identity root keys available in the IRK data structure

30.6.6 IRKPTR

Address offset: 0x508



Pointer to IRK data structure

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW IRKPTR		Pointer to the IRK data structure

30.6.7 ADDRPTR

Address offset: 0x510

Pointer to the resolvable address

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW ADDRPTR		Pointer to the resolvable address (6-bytes)

30.6.8 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

Bitı	numbe	er		31	1 30	29	28	3 27	7 26	5 25	5 24	23	22	21 :	20 1	9 1	8 17	7 16	15	14	13 1	L2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	4 A	Α	Α	Α	Α	A A	Δ Δ	. A	Α	Α	Α	Α	Α	Α	Δ,	А А
Res	et 0x0	0000000		0 0 0 0 0 0 0										0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	alue	:						De	scri	ptio	n																	
Α	RW	SCRATCHPTR										Poi	nte	r to	a so	crate	ch d	ata	area	us	ed f	or te	emp	ora	ry s	tora	ige					
				Pointer to a scratch data area used for temporary storage during resolution. A space of minimum 3 bytes must be																												
												res	erve	ed.																		

30.7 Electrical specification

30.7.1 AAR Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{AAR,8}	Time for address resolution of 8 IRKs		48		μs



31 SPIM — Serial peripheral interface master with EasyDMA

The SPI master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus.

Listed here are the main features for the SPIM

- · Three SPIM instances
- SPI mode 0-3
- · EasyDMA direct transfer to/from RAM for both SPI Slave and SPI Master
- · Individual selection of IO pin for each SPI signal

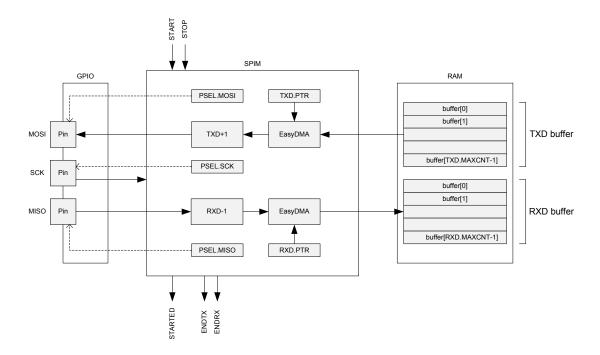


Figure 69: SPIM — SPI master with EasyDMA

The SPIM does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master. The SPIM supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

Table 65: SPI modes

Mode	Clock polarity	Clock phase
	CPOL	СРНА
SPI_MODE	0 (Leading)	0 (Active High)
SPI_MODI	0 (Leading)	1 (Active Low)
SPI_MODI	1 (Trailing)	0 (Active High)
SPI_MODE	1 (Trailing)	1 (Active Low)

31.1 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.



Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 24 for details on peripherals and their IDs.

31.2 EasyDMA

The SPI master implements EasyDMA for reading and writing of data packets from and to the DATA RAM without CPU involvement.

The RXD.PTR and TXD.PTR point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively, see *Figure 69: SPIM* — *SPI master with EasyDMA* on page 281. RXD.MAXCNT and TXD.MAXCNT specify the maximum number of bytes allocated to the buffers.

The SPI master will automatically stop transmitting after TXD.MAXCNT bytes have been transmitted and RXD.MAXCNT bytes have been received. If TXD.MAXCNT is larger than RXD.MAXCNT, the superfluous received bytes will be ignored. If RXD.MAXCNT is larger than TXD.MAXCNT, the remaining transmitted bytes will contain the value defined in the ORC register.

If the RXD.PTR and the TXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next transmission immediately after having received the STARTED event.

The ENDRX/ENDTX event indicate that EasyDMA has finished accessing respectively the RX/TX buffer in RAM. The END event gets generated when both RX and TX are finished accessing the buffers in RAM.

31.2.1 EasyDMA list

EasyDMA supports one list type.

The supported list type is:

Array list

EasyDMA array list

The EasyDMA array list can be represented by the data structure ArrayList_type.

For illustration, see the code example below. This data structure includes only a buffer with size equal to Channel.MAXCNT. EasyDMA will use the Channel.MAXCNT register to determine when the buffer is full. Replace 'Channel' by the specific data channel you want to use, for instance 'NRF_SPIM->RXD', 'NRF_SPIM->TXD', 'NRF_TWIM->RXD', etc.

The Channel.MAXCNT register cannot be specified larger than the actual size of the buffer. If Channel.MAXCNT is specified larger than the size of the buffer, the EasyDMA channel may overflow the buffer.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

```
#define BUFFER_SIZE 4

typedef struct ArrayList
{
  uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type MyArrayList[3];
```



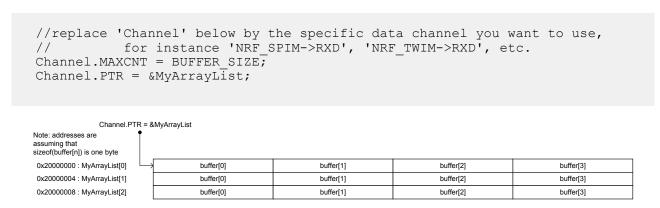


Figure 70: EasyDMA array list

31.3 SPI master transaction sequence

An SPI master transaction consists of a sequence started by the START task followed by a number of events, and finally the STOP task.

An SPI master transaction is started by triggering the START task. The ENDTX event will be generated when the transmitter has transmitted all bytes in the TXD buffer as specified in the TXD.MAXCNT register. The ENDRX event will be generated when the receiver has filled the RXD buffer, i.e. received the last possible byte as specified in the RXD.MAXCNT register.

Following a START task, the SPI master will generate an END event when both ENDRX and ENDTX have been generated.

The SPI master is stopped by triggering the STOP task. A STOPPED event is generated when the SPI master has stopped.

If the ENDRX event has not already been generated when the SPI master has come to a stop, the SPI master will generate the ENDRX event explicitly even though the RX buffer is not full.

If the ENDTX event has not already been generated when the SPI master has come to a stop, the SPI master will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

The SPI master is a synchronous interface, and for every byte that is sent, a different byte will be received at the same time; this is illustrated in *Figure 71: SPI master transaction* on page 284.



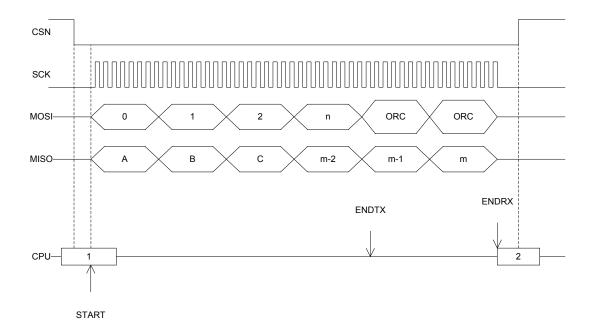


Figure 71: SPI master transaction

31.4 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

31.5 Master mode pin configuration

The SCK, MOSI, and MISO signals associated with the SPI master are mapped to physical pins according to the configuration specified in the PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively.

The PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCK, PSEL.MOSI and PSEL.MISO must only be configured when the SPI master is disabled.

To secure correct behavior in the SPI, the pins used by the SPI must be configured in the GPIO peripheral as described in *Table 66: GPIO configuration* on page 284 prior to enabling the SPI. This configuration must be retained in the GPIO for the selected IOs as long as the SPI is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 66: GPIO configuration

SPI master signal	SPI master pin	Direction	Output value	Comments
SCK	As specified in PSEL.SCK	Output	Same as CONFIG.CPOL	
MOSI	As specified in PSEL.MOSI	Output	0	
MISO	As specified in PSEL.MISO	Input	Not applicable	



31.6 Registers

Table 67: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	SPIM	SPIM0	SPI master 0		
0x40004000	SPIM	SPIM1	SPI master 1		
0x40023000	SPIM	SPIM2	SPI master 2		

Table 68: Register Overview

Register	Offset	Description
TASKS_START	0x010	Start SPI transaction
TASKS_STOP	0x014	Stop SPI transaction
TASKS_SUSPEND	0x01C	Suspend SPI transaction
TASKS_RESUME	0x020	Resume SPI transaction
EVENTS_STOPPED	0x104	SPI transaction has stopped
EVENTS_ENDRX	0x110	End of RXD buffer reached
EVENTS_END	0x118	End of RXD buffer and TXD buffer reached
EVENTS_ENDTX	0x120	End of TXD buffer reached
EVENTS_STARTED	0x14C	Transaction started
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable SPIM
PSEL.SCK	0x508	Pin select for SCK
PSEL.MOSI	0x50C	Pin select for MOSI signal
PSEL.MISO	0x510	Pin select for MISO signal
FREQUENCY	0x524	SPI frequency
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
TXD.LIST	0x550	EasyDMA list type
CONFIG	0x554	Configuration register
ORC	0x5C0	Over-read character. Character clocked out in case and over-read of the TXD buffer.

31.6.1 SHORTS

Address offset: 0x200 Shortcut register

В	t nur	mbe	r		31	1 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	.0	9 8	3 7	' 6	5 5	5 4	3	2	1	0
Ic																			Α																
R	eset	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0) (0	0	0	0
Ic	l F	RW	Field	Value Id						De	scr	ipti	on																						
Α	F	RW	END_START							Sh	ort	cut	bet	we	en	ENI) ev	/en	t ar	ıd S	ΓAR	T ta	sk												
										Se	e <i>E</i>	VEN	TS_	_EN	D a	and	TA:	SKS	_57	AR	-														
				Disabled	0					Dis	sab	le sl	nor	tcut	t																				
				Enabled	1 E				En	abl	e sh	ort	tcut																						

31.6.2 INTENSET

Address offset: 0x304 Enable interrupt



Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E D C B A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW STOPPED			Write '1' to Enable interrupt for STOPPED event
			See EVENTS_STOPPED
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW ENDRX			Write '1' to Enable interrupt for ENDRX event
			See EVENTS_ENDRX
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW END			Write '1' to Enable interrupt for END event
			See EVENTS_END
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW ENDTX			Write '1' to Enable interrupt for ENDTX event
			See EVENTS_ENDTX
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW STARTED			Write '1' to Enable interrupt for STARTED event
			See EVENTS_STARTED
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

31.6.3 INTENCLR

Address offset: 0x308 Disable interrupt

	iumbe	r		31	. 30	29	28	27 :	26 2	25 2	24 2	23 22	2 21	20		18	17	16	15	14	13 1	12 1	11 1	9	8	7	6	5	4	3 2	2 1	0
Id															Ε										D		С		В		Α	
Rese	et 0x0	0000000		0	0	0	0	0	0 (0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						0	Desc	ripti	on																		
Α	RW	STOPPED									٧	Vrite	'1'	to D	isal	ble	inte	erru	ıpt	for	STO	PPE	D e	ent								
											S	ee E	VEN	ITS_	STC	PP	ED															
			Clear	1							0	Disab	le																			
			Disabled	0							F	Read	: Dis	able	ed																	
			Enabled	1							F	Read	: En	able	d																	
В	RW	ENDRX									٧	Vrite	'1'	to E	isal	ble	inte	erru	ıpt	for	END	RX	eve	nt								
											S	see E	VEN	ITS_	ENI	DRX	(
			Clear	1							0	Disab	le																			
			Disabled	0							F	Read	: Dis	able	ed																	
			Enabled	1							F	Read	: En	able	d																	
С	RW	END									٧	Vrite	'1'	to C	isal	ble	inte	erru	ıpt	for	ENC	ev	ent									
											S	ee E	VEN	ITS_	ENI	D																
			Clear	1								Disab	le																			
			Disabled	0							F	Read	: Dis	able	ed																	
			Enabled	1							F	Read	: En	able	d																	
D	RW	ENDTX									٧	Vrite	'1'	to E	isal	ble	inte	erru	ıpt '	for	ENC	XT	eve	nt								
											S	ee E	VEN	ITS_	ENI	отх	(



Bit number		31	30 2	29 2	28 2	7 2	6 25	5 2	4 2	3 22	21	20	19	18	17 1	6 1	5 1	4 13	3 12	11	10	9	8 7	' 6	5 5	4	3	2	1 0
Id													Ε										D	(2	В			Α
Reset 0x00000000		0	0	0	0 () (0 0	(0 0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 ((0 0	0	0	0	0 0
Id RW Field	Value Id	Va	lue						D	escr	ipti	on																	
	Clear	1							D	isab	le																		
	Disabled	0					R	ead:	Dis	able	ed																		
	Enabled						R	ead:	Ena	ble	d																		
E RW STARTED		1					V	/rite	'1' 1	to D	isa	ble	inte	rrup	ot fo	or ST	TAR1	ED	ever	nt									
							S	ee <i>E</i>	VEN	TS_	STA	ARTI	Đ																
	Clear	1				D	isab	le																					
	Disabled	1 0						R	ead:	Dis	able	ed																	
	Enabled	1							R	ead:	Ena	ble	d																

31.6.4 ENABLE

Address offset: 0x500

Enable SPIM

Bit	nu	ımbe	er		31	30	29 :	28 :	27 :	26 2	25 :	24	23	22 :	21 2	20 1	19 :	18 2	17 1	16 1	15	14 :	13 :	L2 1	1 10	9	8	7	6	5	4	3	2	1 0	l
Id																																Α	Α	А А	
Re	set	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	l
Id		RW	Field	Value Id							Des	crip	otio	n																			l		
Α		RW	ENABLE		value						Ena	ble	or	disa	ble	SP	IM																		
				Disabled					Disa	able	SP	IM																							
				Enabled	7 E				Ena	ble	SPI	M																							

31.6.5 PSEL.SCK

Address offset: 0x508 Pin select for SCK

nber		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
		В	ААААА
)xFFFFFFF		1 1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
W Field	Value Id	Value	Description
W PIN		[031]	Pin number
W CONNECT			Connection
	Disconnected	1	Disconnect
	Connected	0	Connect
	IXFFFFFFF W Field W PIN	XFFFFFFFF W Field Value Id W PIN W CONNECT Disconnected	B

31.6.6 PSEL.MOSI

Address offset: 0x50C Pin select for MOSI signal

Bit	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	АААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

31.6.7 PSEL.MISO

Address offset: 0x510

Pin select for MISO signal



Bit	numbe	er		31 30 2	29 2	8 27	7 26	25	24	23 2	22 2	1 20) 19	18 3	17 16	5 15	14 1	.3 12	11	10 9	8	7	6	5	4	3 2	1	0
Id				В																					Α	А А	. A	Α
Res	et 0xF	FFFFFF		1 1	1 1	1 1	1	1	1	1	1 :	1 1	. 1	1	1 1	1	1	1 1	1	1 :	l 1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Value						Des	crip	tion																
Α	RW	PIN		[031]						Pin	nun	ber																
В	RW	CONNECT								Con	nec	tion																
			Disconnected	1						Disc	conn	ect																
			Connected	0						Con	nec	t																

31.6.8 FREQUENCY

Address offset: 0x524

SPI frequency

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Id			A A
Reset 0x04000000		0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
Id RW Field	Value Id	Value Description	
A RW FREQUENCY		SPI master data rate	
	K125	0x02000000 125 kbps	
	K250	0x04000000 250 kbps	
	K500	0x08000000 500 kbps	
	M1	0x10000000 1 Mbps	
	M2	0x20000000 2 Mbps	
	M4	0x40000000 4 Mbps	
	M8	0x80000000 8 Mbps	

31.6.9 RXD.PTR

Address offset: 0x534

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Data pointer

31.6.10 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 17	7 16 15 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	000000000	00000000
ld RW Field	Value Id	Value	Description		
A RW MAXCNT			Maximum number of	hytes in receive buffer	

31.6.11 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
A R AMOUNT			Number of bytes transferred in the last transaction



31.6.12 RXD.LIST

Address offset: 0x540 EasyDMA list type

Bit r	num	ber			31	1 30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 1	16 1	5 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2	1 0
Id																																A	۸ ۸	A A
Res	et O	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RV	N	Field	Value Id	Va	alue	•						De	scri	ptic	n																		
Α	RV	Ν	LIST										List	typ	рe																			
				Disabled	0								Dis	able	e Ea	syD	M	A lis	t															
				ArrayList	1								Use	e arı	ray	list																		

31.6.13 TXD.PTR

Address offset: 0x544

Data pointer

В	it nı	umb	er				3	1	30 2	9 2	28 2	7 2	6 2	25 2	24 2	3 2	2 2	1 2	0 19	9 18	3 17	16	15	14	13	12 :	11 1	9	8	7	6	5	4	3	2	1 0
lc	ł						А		A	Δ,	Α.	A A	۱ ۸	A ,	Δ ,	Δ /	Δ ,	Δ Α	4 Α	A	A	Α	Α	Α	Α	Α	A A	A	Α	Α	Α	Α	Α	Α	A	A A
R	ese	t Ox	00000	000			0		0	0 (0	0 () (0	0 (0 (0 () (0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Ic	ı	RW	Field		Val	ue Id	V	al	ue						C	eso	rip	tio	n																	
Α		RW	PTR												С	ata	ро	inte	er																	

31.6.14 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9 8	7 6	5 4	3 2	1 0
Id					АА	A A	АА	A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0000000000	0 0	0 0	0 0	0 0
Id RW Field	Value Id	Value	Description					
A RW MAXCNT			Maximum number of	bytes in transmit buffer				

31.6.15 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit numl	per		31 3	0 29	28 2	7 26	25 2	24 2	3 22	2 21	20	19 1	.8 1	7 16	15	14	13 1	2 1:	l 10	9	8	7	6	5 4	3	2	1	0
Id																						Α	Α	A A	A	Α	Α	Α
Reset 0	00000000		0 (0 0	0 0	0 0	0	0 0	0	0	0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0
Id RV	/ Field	Value Id	Valu	e				D	escr	ripti	on																	
A R	AMOUNT							N	uml	ber o	of b	vtes	trar	nsfer	red	in tl	ne la	ıst tı	ansa	ictic	on							7

31.6.16 TXD.LIST

Address offset: 0x550 EasyDMA list type

Bit	num	ber			31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	2 :	1 0
Id																																A	A A	A А
Res	et 0	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	R۱	N	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	R۱	N	LIST										List	t ty	pe																			
				Disabled	0								Dis	abl	e Ea	asy[MC	۱is ا	t															
				ArrayList	1								Us	e ar	ray	list																		



31.6.17 CONFIG

Address offset: 0x554 Configuration register

Bit r	iumbe	er		31	30 2	9 2	28 2	7 2	6 25	24	23	22	21 2	20 2	19 1	18 :	17 :	16	15	14 1	.3 1	2 11	. 10	9	8	7	6 !	5 4	1 3	2	1)
Id																														С	В	4
Res	et 0x0	0000000		0	0 () (0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0 (0	0	0)
Id	RW	Field	Value Id	Va	lue						De	scri	ptio	n																		
Α	RW	ORDER									Bit	ord	ler																			
			MsbFirst	0							Mo	ost s	ignit	fica	nt l	bit :	shif	ted	ou	t fir	st											
			LsbFirst	1							Lea	ast s	igni	fica	nt l	bit :	shif	ted	ou	t fir	st											
В	RW	СРНА									Ser	rial o	clock	(S	CK)	ph	ase															
			Leading	0							Sar	mple	e on	lea	din	ıg e	dge	of	clo	ck,	shift	ser	ial d	ata	on t	rai	ling					
											edg	ge																				
			Trailing	1							Sar	mple	e on	tra	ilin	g e	dge	of	clo	ck, s	hift	seri	al d	ata	on l	eac	ling					
											edg	ge																				
С	RW	CPOL									Ser	rial o	clock	c (S	CK)	ро	lari	ty														
			ActiveHigh	0							Act	tive	high	1																		
			ActiveLow	1							Act	tive	low																			

31.6.18 ORC

Address offset: 0x5C0

Over-read character. Character clocked out in case and over-read of the TXD buffer.

Bit	numbe	r		31	. 30	29 :	28 2	7 26	25	5 24	23	22 2	21 2	0 19	9 18	3 17	16	15	14 1	L3 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																									Α	Α	Α	Α.	А А	A	Α
Res	et 0x0(0000000		0	0	0	0 (0 0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						Des	scrip	tio	n																	
Α	RW	ORC									Ove	er-re	ad	char	act	er. (har	act	er cl	ock	ed o	out i	n ca	ise a	and	ove	er-				
											rea	d of	the	TXE) bı	ıffer															

31.7 Electrical specification

31.7.1 SPIM master interface

Symbol	Description	Min.	Тур.	Max.	Units
f _{SPIM}	Bit rates for SPIM ²⁵			8 ²⁶	Mbps
I _{SPIM,2Mbps}	Run current for SPIM, 2 Mbps		50		μΑ
I _{SPIM,8Mbps}	Run current for SPIM, 8 Mbps		50		μΑ
I _{SPIM,IDLE}	Idle current for SPIM (STARTed, no CSN activity)		1		μΑ
t _{spim,start,lp}	Time from START task to transmission started, low power mode		t _{SPIM,STA}	RT,	μs
			+		
			t _{START_HE}	IN	
t _{SPIM,START,CL}	Time from START task to transmission started, constant latency		1		μs
	mode				

31.7.2 Serial Peripheral Interface Master (SPIM) electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{SPIM} ,CSCK,8Mbps	SCK period at 8Mbps		125		ns
t _{SPIM} ,CSCK,4Mbps	SCK period at 4Mbps		250		ns
t _{SPIM,CSCK,2Mbps}	SCK period at 2Mbps		500		ns

Higher bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.



Symbol	Description	Min.	Тур.	Max.	Units
t _{SPIM,RSCK,LD}	SCK rise time, low drive ^a			t _{RF,25pF}	
t _{SPIM,RSCK,HD}	SCK rise time, high drive ^a			t _{HRF,25pF}	
t _{SPIM,FSCK,LD}	SCK fall time, low drive ^a			t _{RF,25pF}	
t _{SPIM,FSCK,HD}	SCK fall time, high drive ^a			t _{HRF,25pF}	
t _{SPIM} , WHSCK	SCK high time ^a	(0.5*t _{CSCI}	d		
		– t _{RSCK}			
t _{SPIM,WLSCK}	SCK low time ^a	(0.5*t _{CSCI}	d		
		- t _{FSCK}			
t _{SPIM,SUMI}	MISO to CLK edge setup time	19			ns
t _{SPIM,HMI}	CLK edge to MISO hold time	18			ns
t _{SPIM,VMO}	CLK edge to MOSI valid			59	ns
t _{SPIM.HMO}	MOSI hold time after CLK edge	20			ns

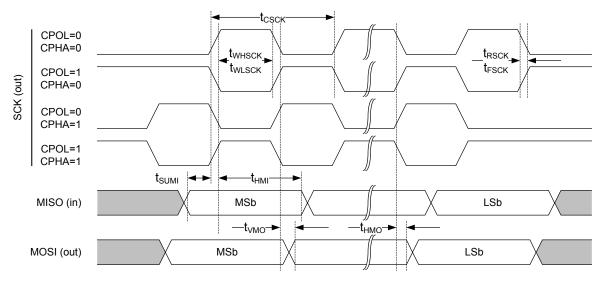


Figure 72: SPIM timing diagram

^a At 25pF load, including GPIO pin capacitance, see GPIO spec.



32 SPIS — Serial peripheral interface slave with EasyDMA

SPI slave (SPIS) is implemented with EasyDMA support for ultra low power serial communication from an external SPI master. EasyDMA in conjunction with hardware-based semaphore mechanisms removes all real-time requirements associated with controlling the SPI slave from a low priority CPU execution context.

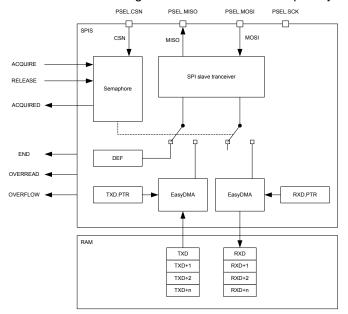


Figure 73: SPI slave

The SPIS supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

Table 69: SPI modes

Mode	Clock polarity CPOL	Clock phase CPHA
SPI_MODE0	0 (Leading)	0 (Active High)
SPI_MODE1	0 (Leading)	1 (Active Low)
SPI_MODE2	1 (Trailing)	0 (Active High)
SPL MODE3	1 (Trailing)	1 (Active Low)

32.1 Shared resources

The SPI slave shares registers and other resources with other peripherals that have the same ID as the SPI slave. Therefore, you must disable all peripherals that have the same ID as the SPI slave before the SPI slave can be configured and used.

Disabling a peripheral that has the same ID as the SPI slave will not reset any of the registers that are shared with the SPI slave. It is important to configure all relevant SPI slave registers explicitly to secure that it operates correctly.

The Instantiation table in *Instantiation* on page 24 shows which peripherals have the same ID as the SPI slave.

32.2 EasyDMA

The SPI slave implements EasyDMA for reading and writing to and from the RAM. The END event indicates that EasyDMA has finished accessing the buffer in RAM.



If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

32.3 SPI slave operation

SPI slave uses two memory pointers, RXD.PTR and TXD.PTR, that point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively. Since these buffers are located in RAM, which can be accessed by both the SPI slave and the CPU, a hardware based semaphore mechanism is implemented to enable safe sharing.

See Figure 74: SPI transaction when shortcut between END and ACQUIRE is enabled on page 294.

Before the CPU can safely update the RXD.PTR and TXD.PTR pointers it must first acquire the SPI semaphore. The CPU can acquire the semaphore by triggering the ACQUIRE task and then receiving the ACQUIRED event. When the CPU has updated the RXD.PTR and TXD.PTR pointers the CPU must release the semaphore before the SPI slave will be able to acquire it. The CPU releases the semaphore by triggering the RELEASE task. This is illustrated in *Figure 74: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 294. Triggering the RELEASE task when the semaphore is not granted to the CPU will have no effect.

The semaphore mechanism does not, at any time, prevent the CPU from performing read or write access to the RXD.PTR register, the TXD.PTR registers, or the RAM that these pointers are pointing to. The semaphore is only telling when these can be updated by the CPU so that safe sharing is achieved.

The semaphore is by default assigned to the CPU after the SPI slave is enabled. No ACQUIRED event will be generated for this initial semaphore handover. An ACQUIRED event will be generated immediately if the ACQUIRE task is triggered while the semaphore is assigned to the CPU.

The SPI slave will try to acquire the semaphore when CSN goes low. If the SPI slave does not manage to acquire the semaphore at this point, the transaction will be ignored. This means that all incoming data on MOSI will be discarded, and the DEF (default) character will be clocked out on the MISO line throughout the whole transaction. This will also be the case even if the semaphore is released by the CPU during the transaction. In case of a race condition where the CPU and the SPI slave try to acquire the semaphore at the same time, as illustrated in lifeline item 2 in *Figure 74: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 294, the semaphore will be granted to the CPU.

If the SPI slave acquires the semaphore, the transaction will be granted. The incoming data on MOSI will be stored in the RXD buffer and the data in the TXD buffer will be clocked out on MISO.

When a granted transaction is completed and CSN goes high, the SPI slave will automatically release the semaphore and generate the END event.

As long as the semaphore is available the SPI slave can be granted multiple transactions one after the other. If the CPU is not able to reconfigure the TXD.PTR and RXD.PTR between granted transactions, the same TX data will be clocked out and the RX buffers will be overwritten. To prevent this from happening, the END_ACQUIRE shortcut can be used. With this shortcut enabled the semaphore will be handed over to the CPU automatically after the granted transaction has completed, giving the CPU the ability to update the TXPTR and RXPTR between every granted transaction.

If the CPU tries to acquire the semaphore while it is assigned to the SPI slave, an immediate handover will not be granted. However, the semaphore will be handed over to the CPU as soon as the SPI slave has released the semaphore after the granted transaction is completed. If the END_ACQUIRE shortcut is enabled and the CPU has triggered the ACQUIRE task during a granted transaction, only one ACQUIRE request will be served following the END event.

The MAXRX register specifies the maximum number of bytes the SPI slave can receive in one granted transaction. If the SPI slave receives more than MAXRX number of bytes, an OVERFLOW will be indicated in the STATUS register and the incoming bytes will be discarded.

The MAXTX parameter specifies the maximum number of bytes the SPI slave can transmit in one granted transaction. If the SPI slave is forced to transmit more than MAXTX number of bytes, an OVERREAD will be indicated in the STATUS register and the ORC character will be clocked out.



The RXD.AMOUNT and TXD.AMOUNT registers are updated when a granted transaction is completed. The TXD.AMOUNT register indicates how many bytes were read from the TX buffer in the last transaction, that is, ORC (over-read) characters are not included in this number. Similarly, the RXD.AMOUNT register indicates how many bytes were written into the RX buffer in the last transaction.

The ENDRX event is generated when the RX buffer has been filled.

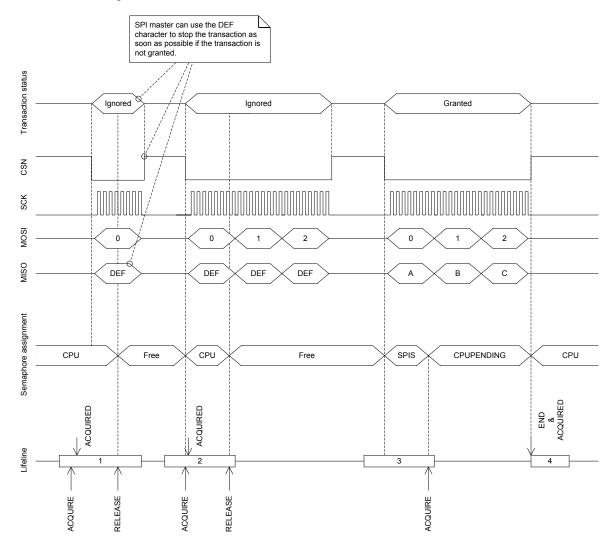


Figure 74: SPI transaction when shortcut between END and ACQUIRE is enabled

32.4 Pin configuration

The CSN, SCK, MOSI, and MISO signals associated with the SPI slave are mapped to physical pins according to the configuration specified in the PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If the CONNECT field of any of these registers is set to Disconnected, the associated SPI slave signal will not be connected to any physical pins.

The PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI slave is enabled, and retained only as long as the device is in System ON mode, see *POWER — Power supply* on page 78 chapter for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI slave is disabled.

To secure correct behavior in the SPI slave, the pins used by the SPI slave must be configured in the GPIO peripheral as described in *Table 70: GPIO configuration before enabling peripheral* on page 295 before enabling the SPI slave. This is to secure that the pins used by the SPI slave are driven correctly if the SPI



slave itself is temporarily disabled, or if the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the SPI slave is to be recognized by an external SPI master.

The MISO line is set in high impedance as long as the SPI slave is not selected with CSN.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 70: GPIO configuration before enabling peripheral

SPI signal	SPI pin	Direction	Output value	Comment
CSN	As specified in PSEL.CSN	Input	Not applicable	
CK	As specified in PSEL.SCK	Input	Not applicable	
IOSI	As specified in PSEL.MOSI	Input	Not applicable	
1ISO	As specified in PSFL MISO	Innut	Not applicable	Emulates that the SPI slave is not selected

32.5 Registers

Table 71: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	SPIS	SPIS0	SPI slave 0		
0x40004000	SPIS	SPIS1	SPI slave 1		
0x40023000	SPIS	SPIS2	SPI slave 2		

Table 72: Register Overview

Register	Offset	Description	
TASKS_ACQUIRE	0x024	Acquire SPI semaphore	
TASKS_RELEASE	0x028	Release SPI semaphore, enabling the SPI slave to acquire it	
EVENTS_END	0x104	Granted transaction completed	
EVENTS_ENDRX	0x110	End of RXD buffer reached	
EVENTS_ACQUIRED	0x128	Semaphore acquired	
SHORTS	0x200	Shortcut register	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
SEMSTAT	0x400	Semaphore status register	
STATUS	0x440	Status from last transaction	
ENABLE	0x500	Enable SPI slave	
PSELSCK	0x508	Pin select for SCK	Deprecated
PSELMISO	0x50C	Pin select for MISO	Deprecated
PSELMOSI	0x510	Pin select for MOSI	Deprecated
PSELCSN	0x514	Pin select for CSN	Deprecated
PSEL.SCK	0x508	Pin select for SCK	
PSEL.MISO	0x50C	Pin select for MISO signal	
PSEL.MOSI	0x510	Pin select for MOSI signal	
PSEL.CSN	0x514	Pin select for CSN signal	
RXDPTR	0x534	RXD data pointer	Deprecated
MAXRX	0x538	Maximum number of bytes in receive buffer	Deprecated
AMOUNTRX	0x53C	Number of bytes received in last granted transaction	Deprecated
RXD.PTR	0x534	RXD data pointer	
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer	
RXD.AMOUNT	0x53C	Number of bytes received in last granted transaction	
TXDPTR	0x544	TXD data pointer	Deprecated
MAXTX	0x548	Maximum number of bytes in transmit buffer	Deprecated
AMOUNTTX	0x54C	Number of bytes transmitted in last granted transaction	Deprecated
TXD.PTR	0x544	TXD data pointer	
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer	
TXD.AMOUNT	0x54C	Number of bytes transmitted in last granted transaction	
CONFIG	0x554	Configuration register	



Register	Offset	Description
DEF	0x55C	Default character. Character clocked out in case of an ignored transaction.
ORC	0x5C0	Over-read character

32.5.1 SHORTS

Address offset: 0x200

Shortcut register

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23 2	22 2	21 2	20 1	9 1	.8 1	7 1	5 15	14	13	12 1	.1 10	9	8	7	6	5	4	3 2	1	0
Id																														Δ	١.	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	tio	n																	
Α	RW	END_ACQUIRE										Sho	rtcu	ıt b	etw	eer	n EN	ND e	ven	t an	d AC	QU	IRE t	ask								
											:	See	EVE	ENT	S_E	ND	and	d T /	SKS	_AC	QUI	RE										
			Disabled	0							١	Disa	ble	sh	orto	ut																
			Enabled	1							ı	Ena	ble	shc	rtcı	ut																

32.5.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C B A
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW END			Write '1' to Enable interrupt for END event
				See EVENTS_END
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW ENDRX			Write '1' to Enable interrupt for ENDRX event
				See EVENTS_ENDRX
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW ACQUIRED			Write '1' to Enable interrupt for ACQUIRED event
				See EVENTS_ACQUIRED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

32.5.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	er		33	1 30	29	2	8 27	7 2	6 2	5 24	4 2	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																									С						В			Α
Res	et 0x0	0000000		0	0	0	0	0	(0	0	(0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue							D	esc	ripti	on																			
Α	RW	END										٧	/rite	'1'	to [Disa	ble	int	err	upt	for	EN	D e	ven	ıt									
												S	ee E	VEN	ITS_	EN	D																	
			Clear	1								D	isab	le																				
			Disabled	0								R	ead	: Dis	abl	ed																		
			Enabled	1								R	ead	: En	able	ed																		
В	RW	ENDRX										٧	/rite	'1'	to [Disa	ble	int	err	upt	for	EN	DR	X ev	ent	t								



Bit r	umbe	er		31	30 2	29 2	28 2	7 2	26 2	5 24	4 23	3 22	21	20	19 1	18 1	17 3	16 1	L5 1	14 1	3 12	2 11	10	9	8	7	6	5	4 3	2	1 0	ı
Id																							С						В		Α	ı
Res	et OxO	0000000		0	0	0	0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0	0 0	ı
Id	RW	Field	Value Id	Va	lue						D	escr	iptio	n																		
											Se	ee <i>E</i>	VENT	TS_	END	ORX																
			Clear	1							Di	isab	le																			
			Disabled	0							Re	ead:	Disa	ble	ed																	
			Enabled	1							Re	ead:	Ena	ble	d																	
С	RW	ACQUIRED									W	/rite	'1' t	o D	isab	le i	nte	rru	pt f	or A	CQI	JIRE	D e	ven	t							
											Se	ee <i>E</i> '	VEN	TS_	ACC	QUII	RED)														
			Clear	1							Di	isab	le																			
			Disabled	0							Re	ead:	Disa	ble	ed																	
			Enabled	1							Re	ead:	Ena	ble	d																	

32.5.4 SEMSTAT

Address offset: 0x400 Semaphore status register

Bitı	numbe	er		31	L 30	29	28	3 27	7 2	6 25	5 24	23	22	21	20	19	18	17	7 16	5 1	5 1	4 1	13 :	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α	Α
Res	et OxO	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Id	RW	Field	Value Id	Va	alue							De	scr	ipti	on																					
Α	R	SEMSTAT										Se	ma	pho	re s	stat	us																			
			Free	0								Se	ma	pho	re i	is fr	ee																			
			CPU	1								Se	ma	pho	re i	is a	ssig	ne	d to	C	PU															
			SPIS	2								Se	ma	pho	re i	is a	ssig	ne	d to	S	PI s	lav	e													
			CPUPending	3								Se	ma	pho	re i	is a	ssig	ne	d to	S	PI b	ut	a h	and	dov	er 1	to t	he	CPL	J is						
												pe	ndi	ng																						

32.5.5 STATUS

Address offset: 0x440

Status from last transaction

Individual bits are cleared by writing a '1' to the bits that shall be cleared

Bit nun	mbe	r		31	30	29	28 2	27 2	26 2	5 2	24 2	3 2	2 21	. 20	19	18	17	16	15 :	14 1	.3 1	2 1	1 10	9	8	7	6	5	4 3	3 2	1	0
Id																															В	Α
Reset (0x00	0000000		0	0	0	0	0	0 (0	0	0 0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0 (0	0	0
ld R	RW	Field	Value Id	Va	lue						0)esc	ripti	ion																		
A R	RW	OVERREAD									Т	Χbι	ıffe	rov	er-r	ead	det	ect	ed,	and	l pr	eve	ntec	ł								
			NotPresent	0							F	lead	: er	ror ı	not	pre	sen	:														
			Present	1							F	lead	: er	ror	pres	ent																
			Clear	1							٧	Vrite	e: cl	ear	erro	r o	n w	ritir	ıg '1	L '												
B R	RW	OVERFLOW									F	X b	uffe	r ov	erfl	ow	dete	ecte	d, a	and	pre	ven	ted									
			NotPresent	0							F	lead	: er	ror ı	not	pre	sen	:														
			Present	1							F	lead	: er	ror	pres	ent																
			Clear	1							٧	Vrite	e: cl	ear	erro	r o	n w	ritir	ıg '1	L'												

32.5.6 ENABLE

Address offset: 0x500 Enable SPI slave

Bit	numbe	er		31	30	29	28 2	7 26	5 25	5 24	1 23	3 22	2 21	L 20	0 19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 :	1 C)
Id																															A	۸ ۸	Δ <i>Α</i>	A.
Re	set 0x0	0000000		0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (o c)
Id	RW	Field	Value Id	Val	lue						D	esci	ript	ion																				
Α	RW	ENABLE									Er	nab	le o	r d	isab	le S	SPI s	lav	e															٦.



Bit number		31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id					A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description		
	Disabled	0	Disable SPI slave		
	Enabled	2	Enable SPI slave		

32.5.7 PSELSCK (Deprecated)

Address offset: 0x508 Pin select for SCK

Bit	numb	er		31	L 30	29	28	27	' 26	25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	alue							De	scri	pti	on																			
Α	RW	PSELSCK		[0.	31]						Pir	n nu	mb	er d	onf	igu	rati	on	for	SPI	SC	K si	gna	al									
			Disconnected	Ωx	FFF	FFF	FF					Dis	cor	ne	:t																			

32.5.8 PSELMISO (Deprecated)

Address offset: 0x50C Pin select for MISO

Bitı	numb	er		31	1 30	29	28	8 2	7 2	5 25	5 24	1 23	3 22	21	20	19	18 :	17 :	16 :	15 :	L4 1	3 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	А		λ Δ	. A	A	A	Α	Α	Α	Α	Α	Α	Α	Α	A ,	4 Δ	A	Α	Α	Α	Α	Α	Α	Α	А А	A	Α
Res	et Oxl	FFFFFFF		1	1	1	1	. 1	L 1	. 1	. 1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Va	alue	•						D	escr	iptio	on																		
Α	RW	PSELMISO		[0	31	L]						Pi	n nı	ımb	ero	onf	iguı	rati	on f	for :	SPI	MIS) się	gnal									
			Disconnected	0>	(FFF	FFF	FF					Di	scoi	nne	ct																		

32.5.9 PSELMOSI (Deprecated)

Address offset: 0x510 Pin select for MOSI

Bit	numbe	er		31	1 30	29	28	8 27	7 26	5 25	5 24	23	22	21	20	19	18 :	17 1	.6 1	L5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	. Α	A	A	. A	Α	Α	Α	Α	Α	Α	Α	A	Δ.	A A	Δ ,	A /	\ A	A A	A	Α	Α	Α	Α	Α	А А	A /	A A
Res	et OxF	FFFFFF		1	1	1	1	. 1	. 1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	L 1	L 1	l 1	1	1	1	1	1	1	1 1	. 1	l 1
Id	RW	Field	Value Id	Va	alue	:						De	scri	ptic	on																		
Α	RW	PSELMOSI		[0	31	.]						Pir	n nu	mb	er c	onf	iguı	atio	n f	or S	PI I	MO:	SI s	igna	I								
			Disconnected	0>	ĸFFF	FFF	FFF					Dis	cor	nec	ct																		

32.5.10 PSELCSN (Deprecated)

Address offset: 0x514 Pin select for CSN

Bitı	iumbe	er		31	. 30	29	28	27	26	25	24	23	22 :	21 2	20 1	L9 1	l8 1	7 1	6 1	5 14	1 13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α .	A A	Δ ,	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	۱ ۸	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	l 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																		
Α	RW	PSELCSN		[0	31]						Pin	nur	nbe	er co	onfi	gur	atic	n fo	r SI	PI C	SN s	igna	al									
			Disconnected	0x	FFF	FFF	FF					Disc	con	nec	t																		

32.5.11 PSEL.SCK

Address offset: 0x508
Pin select for SCK



Bit	numbe	er		3:	1 30	29	28	27	26	25	24	23 :	22 2	21 2	0 19	9 18	3 17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id				В																									A	4 A	Α.	Α
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1 1	1 1	1	. 1	1	1	1	1 :	1 1	. 1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	V	alue							Des	crip	tior	n																	
Α	RW	PIN		[0)31]						Pin	nun	nbe	r																	
В	RW	CONNECT										Con	nec	tior	1																	
			Disconnected	1								Disc	conr	nect																		
			Connected	0								Con	nec	t																		

32.5.12 PSEL.MISO

Address offset: 0x50C Pin select for MISO signal

Bitı	numbe	er		31 3	30 29	28	3 27	26 2	25 2	24 :	23 2	2 21	L 20	19	18	17 1	6 1	5 14	13	12	11 1	.0 9	8	7	6	5	4	3 2	2 1	1 0
Id				В																							Α	A A	A 4	A A
Res	et OxF	FFFFFF		1	1 1	1	1	1	1	1	1 1	۱ 1	1	1	1	1	1 1	۱ 1	1	1	1	1 1	1	1	1	1	1	1 :	L 1	. 1
Id	RW	Field	Value Id	Valu	ıe					ı	Desc	ript	ion																	
Α	RW	PIN		[03	31]					ı	Pin n	ıum	ber																	
В	RW	CONNECT								(Conr	nect	ion																	
			Disconnected	1						- 1	Disco	onne	ect																	
			Connected	0						(Conr	nect																		

32.5.13 PSEL.MOSI

Address offset: 0x510

Pin select for MOSI signal

numbe	er		31	30 2	29 2	28 2	7 26	25	24	23	22 2:	1 20	3 19	18 1	17 1	6 15	14	13	12 1	1 10	9	8	7	6 5	5 4	3	2	1 0
			В																						Α	Α	Α	А А
et 0xF	FFFFFF		1	1	1	1 1	. 1	1	1	1	1 1	. 1	. 1	1	1 1	l 1	1	1	1	1 1	1	1	1	1 1	l 1	1	1	1 1
RW	Field	Value Id	Val	lue						Des	cript	tion																
RW	PIN		[0	.31]						Pin	num	ber																
RW	CONNECT									Cor	nect	ion																
		Disconnected	1							Disc	conn	ect																
		Connected	0							Con	nect																	
	set 0xF RW RW		set 0xFFFFFFF RW Field Value Id RW PIN RW CONNECT Disconnected	B B Set 0xFFFFFFF	B Set 0xFFFFFFF	B	B	B	B	B Set OxFFFFFFFF	B Set 0xFFFFFFFF	B	B	B Set 0xFFFFFFFF	B Set 0xFFFFFFFF	B Set 0xFFFFFFFF	B Set OxFFFFFFFF 1 1 1 1 1 1 1 1	B Set OxFFFFFFF 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	B Set OxFFFFFFF 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	B Set OxFFFFFFF 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	B Set OxFFFFFFF 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	B Set OxFFFFFFF 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	RW Field Value Id Value Id PIN [031] ** ** ** ** ** ** ** ** ** ** ** ** **	A A A A A A A A A A				

32.5.14 PSEL.CSN

Address offset: 0x514

Pin select for CSN signal

Bit	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

32.5.15 RXDPTR (Deprecated)

Address offset: 0x534 RXD data pointer



Bit r	numbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	A A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	RXDPTR										RXI) da	ata	poi	ntei	r																	

32.5.16 MAXRX (Deprecated)

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit r	numbe	er		31	30 2	9 2	28 2	7 26	25	24	23	22 :	21 2	20 1	L9 1	8 1	7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id																										Α	Α	Α	Α.	A A	A	A
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0 () () (0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	otio	n																		
Α	RW	MAXRX									Ma	xim	um	nu	mbe	r o	f by	tes	in r	ece	ive l	ouff	er									

32.5.17 AMOUNTRX (Deprecated)

Address offset: 0x53C

Number of bytes received in last granted transaction

Bit n	umbe	er		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A A A A A A A A
Rese	t 0x0	0000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	R	AMOUNTRX			Number of bytes received in the last granted transaction

32.5.18 RXD.PTR

Address offset: 0x534 RXD data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$
ld RW Field	Value Id	Value Description
A RW PTR		RXD data pointer

32.5.19 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bitı	numbe	er		31	30 29	9 28	8 27	26	25	24	23 :	22 2	21 2	20 1	9 1	8 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																										Α	Α	Α	Α	Α	Α.	А А
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ue						Des	crip	tio	n																		
Α	RW	MAXCNT									Ma	ximı	ım	nur	nbe	r of	byt	es i	n re	cei	/e b	uff	er									

32.5.20 RXD.AMOUNT

Address offset: 0x53C

Number of bytes received in last granted transaction

Id	number set 0x00000000		31 30 29 28 27	26 25 24 23 22 21 20	19 18 17 16	15 14 15	12 11 10	9 6					1 0 A A	
Res	et 0x0	0000000		0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0	0 0 0	0 0 0	0 0	0 (0	0	0 0	0 0
Id	RW	Field	Value Id	Value	Description									

R AMOUNT Number of bytes received in the last granted transaction



32.5.21 TXDPTR (Deprecated)

Address offset: 0x544

TXD data pointer

Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Id Reset 0x00000000 ld RW Field Value Id

RW TXDPTR TXD data pointer

32.5.22 MAXTX (Deprecated)

Address offset: 0x548

Maximum number of bytes in transmit buffer

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Id AAAAAAA Reset 0x00000000 ld RW Field Value Id RW MAXTX Maximum number of bytes in transmit buffer

32.5.23 AMOUNTTX (Deprecated)

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 $\mathsf{A} \ \mathsf{A} \ \mathsf{A}$ Reset 0x00000000 Id RW Field Value Id Value Description

R AMOUNTTX Number of bytes transmitted in last granted transaction

32.5.24 TXD.PTR

Address offset: 0x544

TXD data pointer

Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Id Reset 0x00000000 ld RW Field Description Value Id Value RW PTR TXD data pointer

32.5.25 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Id $\mathsf{A} \ \mathsf{A} \ \mathsf{A}$ Reset 0x00000000 ld RW Field Value Id RW MAXCNT Maximum number of bytes in transmit buffer

32.5.26 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transmitted in last granted transaction



32.5.27 CONFIG

Address offset: 0x554 Configuration register

Bit r	umbe	r		31	30	29	28 :	27 :	26 2	5 2	4 2	3 22	21	20	19	18	17 :	16 1	L5 :	14 1	.3 1	2 11	. 10	9	8	7	6	5	4	3 2	1	0
Id																														С	В	Α
Res	t 0x0	0000000		0	0	0	0	0	0	0 0)	0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						0)escr	iptic	on																		
Α	RW	ORDER									Е	it or	der																			
			MsbFirst	0							Ν	Лost	sign	ific	ant	bit	shif	ted	ou	t fir	st											
			LsbFirst	1							L	.east	sign	ific	ant	bit	shif	ted	ou	t fir	st											
В	RW	СРНА									S	erial	clo	ck (5	SCK) ph	ase															
			Leading	0							S	amp	le o	n le	adiı	ng e	dge	of	clo	ck,	shift	ser	ial d	lata	on 1	trai	iling	5				
											e	dge																				
			Trailing	1							S	amp	le o	n tr	ailir	ng e	dge	of	clo	ck, s	hift	ser	al d	ata	on l	ead	ding	5				
											e	dge																				
С	RW	CPOL									S	erial	clo	ck (SCK) po	lari	ty														
			ActiveHigh	0							A	ctive	e hig	h																		
			ActiveLow	1							A	ctive	e lov	v																		

32.5.28 DEF

Address offset: 0x55C

Default character. Character clocked out in case of an ignored transaction.

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0									
Id			A A A A A A A A									
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0									
ld RW Field	Value Id	Value	Description									
A RW DEF		Default character. Character clocked out in case of an ignored										
			transaction									

32.5.29 ORC

Address offset: 0x5C0
Over-read character

Bit r	umber		31	L 30	29 2	28 27	7 26	25	24	23 :	22 2	1 20	0 19	18	17	16 1	.5 1	4 13	12 3	11 10	9	8	7	6	5 4	1 3	2	1	0	
Id																								Α	Α	A A	Δ Δ	Α	Α	Α
Res	t 0x0000		0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0 0	0	0	0	0	0 (0	0	0	0	
Id	RW Fi	eld	Value Id	Va	alue						Des	cript	tion																	
Α	RW OF	RC		Over-read character. Character clocked out after an over-read																										
				of the transmit buffer.																										



32.6 Electrical specification

32.6.1 SPIS slave interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{SPIS}	Bit rates for SPIS ²⁷			8 ²⁸	Mbps
I _{SPIS,2Mbps}	Run current for SPIS, 2 Mbps		45		μΑ
I _{SPIS,8Mbps}	Run current for SPIS, 8 Mbps		45		μΑ
I _{SPIS,IDLE}	Idle current for SPIS (STARTed, no CSN activity)		1		μΑ
t _{SPIS,LP,START}	Time from RELEASE task to ready to receive/transmit (CSN		t _{SPIS,CL,ST}	AR	μs
	active), Low power mode		+		
			t _{START_HF}	IN	
t _{SPIS,CL,START}	Time from RELEASE task to receive/transmit (CSN active),		0.125		μs
	Constant latency mode				

32.6.2 Serial Peripheral Interface Slave (SPIS) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{SPIS} ,CSCKIN,8Mbps	SCK input period at 8Mbps		125		ns
t _{SPIS,CSCKIN,4Mbps}	SCK input period at 4Mbps		250		ns
t _{SPIS,CSCKIN,2Mbps}	SCK input period at 2Mbps		500		ns
t _{SPIS,RFSCKIN}	SCK input rise/fall time			30	ns
t _{SPIS,WHSCKIN}	SCK input high time	30			ns
t _{SPIS,WLSCKIN}	SCK input low time	30			ns
t _{SPIS,SUCSN,LP}	CSN to CLK setup time, Low power mode	t _{SPIS,SUCS}	N,		ns
		+			
		t _{START_HE}	IN		
t _{SPIS,SUCSN,CL}	CSN to CLK setup time, Constant latency mode	1000			ns
t _{SPIS,HCSN}	CLK to CSN hold time	2000			ns
t _{SPIS,ASO}	CSN to MISO driven ^a			1000	ns
t _{SPIS,DISSO}	CSN to MISO disabled ^a			68	ns
t _{SPIS,CWH}	CSN inactive time	300			ns
t _{SPIS,VSO}	CLK edge to MISO valid			19	ns
t _{SPIS,HSO}	MISO hold time after CLK edge	18 ²⁹			ns
t _{SPIS,SUSI}	MOSI to CLK edge setup time	59			ns
t _{SPIS,HSI}	CLK edge to MOSI hold time	20			ns

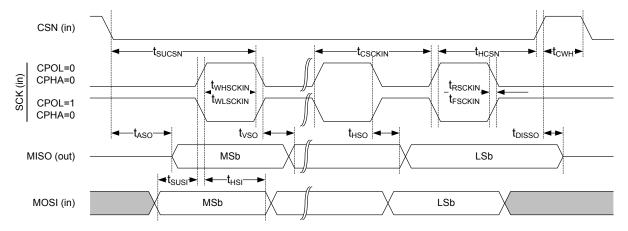


Figure 75: SPIS timing diagram

Higher bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

²⁸ The actual maximum data rate depends on the master's CLK to MISO and MOSI setup and hold timings.

^a At 25pF load, including GPIO capacitance, see GPIO spec.

This is to ensure compatibility to SPI masters sampling MISO on the same edge as MOSI is output



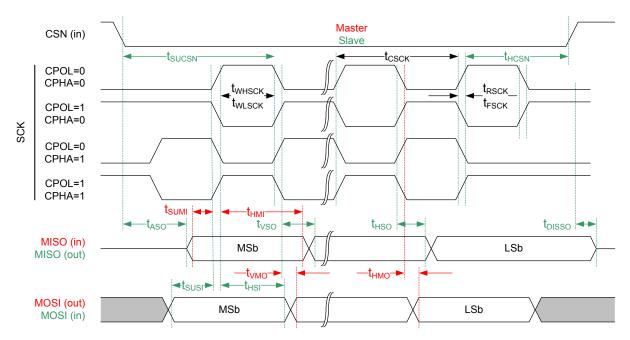


Figure 76: Common SPIM and SPIS timing diagram



33 TWIM — I²C compatible two-wire interface master with EasyDMA

TWI master with EasyDMA (TWIM) is a two-wire half-duplex master which can communicate with multiple slave devices connected to the same bus

Listed here are the main features for TWIM:

- I²C compatible
- 100 kbps, 250 kbps, or 400 kbps
- · Support for clock stretching
- EasyDMA

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. TWIM is not compatible with CBUS.

The GPIOs used for each two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

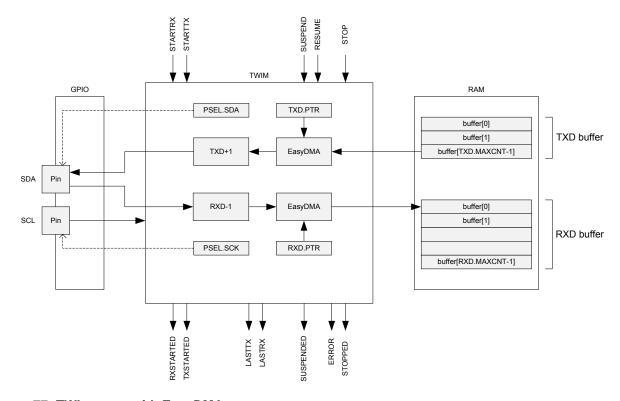


Figure 77: TWI master with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see *Figure 78: A typical TWI setup comprising one master and three slaves* on page 306. This TWIM is only able to operate as a single master on the TWI bus. Multi-master bus configuration is not supported.



Figure 78: A typical TWI setup comprising one master and three slaves

This TWI master supports clock stretching performed by the slaves. The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task. The TWI master will generate a STOPPED event when it has stopped following a STOP task.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

After the TWI master is started, the STARTTX task or the STARTRX task should not be triggered again before the TWI master has stopped, i.e. following a LASTRX, LASTTX or STOPPED event.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

33.1 Shared resources

The TWI master shares registers and other resources with other peripherals that have the same ID as the TWI master. Therefore, you must disable all peripherals that have the same ID as the TWI master before the TWI master can be configured and used.

Disabling a peripheral that has the same ID as the TWI master will not reset any of the registers that are shared with the TWI master. It is therefore important to configure all relevant registers explicitly to secure that the TWI master operates correctly.

The Instantiation table in *Instantiation* on page 24 shows which peripherals have the same ID as the TWI.

33.2 EasyDMA

The TWI master implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

33.2.1 EasyDMA list

EasyDMA supports one list type.

The supported list type is:

Array list

EasyDMA array list

The EasyDMA array list can be represented by the data structure ArrayList_type.

For illustration, see the code example below. This data structure includes only a buffer with size equal to Channel.MAXCNT. EasyDMA will use the Channel.MAXCNT register to determine when the buffer is full. Replace 'Channel' by the specific data channel you want to use, for instance 'NRF_SPIM->RXD', 'NRF_SPIM->TXD', 'NRF_TWIM->RXD', etc.



The Channel.MAXCNT register cannot be specified larger than the actual size of the buffer. If Channel.MAXCNT is specified larger than the size of the buffer, the EasyDMA channel may overflow the buffer.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM

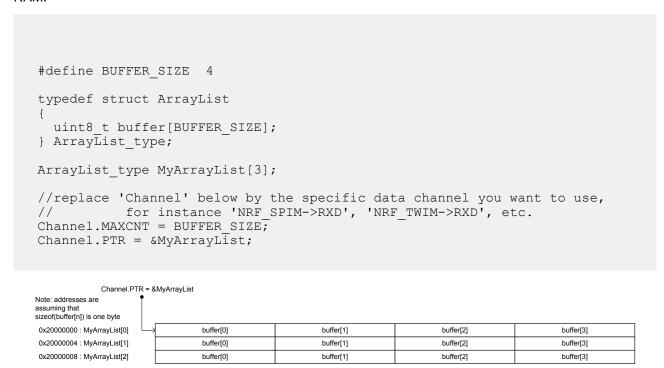


Figure 79: EasyDMA array list

33.3 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes found in the transmit buffer located in RAM at the address specified in the TXD.PTR register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave.

A typical TWI master write sequence is illustrated in *Figure 80: TWI master writing data to a slave* on page 308. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.



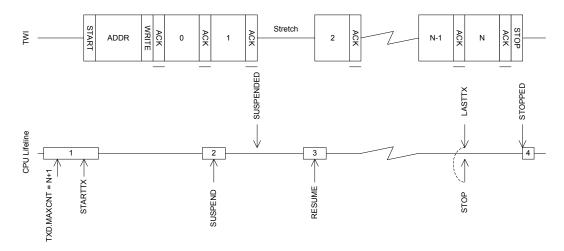


Figure 80: TWI master writing data to a slave

The TWI master will generate a LASTTX event when it starts to transmit the last byte, this is illustrated in *Figure 80: TWI master writing data to a slave* on page 308

The TWI master is stopped by triggering the STOP task, this task should be triggered during the transmission of the last byte to secure that the TWI will stop as fast as possible after sending the last byte. It is safe to use the shortcut between LASTTX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the whole RAM buffer has been sent, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

33.4 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1). The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

Data received will be stored in RAM at the address specified in the RXD.PTR register. The TWI master will generate an ACK after all but the last byte received from the slave. The TWI master will generate a NACK after the last byte received to indicate that the read sequence shall stop.

A typical TWI master read sequence is illustrated in *Figure 81: The TWI master reading data from a slave* on page 309. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.

The TWI master will generate a LASTRX event when it is ready to receive the last byte, this is illustrated in *Figure 81: The TWI master reading data from a slave* on page 309. If RXD.MAXCNT > 1 the LASTRX event is generated after sending the ACK of the previously received byte. If RXD.MAXCNT = 1 the LASTRX event is generated after receiving the ACK following the address and READ bit.

The TWI master is stopped by triggering the STOP task, this task must be triggered before the NACK bit is supposed to be transmitted. The STOP task can be triggered at any time during the reception of the last byte. It is safe to use the shortcut between LASTRX and STOP to accomplish this.



Note that the TWI master does not stop by itself when the RAM buffer is full, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

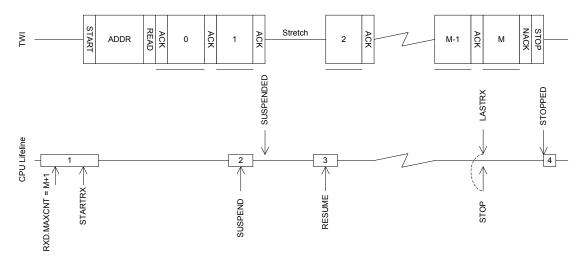


Figure 81: The TWI master reading data from a slave

33.5 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave. This example uses shortcuts to perform the simplest type of repeated start sequence, i.e. one write followed by one read. The same approach can be used to perform a repeated start sequence where the sequence is read followed by write.

The figure Figure 82: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave on page 309 illustrates this:

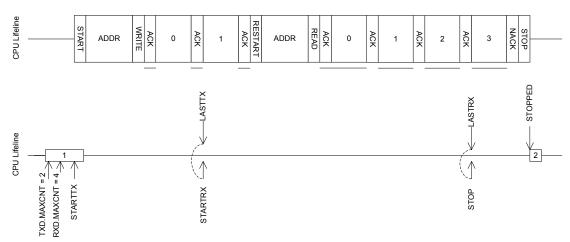


Figure 82: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave

If a more complex repeated start sequence is needed and the TWI firmware drive is serviced in a low priority interrupt it may be necessary to use the SUSPEND task and SUSPENDED event to guarantee that the correct tasks are generated at the correct time. This is illustrated in *Figure 83: A double repeated start* sequence using the SUSPEND task to secure safe operation in low priority interrupts on page 310.



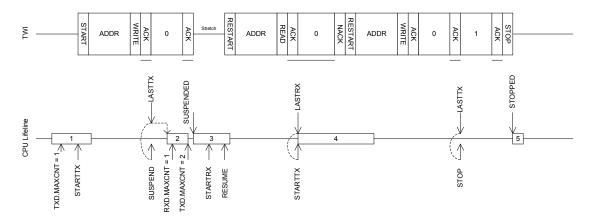


Figure 83: A double repeated start sequence using the SUSPEND task to secure safe operation in low priority interrupts

33.6 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

33.7 Master mode pin configuration

The SCL and SDA signals associated with the TWI master are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI master is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.SCL, PSEL.SDA must only be configured when the TWI master is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table 73: GPIO configuration before enabling peripheral* on page 310.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 73: GPIO configuration before enabling peripheral

TWI master signal	TWI master pin	Direction	Output value	Drive strength
SCL	As specified in PSEL.SCL	Input	Not applicable	SOD1
SDA	As specified in PSEL.SDA	Input	Not applicable	SOD1

33.8 Registers

Table 74: Instances

Base address	Peripheral	Instance	Description	Configuration			
0x40003000	TWIM	TWIM0 Two-wire interface master 0					
0x40004000	TWIM	TWIM1	Two-wire interface master 1				



Table 75: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start TWI receive sequence
TASKS_STARTTX	0x008	Start TWI transmit sequence
TASKS_STOP	0x014	Stop TWI transaction. Must be issued while the TWI master is not suspended.
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_ERROR	0x124	TWI error
EVENTS_SUSPENDED	0x148	Last byte has been sent out after the SUSPEND task has been issued, TWI traffic is now suspended.
EVENTS_RXSTARTED	0x14C	Receive sequence started
EVENTS_TXSTARTED	0x150	Transmit sequence started
EVENTS_LASTRX	0x15C	Byte boundary, starting to receive the last byte
EVENTS_LASTTX	0x160	Byte boundary, starting to transmit the last byte
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4C4	Error source
ENABLE	0x500	Enable TWIM
PSEL.SCL	0x508	Pin select for SCL signal
PSEL.SDA	0x50C	Pin select for SDA signal
FREQUENCY	0x524	TWI frequency
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
TXD.LIST	0x550	EasyDMA list type
ADDRESS	0x588	Address used in the TWI transfer

33.8.1 SHORTS

Address offset: 0x200

Shortcut register

Bit	number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F D C B A
Res	et 0x00000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW LASTTX_STARTRX			Shortcut between LASTTX event and STARTRX task
				See EVENTS_LASTTX and TASKS_STARTRX
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
В	RW LASTTX_SUSPEND			Shortcut between LASTTX event and SUSPEND task
				See EVENTS_LASTTX and TASKS_SUSPEND
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
С	RW LASTTX_STOP			Shortcut between LASTTX event and STOP task
				See EVENTS_LASTTX and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
D	RW LASTRX_STARTTX			Shortcut between LASTRX event and STARTTX task
				See EVENTS_LASTRX and TASKS_STARTTX
		Disabled	0	Disable shortcut



Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			F D C B A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Enabled	1	Enable shortcut
F RW LASTRX_STOP			Shortcut between LASTRX event and STOP task
			See EVENTS_LASTRX and TASKS_STOP
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut

33.8.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit	numbe	er		31 3	30 2	9 2	8 27	26	25	24	23 2	2 21	20	19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5 4	3	2	1	0
Id										J	1		Н	G	F									D							Α	
Res	et 0x0	0000000		0	0 (0 (0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C
ld	RW	Field	Value Id	Valu	ıe						Desc	ripti	ion																			
Α	RW	STOPPED									Enab	le o	r di	isab	le i	nte	rru	ot fo	or S	TOP	PEI	D e	vent	t								
											See	VEN	VTS	_57	ΌР	PEL)															
			Disabled	0							Disal	ole																				
			Enabled	1							Enab	le																				
D	RW	ERROR									Enab	le o	r di	isab	le i	nte	rru	ot fo	or E	RRC	Re	eve	nt									
											See	VEN	VTS	_EF	RRO	R																
			Disabled	0							Disal																					
			Enabled	1							Enab	le																				
F	RW	SUSPENDED									Enab	le o	r di	isab	le i	nte	rru	ot fo	or S	USP	ENI	DE	D ev	ent								
											See	VEN	VTS	_SL	JSP	ENL	DED															
			Disabled	0							Disal	ole																				
			Enabled	1							Enab	le																				
G	RW	RXSTARTED									Enab	le o	r di	isab	le i	nte	rru	ot fo	or R	XST	٩R٦	TEC	eve	ent								
											See	VEN	VTS	R)	(ST)	4RT	ΈD															
			Disabled	0							Disal			_																		
			Enabled	1							Enab	le																				
Н	RW	TXSTARTED									Enab	le o	r di	isab	le i	nte	rru	ot fo	or T	XST	4R1	ΓEC	eve	ent								
											See	VEN	VTS	T)	(ST)	4 <i>RT</i>	ΈD															
			Disabled	0							Disal			_																		
			Enabled	1							Enab	le																				
I	RW	LASTRX									Enab	le o	r di	isab	le i	nte	rru	ot fo	or L	AST	RX (eve	ent									
											See L	VEN	VTS	LA	STI	RX																
			Disabled	0							Disal			_																		
			Enabled	1							Enab	le																				
J	RW	LASTTX									Enab	le o	r di	isab	le i	nte	rru	ot fo	or L	AST	ГΧ є	eve	ent									
											See	VEN	VT.S	i LA	ST	TΧ																
			Disabled	0							Disal																					
			Enabled	1							Enab																					

33.8.3 INTENSET

Address offset: 0x304 Enable interrupt



Bit r	numb	er		31 30	29 2	28 2	7 26	25 2	24 :	2 21 20 19 18 17 16 15 14 13 12 13	10 9	8	7	5 5	4	3 2	2 1	0
Id									J	H G F	D						Α	
Res	et 0x0	00000000		0 0	0	0 0	0	0	0	0 0 0 0 0 0 0 0 0 0 0	0 0	0	0	0 0	0	0 0	0	0
Id	RW	Field	Value Id	Value					ı	cription								
Α	RW	STOPPED							١	e '1' to Enable interrupt for STOPPED	event							
									:	EVENTS_STOPPED								
			Set	1					ı	ole								
			Disabled	0					-	d: Disabled								
			Enabled	1					ı	d: Enabled								
D	RW	ERROR							١	e '1' to Enable interrupt for ERROR e	vent							
									:	EVENTS_ERROR								
			Set	1					ı	ole								
			Disabled	0					1	d: Disabled								
			Enabled	1					-	d: Enabled								
F	RW	SUSPENDED							١	e '1' to Enable interrupt for SUSPEND	ED ev	ent						
									:	EVENTS_SUSPENDED								
			Set	1					ı	ole								
			Disabled	0					-	d: Disabled								
			Enabled	1					ı	d: Enabled								
G	RW	RXSTARTED							١	e '1' to Enable interrupt for RXSTART	ED eve	nt						
									:	EVENTS_RXSTARTED								
			Set	1					ı	ole								
			Disabled	0					ı	d: Disabled								
			Enabled	1					ı	d: Enabled								
Н	RW	TXSTARTED							١	e '1' to Enable interrupt for TXSTART	ED eve	nt						
									:	EVENTS_TXSTARTED								
			Set	1					ı	ole								
			Disabled	0					-	d: Disabled								
			Enabled	1					ı	d: Enabled								
1	RW	LASTRX							١	e '1' to Enable interrupt for LASTRX e	vent							
									:	EVENTS_LASTRX								
			Set	1					ı	ole								
			Disabled	0					-	d: Disabled								
			Enabled	1					ı	d: Enabled								
J	RW	LASTTX							١	e '1' to Enable interrupt for LASTTX e	vent							
									:	EVENTS_LASTTX								
			Set	1					1	ole								
			Disabled	0					ı	d: Disabled								
			Enabled	1					ı	d: Enabled								

33.8.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		J I H G F D A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW STOPPED		Write '1' to Disable interrupt for STOPPED event
		See EVENTS_STOPPED
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
D RW ERROR		Write '1' to Disable interrupt for ERROR event
		See EVENTS_ERROR



Bit number	31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		JI HGF D A
Reset 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
Clear	1	Disable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
F RW SUSPENDED		Write '1' to Disable interrupt for SUSPENDED event
		See EVENTS_SUSPENDED
Clear	1	Disable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
G RW RXSTARTED		Write '1' to Disable interrupt for RXSTARTED event
		See EVENTS_RXSTARTED
Clear	1	Disable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
H RW TXSTARTED		Write '1' to Disable interrupt for TXSTARTED event
		See EVENTS_TXSTARTED
Clear	1	Disable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
I RW LASTRX		Write '1' to Disable interrupt for LASTRX event
		Son EVENTS LASTRY
Clear	1	See EVENTS_LASTRX Disable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
J RW LASTTX	1	Write '1' to Disable interrupt for LASTTX event
J NW LASTIA		·
		See EVENTS_LASTTX
Clear	1	Disable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled

33.8.5 ERRORSRC

Address offset: 0x4C4

Error source

Bit	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			C B A
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
Α	RW OVERRUN		Overrun error
			A new byte was received before previous byte got transferred
			into RXD buffer. (Previous data is lost)
		NotReceived	0 Error did not occur
		Received	1 Error occurred
В	RW ANACK		NACK received after sending the address (write '1' to clear)
		NotReceived	0 Error did not occur
		Received	1 Error occurred
С	RW DNACK		NACK received after sending a data byte (write '1' to clear)
		NotReceived	0 Error did not occur
		Received	1 Error occurred

33.8.6 ENABLE

Address offset: 0x500



Enable TWIM

	Bit n	iumbe	er		31 30	29	28 2	27 2	26 2	5 2	4 2	3 2	2 2	1 2	0 1	9 18	3 17	7 16	15	14	13	12	11 :	10	9 ;	3 7	' 6	5	4	3	2	1 (5
	Id																													Α	Α	A A	Δ
	Rese	et 0x0	0000000		0 0	0	0	0	0 (0) (0) (0) (0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 (o
	Id	RW	Field	Value Id	Value						D	esc	rip	tion	•																		
Ī	Α	RW	ENABLE								Ε	nab	le d	or d	isal	ole .	ΓWI	М															_
				Disabled	0						D	isal	ble	TW	IM																		
				Enabled	6						Ε	nab	le 1	ΓWI	М																		

33.8.7 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

Bit r	numbe	er		33	1 30	29	28	27	26	25	24	23	22	21	20 :	19 1	l8 1	7 16	15	14	13 1	.2 1	1 10	9	8	7	6	5 4	1 3	2	1	0
Id				В																								A	Δ Δ	Α	Α	Α
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1 1	1	1	1	1 1	. 1	1	1	1	1	1 1	L 1	1	1	1
Id	RW	Field	Value Id	V	alue							De	scri	ptic	n																	
Α	RW	PIN		[0)31]						Pin	nu	mbe	er																	
В	RW	CONNECT										Coi	nne	ctio	n																	
			Disconnected	1								Dis	con	nec	t																	
			Connected	0								Coi	nne	ct																		

33.8.8 PSEL.SDA

Address offset: 0x50C Pin select for SDA signal

t numb	er		31 30 29 28 27 26 25 2	$24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0$
			В	АААА
eset Oxl	FFFFFF		1 1 1 1 1 1 1	$1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1$
RW	Field	Value Id	Value	Description
RW	PIN		[031]	Pin number
RW	CONNECT			Connection
		Disconnected	1	Disconnect
		Connected	0	Connect
•	eset 0xF RW	RW PIN	eset 0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	B

33.8.9 FREQUENCY

Address offset: 0x524

TWI frequency

Bitı	numbe	r		31	. 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	. 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	. 4	A
Res	et 0x0	4000000		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue	:						Des	scri	otic	n																			
Α	RW	FREQUENCY										TW	/I m	aste	er c	locl	c fre	qu	end	у														
			K100	0x	019	9800	000)				100) kb	ps																				
			K250	0x	040	000	000)				250) kb	ps																				
						1000) kb																					

33.8.10 RXD.PTR

Address offset: 0x534

Data pointer



Е	3it n	umb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
1	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
F	Rese	t Ox	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
ı	d	RW	Field	Value Id	Va	lue							De	scri	pti	on																			
A	4	RW	PTR										Da	ta p	oin	ter																			

33.8.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

																		_	_	_				
Bit nu	mber		31 30 29 28 27 26	25 24	4 23	22 2	21 20	0 19	18	1/:	16 1	15 1	4 1:	3 12	11 1	.0 9	8	/	6	5	4	3 4	! 1	U
Id																		Α	Α	Α	Α	A A	A	. A
Reset	0x0000000		0 0 0 0 0 0	0 0	0	0	0 0	0	0	0	0	0 (0 (0	0 (0 0	0	0	0	0	0	0 (0	0
Id	RW Field	Value Id	Value		De	scrip	tion	1																
Α	RW MAXCNT		[1255]		Ma	ıximı	ım r	numl	oer (of b	ytes	in i	rece	ive b	uffe	r								

33.8.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit r	umbe	er		33	1 30	29	28	27 2	6 2	5 24	4 2	3 22	21	20 1	19 1	8 1	7 1	5 15	14	13	12	11 1	.0 9	9	8 7	' E	5	4	3	2	1)
Id																									A		A	Α	Α	Α	Α.	4
Res	t OxC	0000000		0	0	0	0	0 0) (0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 ()	0 0	0	0	0	0	0	0)
Id	RW	Field	Value Id	V	alue	•					D	escr	iptic	on																		ı
Α	R	AMOUNT									Ν	umb	er c	f by	tes	trar	ısfe	rred	in	the	last	trar	ısac	tio	n. Ir	ca	se o	f				_
											N	ACK	erro	or, ir	nclu	des	the	NA	CK'e	ed b	yte.											

33.8.13 RXD.LIST

Address offset: 0x540 EasyDMA list type

Bit	numbe	r		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16 1	.5 1	4 1	3 12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																A ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	alue	!						De	scri	ptic	on																		
Α	RW	LIST										Lis	t ty	pe																			
			Disabled	0								Dis	abl	e Ea	syE	M	۱ lis	t															
			ArrayList	1								Us	e ar	ray	list																		
				1											,																		

33.8.14 TXD.PTR

Address offset: 0x544

Data pointer

Bit number		31 30 29 28	27 26 25 24	4 23 22 21	20 19	18 17	16 15 :	l4 13 1	2 11 1	0 9	8	7 6	5 5	4	3 2	2 1	0
Id		A A A A	AAAA	. A A A	АА	АА	АА	Α А .	4 A A	A	Α	A A	A A	Α	A A	A	Α
Reset 0x00000000		0 0 0 0	0 0 0 0	0 0 0	0 0	0 0	0 0	0 0	0 0	0	0	0 (0	0	0 0	0	0
ld RW Field	Value Id	Value		Descripti	on												
A RW PTR				Data poi	nter												

33.8.15 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer



Bit	numb	er		31	30 2	9 2	28 2	7 26	25	24	23	22 2	1 2	0 1	9 18	3 17	16	15	14 1	.3 1	2 11	10	9	8	7	6	5	4	3 2	2 1	0
Id																									Α	Α	Α	Α	A A	A A	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	tio	n																	
Α	RW	MAXCNT		[1.	.255						Ma	ximu	ım	nun	nber	of b	oyte	s in	tra	nsm	it bı	ıffer									

33.8.16 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit r	numbe	er		31	30	29	28 2	7 26	5 25	5 24	23	22	21	20	19 :	18 1	7 1	6 15	14	13	12	11 1	0 9	8	7	6	5	4	3 2	2 1	1 0
Id																									Α	Α	Α	Α	A A	A /	4 А
Res	et OxC	0000000		0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue						De	escri	ptic	on																	
Α	R	AMOUNT									Νι	ımb	er c	of by	ytes	tra	nsfe	rrec	l in	the	last	trar	sact	ion	. In	case	e of				
											N/	ACK	erro	or, i	nclu	ides	the	NA	CK'	ed b	yte.										

33.8.17 TXD.LIST

Address offset: 0x550 EasyDMA list type

Bit	numb	er		31	. 30	29	28	3 27	26	5 25	5 24	1 23	3 22	2 21	20	19	18	17	16	15	14	13	12	11 1	10	9	8	7	6	5	4	3	2 :	. 0
Id																																	Δ Α	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0
Id	RW	Field	Value Id	Va	lue							D	esc	ript	ion																			
Α	RW	LIST										Li	st t	ype																				
			Disabled	0								Di	sak	ole E	asy	DΝ	1A I	ist																
			ArrayList	1								U	se a	arra	y lis	t																		

33.8.18 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

Bit number		31 30 29 28 27	' 26 25 24 23 22 21 20 19 18	3 17 16 15 14 13 12 13	1 10 9 8 7	6 5	4 3	2 1	1 0
Id						A A	А А	A A	4 А
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0	0 0	0 0	0 0	0 0
ld RW Field	Value Id	Value	Description						
A RW ADDRESS			Address used in th	e TWI transfer					

33.9 Electrical specification

33.9.1 TWIM interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIM}	Bit rates for TWIM ³⁰	100		400	kbps
I _{TWIM,100kbps}	Run current for TWIM, 100 kbps		50		μΑ
I _{TWIM,400kbps}	Run current for TWIM, 400 kbps		50		μΑ
t _{TWIM,START,LP}	Time from STARTRX/STARTTX task to transmission started, Low		t _{TWIM,ST}	AR1	μs
	power mode		+		
			t _{START_H}	FIN	
t _{TWIM,START,CL}	Time from STARTRX/STARTTX task to transmission started,		1.5		μs
	Constant latency mode				

Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



33.9.2 Two Wire Interface Master (TWIM) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIM,SCL,100kbps}	SCL clock frequency, 100 kbps		100		kHz
f _{TWIM,SCL,250kbps}	SCL clock frequency, 250 kbps		250		kHz
f _{TWIM,SCL,400kbps}	SCL clock frequency, 400 kbps		400		kHz
t _{TWIM,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t_{TWIM,HD_DAT}	Data hold time after negative edge on SCL – all modes	500			ns
t _{TWIM,HD_STA,100kbps}	TWIM master hold time for START and repeated START condition, 100 kbps	10000			ns
t _{TWIM,HD_STA,250kbps}	TWIM master hold time for START and repeated START condition, 250kbps	4000			ns
$t_{TWIM,HD_STA,400kbps}$	TWIM master hold time for START and repeated START condition, 400 kbps	2500			ns
$t_{\sf TWIM,SU_STO,100kbps}$	TWIM master setup time from SCL high to STOP condition, 100 kbps	5000			ns
t _{TWIM} ,SU_STO,250kbps	TWIM master setup time from SCL high to STOP condition, 250 kbps	2000			ns
t _{TWIM} ,SU_STO,400kbps	TWIM master setup time from SCL high to STOP condition, 400 kbps	1250			ns
t _{TWIM} ,BUF,100kbps	TWIM master bus free time between STOP and START conditions, 100 kbps	5800			ns
t _{TWIM,BUF,250kbps}	TWIM master bus free time between STOP and START conditions, 250 kbps	2700			ns
t _{TWIM} ,BUF,400kbps	TWIM master bus free time between STOP and START conditions, 400 kbps	2100			ns

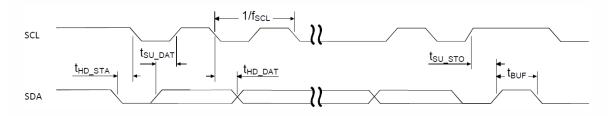


Figure 84: TWIM timing diagram, 1 byte transaction

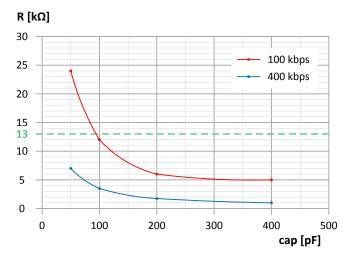


Figure 85: Recommended TWIM pullup value vs. line capacitance

- The I2C specification allows a line capacitance of 400 pF at most.
- The nRF52832 internal pullup has a fixed value of typ. 13 kOhm, see R_{PU} in the GPIO chapter.



34 TWIS — I²C compatible two-wire interface slave with EasyDMA

TWI slave with EasyDMA (TWIS) is compatible with I²C operating at 100 kHz and 400 kHz. The TWI transmitter and receiver implement EasyDMA.

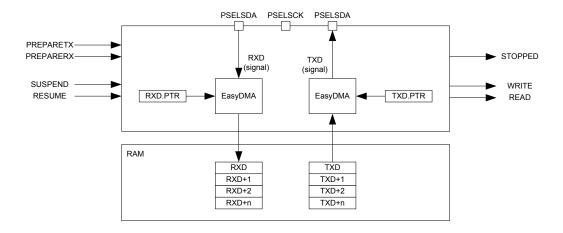


Figure 86: TWI slave with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see *Figure 87: A typical TWI setup comprising one master and three slaves* on page 319. TWIS is only able to operate with a single master on the TWI bus.

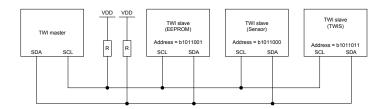


Figure 87: A typical TWI setup comprising one master and three slaves

The TWI slave state machine is illustrated in *Figure 88: TWI slave state machine* on page 320 and *Table 76: TWI slave state machine symbols* on page 320 is explaining the different symbols used in the state machine.



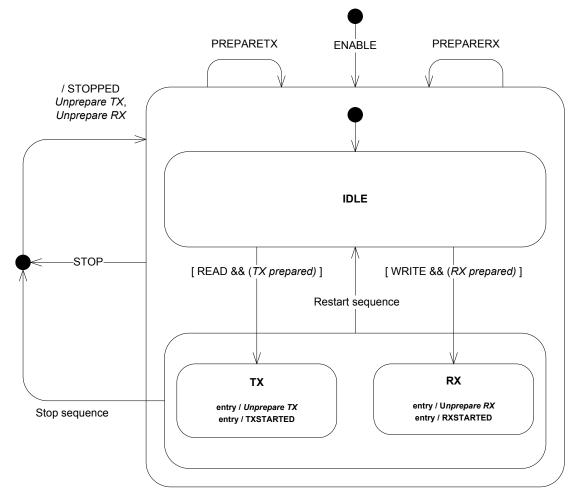


Figure 88: TWI slave state machine

Table 76: TWI slave state machine symbols

Symbol	Туре	Description
ENABLE	Register	The TWI slave has been enabled via the ENABLE register
PREPARETX	Task	The TASKS_PREPARETX task has been triggered
STOP	Task	The TASKS_STOP task has been triggered
PREPARERX	Task	The TASKS_PREPARERX task has been triggered
STOPPED	Event	The EVENTS_STOPPED event was generated
RXSTARTED	Event	The EVENTS_RXSTARTED event was generated
TXSTARTED	Event	The EVENTS_TXSTARTED event was generated
TX prepared	Internal	Internal flag indicating that a TASKS_PREPARETX task has been triggered. This flag is not visible to the user.
RX prepared	Internal	Internal flag indicating that a TASKS_PREPARERX task has been triggered. This flag is not visible to the user.
Unprepare TX	Internal	Clears the internal 'TX prepared' flag until next TASKS_PREPARETX task.
Unprepare RX	Internal	Clears the internal 'RX prepared' flag until next TASKS_PREPARERX task.
Stop sequence	TWI protocol	A TWI stop sequence was detected
Restart sequence	TWI protocol	A TWI restart sequence was detected

The TWI slave supports clock stretching performed by the master.

The TWI slave operates in a low power mode while waiting for a TWI master to initiate a transfer. As long as the TWI slave is not addressed, it will remain in this low power mode.

To secure correct behaviour of the TWI slave, PSEL.SCL, PSEL.SDA, CONFIG and the ADDRESS[n] registers, must be configured prior to enabling the TWI slave through the ENABLE register. Similarly, changing these settings must be performed while the TWI slave is disabled. Failing to do so may result in unpredictable behaviour.



34.1 Shared resources

The TWI slave shares registers and other resources with other peripherals that have the same ID as the TWI slave.

Therefore, you must disable all peripherals that have the same ID as the TWI slave before the TWI slave can be configured and used. Disabling a peripheral that has the same ID as the TWI slave will not reset any of the registers that are shared with the TWI slave. It is therefore important to configure all relevant registers explicitly to secure that the TWI slave operates correctly.

The Instantiation table in *Instantiation* on page 24 shows which peripherals have the same ID as the TWI slave.

34.2 EasyDMA

The TWI slave implements EasyDMA for reading and writing to and from the RAM.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

34.3 TWI slave responding to a read command

Before the TWI slave can respond to a read command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume I_{IDLE} .

A read command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the TWI slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the read command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a READ event when it acknowledges the read command.

The TWI slave is only able to detect a read command from the IDLE state.

The TWI slave will set an internal 'TX prepared' flag when the PREPARETX task is triggered.

When the read command is received the TWI slave will enter the TX state if the internal 'TX prepared' flag is set.

If the internal 'TX prepared' flag is not set when the read command is received, the TWI slave will stretch the master's clock until the PREPARETX task is triggered and the internal 'TX prepared' flag is set.

The TWI slave will generate the TXSTARTED event and clear the 'TX prepared' flag ('unprepare TX') when it enters the TX state. In this state the TWI slave will send the data bytes found in the transmit buffer to the master using the master's clock. The TWI slave will consume I_{TX} in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the TX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the 'TX prepared' flag ('unprepare TX') and go back to the IDLE state when it has stopped.

The transmit buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to send TXD.MAXCNT bytes from the transmit buffer for each transaction. If the TWI master



forces the slave to send more than TXD.MAXCNT bytes, the slave will send the byte specified in the ORC register to the master instead. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see TXD.PTR etc., are latched when the TXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the 'TX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 324.

Each byte sent from the slave will be followed by an ACK/NACK bit sent from the master. The TWI master will generate a NACK following the last byte that it wants to receive to tell the slave to release the bus so that the TWI master can generate the stop condition. The TXD.AMOUNT register can be queried after a transaction to see how many bytes were sent.

A typical TWI slave read command response is illustrated in *Figure 89: The TWI slave responding to a read command* on page 322. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

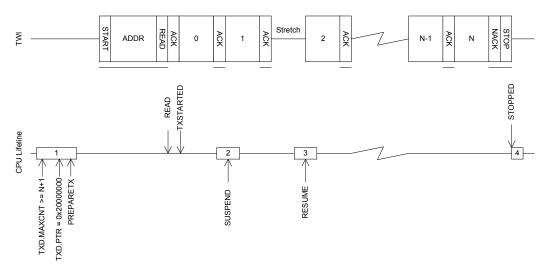


Figure 89: The TWI slave responding to a read command

34.4 TWI slave responding to a write command

Before the TWI slave can respond to a write command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume $I_{\rm IDLE}$.

A write command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the write command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a WRITE event if it acknowledges the write command.

The TWI slave is only able to detect a write command from the IDLE state.

The TWI slave will set an internal 'RX prepared' flag when the PREPARERX task is triggered.

When the write command is received the TWI slave will enter the RX state if the internal 'RX prepared' flag is set.

If the internal 'RX prepared' flag is not set when the write command is received, the TWI slave will stretch the master's clock until the PREPARERX task is triggered and the internal 'RX prepared' flag is set.



The TWI slave will generate the RXSTARTED event and clear the internal 'RX prepared' flag ('unprepare RX') when it enters the RX state. In this state the TWI slave will be able to receive the bytes sent by the TWI master. The TWI slave will consume I_{RX} in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the RX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the internal 'RX prepared' flag ('unprepare RX') and go back to the IDLE state when it has stopped.

The receive buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to receive as many bytes as specified in the RXD.MAXCNT register. If the TWI master tries to send more bytes to the slave than the slave is able to receive, these bytes will be discarded and the bytes will be NACKed by the slave. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see RXD.PTR etc., are latched when the RXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the internal 'RX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 324.

The TWI slave will generate an ACK after every byte received from the master. The RXD.AMOUNT register can be queried after a transaction to see how many bytes were received.

A typical TWI slave write command response is illustrated in *Figure 90: The TWI slave responding to a write command* on page 323. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

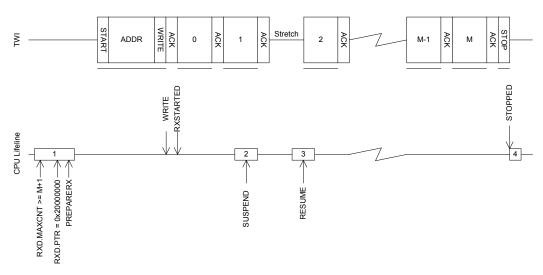


Figure 90: The TWI slave responding to a write command

34.5 Master repeated start sequence

An example of a repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave.

This is illustrated in Figure 91: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave on page 324.

It is here assumed that the receiver does not know in advance what the master wants to read, and that this information is provided in the first two bytes received in the write part of the repeated start sequence. To guarantee that the CPU is able to process the received data before the TWI slave starts to reply to the read command, the SUSPEND task is triggered via a shortcut from the READ event generated when the read command is received. When the CPU has processed the incoming data and prepared the correct data response, the CPU will resume the transaction by triggering the RESUME task.



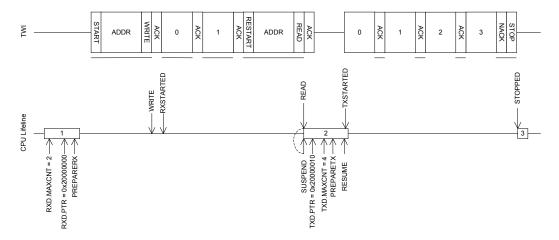


Figure 91: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave

34.6 Terminating an ongoing TWI transaction

In some situations, e.g. if the external TWI master is not responding correctly, it may be required to terminate an ongoing transaction.

This can be achieved by triggering the STOP task. In this situation a STOPPED event will be generated when the TWI has stopped independent of whether or not a STOP condition has been generated on the TWI bus. The TWI slave will release the bus when it has stopped and go back to its IDLE state.

34.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

34.8 Slave mode pin configuration

The SCL and SDA signals associated with the TWI slave are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI slave is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.SCL and PSEL.SDA must only be configured when the TWI slave is disabled.

To secure correct signal levels on the pins used by the TWI slave when the system is in OFF mode, and when the TWI slave is disabled, these pins must be configured in the GPIO peripheral as described in *Table 77: GPIO configuration before enabling peripheral* on page 324.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 77: GPIO configuration before enabling peripheral

TWI slave signal	TWI slave pin	Direction	Output value	Drive strength
SCL	As specified in PSEL.SCL	Input	Not applicable	SOD1
SDA	As specified in PSEL.SDA	Input	Not applicable	S0D1



34.9 Registers

Table 78: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
0x40004000	TWIS	TWIS1	Two-wire interface slave 1	

Table 79: Register Overview

Register	Offset	Description
TASKS_STOP	0x014	Stop TWI transaction
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
TASKS_PREPARERX	0x030	Prepare the TWI slave to respond to a write command
TASKS_PREPARETX	0x034	Prepare the TWI slave to respond to a read command
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_ERROR	0x124	TWI error
EVENTS_RXSTARTED	0x14C	Receive sequence started
EVENTS_TXSTARTED	0x150	Transmit sequence started
EVENTS_WRITE	0x164	Write command received
EVENTS_READ	0x168	Read command received
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4D0	Error source
MATCH	0x4D4	Status register indicating which address had a match
ENABLE	0x500	Enable TWIS
PSEL.SCL	0x508	Pin select for SCL signal
PSEL.SDA	0x50C	Pin select for SDA signal
RXD.PTR	0x534	RXD Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in RXD buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last RXD transaction
TXD.PTR	0x544	TXD Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in TXD buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last TXD transaction
ADDRESS[0]	0x588	TWI slave address 0
ADDRESS[1]	0x58C	TWI slave address 1
CONFIG	0x594	Configuration register for the address match mechanism
ORC	0x5C0	Over-read character. Character sent out in case of an over-read of the transmit buffer.

34.9.1 SHORTS

Address offset: 0x200

Shortcut register

Bit r	numbe	er		33	1 30	29	2	8 2	7 2	6 2	5 2	24 2	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																						В	Α													
Res	et 0x0	0000000		0	0	0	C	0) (0 0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	V	alue	•						ı	Des	scri	iptio	on																				
Α	RW	WRITE_SUSPEND										9	Sho	orto	cut l	etv	we	en '	WR	ITE	eve	nt	and	SU	SPE	ND	tas	k								
												9	See	e E	VEN	TS_	W	RITI	ar	nd 7	'ASI	(S	SUS	PEI	٧D											
			Disabled	0								[Disa	abl	le sh	ort	cu	t																		
			Enabled	1									Ena	ble	e sh	orto	cut	:																		
В	RW	READ_SUSPEND										9	Sho	orto	cut l	oetv	we	en I	REA	D e	evei	nt a	nd :	sus	PEN	ND t	ask									
												9	See	<i>E</i> \	VEN	TS_	RE	AD	and	d TA	ASK.	s_s	USF	PEN	D											



Bit number		31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	L 0
Id			B A	
Reset 0x00000000		0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
Id RW Field	Value Id	Value	Description	
ld RW Field	Value Id Disabled	Value 0	Description Disable shortcut	

34.9.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit ı	numbe	r		33	1 30	29	28	27 2	6 2	5 2	4 23	22	21	20	19	18	17	16	15	14	13	12	11	l 10	9	8	7	6	5	4 3	3 2	2 1	. 0
Id								- 1	Н	ĵ				F	Ε										В							A	,
Res	et 0x0	0000000		0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0) (0
ld	RW	Field	Value Id	V	alue						De	scri	ptic	on																			
Α	RW	STOPPED									Ena	able	or	dis	sabl	e in	iter	rup	t fo	or S	TOF	PPE	Dε	ever	nt								
											See	e E\	'EN	TS_	_ST(OPF	PED																
			Disabled	0							Dis	sabl	е																				
			Enabled	1							Ena	able	9																				
В	RW	ERROR									Ena	able	or	dis	sabl	e in	iter	rup	t fo	r E	RRC	OR (eve	ent									
											See	e <i>E</i> \	'EN	TS_	_ERI	ROF	?																
			Disabled	0							Dis	sabl	е																				
			Enabled	1							Ena	able	2																				
Ε	RW	RXSTARTED									Ena	able	or	dis	sabl	e in	iter	rup	t fo	r R	XST	AR	TE	D ev	ent	t							
											See	e <i>E</i> \	'EN	TS_	_RX	STA	RTI	ED															
			Disabled	0							Dis	sabl	е																				
			Enabled	1							Ena	able	2																				
F	RW	TXSTARTED									Ena	able	or	dis	sabl	e in	iter	rup	t fc	or T	XST	AR	TEI	D ev	ent	t							
											See	e <i>E</i> \	'EN	TS_	_TXS	STA	RT	D															
			Disabled	0							Dis	sabl	е																				
			Enabled	1							Ena	able	•																				
G	RW	WRITE									Ena	able	or	dis	sabl	e in	iter	rup	t fo	r V	۷RI	TE e	eve	nt									
											See	e <i>E</i> \	EN'	TS_	_WF	RITE	Ē																
			Disabled	0							Dis	sabl	е																				
			Enabled	1							Ena	able	9																				
Н	RW	READ									Ena	able	or	dis	sabl	e in	iter	rup	t fc	r R	EA) e	ver	nt									
											See	e <i>E</i> \	'EN	TS_	_RE/	4 <i>D</i>																	
			Disabled	0							Dis	sabl	е																				
			Enabled	1							Ena	able	2																				

34.9.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31 3	0 29	9 2	8 2	7 2	6 25	5 24	4 23	3 22	2 21	20	19	18	17 1	.6 1	15 1	4 1	3 12	11	10	9	8	7	6 !	5 4	1 3	2	1	0
Id								ŀ	H G	j				F	Ε									В							Α	
Res	et 0x0	0000000		0 (0) (0 0) (0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 () (0 0	0	0	0
Id	RW	Field	Value Id	Valu	e						D	esc	ripti	on																		
Α	RW	STOPPED									W	/rite	e '1' '	to E	nab	le i	nter	rup	t fo	r ST	OPF	ED	eve	nt								
											Se	ee E	VEN	ITS_	STC	PP	ED															
			Set	1							Er	nab	le																			
			Disabled	0							Re	ead	: Dis	abl	ed																	
			Enabled	1							Re	ead	: Ena	able	ed																	
В	RW	ERROR									W	rite	e '1' 1	to E	nab	le i	nter	rup	t fo	r ER	ROF	R ev	ent									



Bit number	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	H G	F E B A
Reset 0x00000000	0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value	Description
		See EVENTS_ERROR
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
E RW RXSTARTED		Write '1' to Enable interrupt for RXSTARTED event
		See EVENTS_RXSTARTED
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
F RW TXSTARTED		Write '1' to Enable interrupt for TXSTARTED event
		See EVENTS_TXSTARTED
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
G RW WRITE		Write '1' to Enable interrupt for WRITE event
		See EVENTS_WRITE
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
H RW READ		Write '1' to Enable interrupt for READ event
Cot	1	See EVENTS_READ Enable
Set	1	
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled

34.9.4 INTENCLR

Address offset: 0x308

Disable interrupt

B11 1		24 20 20 20 27 26 25 2	
Bit number			4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		H G	F E B A
Reset 0x00000000		0 0 0 0 0 0 0 0	
Id RW Field	Value Id	Value	Description
A RW STOPPED			Write '1' to Disable interrupt for STOPPED event
			See EVENTS_STOPPED
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW ERROR			Write '1' to Disable interrupt for ERROR event
			See EVENTS_ERROR
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW RXSTARTED			Write '1' to Disable interrupt for RXSTARTED event
			See EVENTS_RXSTARTED
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
F RW TXSTARTED			Write '1' to Disable interrupt for TXSTARTED event
			See EVENTS_TXSTARTED
	Clear	1	Disable



Bit number	31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		H G F E B A
Reset 0x00000000	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value I	d Value	Description
Disable	d 0	Read: Disabled
Enable	i 1	Read: Enabled
G RW WRITE		Write '1' to Disable interrupt for WRITE event
		See EVENTS_WRITE
Clear	1	Disable
Disable	d 0	Read: Disabled
Enable	i 1	Read: Enabled
H RW READ		Write '1' to Disable interrupt for READ event
		See EVENTS_READ
Clear	1	Disable
Disable	d 0	Read: Disabled
Enable	1	Read: Enabled

34.9.5 ERRORSRC

Address offset: 0x4D0

Error source

Bit r	numbe	er		31	30	29 :	28 2	7 2	26 2	5 2	24 2	3 22	21	20	19	18	17	16	15	14 1	.3 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																														СВ		Α
Res	et 0x0	0000000		0	0	0	0 (כ	0 () (0 (0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	iptic	on																		
Α	RW	OVERFLOW									R	X bu	ffer	ove	erflo	w	dete	ecte	ed,	and	pre	ven	ted									
			NotDetected	0							Ε	rror	did ı	not	occ	ur																
			Detected	1							Ε	rror	occı	ırre	d																	
В	RW	DNACK									N	IACK	sen	t af	ter	rec	eivi	ng a	a da	ita k	yte											
			NotReceived	0							Ε	rror	did ı	not	occ	ur																
			Received	1							Ε	rror	occı	ırre	d																	
С	RW	OVERREAD									T	X bu	ffer	ove	er-re	ead	det	ect	ed,	and	l pre	eve	ntec	ł								
			NotDetected	0							Е	rror	did ı	not	occ	ur																
			Detected	1							Ε	rror	occı	ırre	d																	

34.9.6 MATCH

Address offset: 0x4D4

Status register indicating which address had a match

Bitı	numbe	er		31	30	29 2	28 2	7 26	5 25	24	23	22	21 :	20 1	L9 1	.8 1	7 16	5 15	14	13	12 :	1 1	0 9	8	7	6	5	4	3	2 1	L 0
Id																															Α
Res	et OxC	0000000		0	0	0	0 (0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0
ld	RW	Field	Value Id	Va	lue						De	scri	ptio	n																	
Α	R	MATCH		[0.	.1]						Wł	nich	of t	he a	add	ress	es i	n {A	DDI	RESS	s} m	atch	ed t	he	inco	mir	ng				
											ad	dres	S																		

34.9.7 ENABLE

Address offset: 0x500

Enable TWIS

Bit	number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A
Res	et 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW ENABLE			Enable or disable TWIS
		Disabled	0	Disable TWIS



Reset 0x000000000	
Reset 0x000000000 0 0 0 0 0 0 0 0 0 0 0 0 0	
ld	0 0 0 0 0 0 0 0 0
	A A A A
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0

34.9.8 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

Bit r	numbe	er		31 30 29 28 27 26	25 2	4 23	22	21	20	19	18 1	7 16	15	14	L3 12	11	10 9	8 6	7	6	5	4 3	3 2	1	0
Id				В																		A A	A A	Α	Α
Res	et OxF	FFFFFF		1 1 1 1 1 1	1 1	1 1	1	1	1	1	1 1	l 1	1	1	1 1	1	1 :	l 1	1	1	1	1 :	l 1	1	1
Id	RW	Field	Value Id	Value		De	scri	ptic	on																
Α	RW	PIN		[031]		Pir	n nu	mb	er																
В	RW	CONNECT				Co	nne	ctio	n																
			Disconnected	1		Dis	scon	nec	ct																
			Connected	0		Co	nne	ct																	

34.9.9 PSEL.SDA

Address offset: 0x50C Pin select for SDA signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

34.9.10 RXD.PTR

Address offset: 0x534 RXD Data pointer

Bit	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	0	9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ.	Α	Α	Α	Α	Α	Α	Α.	Δ,	A	Δ
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 Value Description										0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0)			
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																															
Α	RW	PTR		RXD Data pointer																											Ξ.				

34.9.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in RXD buffer

Bit r	umber			31	30	29	28	27 2	26 2	25 2	24 :	23 2	22 2	21 2	20 1	9 1	8 1	7 1	5 15	14	13	12	11	10	9	8	7	6 !	5 4	1 3	2	1	0
Id																										,	Д	A A	Δ Α	A A	Α	Α	Α
Res	et 0x000	00000													0	0 (0 (0	0	0	0	0	0	0	0	0 (0	0 (0 (0 0	0	0	0
Id	RW F	ield	Value Id												n																		
Α	RW N	/AXCNT											kim	um	nur	nbe	r of	by	es i	n R	XD I	buff	er										

34.9.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last RXD transaction



Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0						
Id					A A A A A A A						
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0						
ld RW Field	Value Id	Value	Description								
A R AMOUNT		Number of bytes transferred in the last RXD transaction									

34.9.13 TXD.PTR

Address offset: 0x544
TXD Data pointer

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۱ ۸	А А
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 (
Id	RW	Field	Value Id	Va	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																													
Α	RW	PTR		TXD Data pointer																														

34.9.14 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in TXD buffer

Bit number	31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
A RW MAXCNT		Maximum number of bytes in TXD buffer

34.9.15 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last TXD transaction

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1)
Id																												Α	Α	Α	Α	A	Δ	A	١
Res	et 0x0	0000000		0 0 0 Value Id Value										0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 0 ue ld Value E											on																				ı
Α	R	AMOUNT											mbe	er c	of b	yte	s tr	ans	feri	red	in t	he	last	TX	D tr	ans	sact	ion							7

34.9.16 ADDRESS[0]

Address offset: 0x588 TWI slave address 0

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW ADDRESS			TWI slave address

34.9.17 ADDRESS[1]

Address offset: 0x58C TWI slave address 1

Bit	number			31	30 29	28 2	27 26	6 25	24	23 2	22 2	1 20	19	18	17 :	16 1	.5 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2 1	1 0
Id																									Α	Α	Α	Α	A A	A A
Res	et 0x000	00000		0	0	0 0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 0	0 0	
Id	RW Fi	ield	Value Id	Val	ue					Des	crip	tion																		

RW ADDRESS TWI slave address



34.9.18 CONFIG

Address offset: 0x594

Configuration register for the address match mechanism

Bit r	numbe	er		31	30	29	28	27 :	26 2	25 2	24 2	23 2	2 2	1 20	19	9 18	3 1	7 16	5 15	5 14	13	12	11	10	9	8	7	6 !	5 4	4 3	2	1 0	
Id																																ВА	ı
Res	et OxO	0000001		0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0 1	ı
Id	RW	Field	Value Id	Va	lue						0	Desc	rip	tion																			
Α	RW	ADDRESS0		0										or di	sak	ole a	add	res	s m	atcl	ning	on	ADI	DRE	SS[0]							
			Disabled	0										d																			
			Enabled	0 1										l																			
В	RW	ADDRESS1		1										or di	sak	ole a	add	res	s m	atcl	ning	on	ADI	DRE	SS[1]							
			Disabled	0										d																			
			Enabled	1									oled	I																			

34.9.19 ORC

Address offset: 0x5C0

Over-read character. Character sent out in case of an over-read of the transmit buffer.

Bit	numbe	er		31 3	30 29	9 28	27 2	6 2	5 24	23	22	21 2	20 19	9 18	3 17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																								Α	Α	Α	Α	А А	Α	Α
Res	et 0x0	0000000		0	0 0	0	0 0) (0 0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Valu	ıe					De	scrip	otio	n																	
Α	RW	ORC								Ov	er-re	ead	char	act	er. (Char	act	er s	ent	out	in ca	ise (of a	n o	ver-	read	d			
										οf	the	tran	smit	hir	ffer															

34.10 Electrical specification

34.10.1 TWIS slave interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f_{TWIS}	Bit rates for TWIS ³¹	100		400	kbps
I _{TWIS,100kbps}	Run current for TWIS (Average current to receive and transfer a		45		μΑ
	byte to RAM), 100 kbps				
I _{TWIS,400kbps}	Run current for TWIS (Average current to receive and transfer a		45		μΑ
	byte to RAM), 400 kbps				
I _{TWIS,IDLE}	Idle current for TWIS		1		μΑ
t _{TWIS,START,LP}	Time from PREPARERX/PREPARETX task to ready to receive/		t _{TWIS,START}	τ,	μs
	transmit, Low power mode		+		
			t _{START_HFI}	V	
t _{TWIS,START,CL}	Time from PREPARERX/PREPARETX task to ready to receive/		1.5		μs
	transmit, Constant latency mode				

34.10.2 TWIS slave timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIS,SCL,400kbps}	SCL clock frequency, 400 kbps			400	kHz
t _{TWIS,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t _{TWIS,HD_DAT}	Data hold time after negative edge on SCL – all modes	500			ns
t _{TWIS,HD_STA,100kbps}	TWI slave hold time from for START condition (SDA low to SCL	5200			ns
	low), 100 kbps				
t _{TWIS,HD_STA,400kbps}	TWI slave hold time from for START condition (SDA low to SCL	1300			ns
	low), 400 kbps				

Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Symbol	Description	Min.	Тур.	Max.	Units
t _{TWIS,SU_STO,100kbps}	TWI slave setup time from SCL high to STOP condition, 100 kbps	5200			ns
t _{TWIS,SU_STO,400kbps}	TWI slave setup time from SCL high to STOP condition, 400 kbps	1300			ns
t _{TWIS,BUF,100kbps}	TWI slave bus free time between STOP and START conditions,		4700		ns
	100 kbps				
t _{TWIS,BUF,400kbps}	TWI slave bus free time between STOP and START conditions,		1300		ns
	400 khns				

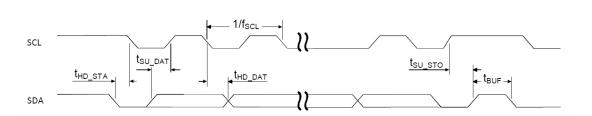


Figure 92: TWIS timing diagram, 1 byte transaction



35 UARTE — Universal asynchronous receiver/ transmitter with EasyDMA

The Universal asynchronous receiver/transmitter with EasyDMA (UARTE) offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware at a rate up to 1 Mbps, and EasyDMA data transfer from/to RAM.

Listed here are the main features for UARTE:

- Full-duplex operation
- · Automatic hardware flow control
- Parity checking and generation for the 9th data bit
- EasyDMA
- Up to 1 Mbps baudrate
- · Return to IDLE between transactions supported (when using HW flow control)
- One stop bit
- Least significant bit (LSB) first

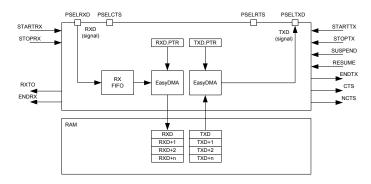


Figure 93: UARTE configuration

The GPIOs used for each UART interface can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

35.1 Shared resources

The UARTE shares registers and other resources with other peripherals that have the same ID as the UARTE.

Therefore, you must disable all peripherals that have the same ID as the UARTE before the UARTE can be configured and used. Disabling a peripheral that has the same ID as the UARTE will not reset any of the registers that are shared with the UARTE. It is therefore important to configure all relevant UARTE registers explicitly to ensure that it operates correctly.

See the Instantiation table in *Instantiation* on page 24 for details on peripherals and their IDs.

35.2 EasyDMA

The UARTE implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.



The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The ENDRX/ENDTX event indicates that EasyDMA has finished accessing respectively the RX/TX buffer in RAM.

35.3 Transmission

The first step of a DMA transmission is storing bytes in the transmit buffer and configuring EasyDMA. This is achieved by writing the initial address pointer to TXD.PTR, and the number of bytes in the RAM buffer to TXD.MAXCNT. The UARTE transmission is started by triggering the STARTTX task.

After each byte has been sent over the TXD line, a TXDRDY event will be generated.

When all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have been transmitted, the UARTE transmission will end automatically and an ENDTX event will be generated.

A UARTE transmission sequence is stopped by triggering the STOPTX task, a TXSTOPPED event will be generated when the UARTE transmitter has stopped.

If the ENDTX event has not already been generated when the UARTE transmitter has come to a stop, the UARTE will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

If flow control is enabled, a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in *Figure 94: UARTE transmission* on page 334. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended.

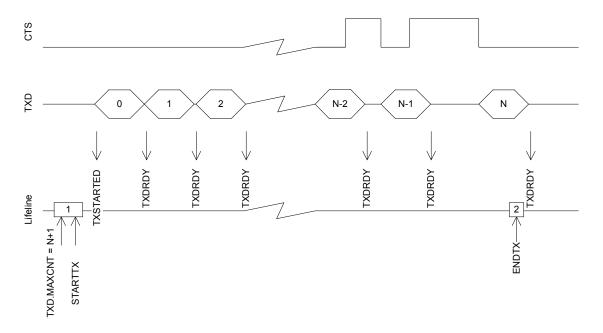


Figure 94: UARTE transmission

The UARTE transmitter will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTTX or after it has been stopped via STOPTX and the TXSTOPPED event has been generated. See *POWER* — *Power supply* on page 78 for more information about power modes.

35.4 Reception

The UARTE receiver is started by triggering the STARTRX task. The UARTE receiver is using EasyDMA to store incoming data in an RX buffer in RAM.



The RX buffer is located at the address specified in the RXD.PTR register. The RXD.PTR register is double-buffered and it can be updated and prepared for the next STARTRX task immediately after the RXSTARTED event is generated. The size of the RX buffer is specified in the RXD.MAXCNT register and the UARTE will generate an ENDRX event when it has filled up the RX buffer, see *Figure 95: UARTE reception* on page 335.

For each byte received over the RXD line, an RXDRDY event will be generated. This event is likely to occur before the corresponding data has been transferred to Data RAM.

The RXD.AMOUNT register can be queried following an ENDRX event to see how many new bytes have been transferred to the RX buffer in RAM since the previous ENDRX event.

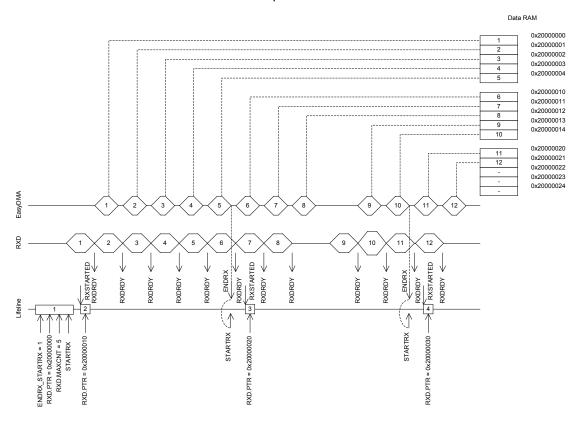


Figure 95: UARTE reception

The UARTE receiver is stopped by triggering the STOPRX task. An RXTO event is generated when the UARTE has stopped. The UARTE will make sure that an impending ENDRX event will be generated before the RXTO event is generated. This means that the UARTE will guarantee that no ENDRX event will be generated after RXTO, unless the UARTE is restarted or a FLUSHRX command is issued after the RXTO event is generated.

Important: If the ENDRX event has not already been generated when the UARTE receiver has come to a stop, which implies that all pending content in the RX FIFO has been moved to the RX buffer, the UARTE will generate the ENDRX event explicitly even though the RX buffer is not full. In this scenario the ENDRX event will be generated before the RXTO event is generated.

To be able to know how many bytes have actually been received into the RX buffer, the CPU can read the RXD.AMOUNT register following the ENDRX event or the RXTO event.

The UARTE is able to receive up to four bytes after the STOPRX task has been triggered as long as these are sent in succession immediately after the RTS signal is deactivated. This is possible because after the RTS is deactivated the UARTE is able to receive bytes for an extended period equal to the time it takes to send 4 bytes on the configured baud rate.

After the RXTO event is generated the internal RX FIFO may still contain data, and to move this data to RAM the FLUSHRX task must be triggered. To make sure that this data does not overwrite data in the RX buffer, the RX buffer should be emptied or the RXD.PTR should be updated before the FLUSHRX task is triggered.



To make sure that all data in the RX FIFO is moved to the RX buffer, the RXD.MAXCNT register must be set to RXD.MAXCNT > 4, see *Figure 96: UARTE reception with forced stop via STOPRX* on page 336. The UARTE will generate the ENDRX event after completing the FLUSHRX task even if the RX FIFO was empty or if the RX buffer does not get filled up. To be able to know how many bytes have actually been received into the RX buffer in this case, the CPU can read the RXD.AMOUNT register following the ENDRX event.

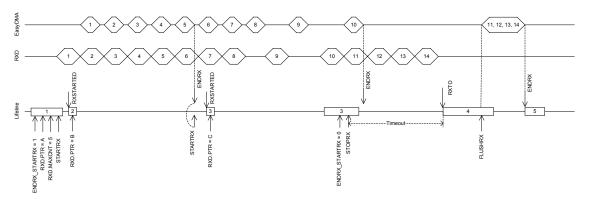


Figure 96: UARTE reception with forced stop via STOPRX

If HW flow control is enabled the RTS signal will be deactivated when the receiver is stopped via the STOPRX task or when the UARTE is only able to receive four more bytes in its internal RX FIFO.

With flow control disabled, the UARTE will function in the same way as when the flow control is enabled except that the RTS line will not be used. This means that no signal will be generated when the UARTE has reached the point where it is only able to receive four more bytes in its internal RX FIFO. Data received when the internal RX FIFO is filled up, will be lost.

The UARTE receiver will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTRX or after it has been stopped via STOPRX and the RXTO event has been generated. See *POWER* — *Power supply* on page 78 for more information about power modes.

35.5 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.

An ERROR event will not stop reception. If the error was a parity error, the received byte will still be transferred into Data RAM, and so will following incoming bytes. If there was a framing error (wrong stop bit), that specific byte will NOT be stored into Data RAM, but following incoming bytes will.

35.6 Using the UARTE without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

35.7 Parity configuration

When parity is enabled, the parity will be generated automatically from the even parity of TXD and RXD for transmission and reception respectively.

35.8 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.



The STOPTX and STOPRX tasks may not be always needed (the peripheral might already be stopped), but if STOPTX and/or STOPRX is sent, software shall wait until the TXSTOPPED and/or RXTO event is received in response, before disabling the peripheral through the ENABLE register.

35.9 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UARTE are mapped to physical pins according to the configuration specified in the PSEL.RXD, PSEL.RTS, and PSEL.TXD registers respectively.

The PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers and their configurations are only used as long as the UARTE is enabled, and retained only for the duration the device is in ON mode. PSEL.RXD, PSEL.RTS and PSEL.TXD must only be configured when the UARTE is disabled.

To secure correct signal levels on the pins by the UARTE when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Table 80: GPIO configuration before enabling peripheral* on page 337.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 80: GPIO configuration before enabling peripheral

UARTE signal	UARTE pin	Direction	Output value
RXD	As specified in PSEL.RXD	Input	Not applicable
CTS	As specified in PSEL.CTS	Input	Not applicable
RTS	As specified in PSEL.RTS	Output	1
TXD	As specified in PSEL.TXD	Output	1

35.10 Registers

Table 81: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40002000	UARTE	UARTE0	Universal Asynchronous Receiver/	
			Transmitter with EasyDMA	

Table 82: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS_STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_FLUSHRX	0x02C	Flush RX FIFO into RX buffer
EVENTS_CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_RXDRDY	0x108	Data received in RXD (but potentially not yet transferred to Data RAM)
EVENTS_ENDRX	0x110	Receive buffer is filled up
EVENTS_TXDRDY	0x11C	Data sent from TXD
EVENTS_ENDTX	0x120	Last TX byte transmitted
EVENTS_ERROR	0x124	Error detected
EVENTS_RXTO	0x144	Receiver timeout
EVENTS_RXSTARTED	0x14C	UART receiver has started
EVENTS_TXSTARTED	0x150	UART transmitter has started
EVENTS_TXSTOPPED	0x158	Transmitter stopped
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
INTENCLR	0x308	Disable interrupt



Register	Offset	Description
ERRORSRC	0x480	Error source
ENABLE	0x500	Enable UART
PSEL.RTS	0x508	Pin select for RTS signal
PSEL.TXD	0x50C	Pin select for TXD signal
PSEL.CTS	0x510	Pin select for CTS signal
PSEL.RXD	0x514	Pin select for RXD signal
BAUDRATE	0x524	Baud rate. Accuracy depends on the HFCLK source selected.
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
CONFIG	0x56C	Configuration of parity and hardware flow control

35.10.1 SHORTS

Address offset: 0x200

Bit	numbe	er		31	L 30	29	28	27	26	25	24	23 :	22 :	21 2	0 1	.9 1	8 1	7 1	5 1!	5 1	4 13	3 12	2 11	. 10	9	8	7	6	5 4	1 3	2	1	0
Id																												D	С				
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 () (0 () (0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Va	alue	!						Des	crip	otior	1																		
С	RW	ENDRX_STARTRX										Sho	rtcı	ut be	etw	eer	EN	IDR:	X e	ven	t an	d S	TAF	(TR	(tas	sk							
												See	EV	ENT.	S_ <i>E</i>	ND	RX a	and	TA.	SKS	_ST	AR	ΓRX										
			Disabled	0								Disa	able	sho	rtc	ut																	
			Enabled	1								Ena	ble	sho	rtcı	ut																	
D	RW	ENDRX_STOPRX										Sho	rtcı	ut be	etw	eer	EN	IDR:	X e	ven	t an	d S	TOF	PRX	task	(
												See	EV	ENT.	S_ <i>E</i>	ND	RX a	and	TA.	SKS	_ST	OPI	RX										
			Disabled	0								Disa	able	sho	rtc	ut																	
			Enabled	1								Ena	ble	sho	rtcı	ut																	

35.10.2 INTEN

Address offset: 0x300

Enable or disable interrupt

			•		
Bit r	numbe	er		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					L J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value	Description
Α	RW	CTS			Enable or disable interrupt for CTS event
					See EVENTS_CTS
			Disabled	0	Disable
			Enabled	1	Enable
В	RW	NCTS			Enable or disable interrupt for NCTS event
					See EVENTS_NCTS
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	RXDRDY			Enable or disable interrupt for RXDRDY event
					See EVENTS_RXDRDY
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	ENDRX			Enable or disable interrupt for ENDRX event
					See EVENTS_ENDRX



Bit	number		31 30 2	9 28	27 2	26 2	5 24	23 22 2	21 2	20 1	9 18	3 17	16	15	14 1	13 1	2 11	10	9	8	7	6 !	5 4	4 3	2	1	0
Id								L		JI		Н							G	F	Ε		-)	С	В	Α
Res	et 0x00000000		0 0 0	0 0	0	0 (0	0 0	0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0 (0 (0 0	0	0	0
Id	RW Field	Value Id	Value					Descrip	tio	n																	
		Disabled	0					Disable	:																		
		Enabled	1					Enable																			
E	RW TXDRDY							Enable	or	disal	ole i	ntei	rup	t fo	r TX	DRE	Y ev	/ent									
								See <i>EV</i>	EN7	S_T	XDR	DY															
		Disabled	0					Disable	!																		
		Enabled	1					Enable																			
F	RW ENDTX							Enable	or (disal	ole i	ntei	rrup	ot fo	r EN	DTX	eve	ent									
								See <i>EV</i>	EN7	'S E	NDI	X															
		Disabled	0					Disable																			
		Enabled	1					Enable																			
G	RW ERROR							Enable	or	disal	ole i	ntei	rup	t fo	r ER	ROF	eve	ent									
								See <i>EV</i>	ENIT	с г	DDC	1D															
		Disabled	0					Disable		3_E	KKC	rK															
		Enabled	1					Enable																			
Н	RW RXTO	Enabled	•					Enable	or	disal	ole i	ntei	rur	ot fo	r RX	TO (ever	nt									
		Disabled	0					See EV		5_ <i>K</i> .	XIC	,															
		Enabled	0 1					Enable	!																		
	RW RXSTART		1					Enable	or	dical	ale i	ntei	rur	nt fo	r RY	ςτα	RTF	D ev	ont								
•	1000171111													,,,,,		5171			ciic								
			_					See EV		S_R.	XST.	ART	ED														
		Disabled	0					Disable	!																		
J	RW TXSTART	Enabled	1					Enable		dical	ا مام	nto		.+ f.	- TV	CT A	DTE	.	on+								
J	KW IXSIAKI							Enable	01 (uisai	oie i	ntei	rup	טנ זכ	LIX	SIA	KIEI	J ev	ent								
								See EV	EN7	S_T	XST.	4RT	ED														
		Disabled	0					Disable	!																		
		Enabled	1					Enable																			
L	RW TXSTOPF	ED						Enable	or	disal	ole i	ntei	rup	ot fo	r TX	STO	PPE	D ev	ent								
								See <i>EV</i>	EN7	S_T	XST	OPP	ED														
		Disabled	0					Disable	!																		

35.10.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	numbe	er		31	30 2	9 28	3 27	26 2	5 2	24 23	22	21 2	0 1	.9 18	8 17	7 16	15	14	13 1	2 11	. 10	9	8	7	6 5	4	3	2	1 0
Id											L		ı	l	Н	ł						G	F	Ε		D		С	ВА
Res	et 0x0	0000000		0	0 0	0	0	0 (0	0 0	0	0 () (0 0	0	0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0 0
Id	RW	Field	Value Id	Val	ue					De	scri	ptior	1																
Α	RW	CTS								W	rite '	'1' to	En	able	e int	terr	upt	for (CTS (even	t								
										Se	e <i>EV</i>	ENT.	s_ <i>c</i>	TS															
			Set	1						En	able	:																	
			Disabled	0						Re	ad:	Disab	oled	b															
			Enabled	1						Re	ad:	Enab	led	I															
В	RW	NCTS								W	rite '	'1' to	En	able	e int	terr	upt	for I	NCTS	eve	nt								
										Se	e <i>EV</i>	ENT:	S_	ICTS	5														
			Set	1						En	able	:																	
			Disabled	0						Re	ad:	Disab	oled	b															
			Enabled	1						Re	ad:	Enab	led																
С	RW	RXDRDY								W	rite '	'1' to	En	able	e int	terr	upt	for I	RXDI	RDY	ever	nt							



Bit r	numbe	er		31 30	29	28 27	7 26 :	25 24	23 22 21 2	0 19 18	8 17 :	16 15	14 13	3 12 1	11 10	9	8	7 6	5 5	4	3 2	1	0
Id -										JI	Н						F			D		В	
		0000000	Value Id		0	0 0	0	0 0	0 0 0 (0	0 0	0 0	0	0 0	0	0 () (0	0	0 0	0	0
ld	KW	Field	Value Id	Value					Description See EVENT		אחצ												
			Set	1					Enable	3_NXDI	101												
			Disabled	0					Read: Disal	bled													
			Enabled	1					Read: Enab														
D	RW	ENDRX							Write '1' to	Enable	e inte	rrupt f	or EN	DRX	even	t							
									See <i>EVENT</i>	S_ENDF	RX												
			Set	1					Enable														
			Disabled	0					Read: Disal	bled													
			Enabled	1					Read: Enab	oled													
Е	RW	TXDRDY							Write '1' to	Enable	inte	rrupt f	or TX	DRDY	evei eve	nt							
									See EVENT	S_TXDR	RDY												
			Set	1					Enable														
			Disabled	0					Read: Disal	bled													
			Enabled	1					Read: Enab														
F	RW	ENDTX							Write '1' to	Enable	inte	rrupt f	or EN	DTX	event								
									See EVENT	S_END1	ΓX												
			Set	1					Enable														
			Disabled	0					Read: Disal														
G	R\M	ERROR	Enabled	1					Read: Enab Write '1' to		into	rrunt f	or FR	ROR (ovent								
J	11.00	Linon										Tupti	OI LIV	NON .	cvciii								
			Cot	1					See EVENT	S_ERRC)K												
			Set Disabled	1					Enable Read: Disal	blad													
			Enabled	1					Read: Enab														
Н	RW	RXTO							Write '1' to		e inte	rrupt f	or RX	TO ev	/ent								
									See EVENT	S RXTC)												
			Set	1					Enable	5_11)(10													
			Disabled	0					Read: Disal	bled													
			Enabled	1					Read: Enab	oled													
I	RW	RXSTARTED							Write '1' to	Enable	inte	rrupt f	or RX	STAR	TED (even	t						
									See EVENT	S_RXST	ARTE	D											
			Set	1					Enable														
			Disabled	0					Read: Disal	bled													
			Enabled	1					Read: Enab														
J	RW	TXSTARTED							Write '1' to	Enable	inte	rrupt f	or TX	STAR	TED 6	even	t						
									See EVENT	S_TXST.	ARTE	D											
			Set	1					Enable														
			Disabled	0					Read: Disal														
L	R\M	TXSTOPPED	Enabled	1					Read: Enab Write '1' to		inte	rrunt f	or TY	STOP	PED 4	aver	t						
-	11.00	17.51011 ED											J1 1A	J10P		- v C I							
			Cot	1					See EVENT	5_ <i>1X5T</i>	OPPE	υ											
			Set Disabled	1					Enable Read: Disal	hlad													
			Enabled	1					Read: Enab														
			LIMBICU	-					ncuu. Liidk	,,cu													

35.10.4 INTENCLR

Address offset: 0x308

Disable interrupt



Bitı	number	-		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					L JIH GFE D CBA
Res	et 0x00	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	CTS			Write '1' to Disable interrupt for CTS event
					See EVENTS_CTS
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	NCTS			Write '1' to Disable interrupt for NCTS event
					See EVENTS_NCTS
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	RXDRDY			Write '1' to Disable interrupt for RXDRDY event
					See EVENTS_RXDRDY
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	ENDRX			Write '1' to Disable interrupt for ENDRX event
					See EVENTS_ENDRX
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Ε	RW	TXDRDY			Write '1' to Disable interrupt for TXDRDY event
					See EVENTS_TXDRDY
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	ENDTX			Write '1' to Disable interrupt for ENDTX event
					See EVENTS_ENDTX
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	ERROR			Write '1' to Disable interrupt for ERROR event
					See EVENTS_ERROR
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	RXTO			Write '1' to Disable interrupt for RXTO event
					See EVENTS_RXTO
			Clear	1	Disable
			Disabled	0	Read: Disabled
	D)A/	DVCTADTED	Enabled	1	Read: Enabled
ı	KVV	RXSTARTED			Write '1' to Disable interrupt for RXSTARTED event
					See EVENTS_RXSTARTED
			Clear	1	Disable
			Disabled	0	Read: Disabled
1	D/V	TYCTADTED	Enabled	1	Read: Enabled Write '1' to Disable interrupt for TYSTARTED event
J	KW	TXSTARTED			Write '1' to Disable interrupt for TXSTARTED event
					See EVENTS_TXSTARTED
			Clear	1	Disable
			Disabled	0	Read: Disabled
	DV#1	TYCTODDED	Enabled	1	Read: Enabled Write 11 to Disable interrupt for TYSTOPPED event
L	KVV	TXSTOPPED			Write '1' to Disable interrupt for TXSTOPPED event



Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L JIH GFE D CBA
Reset 0x00000000		0 0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
			See EVENTS_TXSTOPPED
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

35.10.5 ERRORSRC

Address offset: 0x480

Error source

								_																			_				_		
	numb	er		31	. 30	29	28 2	2/ 2	26 2	25 .	24 2	23	22 2	21 2	0 1	9 1	8 1	/ 1	b 1	5 1	41	3 1.	2 1:	1 10	1 9	8	7	6	5		3 2	2]	. 0
Id																															D (3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0) () () () () () (0	0	0	0	0	0	0	0	0	0 () (0
Id	RW	Field	Value Id	Va	alue						0	Des	scrip	tio	n																		
Α	RW	OVERRUN									C	Οve	errui	n er	ror																		
											A	A st	tart	bit i	is re	cei	ved	l wh	ile	the	pr	evio	us	data	sti	II lie	s in	RXI	D.				
											(Pre	evio	us c	lata	is I	ost	.)															
			NotPresent	0							F	Rea	ad: e	rro	r no	t pı	ese	ent															
			Present	1							F	Rea	ad: e	rro	r pre	ese	nt																
В	RW	PARITY									P	Par	ity e	rro	r																		
											_	۵ دا	hara	rte	r wi	th k	her	nai	itv	ic r	ore	ive	۱ if	н\Λ	/ na	ritv	che	ck i	c				
													abled				Juu	pu	···y	.5.			۰, ۰۰		ρu		Ciic	CIC I	,				
			NotPresent	0									ad: e		r no	t pr	ese	ent															
			Present	1									ad: e			•																	
С	RW	FRAMING											min		•			ed															
																												۲.					
													alid											iai c	ıata	inp	ut a	irre	r aı				
				_									s in a						oee	en re	ece	ived	١.										
			NotPresent	0									ad: e			•		ent															
_		225.11	Present	1									ad: e		•		nt																
D	RW	BREAK									E	3re	ak c	onc	litio	n																	
											Т	Γhe	e ser	ial d	data	inp	out	is '()' fo	or lo	ong	er tl	han	the	len	gth	of a	a da	ta				
											f	rar	me.	(Th	e da	ta f	rar	ne l	eng	gth	is 1	0 bi	ts v	vith	out	par	ity k	oit, a	and	l			
											1	11	bits	wit	h pa	rity	/ bi	t.).															
			NotPresent	0							F	Rea	ad: e	rro	r no	t pı	ese	ent															
			Present	1							F	Rea	ad: e	rro	r pre	ese	nt																

35.10.6 ENABLE

Address offset: 0x500

Enable UART

Bit	numbe	er		31	1 30	29	28	3 27	7 26	6 2	5 2	4 2	3 2	2 2	1 2	0 1	9 :	18	17	16	15	14	13	12	2 1:	1 10	9	8	7	6	5	4	3	2	1 0
Id																																	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0) (0 () () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue	•						D	eso	rip	tio	n																			
Α	RW	ENABLE										Ε	nak	ole (or c	disa	ble	U,	AR	ГΕ															
			Disabled	0								D	Disa	ble	UA	RT	Ε																		
			Enabled	8								Е	nak	ole	JAI	RTE																			

35.10.7 PSEL.RTS

Address offset: 0x508

Pin select for RTS signal



Bit	numbe	er		31	30 2	29 2	28 2	7 2	6 25	5 24	1 23	3 22	21	20	19	18 1	7 1	6 15	14	13	12 1	.1 10	9	8	7	6	5	4	3 2	1	0
Id				В																								Α.	А А	Α	Α
Re	et 0xF	FFFFFF		1	1	1	1 1	1 :	1 1	. 1	1	1	1	1	1	1	1 1	. 1	1	1	1	1 1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	lue						De	escri	iptic	on																	
Α	RW	PIN		[0.	.31]						Piı	n nu	ımb	er																	
В	RW	CONNECT									Co	onne	ectic	n																	
			Disconnected	1							Di	scor	nne	ct																	
			Connected	0							Co	onne	ect																		

35.10.8 PSEL.TXD

Address offset: 0x50C Pin select for TXD signal

Bit	numbe	er		31 30	29	28	3 27	26	25	24	23 2	22 2	1 20	0 19	18	17 1	.6 15	5 14	13 1	2 1:	l 10	9	8	7	6	5	4	3 2	1	0
Id				В																							Α	А А	Α	Α
Res	et 0xF	FFFFFF		1 1	1	1	1	1	1	1	1	1 1	1 1	. 1	1	1	1 1	1	1 :	l 1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Value							Des	crip	tion	1																
Α	RW	PIN		[031]						Pin	num	ber	-																
В	RW	CONNECT									Con	nec	tion																	
			Disconnected	1							Disc	conn	ect																	
			Connected	0							Con	nec	t																	

35.10.9 PSEL.CTS

Address offset: 0x510

Pin select for CTS signal

Bit	numbe	er		31 30 29 28 27 26 25 2	$24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0$
Id				В	A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

35.10.10 PSEL.RXD

Address offset: 0x514

Pin select for RXD signal

Bit	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

35.10.11 BAUDRATE

Address offset: 0x524

Baud rate. Accuracy depends on the HFCLK source selected.



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x04000000		0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW BAUDRATE		Baud rate
	Baud1200	0x0004F000 1200 baud (actual rate: 1205)
	Baud2400	0x0009D000 2400 baud (actual rate: 2396)
	Baud4800	0x0013B000 4800 baud (actual rate: 4808)
	Baud9600	0x00275000 9600 baud (actual rate: 9598)
	Baud14400	0x003AF000 14400 baud (actual rate: 14401)
	Baud19200	0x004EA000 19200 baud (actual rate: 19208)
	Baud28800	0x0075C000 28800 baud (actual rate: 28777)
	Baud38400	0x009D0000 38400 baud (actual rate: 38369)
	Baud57600	0x00EB0000 57600 baud (actual rate: 57554)
	Baud76800	0x013A9000 76800 baud (actual rate: 76923)
	Baud115200	0x01D60000 115200 baud (actual rate: 115108)
	Baud230400	0x03B00000 230400 baud (actual rate: 231884)
	Baud250000	0x04000000 250000 baud
	Baud460800	0x07400000 460800 baud (actual rate: 457143)
	Baud921600	0x0F000000 921600 baud (actual rate: 941176)
	Baud1M	0x10000000 1Mega baud

35.10.12 RXD.PTR

Address offset: 0x534

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW PTR		Data pointer

35.10.13 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit	numbe	er		31 3	30 29	28	27	26 2	25 2	24 2	3 22	2 21	20	19	18	17 1	16	15 1	.4 1	3 12	2 11	. 10	9	8	7	6	5	4	3 2	2 1	0
Id																									Α	Α	Α	Α	A A	A A	. А
Res	et 0x0	0000000		0	0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Valu	ıe					D	esci	ripti	on																		
Α	RW	MAXCNT								Ν	1axii	mur	ท ทเ	ımb	er c	of b	yte:	s in	rece	eive	buf	fer									

35.10.14 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1
Id					A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description		
A R AMOUNT			Number of bytes trans	sferred in the last transactio	n

35.10.15 TXD.PTR

Address offset: 0x544

Data pointer



Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 1	16	15 1	14 1	13 :	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A i	4
Rese	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α	RW	PTR										Da	ta n	oin	ter																				7

35.10.16 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit	numb	er		31	30 2	9 2	8 27	26	25	24	23	22 :	21 2	20 :	19 1	8 1	17 1	16 1	.5 1	4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																										Α	Α	Α	Α	Α	Α.	А А
Re	set 0x	00000000		0	0 0) (0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0 0) (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Val	ue						Des	crip	otio	n																		
Α	RW	MAXCNT									Ma	xim	um	nu	mbe	er o	f by	/tes	in	trai	ารm	it b	uffe	r								

35.10.17 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit number		31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A R AMOUNT			Number of bytes transferred in the last transaction

35.10.18 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

Di+	numbe	or.		21	30 2	0.2	00 2-	7 20	י זכ	24	าว	22	21	20	10	110	1-	7 1	2 10	= 1,	1 1 2	12	11	10	0	0	7	<i>C</i>	С	1	3 2	1	0
	iluilibe	:1		21	3U Z	.J Z	.0 21	/ 20	, 23	24	. 23	22	. 21	20	15	1 10	, т.	, T(J 1.) 1º	13	12	11	10	9	0	′	Ο.	٠, ر			Ī	_
Id																															3 B	В	Α
Res	et 0x0	0000000		0	0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Val	ue						De	scr	ipti	on																			
Α	RW	HWFC									На	rdv	vare	e flo	ow	cor	ntro	ol															
			Disabled	0							Dis	ab	led																				
			Enabled	1							En	abl	ed																				
В	RW	PARITY									Pa	rity	,																				
			Excluded	0x0							Ex	clud	de p	ari	ty b	oit																	
			Included	0x7							Inc	lud	le p	arit	ty b	it																	

35.11 Electrical specification

35.11.1 UARTE electrical specification

Symbol	Description	Min.	Тур.	Max.	Units
f _{UARTE}	Baud rate for UARTE ³² .			1000	kbps
I _{UARTE1M}	Run current at max baud rate.		55		μΑ
I _{UARTE115k}	Run current at 115200 bps.		55		μΑ
I _{UARTE1k2}	Run current at 1200 bps.		55		μΑ
I _{UARTE,IDLE}	Idle current for UARTE (STARTed, no XXX activity)		1		μΑ
t _{UARTE,CTSH}	CTS high time	1			μs

Higher baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Symbol	Description	Min.	Тур.	Max.	Units
t _{UARTE,START,LP}	Time from STARTRX/STARTTX task to transmission started, low		t _{UARTE,ST}	AR	μs
	power mode		+		
			t _{START_H}	IN	
t _{UARTE,START,CL}	Time from STARTRX/STARTTX task to transmission started,		1		μs
	constant latency mode				



36 QDEC — Quadrature decoder

The Quadrature decoder (QDEC) provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors.

The sample period and accumulation are configurable to match application requirements. The QDEC provides the following:

- Decoding of digital waveform from off-chip quadrature encoder.
- · Sample accumulation eliminating hard real-time requirements to be enforced on application.
- Optional input de-bounce filters.
- Optional LED output signal for optical encoders.

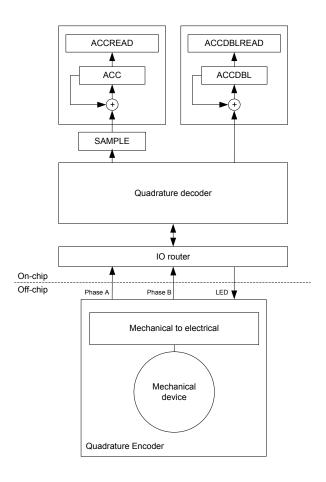


Figure 97: Quadrature decoder configuration

36.1 Sampling and decoding

The QDEC decodes the output from an incremental motion encoder by sampling the QDEC phase input pins (A and B).

The off-chip quadrature encoder is an incremental motion encoder outputting two waveforms, phase A and phase B. The two output waveforms are always 90 degrees out of phase, meaning that one always changes level before the other. The direction of movement is indicated by which of these two waveforms that changes level first. Invalid transitions may occur, that is when the two waveforms switch simultaneously. This may occur if the wheel rotates too fast relative to the sample rate set for the decoder.



The QDEC decodes the output from the off-chip encoder by sampling the QDEC phase input pins (A and B) at a fixed rate as specified in the SAMPLEPER register.

If the SAMPLEPER value needs to be changed, the QDEC shall be stopped using the STOP task. SAMPLEPER can be then changed upon receiving the STOPPED event, and QDEC can be restarted using the START task. Failing to do so may result in unpredictable behaviour.

It is good practice to change other registers (LEDPOL, REPORTPER, DBFEN and LEDPRE) only when the QDEC is stopped.

When started, the decoder continuously samples the two input waveforms and decodes these by comparing the current sample pair (n) with the previous sample pair (n-1).

The decoding of the sample pairs is described in the table below.

Table 83: Sampled value encoding

Previous sample - 1)	us e pair(n	Curre	ent oles pair(n)	SAMPLE register	ACC operation	ACCDBL operation	Description
Α	В	Α	В				
0	0	0	0	0	No change	No change	No movement
0	0	0	1	1	Increment	No change	Movement in positive direction
0	0	1	0	-1	Decrement	No change	Movement in negative direction
0	0	1	1	2	No change	Increment	Error: Double transition
0	1	0	0	-1	Decrement	No change	Movement in negative direction
0	1	0	1	0	No change	No change	No movement
0	1	1	0	2	No change	Increment	Error: Double transition
0	1	1	1	1	Increment	No change	Movement in positive direction
1	0	0	0	1	Increment	No change	Movement in positive direction
1	0	0	1	2	No change	Increment	Error: Double transition
1	0	1	0	0	No change	No change	No movement
1	0	1	1	-1	Decrement	No change	Movement in negative direction
1	1	0	0	2	No change	Increment	Error: Double transition
1	1	0	1	-1	Decrement	No change	Movement in negative direction
1	1	1	0	1	Increment	No change	Movement in positive direction
1	1	1	1	0	No change	No change	No movement

36.2 LED output

The LED output follows the sample period, and the LED is switched on a given period before sampling and switched off immediately after the inputs are sampled. The period the LED is switched on before sampling is given in the LEDPRE register.

The LED output pin polarity is specified in the LEDPOL register.

For using off-chip mechanical encoders not requiring a LED, the LED output can be disabled by writing value 'Disconnected' to the CONNECT field of the PSEL.LED register. In this case the QDEC will not acquire access to a LED output pin and the pin can be used for other purposes by the CPU.

36.3 Debounce filters

Each of the two-phase inputs have digital debounce filters.

When enabled through the DBFEN register, the filter inputs are sampled at a fixed 1 MHz frequency during the entire sample period (which is specified in the SAMPLEPER register), and the filters require all of the samples within this sample period to equal before the input signal is accepted and transferred to the output of the filter.

As a result, only input signal with a steady state longer than twice the period specified in SAMPLEPER are guaranteed to pass through the filter, and any signal with a steady state shorter than SAMPLEPER will always be suppressed by the filter. (This is assumed that the frequency during the debounce period never exceeds 500 kHz (as required by the Nyquist theorem when using a 1 MHz sample frequency).

The LED will always be ON when the debounce filters are enabled, as the inputs in this case will be sampled continuously.



Note that when when the debounce filters are enabled, displacements reported by the QDEC peripheral are delayed by one SAMPLEPER period.

36.4 Accumulators

The quadrature decoder contains two accumulator registers, ACC and ACCDBL, that accumulate respectively valid motion sample values and the number of detected invalid samples (double transitions).

The ACC register will accumulate all valid values (1/-1) written to the SAMPLE register. This can be useful for preventing hard real-time requirements from being enforced on the application. When using the ACC register the application does not need to read every single sample from the SAMPLE register, but can instead fetch the ACC register whenever it fits the application. The ACC register will always hold the relative movement of the external mechanical device since the previous clearing of the ACC register. Sample values indicating a double transition (2) will not be accumulated in the ACC register.

An ACCOF event will be generated if the ACC receives a SAMPLE value that would cause the register to overflow or underflow. Any SAMPLE value that would cause an ACC overflow or underflow will be discarded, but any samples not causing the ACC to overflow or underflow will still be accepted.

The accumulator ACCDBL accumulates the number of detected double transitions since the previous clearing of the ACCDBL register.

The ACC and ACCDBL registers can be cleared by the READCLRACC and subsequently read using the ACCREAD and ACCDBLREAD registers.

The ACC register can be separately cleared by the RDCLRACC and subsequently read using the ACCREAD registers.

The ACCDBL register can be separately cleared by the RDCLRDBL and subsequently read using the ACCDBLREAD registers.

The REPORTPER register allows automating the capture of several samples before it can send out a REPORTRDY event in case a non-null displacement has been captured and accumulated, and a DBLRDY event in case one or more double-displacements have been captured and accumulated. The REPORTPER field in this register selects after how many samples the accumulators contents are evaluated to send (or not) REPORTRDY and DBLRDY events.

Using the RDCLRACC task (manually sent upon receiving the event, or using the DBLRDY_RDCLRACC shortcut), ACCREAD can then be read.

In case at least one double transition has been captured and accumulated, a DBLRDY event is sent. Using the RDCLRDBL task (manually sent upon receiving the event, or using the DBLRDY_RDCLRDBL shortcut), ACCDBLREAD can then be read.

36.5 Output/input pins

The QDEC uses a three-pin interface to the off-chip quadrature encoder.

These pins will be acquired when the QDEC is enabled in the ENABLE register. The pins acquired by the QDEC cannot be written by the CPU, but they can still be read by the CPU.

The pin numbers to be used for the QDEC are selected using the PSEL.n registers.

36.6 Pin configuration

The Phase A, Phase B, and LED signals are mapped to physical pins according to the configuration specified in the PSEL.A, PSEL.B, and PSEL.LED registers respectively.

If the CONNECT field value 'Disconnected' is specified in any of these registers, the associated signal will not be connected to any physical pin. The PSEL.A, PSEL.B, and PSEL.LED registers and their configurations are only used as long as the QDEC is enabled, and retained only as long as the device is in



ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register.

To secure correct behavior in the QDEC, the pins used by the QDEC must be configured in the GPIO peripheral as described in *Table 84: GPIO configuration before enabling peripheral* on page 350 before enabling the QDEC. This configuration must be retained in the GPIO for the selected IOs as long as the QDEC is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 84: GPIO configuration before enabling peripheral

QDEC signal	QDEC pin	Direction	Output value	Comment	
Phase A	As specified in PSEL.A	Input	Not applicable		
Phase B	As specified in PSEL.B	Input	Not applicable		
LED	As specified in PSEL.LED	Input	Not applicable		

36.7 Registers

Table 85: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40012000	QDEC	QDEC	Quadrature decoder	

Table 86: Register Overview

Register	Offset	Description
TASKS_START	0x000	Task starting the quadrature decoder
TASKS_STOP	0x004	Task stopping the quadrature decoder
TASKS_READCLRACC	0x008	Read and clear ACC and ACCDBL
TASKS_RDCLRACC	0x00C	Read and clear ACC
TASKS_RDCLRDBL	0x010	Read and clear ACCDBL
EVENTS_SAMPLERDY	0x100	Event being generated for every new sample value written to the SAMPLE register
EVENTS_REPORTRDY	0x104	Non-null report ready
EVENTS_ACCOF	0x108	ACC or ACCDBL register overflow
EVENTS_DBLRDY	0x10C	Double displacement(s) detected
EVENTS_STOPPED	0x110	QDEC has been stopped
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable the quadrature decoder
LEDPOL	0x504	LED output pin polarity
SAMPLEPER	0x508	Sample period
SAMPLE	0x50C	Motion sample value
REPORTPER	0x510	Number of samples to be taken before REPORTRDY and DBLRDY events can be generated
ACC	0x514	Register accumulating the valid transitions
ACCREAD	0x518	Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task
PSEL.LED	0x51C	Pin select for LED signal
PSEL.A	0x520	Pin select for A signal
PSEL.B	0x524	Pin select for B signal
DBFEN	0x528	Enable input debounce filters
LEDPRE	0x540	Time period the LED is switched ON prior to sampling
ACCDBL	0x544	Register accumulating the number of detected double transitions
ACCDBLREAD	0x548	Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

36.7.1 SHORTS

Address offset: 0x200 Shortcut register



Bit	numbe	r		31 30	29 28	3 27 2	6 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								G F E D C B A
Res	et 0x00	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
Α	RW	REPORTRDY_READCLRACG	С					Shortcut between REPORTRDY event and READCLRACC task
								See EVENTS_REPORTRDY and TASKS_READCLRACC
			Disabled	0				Disable shortcut
			Enabled	1				Enable shortcut
В	RW	SAMPLERDY_STOP						Shortcut between SAMPLERDY event and STOP task
								See EVENTS_SAMPLERDY and TASKS_STOP
			Disabled	0				Disable shortcut
			Enabled	1				Enable shortcut
С	RW	REPORTRDY_RDCLRACC						Shortcut between REPORTRDY event and RDCLRACC task
								See EVENTS_REPORTRDY and TASKS_RDCLRACC
			Disabled	0				Disable shortcut
			Enabled	1				Enable shortcut
D	RW	REPORTRDY_STOP						Shortcut between REPORTRDY event and STOP task
								See EVENTS_REPORTRDY and TASKS_STOP
			Disabled	0				Disable shortcut
			Enabled	1				Enable shortcut
Ε	RW	DBLRDY_RDCLRDBL						Shortcut between DBLRDY event and RDCLRDBL task
								See EVENTS_DBLRDY and TASKS_RDCLRDBL
			Disabled	0				Disable shortcut
			Enabled	1				Enable shortcut
F	RW	DBLRDY_STOP						Shortcut between DBLRDY event and STOP task
								See EVENTS_DBLRDY and TASKS_STOP
			Disabled	0				Disable shortcut
			Enabled	1				Enable shortcut
G	RW	SAMPLERDY_READCLRAC	С					Shortcut between SAMPLERDY event and READCLRACC task
								See EVENTS_SAMPLERDY and TASKS_READCLRACC
			Disabled	0				Disable shortcut
			Enabled	1				Enable shortcut

36.7.2 INTENSET

Address offset: 0x304 Enable interrupt

Bit r	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E D C B A
Res	et 0x00000000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW SAMPLERDY			Write '1' to Enable interrupt for SAMPLERDY event
				See EVENTS_SAMPLERDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW REPORTRDY			Write '1' to Enable interrupt for REPORTRDY event
				See EVENTS_REPORTRDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW ACCOF			Write '1' to Enable interrupt for ACCOF event
				See EVENTS_ACCOF
		Set	1	Enable



Bit numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E D C B A
Reset 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW	Field	Value Id	Value	Description
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D RW	DBLRDY			Write '1' to Enable interrupt for DBLRDY event
				See EVENTS_DBLRDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E RW	STOPPED			Write '1' to Enable interrupt for STOPPED event
				See EVENTS_STOPPED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

36.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	er		3	1 30	29	28	27	26	25	5 24	1 2	3 :	22 2	21 2	0 1	9 1	8	17 1	.6	15	14	13	12	2 1:	1 10) 9	9 (7	6	5	4	3	2	1	0
Id																																Ε	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	()	0 (0 ()	0 (0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	alue							D	es	scrip	tior	1																				
Α	RW	SAMPLERDY										V	Vri	ite '1	l' to	Di	sab	le i	nte	rru	pt	for	SA	MF	PLE	RD	Y e	ven	t							
												S	ee	EVE	NT.	s_s	AM	1PL	ERL	Y																
			Clear	1								D	isa	able																						
			Disabled	0								R	ea	ad: D	isal	ole	b																			
			Enabled	1								R	ea	ad: E	nab	lec	ı																			
В	RW	REPORTRDY										W	Vri	ite '1	l' to	Di	sab	le i	nte	rru	pt	for	RE	РО	RT	RD۱	∕ e\	/en								
												S	ee	EVE	NT.	S_ <i>F</i>	REP	OR	TRD	Y																
			Clear	1								D	isa	able																						
			Disabled	0								R	ea	ad: D	isal	ole	b																			
			Enabled	1								R	ea	ad: E	nab	lec	ı																			
С	RW	ACCOF										W	Vri	ite '1	L' to	Di	sab	le i	nte	rru	pt	for	AC	СО)F e	ver	nt									
												S	ee	EVE	NT.	s_ <i>A</i>	ICC	OF																		
			Clear	1								D	isa	able																						
			Disabled	0								R	ea	ad: D	isal	ole	b																			
			Enabled	1								R	ea	ad: E	nab	lec	ı																			
D	RW	DBLRDY										W	Vri	ite '1	l' to	Di	sab	le i	nte	rru	pt	for	DB	LR	DY	eve	ent									
												S	ee	EVE	NT.	S_ <i>L</i>	BLI	RD	Υ																	
			Clear	1								D	isa	able																						
			Disabled	0								R	ea	ad: D	isal	ole	b																			
			Enabled	1								R	ea	ad: E	nab	lec	ı																			
Ε	RW	STOPPED										٧	Vri	ite '1	l' to	Di	sab	le i	nte	rru	pt	for	ST	OP	PEI) e	ven	t								
												S	ee	EVE	NT.	s_s	ΤΟΙ	PPI	ED																	
			Clear	1								D	isa	able																						
			Disabled	0								R	ea	ad: D	isal	ole	d																			
			Enabled	1								R	ea	ad: E	nab	lec	ı																			

36.7.4 ENABLE

Address offset: 0x500

Enable the quadrature decoder



В	t nur	mbe	r		31	L 30	29	28	8 27	7 2	26 25	5 2	24 2	3 22	2 21	20	19	18	3 17	7 16	5 15	5 14	1 13	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1	0
Id																																				Α
R	eset	0x0	0000000		0	0	0	0	0	(0 0) (0 0	0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0
Ic	l F	RW	Field	Value Id	Va	alue							D	esci	ripti	ion																				
Α	F	RW	ENABLE										Е	nabl	le o	r dis	sab	le t	he	qua	dra	atur	e d	lec	ode	r										
													W	/her	n en	nabl	ed	the	de	coc	ler	pin	s w	ill b	e a	ctiv	e. V	Vhe	n d	isal	oled	t				
													tŀ	ne q	uad	Iratı	ure	de	coc	ler	pins	ar	e n	ot a	acti	ve a	ınd	can	be	use	ed a	is				
													G	PIO																						
				Disabled	0								D	isab	le																					
				Enabled	1								Е	nabl	le																					

36.7.5 LEDPOL

Address offset: 0x504 LED output pin polarity

Bit	num	nber			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			Α
Res	et 0)x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	R۱	W	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	R۱	W	LEDPOL										LEC) ou	ıtpı	ıt p	in p	ola	rity	,															
				ActiveLow	0								Lec	l ac	tive	on	ou	tpu	t pi	n lo	ow														
				ActiveHigh	1								Lec	l ac	tive	on	ou	tpu	t pi	n h	igh														

36.7.6 SAMPLEPER

Address offset: 0x508

Sample period

Bit number			31	30 29	28 2	27 2	6 25	24	23 22	2 21	20 1	19 1	8 17	' 16	15	14 1	13 12	2 11	10	9 1	3 7	6	5	4 3	3 2	1	0
Id																								A	A A	Α	Α
Reset 0x000	00000		0	0 0	0	0 0	0	0	0 0	0	0	0 (0	0	0	0	0 0	0	0	0 (0	0	0	0 (0	0	0
ld RW Fi	eld	Value Id	Val	ue					Desc	riptic	on																
A RW SA	AMPLEPER								Samp	ole pe	erio	d. Th	ne SA	AMP	LE r	egis	ter v	vill b	e up	dat	ed fo	or ev	ery				
									new	samp	le																
		128us	0						128 ι	ıs																	
		256us	1						2 56 ι	ıs																	
		512us	2						512 ι	ıs																	
		1024us	3						1024	us																	
		2048us	4						2048	us																	
		4096us	5						4096	us																	
		8192us	6						8192	us																	
		16384us	7						1638	4 us																	
		32ms	8						3276	8 us																	
		65ms	9						6553	6 us																	
		131ms	10						1310	72 us	5																

36.7.7 SAMPLE

Address offset: 0x50C Motion sample value

Bit	num	ber		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 :	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	А А
Re	set 0:	k00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()	0 0
Id	RV	V Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	R	SAMPLE		[-1	21							Las	t m	otio	n s	am	nle																	



Id RW Field Value Id Value		Description			
Reset 0x00000000 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0
Id A A	A A A A A A	A A A A A A	A A A A A	A A A A A	A A A A A A
Bit number 31 30	30 29 28 27 26 25 24	23 22 21 20 19 18 1	7 16 15 14 13 12	11 10 9 8 7	6 5 4 3 2 1 0

The value is a 2's complement value, and the sign gives the direction of the motion. The value '2' indicates a double transition.

36.7.8 REPORTPER

Address offset: 0x510

Number of samples to be taken before REPORTRDY and DBLRDY events can be generated

Bit	numb	er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					АААА
Res	et 0x(00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	REPORTPER			Specifies the number of samples to be accumulated in the ACC
					register before the REPORTRDY and DBLRDY events can be
					generated
					The report period in [us] is given as: RPUS = SP * RP Where
					RPUS is the report period in [us/report], SP is the sample period
					in [us/sample] specified in SAMPLEPER, and RP is the report
					period in [samples/report] specified in REPORTPER.
			10Smpl	0	10 samples / report
			40Smpl	1	40 samples / report
			80Smpl	2	80 samples / report
			120Smpl	3	120 samples / report
			160Smpl	4	160 samples / report
			200Smpl	5	200 samples / report
			240Smpl	6	240 samples / report
			280Smpl	7	280 samples / report
			1Smpl	8	1 sample / report

36.7.9 ACC

Address offset: 0x514

Register accumulating the valid transitions

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A R ACC		[-10241023] Register accumulating all valid samples (not double transition)
		read from the SAMPLE register
		Double transitions (SAMPLE = 2) will not be accumulated in
		Double transitions (SAINFEE = 2) will not be accumulated in
		this register. The value is a 32 bit 2's complement value. If a
		sample that would cause this register to overflow or underflow
		is received, the sample will be ignored and an overflow event
		(ACCOF) will be generated. The ACC register is cleared by
		· · · · · · · · · · · · · · · · · · ·

36.7.10 ACCREAD

Address offset: 0x518

Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task



Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 1	16 1	15 1	L4 1	.3 1	2 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α.	A ,	Δ ,	A A	A A	A	. A	Α	Α	Α	Α	Α ,	Δ.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Δ	R	ACCREAD		ſ ₋ 1	024	10	123	1				Sna	nsk	not	of t	he	۵۲۲	'rec	oist.	٥r													

The ACCREAD register is updated when the READCLRACC or RDCLRACC task is triggered

36.7.11 PSEL.LED

Address offset: 0x51C Pin select for LED signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	АААА
Rese	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

36.7.12 PSEL.A

Address offset: 0x520 Pin select for A signal

Bit	numbe	er		31 30	29	28	3 27	26	25	24	23 2	22 2	21 2	0 19	9 18	3 17	16	15	14 1	.3 12	11	10	9	8	7 6	5 5	5 4	3	2	1 0
Id				В																							Α	Α	Α	А А
Res	et 0xF	FFFFFF		1 1	1	1	1	1	1	1	1	1	1 1	l 1	. 1	1	1	1	1 :	1 1	1	1	1	1	1 1	L 1	l 1	1	1	1 1
Id	RW	Field	Value Id	Value							Des	crip	tior	1																
Α	RW	PIN		[031]						Pin	nur	nbe	r																
В	RW	CONNECT									Con	nec	tion	1																
			Disconnected	1							Disc	coni	nect																	
			Connected	0							Con	nec	t																	

36.7.13 PSEL.B

Address offset: 0x524 Pin select for B signal

Bit r	iumbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

36.7.14 DBFEN

Address offset: 0x528

Enable input debounce filters



Bit	numl	ber			31 3	0 29	28	3 27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																																Α
Res	et 0	x00	000000		0 0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RV	N	Field	Value Id	Value			Des	crip	otio	n																					
Α	RV	N	DBFEN									Ena	ble	inp	ut d	ebo	ounc	e fi	lter	S												
				Disabled	0 Debounce input filters disabled																											
				Enabled	1 Debounce input filters enabled																											

36.7.15 LEDPRE

Address offset: 0x540

Time period the LED is switched ON prior to sampling

Bit numl	per		31	30 2	9 2	8 27	26	25	24	23 2	22 2	1 20	0 19	18	17	16	15 3	14 1	3 12	11	10	9	8 7	6	5	4	3	2	1 0
Id																							A A	. Д	A	Α	Α	A	АА
Reset 0x	00000010		0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0 0	0	0	1	0	0	0 0
Id RV	/ Field	Value Id	Val	ue						Des	cript	tion	1																
A RW	A RW LEDPRE			511]						Peri	od ii	n us	the	LE) is	swit	tche	d or	n pri	or to	sar	npl	ing						

36.7.16 ACCDBL

Address offset: 0x544

Register accumulating the number of detected double transitions

Bit no	umbe	r		31	30 :	29	28 2	27 :	26 2	25 2	24 2	23 22	21	20	19 :	18 1	17 1	l6 1	L5 1	4 1	3 12	11	10	9	8 .	7	6	5 4		3 2 4 A	1 A	0 . A
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0 0	0	0	0	0	0 ()	0	0 () (0	0	0
Id	RW	Field	Value Id	Va	lue						C	Descr	iptic	n																		
A	R	ACCDBL		[0.	15]						t V a c il	Regis ransi Wher accur overf Ilega reach	tions n this nulat low e l tran	s. (reation evensiti	SAN giste n of nt (ions ifiel	IPL er h dou ACC are	E = las r lble COF e de	2). reac /il :) w	ched lega vill l	d its al tra pe ge afte	max ansit ener er th	imu ions ateo	ım v s will d if a axim	alu I ste ny nun	e th op. a dou n va	e An ble	or wa	ıs				

36.7.17 ACCDBLREAD

Address offset: 0x548

Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

Bit	numb	er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					АААА
Res	et 0x(0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
					Description
Α	R	ACCDBLREAD		[015]	Snapshot of the ACCDBL register. This field is updated when the

36.8 Electrical specification

36.8.1 QDEC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{QDEC}	Run current		5		μΑ
t _{SAMPLE}	Time between sampling signals from quadrature decoder	128		131072	μs
t _{LED}	Time from LED is turned on to signals are sampled	0		511	μs



37 SAADC — Successive approximation analog-todigital converter

The ADC is a differential successive approximation register (SAR) analog-to-digital converter.

Listed here are the main features of SAADC:

- 8/10/12-bit resolution, 14-bit resolution with oversampling
- Up to eight input channels
 - One channel per single-ended input and two channels per differential input
 - Scan mode can be configured with both single-ended channels and differential channels.
- Full scale input range (0 to VDD)
- Sampling triggered via a task from software or a PPI channel for full flexibility on sample frequency source from low power 32.768kHz RTC or more accurate 1/16MHz Timers
- One-shot conversion mode to sample a single channel
- Scan mode to sample a series of channels in sequence. Sample delay between channels is t_{ack} + t_{conv} which may vary between channels according to user configuration of t_{ack}.
- Support for direct sample transfer to RAM using EasyDMA
- · Interrupts on single sample and full buffer events
- Samples stored as 16-bit 2's complement values for differential and single-ended sampling
- · Continuous sampling without the need of an external timer
- Internal resistor string
- · Limit checking on the fly

37.1 Shared resources

The ADC can coexist with COMP, LPCOMP and other peripherals using one of AIN0-AIN7, provided these are assigned to different pins.

It is not recommended to select the same analog input pin for both modules.

37.2 Overview

The ADC supports up to eight external analog input channels, depending on package variant. It can be operated in a one-shot mode with sampling under software control, or a continuous conversion mode with a programmable sampling rate.

The analog inputs can be configured as eight single-ended inputs, four differential inputs or a combination of these. Each channel can be configured to select AIN0 to AIN7 pins, or the VDD pin. Channels can be sampled individually in one-shot or continuous sampling modes, or, using scan mode, multiple channels can be sampled in sequence. Channels can also be oversampled to improve noise performance.



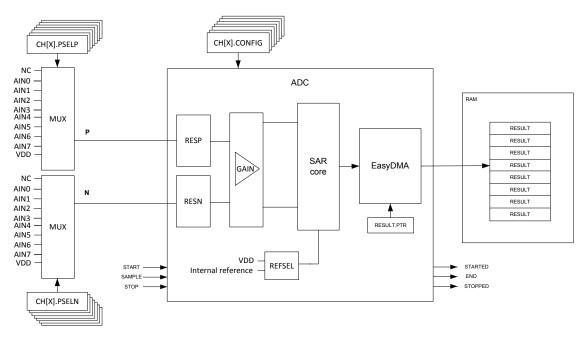


Figure 98: Simplified ADC block diagram

Internally, the ADC is always a differential analog-to-digital converter, but by default it is configured with single-ended input in the MODE field of the CH[n].CONFIG register. In single-ended mode, the negative input will be shorted to ground internally.

The assumption in single-ended mode is that the internal ground of the ADC is the same as the external ground that the measured voltage is referred to. The ADC is thus sensitive to ground bounce on the PCB in single-ended mode. If this is a concern we recommend using differential measurement.

37.3 Digital output

The output result of the ADC depends on the settings in the CH[n].CONFIG and RESOLUTION registers as follows:

```
RESULT = [V(P) - V(N)] * GAIN/REFERENCE * 2 (RESOLUTION - m)
```

where

V(P)

is the voltage at input P

V(N)

is the voltage at input N

GAIN

is the selected gain setting

REFERENCE

is the selected reference voltage

and m=0 if CONFIG.MODE=SE, or m=1 if CONFIG.MODE=Diff.

The result generated by the ADC will deviate from the expected due DC errors like offset, gain, differential non-linearity (DNL), and integral non-linearity (INL). See *Electrical specification* for details on these parameters. The result can also vary due to AC errors like non-linearities in the GAIN block, settling errors due to high source impedance and sampling jitter. For battery measurement the DC errors are most noticeable.



The ADC has a wide selection of gains controlled in the GAIN field of the CH[n].CONFIG register. If CH[n].CONFIG.REFSEL=0, the input range of the ADC core is nominally ± 0.6 V differential and the input must be scaled accordingly.

The ADC has a temperature dependent offset. If the ADC is to operate over a large temperature range, we recommend running CALIBRATEOFFSET at regular intervals, a CALIBRATEDONE event will be fired when the calibration is complete

37.4 Analog inputs and channels

Up to eight analog input channels, CH[n](n=0..7), can be configured.

See Shared resources on page 357 for shared input with comparators.

Any one of the available channels can be enabled for the ADC to operate in one-shot mode. If more than one CH[n] is configured, the ADC enters scan mode.

An analog input is selected as a positive converter input if CH[n].PSELP is set, setting CH[n].PSELP also enables the particular channel.

An analog input is selected as a negative converter input if CH[n].PSELN is set. The CH[n].PSELN register will have no effect unless differential mode is enabled, see MODE field in CH[n].CONFIG register.

If more than one of the CH[n].PSELP registers is set, the device enters scan mode. Input selections in scan mode are controlled by the CH[n].PSELP and CH[n].PSELN registers, where CH[n].PSELN is only used if the particular scan channel is specified as differential, see MODE field in CH[n].CONFIG register.

Important: Channels selected for either COMP or LPCOMP cannot be used at the same time for ADC sampling, though channels not selected for use by these blocks can be used by the ADC.

Table 87: Legal connectivity CH[n] vs. analog input

Channel input	Source	Connectivity
CH[n].PSELP	AINOAIN7	Yes(any)
CH[n].PSELP	VDD	Yes
CH[n].PSELN	AINOAIN7	Yes(any)
CH[n].PSELN	VDD	Yes

37.5 Operation modes

The ADC input configuration supports one-shot mode, continuous mode and scan mode.

Scan mode and oversampling cannot be combined.

37.5.1 One-shot mode

One-shot operation is configured by enabling only one of the available channels defined by CH[n].PSELP, CH[n].PSELN, and CH[n].CONFIG registers.

Upon a SAMPLE task, the ADC starts to sample the input voltage. The CH[n].CONFIG.TACQ controls the acquisition time.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA. For more information, see *EasyDMA* on page 361.

37.5.2 Continuous mode

Continuous sampling can be achieved by using the internal timer in the ADC, or triggering the SAMPLE task from one of the general purpose timers through the PPI.

Care shall be taken to ensure that the sample rate fulfils the following criteria, depending on how many channels are active:

 $f_{SAMPLE} < 1/[t_{ACQ} + t_{conv}]$



The SAMPLERATE register can be used as a local timer instead of triggering individual SAMPLE tasks. When SAMPLERATE.MODE is set to Timers, it is sufficient to trigger SAMPLE task only once in order to start the SAADC and triggering the STOP task will stop sampling. The SAMPLERATE.CC field controls the sample rate.

The SAMPLERATE timer mode cannot be combined with SCAN mode, and only one channel can be enabled in this mode.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

37.5.3 Oversampling

An accumulator in the ADC can be used to average noise on the analog input. In general, oversampling improves the signal-to-noise ratio (SNR). Oversampling, however, does not improve the integral non-linearity (INL), or differential non-linearity (DNL).

Oversampling and scan should not be combined, since oversampling and scan will average over input channels.

The accumulator is controlled in the OVERSAMPLE register. The SAMPLE task must be set 2^{OVERSAMPLE} number of times before the result is written to RAM. This can be achieved by:

- Configuring a fixed sampling rate using the local timer or a general purpose timer and PPI to trigger a SAMPLE task
- Triggering SAMPLE 2^{OVERSAMPLE} times from software
- · Enabling BURST mode

CH[n].CONFIG.BURST can be enabled to avoid setting SAMPLE task $2^{\text{OVERSAMPLE}}$ times. With BURST = 1 the ADC will sample the input $2^{\text{OVERSAMPLE}}$ times as fast as it can (actual timing: $<(t_{\text{ACQ}}+t_{\text{CONV}})\times2^{\text{OVERSAMPLE}})$. Thus, for the user it will just appear like the conversion took a bit longer time, but other than that, it is similar to one-shot mode. Scan mode can be combined with BURST=1, if burst is enabled on all channels.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals that enough conversions have taken place for an oversampled result to get transferred into RAM. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

37.5.4 Scan mode

A channel is considered enabled if CH[n].PSELP is set. If more than one channel, CH[n], is enabled, the ADC enters scan mode.

In scan mode, one SAMPLE task will trigger one conversion per enabled channel. The time it takes to sample all channels is:

```
Total time < Sum (CH[x].t<sub>ACO</sub>+t<sub>CONV</sub>), x=0..enabled channels
```

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual values have been transferred into RAM by EasyDMA.

Figure 99: Example of RAM placement (even RESULT.MAXCNT), channels 1, 2 and 5 enabled on page 361 provides an example of results placement in Data RAM, with an even RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled.



	31 16	15 0
RESULT.PTR	CH[2] 1 st result	CH[1] 1 st result
RESULT.PTR + 4	CH[1] 2 nd result	CH[5] 1 st result
RESULT.PTR + 8	CH[5] 2 nd result	CH[2] 2 nd result
	(.)
RESULT.PTR + 2*(RESULT.MAXCNT – 2)	CH[5] last result	CH[2] last result

Figure 99: Example of RAM placement (even RESULT.MAXCNT), channels 1, 2 and 5 enabled

Figure 100: Example of RAM placement (odd RESULT.MAXCNT), channels 1, 2 and 5 enabled on page 361 provides an example of results placement in Data RAM, with an odd RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled. The last 32-bit word is populated only with one 16-bit result.

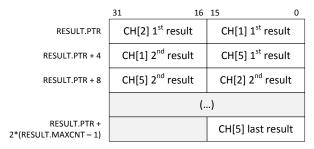


Figure 100: Example of RAM placement (odd RESULT.MAXCNT), channels 1, 2 and 5 enabled

37.6 EasyDMA

After configuring RESULT.PTR and RESULT.MAXCNT, the ADC resources are started by triggering the START task. The ADC is using EasyDMA to store results in a Result buffer in RAM.

The Result buffer is located at the address specified in the RESULT.PTR register. The RESULT.PTR register is double-buffered and it can be updated and prepared for the next START task immediately after the STARTED event is generated. The size of the Result buffer is specified in the RESULT.MAXCNT register and the ADC will generate an END event when it has filled up the Result buffer, see *Figure 101: ADC* on page 362. Results are stored in little-endian byte order in Data RAM. Every sample will be sign extended to 16 bit before stored in the Result buffer.

The ADC is stopped by triggering the STOP task. The STOP task will terminate an ongoing sampling. The ADC will generate a STOPPED event when it has stopped. If the ADC is already stopped when the STOP task is triggered, the STOPPED event will still be generated.



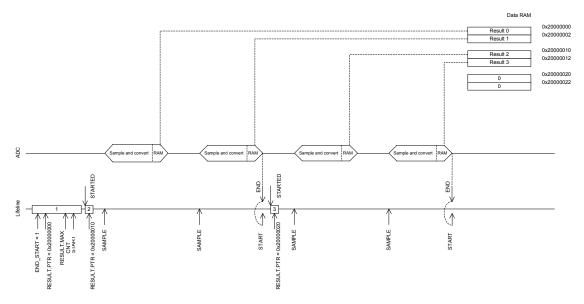


Figure 101: ADC

If the RESULT.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

The EasyDMA will have finished accessing the RAM when the END or STOPPED event has been generated.

The RESULT.AMOUNT register can be read following an END event or a STOPPED event to see how many results have been transferred to the Result buffer in RAM since the START task was triggered.

In Scan mode, the size of the Result buffer must be large enough to have room for a minimum one result from each of the enabled channels. To secure this, RESULT.MAXCNT must be specified to RESULT.MAXCNT >= "number of channels enabled". See *Scan mode* on page 360 for more information about Scan mode.

37.7 Resistor ladder

The ADC has an internal resistor string for positive and negative input.

See Figure 102: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP) on page 363. The resistors are controlled in the CH[n].CONFIG.RESP and CH[n].CONFIG.RESN registers.



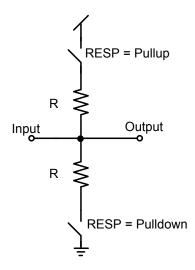


Figure 102: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP)

37.8 Reference

The ADC can use two different references, controlled in the REFSEL field of the CH[n].CONFIG register.

These are:

- · Internal reference
- · VDD as reference

The internal reference results in an input range of ± 0.6 V on the ADC core. VDD as reference results in an input range of $\pm VDD/4$ on the ADC core. The gain block can be used to change the effective input range of the ADC.

```
Input range = (+- 0.6 V or +-VDD/4)/Gain
```

For example, choosing VDD as reference, single ended input (grounded negative input), and a gain of 1/4 the input range will be:

```
Input range = (VDD/4)/(1/4) = VDD
```

With internal reference, single ended input (grounded negative input), and a gain of 1/6 the input range will be:

```
Input range = (0.6 \text{ V})/(1/6) = 3.6 \text{ V}
```

The AIN0-AIN7 inputs cannot exceed VDD, or be lower than VSS.

37.9 Acquisition time

To sample the input voltage, the ADC connects a capacitor to the input.

For illustration, see *Figure 103: Simplified ADC sample network* on page 364. The acquisition time indicates how long the capacitor is connected, see TACQ field in CH[n].CONFIG register. The required acquisition time depends on the source (R_{source}) resistance. For high source resistance the acquisition time should be increased, see *Table 88: Acquisition time* on page 364.



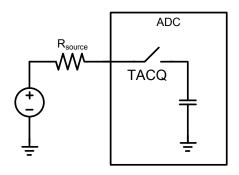


Figure 103: Simplified ADC sample network

Table 88: Acquisition time

TACQ [µs]	Maximum source resistance [kOhm]
3	10
5	40
10	100
15	200
20	400
40	800

37.10 Limits event monitoring

A channel can be event monitored by configuring limit register CH[n].LIMIT.

If the conversion result is higher than the defined high limit, or lower than the defined low limit, the appropriate event will get fired.

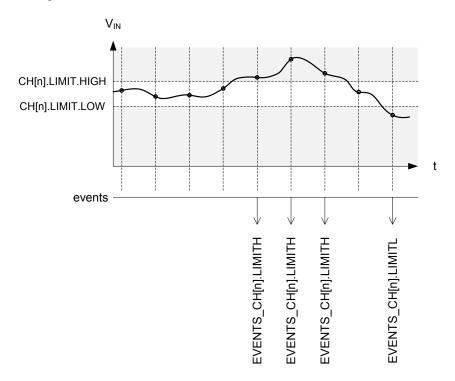


Figure 104: Example of limits monitoring on channel 'n'

Note that when setting the limits, CH[n].LIMIT.HIGH shall always be higher than or equal to CH[n].LIMIT.LOW . In other words, an event can be fired only when the input signal has been sampled



outside of the defined limits. It is not possible to fire an event when the input signal is inside a defined range by swapping high and low limits.

The comparison to limits always takes place, there is no need to enable it. If comparison is not required on a channel, the software shall simply ignore the related events. In that situation, the value of the limits registers is irrelevant, so it does not matter if CH[n].LIMIT.LOW is lower than CH[n].LIMIT.HIGH or not.

37.11 Registers

Table 89: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40007000	SAADC	SAADC	Analog to digital converter		

Table 90: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start the ADC and prepare the result buffer in RAM
TASKS_SAMPLE	0x004	Take one ADC sample, if scan is enabled all channels are sampled
TASKS_STOP	0x008	Stop the ADC and terminate any on-going conversion
TASKS_CALIBRATEOFFS	E 0x00C	Starts offset auto-calibration
EVENTS_STARTED	0x100	The ADC has started
EVENTS_END	0x104	The ADC has filled up the Result buffer
EVENTS_DONE	0x108	A conversion task has been completed. Depending on the mode, multiple conversions might be
		needed for a result to be transferred to RAM.
EVENTS_RESULTDONE	0x10C	A result is ready to get transferred to RAM.
EVENTS_CALIBRATEDO	N 0x110	Calibration is complete
EVENTS_STOPPED	0x114	The ADC has stopped
EVENTS_CH[0].LIMITH	0x118	Last results is equal or above CH[0].LIMIT.HIGH
EVENTS_CH[0].LIMITL	0x11C	Last results is equal or below CH[0].LIMIT.LOW
EVENTS_CH[1].LIMITH	0x120	Last results is equal or above CH[1].LIMIT.HIGH
EVENTS_CH[1].LIMITL	0x124	Last results is equal or below CH[1].LIMIT.LOW
EVENTS_CH[2].LIMITH	0x128	Last results is equal or above CH[2].LIMIT.HIGH
EVENTS_CH[2].LIMITL	0x12C	Last results is equal or below CH[2].LIMIT.LOW
EVENTS_CH[3].LIMITH	0x130	Last results is equal or above CH[3].LIMIT.HIGH
EVENTS_CH[3].LIMITL	0x134	Last results is equal or below CH[3].LIMIT.LOW
EVENTS_CH[4].LIMITH	0x138	Last results is equal or above CH[4].LIMIT.HIGH
EVENTS_CH[4].LIMITL	0x13C	Last results is equal or below CH[4].LIMIT.LOW
EVENTS_CH[5].LIMITH	0x140	Last results is equal or above CH[5].LIMIT.HIGH
EVENTS_CH[5].LIMITL	0x144	Last results is equal or below CH[5].LIMIT.LOW
EVENTS_CH[6].LIMITH	0x148	Last results is equal or above CH[6].LIMIT.HIGH
EVENTS_CH[6].LIMITL	0x14C	Last results is equal or below CH[6].LIMIT.LOW
EVENTS_CH[7].LIMITH	0x150	Last results is equal or above CH[7].LIMIT.HIGH
EVENTS_CH[7].LIMITL	0x154	Last results is equal or below CH[7].LIMIT.LOW
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STATUS	0x400	Status
ENABLE	0x500	Enable or disable ADC
CH[0].PSELP	0x510	Input positive pin selection for CH[0]
CH[0].PSELN	0x514	Input negative pin selection for CH[0]
CH[0].CONFIG	0x518	Input configuration for CH[0]
CH[0].LIMIT	0x51C	High/low limits for event monitoring a channel
CH[1].PSELP	0x520	Input positive pin selection for CH[1]
CH[1].PSELN	0x524	Input negative pin selection for CH[1]
CH[1].CONFIG	0x528	Input configuration for CH[1]
CH[1].LIMIT	0x52C	High/low limits for event monitoring a channel
CH[2].PSELP	0x530	Input positive pin selection for CH[2]



Register	Offset	Description
CH[2].PSELN	0x534	Input negative pin selection for CH[2]
CH[2].CONFIG	0x538	Input configuration for CH[2]
CH[2].LIMIT	0x53C	High/low limits for event monitoring a channel
CH[3].PSELP	0x540	Input positive pin selection for CH[3]
CH[3].PSELN	0x544	Input negative pin selection for CH[3]
CH[3].CONFIG	0x548	Input configuration for CH[3]
CH[3].LIMIT	0x54C	High/low limits for event monitoring a channel
CH[4].PSELP	0x550	Input positive pin selection for CH[4]
CH[4].PSELN	0x554	Input negative pin selection for CH[4]
CH[4].CONFIG	0x558	Input configuration for CH[4]
CH[4].LIMIT	0x55C	High/low limits for event monitoring a channel
CH[5].PSELP	0x560	Input positive pin selection for CH[5]
CH[5].PSELN	0x564	Input negative pin selection for CH[5]
CH[5].CONFIG	0x568	Input configuration for CH[5]
CH[5].LIMIT	0x56C	High/low limits for event monitoring a channel
CH[6].PSELP	0x570	Input positive pin selection for CH[6]
CH[6].PSELN	0x574	Input negative pin selection for CH[6]
CH[6].CONFIG	0x578	Input configuration for CH[6]
CH[6].LIMIT	0x57C	High/low limits for event monitoring a channel
CH[7].PSELP	0x580	Input positive pin selection for CH[7]
CH[7].PSELN	0x584	Input negative pin selection for CH[7]
CH[7].CONFIG	0x588	Input configuration for CH[7]
CH[7].LIMIT	0x58C	High/low limits for event monitoring a channel
RESOLUTION	0x5F0	Resolution configuration
OVERSAMPLE	0x5F4	Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is
		applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.
SAMPLERATE	0x5F8	Controls normal or continuous sample rate
RESULT.PTR	0x62C	Data pointer
RESULT.MAXCNT	0x630	Maximum number of buffer words to transfer
RESULT.AMOUNT	0x634	Number of buffer words transferred since last START

37.11.1 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit r	numb	er		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	STARTED			Enable or disable interrupt for STARTED event
					See EVENTS_STARTED
			Disabled	0	Disable
			Disabled	0	
			Enabled	1	Enable
В	RW	END			Enable or disable interrupt for END event
					See EVENTS_END
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	DONE			Enable or disable interrupt for DONE event
					See EVENTS_DONE
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	RESULTDONE			Enable or disable interrupt for RESULTDONE event
					See EVENTS_RESULTDONE
			Disabled	0	Disable
			Enabled	1	Enable



Bit r	iumbe	er		31 30	29 2	28 27	26 2	5 24 :	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 V U T S R Q P O N M L K J I H G F E D C B A
	et OxO	0000000		0 0	0 (0 0	0 (0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
Ε	RW	CALIBRATEDONE							Enable or disable interrupt for CALIBRATEDONE event
								:	See EVENTS_CALIBRATEDONE
			Disabled	0					Disable
			Enabled	1					Enable
F	RW	STOPPED							Enable or disable interrupt for STOPPED event
				_					See EVENTS_STOPPED
			Disabled Enabled	0 1					Disable Enable
G	RW	CHOLIMITH	Ellabled	1					Enable or disable interrupt for CH[0].LIMITH event
			Disabled	0					See EVENTS_CH[0].LIMITH Disable
			Enabled	1					Enable
Н	RW	CHOLIMITL							Enable or disable interrupt for CH[0].LIMITL event
								:	See EVENTS_CH[0].LIMITL
			Disabled	0					Disable
			Enabled	1					Enable
I	RW	CH1LIMITH							Enable or disable interrupt for CH[1].LIMITH event
								:	See EVENTS_CH[1].LIMITH
			Disabled	0					Disable
	D\A/	CH1LIMITL	Enabled	1					Enable
J	KVV	CHILIMITE							Enable or disable interrupt for CH[1].LIMITL event
			Disabled	0					See EVENTS_CH[1].LIMITL Disable
			Enabled	1					Enable
K	RW	CH2LIMITH		_					Enable or disable interrupt for CH[2].LIMITH event
									See EVENTS_CH[2].LIMITH
			Disabled	0					Disable
			Enabled	1					Enable
L	RW	CH2LIMITL							Enable or disable interrupt for CH[2].LIMITL event
								:	See EVENTS_CH[2].LIMITL
			Disabled	0					Disable
	DIM	CURLINATE	Enabled	1					Enable
М	RW	CH3LIMITH							Enable or disable interrupt for CH[3].LIMITH event
			S. 11.1						See EVENTS_CH[3].LIMITH
			Disabled Enabled	0 1					Disable Enable
N	RW	CH3LIMITL	Lilabieu						Enable or disable interrupt for CH[3].LIMITL event
									See EVENTS CH[3].LIMITL
			Disabled	0					Disable
			Enabled	1					Enable
0	RW	CH4LIMITH							Enable or disable interrupt for CH[4].LIMITH event
								:	See EVENTS_CH[4].LIMITH
			Disabled	0					Disable
			Enabled	1					Enable
Р	RW	CH4LIMITL							Enable or disable interrupt for CH[4].LIMITL event
									See EVENTS_CH[4].LIMITL
			Disabled	0					Disable
Q	D/V/	CH5LIMITH	Enabled	1					Enable Enable or disable interrupt for CH[5].LIMITH event
ų	IVVV	CHUCHITA							
									See EVENTS_CH[5].LIMITH



Bit r	numbe	er		3	1 3	0 29	9 28	27	26	25	24	23	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id														V	U	Т	S	R	Q	Р	0	Ν	М	L	K	J	L	Н	G	F	Ε	D (С Е	3 A
Res	et 0x0	0000000		0	O	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	alu	е						De	escr	riptio	on																			
			Disabled	0								Di	isab	ole																				
			Enabled	1								En	nabl	le																				
R	RW	CH5LIMITL										En	nabl	le or	dis	sab	le ii	nte	rrup	t fo	or C	H[5].LII	MIT	L e	/ent	t							
												Se	ee <i>E</i>	VEN	ITS_	_CH	I[5]	LIN	ЛΙΤΙ															
			Disabled	0								Di	isab	ole																				
			Enabled	1								En	nabl	le																				
S	RW	CH6LIMITH										En	nabl	le or	dis	sab	le ii	nte	rrup	t fo	or C	H[6].LII	MIT	Не	ven	t							
												Se	ee <i>E</i> '	VEN	ITS	CH	1[6]	LIN	ЛΙΤΙ	1														
			Disabled	0									isab																					
			Enabled	1								En	nabl	le																				
Т	RW	CH6LIMITL										En	nabl	le or	dis	sab	le iı	nte	rrup	t fo	or C	H[6].LII	MIT	L ev	/ent	t							
												Se	e E	VEN	ITS	CH	1161	LIN	ЛΙΤΙ															
			Disabled	0									isab				.[-]																	
			Enabled	1								En	nabl	le																				
U	RW	CH7LIMITH										En	nabl	le or	dis	sab	le iı	nte	rrup	t fo	or C	H[7].LII	MIT	Не	ven	t							
												۵۷	م <i>F</i> ا	VEN	ITS	CH	1[7]	110	літі	,														
			Disabled	0									isab		,,,		11/1	·Liii	,,,,,															
			Enabled	1									nabl																					
V	RW	CH7LIMITL												le or	dis	sab	le iı	nte	rrup	t fo	or C	H[7	'].LII	MIT	L e	/ent	t							
																			Ċ				-											
			Disabled	0									ee <i>E</i> isab	VEN	115_	_CH	[7]	.LIN	/1111															
			Disabled	0																														
			Enabled	1								En	nabl	ie																				

37.11.2 INTENSET

Address offset: 0x304

Enable interrupt

	number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0														
Id				V U T S R Q P O N M L K J I H G F E D C B A														
Res	et 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0														
ld	RW Field V	/alue Id	Value	Description														
Α	RW STARTED			Write '1' to Enable interrupt for STARTED event														
				See EVENTS_STARTED														
	Se	et	1	Enable														
	D	Disabled	0	Read: Disabled														
	E	nabled	1	Read: Enabled														
В	RW END			Write '1' to Enable interrupt for END event														
				See EVENTS_END														
	Se	et	1	Enable														
	D	Disabled	0	Read: Disabled														
	E	nabled	1	Read: Enabled														
С	RW DONE			Write '1' to Enable interrupt for DONE event														
				See EVENTS_DONE														
	Se	et	1	Enable														
	D	Disabled	0	Read: Disabled														
	E	nabled	1	Read: Enabled														
D	RW RESULTDONE			Write '1' to Enable interrupt for RESULTDONE event														
				See EVENTS_RESULTDONE														
	Se	et	1	Enable														
	D	Disabled	0	Read: Disabled														
	E	nabled	1	Read: Enabled														



Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value	Description
E	RW	CALIBRATEDONE			Write '1' to Enable interrupt for CALIBRATEDONE event
					See EVENTS_CALIBRATEDONE
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	STOPPED			Write '1' to Enable interrupt for STOPPED event
					See EVENTS_STOPPED
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	CHOLIMITH			Write '1' to Enable interrupt for CH[0].LIMITH event
					See EVENTS_CH[0].LIMITH
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	CHOLIMITL			Write '1' to Enable interrupt for CH[0].LIMITL event
					See EVENTS_CH[0].LIMITL
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
I	RW	CH1LIMITH			Write '1' to Enable interrupt for CH[1].LIMITH event
					See EVENTS_CH[1].LIMITH
			Set	1	Enable
			Disabled	0	Read: Disabled
	5144		Enabled	1	Read: Enabled
J	RW	CH1LIMITL			Write '1' to Enable interrupt for CH[1].LIMITL event
					See EVENTS_CH[1].LIMITL
			Set	1	Enable
			Disabled	0	Read: Disabled
	DIA	CHALINATH	Enabled	1	Read: Enabled
K	RW	CH2LIMITH			Write '1' to Enable interrupt for CH[2].LIMITH event
					See EVENTS_CH[2].LIMITH
			Set	1	Enable
			Disabled	0	Read: Disabled
	D\A/	CH2LIMITL	Enabled	1	Read: Enabled Write '1' to Enable interrupt for CH[2].LIMITL event
L	NVV	CHZLIMITL			
					See EVENTS_CH[2].LIMITL
			Set	1	Enable
			Disabled	0	Read: Disabled
М	R\M	CH3LIMITH	Enabled	1	Read: Enabled Write '1' to Enable interrupt for CH[3].LIMITH event
141	11.00	CHISCHVIIII			
			6.1		See EVENTS_CH[3].LIMITH
			Set	1	Enable Pead: Disabled
			Disabled Enabled	0	Read: Disabled Read: Enabled
N	RW/	CH3LIMITL	Lilabicu	1	Write '1' to Enable interrupt for CH[3].LIMITL event
.,		S. ISENTILE			
					See EVENTS_CH[3].LIMITL
			Set	1	Enable Pand: Disabled
			Disabled Enabled	0	Read: Disabled Read: Enabled
0	R/V/	CH4LIMITH	LITADICU	1	Write '1' to Enable interrupt for CH[4].LIMITH event
J	11.44	CHTENVILLI			write I to Enable interrupt for Crit+j. Liivii i i event



Bit r	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
				See EVENTS_CH[4].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Р	RW CH4LIMITL			Write '1' to Enable interrupt for CH[4].LIMITL event
				See EVENTS_CH[4].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Q	RW CH5LIMITH			Write '1' to Enable interrupt for CH[5].LIMITH event
				See EVENTS_CH[5].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
R	RW CH5LIMITL			Write '1' to Enable interrupt for CH[5].LIMITL event
				See EVENTS_CH[5].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
S	RW CH6LIMITH			Write '1' to Enable interrupt for CH[6].LIMITH event
				See EVENTS_CH[6].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Т	RW CH6LIMITL			Write '1' to Enable interrupt for CH[6].LIMITL event
				See EVENTS_CH[6].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
U	RW CH7LIMITH			Write '1' to Enable interrupt for CH[7].LIMITH event
				See EVENTS_CH[7].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
V	RW CH7LIMITL			Write '1' to Enable interrupt for CH[7].LIMITL event
				See EVENTS CH[7].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
		Litabica	-	neua: Enableu

37.11.3 INTENCLR

Address offset: 0x308 Disable interrupt

Bit n	umber 31 30 29 28 27 26 25									25	24	23	22	21	20 :	19 :	18 1	17 1	16 :	15 :	14	13 1	12 1	.1 10	9	8	7	6	5	4	3	2	1	0
Id														٧	U	Т	S	R	Q	Р	0	N I	M	L K	J	1	Н	G	F	Ε	D	С	В.	Α
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0
ld	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	STARTED										Wr	ite '	'1' t	o D	isab	le i	nte	rru	pt f	or :	STA	RTE	D ev	ent									_
													e <i>EV</i>		TS_S	STA	RTE	D																
			Clear	1								Dis	able	е																				



Bit r	numb	er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x(0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	END			Write '1' to Disable interrupt for END event
					See EVENTS_END
			Clear	1	Disable
			Disabled	0	Read: Disabled
_	DVA	DONE	Enabled	1	Read: Enabled
С	RW	DONE			Write '1' to Disable interrupt for DONE event
					See EVENTS_DONE
			Clear	1	Disable
			Disabled Enabled	0	Read: Disabled Read: Enabled
D	RW	RESULTDONE	Lilableu	1	Write '1' to Disable interrupt for RESULTDONE event
		RESOLIDONE			
			Class	4	See EVENTS_RESULTDONE
			Clear Disabled	0	Disable Read: Disabled
			Enabled	1	Read: Enabled
E	RW	CALIBRATEDONE	Enabled	-	Write '1' to Disable interrupt for CALIBRATEDONE event
			Clear	1	See EVENTS_CALIBRATEDONE Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	STOPPED			Write '1' to Disable interrupt for STOPPED event
					See EVENTS_STOPPED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	CHOLIMITH			Write '1' to Disable interrupt for CH[0].LIMITH event
					See EVENTS_CH[0].LIMITH
			Clear	1	Disable
			Disabled	0	Read: Disabled
	D\A/	CHOLINAITI	Enabled	1	Read: Enabled
Н	KVV	CHOLIMITL			Write '1' to Disable interrupt for CH[0].LIMITL event
					See EVENTS_CH[0].LIMITL
			Clear	0	Disable Read Disabled
			Disabled Enabled	1	Read: Disabled Read: Enabled
1	RW	CH1LIMITH		_	Write '1' to Disable interrupt for CH[1].LIMITH event
			Clear	1	See EVENTS_CH[1].LIMITH Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
J	RW	CH1LIMITL			Write '1' to Disable interrupt for CH[1].LIMITL event
					See EVENTS_CH[1].LIMITL
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
K	RW	CH2LIMITH			Write '1' to Disable interrupt for CH[2].LIMITH event
					See EVENTS_CH[2].LIMITH
			Clear	1	Disable
			Disabled	0	Read: Disabled



Bit r	numbe	er		31	30	29	28 2 ⁻	7 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id										V U T S R Q P O N M L K J I H G F E D C B A
Rese	et OxC	0000000		0	0	0	0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Va	lue					Description
			Enabled	1						Read: Enabled
L	RW	CH2LIMITL								Write '1' to Disable interrupt for CH[2].LIMITL event
										See EVENTS_CH[2].LIMITL
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
М	RW	CH3LIMITH								Write '1' to Disable interrupt for CH[3].LIMITH event
										See EVENTS_CH[3].LIMITH
			Clear	1						Disable
			Disabled	0						Read: Disabled
N	D\A/	CH3LIMITL	Enabled	1						Read: Enabled Write '1' to Disable interrupt for CH[3].LIMITL event
IN	IVV	CHISCHWITE								
										See EVENTS_CH[3].LIMITL
			Clear	1						Disable
			Disabled Enabled	0						Read: Disabled Read: Enabled
0	RW	CH4LIMITH	Ellableu	1						Write '1' to Disable interrupt for CH[4].LIMITH event
			Clear	1						See EVENTS_CH[4].LIMITH Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Р	RW	CH4LIMITL								Write '1' to Disable interrupt for CH[4].LIMITL event
										See EVENTS_CH[4].LIMITL
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Q	RW	CH5LIMITH								Write '1' to Disable interrupt for CH[5].LIMITH event
										See EVENTS_CH[5].LIMITH
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
R	RW	CH5LIMITL								Write '1' to Disable interrupt for CH[5].LIMITL event
										See EVENTS_CH[5].LIMITL
			Clear	1						Disable
			Disabled	0						Read: Disabled
_	DIA	CUCURATU	Enabled	1						Read: Enabled
S	ĸw	CH6LIMITH								Write '1' to Disable interrupt for CH[6].LIMITH event
				_						See EVENTS_CH[6].LIMITH
			Clear Disabled	1						Disable Read: Disabled
			Enabled	1						Read: Enabled
Т	RW	CH6LIMITL		_						Write '1' to Disable interrupt for CH[6].LIMITL event
			Clear	1						See EVENTS_CH[6].LIMITL Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
U	RW	CH7LIMITH								Write '1' to Disable interrupt for CH[7].LIMITH event
										See EVENTS_CH[7].LIMITH
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled



Bit	numbe	er		3:	1 30	29	2	8 27	7 2	26 2	5 2	24 :	23 :	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 .	4 3	2	1	0
Id															٧	U	Т	S	R	Q	Р	О	Ν	М	L	K	J	1	Н	G	F	E D	С	В	Α
Res	et 0x0	0000000		0	0	0	C	0) (0 ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	V	alue							- 1	Des	cri	ptic	n																			
٧	RW	CH7LIMITL										١	Wri	te '	'1' t	o D	isa	ble	inte	erru	ıpt	for	СН	[7].	LIM	ITL	eve	ent							
												:	See	EV	'EN	TS_	СН	[7].	LIM	ITL															
			Clear	1								- 1	Disa	able	е																				
			Disabled	0								- 1	Rea	ıd: I	Disa	ble	ed																		
			Enabled	1								ı	Rea	d: I	Ena	ble	d																		

37.11.4 STATUS

Address offset: 0x400

Status

Bit	numbe	er		3	1 30	29	28	8 27	7 20	6 25	5 24	1 23	22	21	20	19	18	17 :	16	15	14	13	12 :	11 1	0 9	9 :	3 7	7 6	5 5	4	3	2	1	0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 (0 () (0	0	0	0	0	0
Id	RW	Field	Value Id	٧	'alu	е						De	scr	ipti	on																			
Α	R	STATUS										St	atus	5																				
			Ready	0								Αſ	C is	s rea	ady.	. No	on	-goi	ing	cor	ive	rsio	n.											
			Busy	1								ΑĽ	C is	s bu	sy.	Con	ver	sior	ı in	pro	ogre	ess.												

37.11.5 ENABLE

Address offset: 0x500 Enable or disable ADC

Bitı	numbe	er		31 30	29	28 2	7 26	25	24	23 :	22 :	21 2	20 1	19 1	8 1	7 1	5 15	14	13	12 1	111	0 9	8	7	6	5	4	3	2	1 0
Id																														Α
Res	et 0x0	0000000		0 0	0	0 (0 0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value						Des	cri	ptio	n																	
Α	RW	ENABLE								Ena	ble	or	disa	ble	ΑD	С														
			Disabled	0						Disa	able	e AD	C																	
			Enabled	1						Ena	ble	AD	C																	
										Wh	en (ena	ble	d, th	ne A	ADC	will	acq	uire	acc	ess	to th	ne a	nalo	g ir	าри	ıt			
										pins	s sp	ecif	fied	in t	he (CH[ı	n].P:	SELF	and	d CH	l[n].	PSE	LN r	egis	ters	s.				

37.11.6 CH[0].PSELP

Address offset: 0x510

Input positive pin selection for CH[0]

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		АААА
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PSELP		Analog positive input channel
	NC	0 Not connected
	AnalogInput0	1 AINO
	AnalogInput1	2 AIN1
	AnalogInput2	3 AIN2
	AnalogInput3	4 AIN3
	AnalogInput4	5 AIN4
	AnalogInput5	6 AIN5
	AnalogInput6	7 AIN6
	AnalogInput7	8 AIN7
	VDD	9 VDD



37.11.7 CH[0].PSELN

Address offset: 0x514

Input negative pin selection for CH[0]

Bit n	numbe	r		31	30 2	9 2	8 27	7 26	25 2	4 2	3 22	21 2	0 1	19 18	3 1	7 16	15	14	13	12	11	10	9	8	7	6	5	4 3	3 2	1	0
Id																												A A	A A	Α	Α
Rese	et 0x0	0000000		0	0 () (0 0	0	0 (0 (0	0 0) (0 0	C	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue					D	escri	ption	١																		
Α	RW	PSELN								Α	nalo	g neg	ati	ve in	pu	t, er	nab	es	diffe	eren	tial	cha	ınn	el							
			NC	0						N	ot co	nnec	te	d																	
			AnalogInput0	1						Α	IN0																				
			AnalogInput1	2						Α	IN1																				
			AnalogInput2	3						Α	IN2																				
			AnalogInput3	4						Α	IN3																				
			AnalogInput4	5						Α	IN4																				
			AnalogInput5	6						Α	IN5																				
			AnalogInput6	7						Α	IN6																				
			AnalogInput7	8						Α	IN7																				
			VDD	9						٧	DD																				

37.11.8 CH[0].CONFIG

Address offset: 0x518

Input configuration for CH[0]

Bit	numb	er		31	. 30	29	28	27 :	26 2	25 2	24 2	23	22 23	1 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	. 1	. 0
Id											G			F			Ε					D		С					В				ι A
Res	et 0x(00020000		0	0	0	0	0	0	0	0	0	0 0	0	0				0	0	0		0				0				0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	script	ion																			
Α	RW	RESP									F	Pos	sitive	cha	nne	l re	sist	or o	on	trol													
			Bypass	0							Е	Byp	pass r	esis	tor	lado	der																
			Pulldown	1							F	Pul	II-dow	n to	o GN	ND																	
			Pullup	2							F	Pul	ll-up t	o V	DD																		
			VDD1_2	3							5	Set	t inpu	t at	VDI)/2																	
В	RW	RESN									١	Ne	gative	ch	ann	el r	esis	tor	COI	ntro	ıl												
			Bypass	0							E	Byp	pass r	esis	tor	lad	der																
			Pulldown	1							F	Pul	II-dow	n to	o GN	ND																	
			Pullup	2							F	Pul	ll-up t	o V	DD																		
			VDD1_2	3							S	Set	t inpu	t at	VDI)/2																	
С	RW	GAIN									(Gai	in cor	tro	l																		
			Gain1_6	0							1	1/6	5																				
			Gain1_5	1							1	1/5	5																				
			Gain1_4	2							1	1/4	4																				
			Gain1_3	3							1	1/3	3																				
			Gain1_2	4							1	1/2	2																				
			Gain1	5							1	1																					
			Gain2	6							2	2																					
			Gain4	7							4	4																					
D	RW	REFSEL									F	Ref	feren	ce c	onti	rol																	
			Internal	0									ernal					(V															
			VDD1_4	1									D/4 a																				
E	RW	TACQ									A	Acc	quisiti	on 1	time	e, th	ne t	ime	th	e A	DC I	ıse	s to	sar	npl	e th	e ii	npu	t				
											٧	vol	ltage																				
			3us	0								3 u																					
			5us	1								5 u																					
			10us	2							1	10	us																				
			15us	3							1	15	us																				
			20us	4							2	20	us																				



Bit nu	umbe	er		31 30	29	28 2	27 :	26 2	5 2	24 2	23 2	2 21	20	19	18	17 1	16 1	15 1	4 1	3 12	11	10	9	8	7	6 5	4	3	2	1 0
Id									(G			F		Ε	Ε	E			D		С	С	С		В	В			A A
Reset	t 0x0	0020000		0 0	0	0	0	0 (0	0	0 0	0	0	0	0	1	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	0 0
Id	RW	Field	Value Id	Value	:						Desc	ripti	on																	
			40us	5						4	l0 us	5																		
F	RW	MODE								E	nab	le di	ffer	enti	al n	nod	e													
			SE	0						5	ingl	e en	ded	, PS	ELN	l wil	l be	e igi	nore	d, n	egat	ive	inp	ut t) Al	DC				
										S	hor	ted t	o GI	ND																
			Diff	1						[Diffe	rent	ial																	
G	RW	BURST								E	nab	le bu	ırst	mo	de															
			Disabled	0						E	Burs	t mo	de i	s dis	sabl	ed	(no	rma	ıl op	erat	ion)									
			Enabled	1						E	Burs	t mo	de i	s en	abl	ed.	SAA	ADC	tak	es 2	^OV	ERS	ΑM	IPLE	nu	mbe	r of			
										,	amr	oles a	as fa	ist a	s it	car	ıar	nd s	end	s the	av.	erag	e t	o Da	ıta	RAN	1.			

37.11.9 CH[0].LIMIT

Address offset: 0x51C

High/low limits for event monitoring a channel

Bit	nur	mbe	r		31	. 30	29	28	27	26	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	1 0
Id					В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А		A A
Res	et (0x7	FFF8000		0	1	1	1	1	1	1	1	. 1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0 0	C	0 0
Id	R	w	Field	Value Id	Va	lue							De	escr	ipti	on																			
Α	R	RW	LOW		[-3	3276	58 t	0 +	327	767]		Lo	w le	evel	lim	it																		
В	R	RW	HIGH		[-3	3276	58 t	0 +	327	767	1		Hi	gh I	eve	l lim	nit																		

37.11.10 CH[1].PSELP

Address offset: 0x520

Input positive pin selection for CH[1]

Bit r	iumbe	r		31	30 2	29 2	28 2	7 2	6 25	5 24	4 23	22	21 2	0 1	19 1	8 1	7 1	5 15	5 14	1 13	3 12	11	10	9	8	7	6 5	5 4	3	2	1	0
Id																												Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0 0) (0 0	0	0	0	0 0) (0 0) (0	0	0	0	0	0	0	0	0 (0	0 0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						De	escri	ptior	١																		
Α	RW	PSELP									Ar	nalog	g pos	itiv	e in	put	cha	ann	el													
			NC	0							No	ot co	nnec	te	d																	
			AnalogInput0	1							ΑI	N0																				
			AnalogInput1	2							ΑI	N1																				
			AnalogInput2	3							ΑI	N2																				
			AnalogInput3	4							ΑI	N3																				
			AnalogInput4	5							ΑI	N4																				
			AnalogInput5	6							ΑI	N5																				
			AnalogInput6	7							ΑI	N6																				
			AnalogInput7	8							ΑI	N7																				
			VDD	9							VE	DD																				

37.11.11 CH[1].PSELN

Address offset: 0x524

Input negative pin selection for CH[1]

Bitı	numbe	er		31 3	0 2	9 28	3 27	26	25	24 :	23 2	22 2	1 20	19	18	17	16	15	14	13 1	2 13	10	9	8	7	6	5	4	3 2	1	0
Id																												Α	ΑА	. A	Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Valu	ie					ı	Des	cript	ion																		
Α	RW	PSELN								,	٩na	log r	nega	ativ	e in	put,	ena	able	s d	ffer	enti	al ch	anr	nel							
			NC	0						ı	Not	con	nect	ted																	
			AnalogInput0	1						,	AIN	0																			



Bit number		31	L 30	29	28	27	26	25	24	23 2	22 2	21 2	0 1	9 1	8 1	7 1	6 1	5 1	4 1	3 1	2 11	. 10	9	8	7	6	5 .	4	3 2	1	0
Id																												A A	Δ Δ	Α	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0 () (0 (0) () () () (0	0	0	0	0	0	0	0	0 (0	0	0
Id RW Field	Value Id	Va	alue							Des	crip	tior	1																		
	AnalogInput1	2								AIN:	1																				
	AnalogInput2	3								AIN:	2																				
	AnalogInput3	4								AIN:	3																				
	AnalogInput4	5								٩IN	4																				
	AnalogInput5	6								AIN!	5																				
	AnalogInput6	7								AIN	6																				
	AnalogInput7	8								AIN:	7																				
	VDD	9							,	/DD)																				

37.11.12 CH[1].CONFIG

Address offset: 0x528

Input configuration for CH[1]

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
d			G FEEE D CCC BB AA
Reset 0x00020000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0
d RW Field	Value Id	Value	Description
A RW RESP			Positive channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
B RW RESN			Negative channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
C RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
	Gain4	7	4
O RW REFSEL			Reference control
	Internal	0	Internal reference (0.6 V)
	VDD1_4	1	VDD/4 as reference
RW TACQ			Acquisition time, the time the ADC uses to sample the input
			voltage
	3us	0	3 us
	5us	1	5 us
	10us	2	10 us
	15us	3	15 us
	20us	4	20 us
	40us	5	40 us
RW MODE			Enable differential mode
	SE	0	Single ended, PSELN will be ignored, negative input to ADC
			shorted to GND
	Diff	1	Differential
G RW BURST			Enable burst mode
	Disabled	0	Burst mode is disabled (normal operation)



Bit number		31 30 29 28 27 26 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Id			G FEEE D CCC BB	3 A A
Reset 0x00020000		0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0
Id RW Field	Value Id	Value	Description	
	Enabled	1	Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of	f
			camples as fact as it can, and conds the average to Data PAM	

37.11.13 CH[1].LIMIT

Address offset: 0x52C

High/low limits for event monitoring a channel

Bit r	numbe	er		31	1 30	29	28	27	7 26	5 25	5 2	4 2	3 2	2 2	1 2	0 1	9 1	8 17	7 16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	. 1	L 0
Id				В	В	В	В	В	В	В	S E	3 E	3 E	3 E	3 E	3 E	B E	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А		A A
Res	et 0x7	FFF8000		0	1	1	1	1	1	1	. 1	1 1	L 1	1 1	1 1	1	. 1	. 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0 0	(0 0
Id	RW	Field	Value Id	Va	alue	•						D	esc	rip	tio	1																		
Α	RW	LOW		[-3	327	68 1	to +	327	767]		L	ow	lev	el li	mit																		
В	RW	HIGH		[_3	327	68 t	to +	327	767	1		Н	iøh	lev	el l	imit																		

37.11.14 CH[2].PSELP

Address offset: 0x530

Input positive pin selection for CH[2]

Bit i	numbe	er		31	30 :	29 2	28 2	7 26	5 25	24	23 2	2 21	. 20	19	18 1	.7 1	6 15	5 14	13	12	11 :	10 9)	3 7	6	5		3 2 A A	_	0 A
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0 (0 0	0	0	0	0 (0	0	0	0	0	0 ()	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						Desc	cripti	on																	
Α	RW	PSELP									Anal	log p	osit	ive i	npu	t ch	ann	el												
			NC	0							Not	conn	ect	ed																
			AnalogInput0	1							AINO)																		
			AnalogInput1	2							AIN1	l																		
			AnalogInput2	3							AIN2	2																		
			AnalogInput3	4							AIN	3																		
			AnalogInput4	5							AIN4	1																		
			AnalogInput5	6							AINS	5																		
			AnalogInput6	7							AIN	õ																		
			AnalogInput7	8							AIN	7																		
			VDD	9							VDD	,																		

37.11.15 CH[2].PSELN

Address offset: 0x534

Input negative pin selection for CH[2]

-		
Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		АААА
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PSELN		Analog negative input, enables differential channel
	NC	0 Not connected
	AnalogInput0	1 AINO
	AnalogInput1	2 AIN1
	AnalogInput2	3 AIN2
	AnalogInput3	4 AIN3
	AnalogInput4	5 AIN4
	AnalogInput5	6 AIN5
	AnalogInput6	7 AIN6
	AnalogInput7	8 AIN7



Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A
Reset 0x00000000		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
ld RW Field	Value Id	Value	Description
	VDD	9	VDD

37.11.16 CH[2].CONFIG

Address offset: 0x538

Input configuration for CH[2]

	numbe	er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				G	G FEEE D CCC BB A
Res	et 0x0	00020000		0 0 0 0 0 0 0	0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	RESP			Positive channel resistor control
			Bypass	0	Bypass resistor ladder
			Pulldown	1	Pull-down to GND
			Pullup	2	Pull-up to VDD
			VDD1_2	3	Set input at VDD/2
В	RW	RESN			Negative channel resistor control
			Bypass	0	Bypass resistor ladder
			Pulldown	1	Pull-down to GND
			Pullup	2	Pull-up to VDD
			VDD1_2	3	Set input at VDD/2
С	RW	GAIN			Gain control
			Gain1_6	0	1/6
			Gain1_5	1	1/5
			Gain1_4	2	1/4
			Gain1_3	3	1/3
			Gain1_2	4	1/2
			Gain1	5	1
			Gain2	6	2
			Gain4	7	4
D	RW	REFSEL			Reference control
			Internal	0	Internal reference (0.6 V)
			VDD1_4	1	VDD/4 as reference
E	RW	TACQ			Acquisition time, the time the ADC uses to sample the input
					voltage
			3us	0	3 us
			5us	1	5 us
			10us	2	10 us
			15us	3	15 us
			20us	4	20 us
			40us	5	40 us
F	RW	MODE			Enable differential mode
			SE	0	Single ended, PSELN will be ignored, negative input to ADC
					shorted to GND
			Diff	1	Differential
G	RW	BURST			Enable burst mode
			Disabled	0	Burst mode is disabled (normal operation)
			Enabled	1	Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
					samples as fast as it can, and sends the average to Data RAM.

37.11.17 CH[2].LIMIT

Address offset: 0x53C

High/low limits for event monitoring a channel



Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	.8 1	7 1	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				В	В	В	В	В	В	В	В	В	В	В	ВЕ	3 E	ВВ	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Δ,	А А
Res	et 0x7	'FFF8000		0	1	1	1	1	1	1	1	1	1	1	1 1	1 :	1 1	. 1	1	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	LOW		[-3	3276	58 t	to +	327	67]			Lov	v lev	el l	imit																		
В	RW	HIGH		[-3	3276	58 t	to +	327	67]			Hig	h le	vel	limit																		

37.11.18 CH[3].PSELP

Address offset: 0x540

Input positive pin selection for CH[3]

Bit r	numbe	er		31	30 2	29 2	28 2	7 26	5 25	24	23 22	2 21 :	20	19 1	L8 1	7 1	6 1	5 14	13	12	11	10	9	8	7	6	5 4 A	J	2 . A	1 A	
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						Desci	riptio	n																		
Α	RW	PSELP									Analo	og po	siti	ve ir	npu	t ch	ann	el													
			NC	0							Not c	onne	cte	d																	
			AnalogInput0	1							AIN0																				
			AnalogInput1	2							AIN1																				
			AnalogInput2	3							AIN2																				
			AnalogInput3	4							AIN3																				
			AnalogInput4	5							AIN4																				
			AnalogInput5	6							AIN5																				
			AnalogInput6	7							AIN6																				
			AnalogInput7	8							AIN7																				
			VDD	9							VDD																				

37.11.19 CH[3].PSELN

Address offset: 0x544

Input negative pin selection for CH[3]

Bit number	31 30 29 2	28 27 26 25 24 23 22 21 2	0 19 18 17 16 15 14 13	3 12 11 10 9 8 7	6 5 4 3 2 1 0
Id					$A \ A \ A \ A \ A \ A$
Reset 0x00000000	0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description	1		
A RW PSELN		Analog neg	ative input, enables diff	ferential channel	
NC	0	Not connec	cted		
AnalogIı	nput0 1	AIN0			
AnalogIı	nput1 2	AIN1			
AnalogI	nput2 3	AIN2			
AnalogIı	nput3 4	AIN3			
AnalogIı	nput4 5	AIN4			
AnalogIı	nput5 6	AIN5			
AnalogIı	nput6 7	AIN6			
Analogli	nput7 8	AIN7			
VDD	9	VDD			

37.11.20 CH[3].CONFIG

Address offset: 0x548

Input configuration for CH[3]

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		G FEEE D CCC BB AA
Reset 0x00020000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
ld RW Field	Value Id	Value Description
Δ RW RESP		Positive channel resistor control



Bit number		31 30 2	9 28	27 2	26 25	24	23 22	2 21	20 :	19 1	.8 17	16	5 15	14 1	13 12	2 11	10	9	8 7	6	5	4	3	2 1	0
Id						G			F	ı	ΕЕ	Ε			D		С	С	С		В	В		Д	A
Reset 0x00020000		0 0	0 0	0	0 0	0	0 0	0 0	0	0 (0 1	0	0	0	0 0	0	0	0	0 0	0	0	0	0	0 0	0
ld RW Field Va	alue Id	Value					Desc	riptic	on																
Ву	/pass	0					Вура	iss re	sisto	or la	dder														
Pu	ılldown	1					Pull-c	down	ı to	GNE)														
Pu	ıllup	2					Pull-ı	up to	VD	D															
VD	DD1_2	3				:	Set ir	nput	at V	DD/	2														
B RW RESN							Nega	ative (char	nnel	resis	sto	r cor	itrol											
Ву	pass	0					Вура	iss re	sisto	or la	dder														
Pu	ılldown	1					Pull-d	down	ı to	GNE)														
Pu	ıllup	2					Pull-ı	up to	VD	D															
VD	DD1_2	3				:	Set ir	nput	at V	DD/	2														
C RW GAIN							Gain	cont	rol																
Ga	ain1_6	0					1/6																		
Ga	ain1_5	1					1/5																		
Ga	ain1_4	2					1/4																		
Ga	ain1_3	3					1/3																		
Ga	ain1_2	4					1/2																		
Ga	ain1	5					1																		
Ga	ain2	6					2																		
Ga	ain4	7					4																		
D RW REFSEL							Refe	rence	e coi	ntro	I														
Int	ternal	0					Inter	nal re	efer	ence	e (0.6	5 V)												
VD	DD1_4	1				,	VDD/	/4 as	refe	eren	ce														
E RW TACQ							Acqu	uisitio	n tii	me,	the t	tim	e the	AD	C us	es to	san	nple	the	inp	out				
						,	volta	age																	
3u	IS	0					3 us																		
5u	IS	1					5 us																		
10)us	2					10 us	S																	
15	ius	3					15 us	S																	
20)us	4					20 us	S																	
40)us	5					40 us	S																	
F RW MODE							Enab	ole dif	ffere	entia	al mo	de													
SE		0				:	Single	e enc	ded,	PSE	LN v	vill	be ig	nor	ed, n	ega	tive	inpu	ıt to	ΑD	С				
						:	short	ted to	o GN	ND															
Dif	ff	1					Diffe	renti	al																
G RW BURST							Enab	ole bu	ırstı	mod	le														
Dis	sabled	0					Burst	t mod	de is	dis	abled	d (r	orm	al o	pera	tion)								
En	nabled	1					Burst	t mod	de is	ena	abled	1. S	AAD	C tal	kes 2	^0\	/ERS	AM	PLE r	nur	nber	of			
						:	samp	ples a	s fa	st as	s it ca	an,	and	sen	ds th	e av	erag	e to	Dat	a R	AM.				

37.11.21 CH[3].LIMIT

Address offset: 0x54C

High/low limits for event monitoring a channel

Bit r	umber		31	30	29	28	27	26	25	24	23	22 2	1 2	0 19	18	17	16	15	14	13	12	11 1	.0 9	9	8	7	6	5	4	3 2	1	. 0
Id			В	В	В	В	В	В	В	В	В	ВЕ	3 E	3 B	В	В	В	Α	Α	Α	Α	A	Δ ,	Α.	Α	Α	Α	Α	Α	A A	A	А
Res	et 0x7FFF8000		0	1	1	1	1	1	1	1	1	1 1	L 1	۱ 1	1	1	1	1	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0
1.1																																
ıa	RW Field	Value Id	Va	llue							Des	crip	tior	1																		
A	RW Field RW LOW	Value Id				to +	327	767]				crip lev																				

37.11.22 CH[4].PSELP

Address offset: 0x550

Input positive pin selection for CH[4]



Bit number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			АААА
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW PSELP			Analog positive input channel
	NC	0	Not connected
	AnalogInput0	1	AIN0
	AnalogInput1	2	AIN1
	AnalogInput2	3	AIN2
	AnalogInput3	4	AIN3
	AnalogInput4	5	AIN4
	AnalogInput5	6	AIN5
	AnalogInput6	7	AIN6
	AnalogInput7	8	AIN7
	VDD	9	VDD

37.11.23 CH[4].PSELN

Address offset: 0x554

Input negative pin selection for CH[4]

Bit r	numbe	er		31	30 2	29 :	28 2	7 2	6 25	5 24	23 2	22 2	21 20	19	9 18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	,	 3 2	_	0
	et 0x0	000000		0	0	0	0 0) (0 0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0		A A O O		A 0
Id	RW	Field	Value Id	Va	lue						Des	crip	tion																	
Α	RW	PSELN									Ana	alog	nega	tiv	e in	put,	en	able	es d	iffer	ent	al cl	nanr	nel						
			NC	0							Not	cor	nect	ed																
			AnalogInput0	1							AIN	10																		
			AnalogInput1	2							AIN	11																		
			AnalogInput2	3							AIN	12																		
			AnalogInput3	4							AIN	13																		
			AnalogInput4	5							AIN	14																		
			AnalogInput5	6							AIN:	15																		
			AnalogInput6	7							AIN	16																		
			AnalogInput7	8							AIN	17																		
			VDD	9							VDD	D																		

37.11.24 CH[4].CONFIG

Address offset: 0x558

Input configuration for CH[4]

Bit	numbe	er		31	30 2	9 2	28 2	7 2	6 25	24	23 2	22 2	1 20	19	18	17	16	15	14 :	13 1	2 11	10	9	8	7	6	5	4 3	2	1)
Id										G			F		Ε	Ε	Ε			[)	С	С	С			В	В		Α .	Δ
Res	et 0x0	0020000		0	0 ()	0 0) (0 0	0	0	0 0	0	0	0	1	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	o
Id	RW	Field	Value Id	Va	lue						Des	cript	ion																		ı
Α	RW	RESP									Posi	tive	chai	nne	l re	sist	or c	ont	rol												Ī
			Bypass	0							Вура	ass r	esis	tor I	ado	der															
			Pulldown	1							Pull-	-dov	n to	G۱	ID																
			Pullup	2							Pull-	up t	o VI	DD																	
			VDD1_2	3							Set i	inpu	t at	VDE)/2																
В	RW	RESN									Neg	ative	e cha	anne	el re	esis	tor	cor	trol												
			Bypass	0							Вура	ass r	esis	tor I	ado	der															
			Pulldown	1							Pull-	-dov	n to	GN	ID																
			Pullup	2							Pull-	-up t	o VI	DD																	
			VDD1_2	3							Set i	inpu	t at	VDE)/2																
С	RW	GAIN									Gair	cor	ntrol																		
			Gain1_6	0							1/6																				
			Gain1_5	1							1/5																				



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		G F E E E D C C C B B A
Reset 0x00020000		$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value Description
	Gain1_4	2 1/4
	Gain1_3	3 1/3
	Gain1_2	4 1/2
	Gain1	5 1
	Gain2	6 2
	Gain4	7 4
D RW REFSEL		Reference control
	Internal	0 Internal reference (0.6 V)
	VDD1_4	1 VDD/4 as reference
E RW TACQ		Acquisition time, the time the ADC uses to sample the input
		voltage
	3us	0 3 us
	5us	1 5 us
	10us	2 10 us
	15us	3 15 us
	20us	4 20 us
	40us	5 40 us
F RW MODE		Enable differential mode
	SE	O Single ended, PSELN will be ignored, negative input to ADC
		shorted to GND
	Diff	1 Differential
G RW BURST		Enable burst mode
	Disabled	0 Burst mode is disabled (normal operation)
	Enabled	1 Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
		samples as fast as it can, and sends the average to Data RAM.

37.11.25 CH[4].LIMIT

Address offset: 0x55C

High/low limits for event monitoring a channel

Bit number	31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	B B B B B B	B B B B B B B B A A A A A A
Reset 0x7FFF8000	0 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
A RW LOW	[-32768 to +32767]	Low level limit
B RW HIGH	[-32768 to +32767]	High level limit

37.11.26 CH[5].PSELP

Address offset: 0x560

Input positive pin selection for CH[5]

Bit number	31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A
Reset 0x00000000	0 0 0 0 0 0 0	
Id RW Field Value Id	Value	Description
A RW PSELP		Analog positive input channel
NC	0	Not connected
AnalogInput0	1	AIN0
AnalogInput1	2	AIN1
AnalogInput2	3	AIN2
AnalogInput3	4	AIN3
AnalogInput4	5	AIN4
AnalogInput5	6	AIN5



Bit number		31 3	30 2	9 28	3 27	26	25	24	23 :	22 2	21 2	0 1	9 1	8 17	7 16	15	14	13	12	11 1	9	8	7	6	5	4	3	2 1	1 0
Id																										Α	Α	A A	A A
Reset 0x00000000		0	0 (0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
ld RW Field	Value Id	Valu	ıe						Des	crip	tio	n																	
	AnalogInput6	7							AIN	6																			
	AnalogInput7	8							AIN	7																			
	VDD	9							VDE)																			

37.11.27 CH[5].PSELN

Address offset: 0x564

Input negative pin selection for CH[5]

Bit	numb	per		31	30 2	9 2	28 2	7 2	26 25	5 24	4 23	3 22	21 2	0 1	19 1	8 1	7 1	6 1	5 14	4 13	3 12	11	10	9	8	7	6 !	5 4	3	2	1	0
Id																												Δ	A	Α	Α	Α
Res	et 0x	00000000		0	0	0	0 (0	0 0	0	0	0	0 (0	0 (0 (0) (0	0	0	0	0	0	0	0	0 (0	0	0	0	0
Id	RW	/ Field	Value Id	Va	lue						De	escri	ptio	n																		
Α	RW	/ PSELN									Ar	nalo	g neg	ati	ve i	npu	ıt, e	nat	oles	diff	ere	ntia	l cha	ann	el							
			NC	0							No	ot co	nne	cte	d																	
			AnalogInput0	1							ΑI	N0																				
			AnalogInput1	2							ΑI	N1																				
			AnalogInput2	3							ΑI	N2																				
			AnalogInput3	4							ΑI	N3																				
			AnalogInput4	5							ΑI	N4																				
			AnalogInput5	6							ΑI	N5																				
			AnalogInput6	7							ΑI	N6																				
			AnalogInput7	8							ΑI	N7																				
			VDD	9							VI	DD																				

37.11.28 CH[5].CONFIG

Address offset: 0x568

Input configuration for CH[5]

Bit number			24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			G FEEE D C C C B B A A
Reset 0x00020000			0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW RESP			Positive channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
B RW RESN			Negative channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
C RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
	Gain4	7	4
D RW REFSEL			Reference control
	Internal	0	Internal reference (0.6 V)



Bitı	numbe	er		31	30 2	29 2	8 2	7 20	6 25	5 24	23 2	2 2	1 20	19	18	17	16	15 1	14 1	3 12	2 11	. 10	9	8	7	5 5	4	3	2	1 0
Id										G			F		Ε	Ε	Е			D)	С	С	С		В	В		,	А А
Res	et 0x0	00020000		0	0	0 (0 0	0	0	0	0	0 0	0	0	0	1	0	0	0 (0	0	0	0	0	0	0 0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						Des	cript	ion																	
			VDD1_4	1							VDD	/4 a	s ref	fere	nce	:														
Ε	RW	TACQ									Acq	uisiti	ion t	ime	e, th	e ti	me	the	AD	C us	es t	o sa	mpl	e th	e in	put				
											volta	age																		
			3us	0							3 us																			
			5us	1							5 us																			
			10us	2							10 u	S																		
			15us	3							15 u	S																		
			20us	4							20 u	S																		
			40us	5							40 u	S																		
F	RW	MODE									Enal	ole d	liffer	ent	tial ı	mod	de													
			SE	0							Sing	le er	nded	l, PS	SELN	N W	ill be	e igi	nore	ed, n	ega	tive	inp	ut to	ıA c	OC				
											shor	ted	to G	ND																
			Diff	1							Diffe	eren	tial																	
G	RW	BURST									Enal	ole b	urst	mo	ode															
			Disabled	0							Burs	t mo	ode i	is d	isab	led	(no	rma	al op	era	tion)								
			Enabled	1							Burs	t mo	ode i	is e	nab	led.	SA	ADC	tak	es 2	2^0	VER:	SAN	IPLE	nu	mbe	r of			
											sam	ples	as f	ast	as it	t ca	n, a	nd s	enc	ls th	e av	/era	ge t	o Da	ita I	RAN	1.			

37.11.29 CH[5].LIMIT

Address offset: 0x56C

High/low limits for event monitoring a channel

Bit r	iumbe	er		31	. 30	29	28	27	26	25	24	23 2	22 21	20	19	18	17 :	l6 1	5 1	4 13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				В	В	В	В	В	В	В	В	В	ВВ	В	В	В	В	ВА	4 /	4 A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α	Α
Res	et Ox7	7FFF8000		0	1	1	1	1	1	1	1	1	1 1	1	1	1	1	1 1	1 (0 0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Doc	cript	ion																		
		riciu	value la	•••	iiuc							Desi	cript	IUII																		
Α	RW		value la				0 +3	327	'67]				leve		nit																	

37.11.30 CH[6].PSELP

Address offset: 0x570

Input positive pin selection for CH[6]

Bit number		31 3	0 29	9 28	27	26 2	!5 24	4 2:	3 22	21	20 :	19 1	L8 1	7 1	6 1!	5 14	1 13	3 12	11	10	9	8	7 6	5 5		2 2	1 0 A A
Reset 0x00000000		0 (0 0	0	0	0 (0 0) (0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0			0 0
Id RW Field	Value Id	Valu	e					D	escr	iptic	n																
A RW PSELP								Α	nalo	g po	sitiv	ve ir	npu	t ch	ann	el											
I	NC	0						Ν	ot c	onne	cte	d															
	AnalogInput0	1						Α	IN0																		
	AnalogInput1	2						Α	IN1																		
	AnalogInput2	3						Α	IN2																		
	AnalogInput3	4						Α	IN3																		
	AnalogInput4	5						Α	IN4																		
	AnalogInput5	6						Α	IN5																		
	AnalogInput6	7						Α	IN6																		
	AnalogInput7	8						Α	IN7																		
,	VDD	9						٧	DD																		

37.11.31 CH[6].PSELN

Address offset: 0x574

Input negative pin selection for CH[6]



Bitı	numb	er		31	30 2	29 2	28 2	7 2	26 25	24	23 2	22 21	1 20	19	18	17	16	15	14 :	l3 1	2 13	10	9	8	7	6	5	4	3 2	1	0
Id																												A	4 Δ	A	Α
Res	et 0x0	0000000		0	0	0	0 () (0 0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						Des	cript	ion																		
Α	RW	PSELN									Ana	log n	nega	tive	inp	ut,	ena	able	s di	ffer	enti	al ch	anr	ıel							
			NC	0							Not	coni	nect	ed																	
			AnalogInput0	1							AIN)																			
			AnalogInput1	2							AIN:	1																			
			AnalogInput2	3							AIN	2																			
			AnalogInput3	4							AIN:	3																			
			AnalogInput4	5							AIN	4																			
			AnalogInput5	6							AINS	5																			
			AnalogInput6	7							AIN	5																			
			AnalogInput7	8							AIN	7																			
			VDD	9							VDD)																			

37.11.32 CH[6].CONFIG

Address offset: 0x578

Input configuration for CH[6]

Bit	numbe	er		31	30 2	9 28	27	26	25 2	4 23	3 22 2	21 2	0 19	9 18	3 17	16	15	14	13	12	11	10	9	8	7	6	5 4	4 3	3 2	1	0
Id									(à		F	=	Ε	Ε	Ε				D		С	С	С			В	В		Α	Α
Res	et 0x0	0020000		0	0 0	0	0	0	0 (0	0 0	0 0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0
Id	RW	Field	Value Id	Val	ue					D	escrip	tion	1																		
Α	RW	RESP								Po	ositive	e cha	ann	el re	esist	or o	con	trol													
			Bypass	0						В	ypass	resi	stor	r lad	lder																
			Pulldown	1						Pi	ull-do	wn t	to G	ND																	
			Pullup	2						Pi	ull-up	to V	/DD																		
			VDD1_2	3						Se	et inpi	ut at	t VD	D/2	2																
В	RW	RESN								N	legativ	e ch	nanı	nel ı	resis	tor	100	ntro	ol												
			Bypass	0						В	ypass	resi	stor	r lad	lder																
			Pulldown	1						Pi	ull-do	wn t	to G	ND																	
			Pullup	2						Pi	ull-up	to V	/DD																		
			VDD1_2	3						Se	et inpi	ut at	t VD	D/2	2																
С	RW	GAIN								G	ain co	ntro	ol																		
			Gain1_6	0						1,	/6																				
			Gain1_5	1						1,	/5																				
			Gain1_4	2						1,	/4																				
			Gain1_3	3						1,	/3																				
			Gain1_2	4						1,	/2																				
			Gain1	5						1																					
			Gain2	6						2																					
			Gain4	7						4																					
D	RW	REFSEL								R	eferer	nce o	cont	trol																	
			Internal	0						In	nterna	l ref	ere	nce	(0.6	(V															
			VDD1_4	1						V	DD/4	as re	efer	enc	e																
Е	RW	TACQ								A	cquisi	tion	tim	ie, t	he t	ime	e th	e Al	DC	use	s to	saı	mpl	e th	e ir	put	t				
										V	oltage																				
			3us	0						3	us																				
			5us	1						5	us																				
			10us	2						10	0 us																				
			15us	3						15	5 us																				
			20us	4						20	0 us																				
			40us	5						40	0 us																				
F	RW	MODE								Er	nable	diffe	erer	ntial	mo	de															
			SE	0						Si	ingle e	ende	ed, F	PSEL	N w	/ill k	oe ię	gno	red	, ne	egat	tive	inp	ut t	o A	DC					
										sł	horted	l to	GNI	D																	
			Diff	1						D	ifferei	ntial																			



Bit	nur	nbe	r		3:	1 30	29	9 28	8 27	7 26	25	24	1 23	3 22	21	20	19	18	17	16	15	14	13	12 1	11 1	LO	9	8	7	6	5	4	3	2	1 (0
Id												G				F		Ε	Ε	Ε				D		С	С	С			В	В		,	Δ ,	Α
Re	set (0x0	0020000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0
Id	R	RW	Field	Value Id	V	alue	:						D	escr	pti	on																				
G	R	RW	BURST										Er	nabl	e bu	ırst	mo	de																		7
				Disabled	0								Вι	urst	mo	de i	s di	sab	led	(no	orm	al o	per	atic	n)											
				Enabled	1								Вι	urst	mo	de i	s er	nab	led	. SA	AD	C ta	kes	2^(OVE	RSA	٩M	PLE	nu	mb	er	of				
													sa	ampl	es a	s fa	ast a	as it	ca	n, a	ınd	sen	ds t	he i	ave	rag	e to	o Da	ita	RAI	M.					

37.11.33 CH[6].LIMIT

Address offset: 0x57C

High/low limits for event monitoring a channel

Bit r	nur	nbe	r		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2 :	1 0
Id					В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۱ ۸	А А
Res	et (0x7	FFF8000		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	R	RW	Field	Value Id	Va	alue	:						De	scri	ptic	on																			
Α	R	RW	LOW		[-3	327	68 t	to +	327	767]			Lov	v le	vel	lim	it																		
В	R	RW	HIGH		[-3	327	68 1	to +	327	767]			Hig	h le	evel	lim	it																		

37.11.34 CH[7].PSELP

Address offset: 0x580

Input positive pin selection for CH[7]

Bit nu	umbe	r		31	30 2	29	28 2	27 :	26 2	5 2	24 2	23 22	21	20	19	18	17	16	15	14	13 :	12 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																													A	Д Д	Α.	Α
Rese	t 0x0	0000000		0	0	0	0	0	0)	0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						ı	Desci	iptio	on																		
Α	RW	PSELP									,	Analo	g po	siti	ve i	npı	ıt c	har	nne	I												
			NC	0							ı	Not c	onn	ecte	ed																	
			AnalogInput0	1							,	AIN0																				
			AnalogInput1	2							,	AIN1																				
			AnalogInput2	3							,	AIN2																				
			AnalogInput3	4							,	AIN3																				
			AnalogInput4	5							,	AIN4																				
			AnalogInput5	6							,	AIN5																				
			AnalogInput6	7							,	AIN6																				
			AnalogInput7	8							,	AIN7																				
			VDD	9							١	VDD																				

37.11.35 CH[7].PSELN

Address offset: 0x584

Input negative pin selection for CH[7]

	31	30 2	29 2	8 27	26	25 2	24 2	23 2:	2 21	L 20	19	18	17 1	16 1	5 14	1 13	12	11 1	.0 9	8	7	6	5	4 3	2	1	0
																								A A	Α	Α	Α
00	0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0 0	0	0	0
Value Id	Va	lue					ı	Desc	ript	ion																	
							,	Anal	og n	ega	tive	inp	ut, e	enab	oles	diffe	eren	tial	char	nnel							
NC	0						ı	Not o	conr	nect	ed																
AnalogInput0	1						,	AIN0)																		
AnalogInput1	2						,	AIN1																			
AnalogInput2	3						,	AIN2	!																		
AnalogInput3	4						,	AIN3																			
AnalogInput4	5						,	AIN4	ļ																		
AnalogInput5	6						,	AIN5	,																		
	N NC AnalogInput0 AnalogInput1 AnalogInput2 AnalogInput3 AnalogInput4	NOO Value Id Va NOO	N NC 0 AnalogInput0 1 AnalogInput2 3 AnalogInput3 4 AnalogInput4 5	N NC 0 AnalogInput0 1 AnalogInput1 2 AnalogInput2 3 AnalogInput3 4 AnalogInput4 5	N NC O AnalogInput0 1 AnalogInput1 2 AnalogInput2 3 AnalogInput3 4 AnalogInput4 5	N Value Id Value N NC 0 AnalogInput0 1 AnalogInput1 2 AnalogInput2 3 AnalogInput3 4 AnalogInput4 5	N	N	Value Id Value Value Description N Analoginput0 1 Analoginput1 Analoginput2 Analoginput2 Analoginput3 Analoginput3 Analoginput4 Analo	Value Id	Value Id Value Description N Analog negation Analog negation NC 0 Not connect AnalogInput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput2 3 AIN2 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4	Value Id Value Description N Analog negative NC 0 Not connected AnalogInput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput2 3 AIN2 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4	Value Id Value Description N Analog negative inp NC 0 Not connected AnalogInput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput2 3 AIN2 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4	Value Id	No No No No No No No No	Value Id	NC	Value Id Value Description NC 0 Not connected AnalogInput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput2 3 AIN2 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4	NC	Value Id Value Description Analog negative input, enables differential chart NC 0 Not connected AnalogInput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput2 3 AIN2 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4	Value Id Value Description Analog negative input, enables differential channel NC 0 Not connected AnalogInput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput2 3 AIN2 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4	Value Id Value	No value Id	Value Id Val	No	NOC Value Id Value NOC 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	NOC Value Id Value Representation of the control of



Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ААААА
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	AnalogInput6	7	AIN6
	AnalogInput7	8	AIN7
	VDD	9	VDD

37.11.36 CH[7].CONFIG

Address offset: 0x588

Input configuration for CH[7]

		er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld				C	FEEE DCCC BB A
Res	et 0x0	0020000		0 0 0 0 0 0 0	0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
A	RW	RESP			Positive channel resistor control
			Bypass	0	Bypass resistor ladder
			Pulldown	1	Pull-down to GND
			Pullup	2	Pull-up to VDD
			VDD1_2	3	Set input at VDD/2
В	RW	RESN			Negative channel resistor control
			Bypass	0	Bypass resistor ladder
			Pulldown	1	Pull-down to GND
			Pullup	2	Pull-up to VDD
			VDD1_2	3	Set input at VDD/2
С	RW	GAIN			Gain control
			Gain1_6	0	1/6
			Gain1_5	1	1/5
			Gain1_4	2	1/4
			Gain1_3	3	1/3
			Gain1_2	4	1/2
			Gain1	5	1
			Gain2	6	2
			Gain4	7	4
D	RW	REFSEL			Reference control
			Internal	0	Internal reference (0.6 V)
			VDD1_4	1	VDD/4 as reference
E	RW	TACQ			Acquisition time, the time the ADC uses to sample the input
					voltage
			3us	0	3 us
			5us	1	5 us
			10us	2	10 us
			15us	3	15 us
			20us	4	20 us
			40us	5	40 us
F	RW	MODE			Enable differential mode
			SE	0	Single ended, PSELN will be ignored, negative input to ADC
					shorted to GND
			Diff	1	Differential
G	RW	BURST			Enable burst mode
			Disabled	0	Burst mode is disabled (normal operation)
			Enabled	1	Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
					samples as fast as it can, and sends the average to Data RAM.

37.11.37 CH[7].LIMIT

Address offset: 0x58C



High/low limits for event monitoring a channel

Bit r	numb	er			31	1 30	29	28	3 27	7 26	25	24	23	22	21 :	20 1	19 1	8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4 3	2	1	0
Id					В	В	В	В	В	В	В	В	В	В	В	В	В	В	3 E	S A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A A	A	Α	Α
Res	et Ox	7F	FF8000		0	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	<i> </i>	Field	Value Id	Va	alue							De	scri	ptio	n																		
Α	RW	/	LOW		[-3	3276	68 t	to +	327	767]	ı		Lov	w le	vel	imi	t																	_
В	RW	/	HIGH		[-3	3276	58 t	to +	327	767]	1		Hig	gh le	evel	lim	it																	

37.11.38 RESOLUTION

Address offset: 0x5F0 Resolution configuration

Bitı	number			31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9 8	3 7	6	5	4	3	2	1 0
Id																																Α	А А
Res	et 0x00	000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 1
Id	RW	Field	Value Id	Va	alue							De	scri	pti	on																		
Α	RW	VAL										Set	th	e re	esol	utio	on																
			8bit	0								8 b	it																				
			10bit	1								10	bit																				
			12bit	2								12	bit																				
			14bit	3								14	bit																				

37.11.39 OVERSAMPLE

Address offset: 0x5F4

Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.

Bit r	numbe	er		31	. 30	29	28 2	27 2	26 2	5 24	1 23	3 22	21 2	20 2	19 1	8 1	7 16	5 15	14 1	3 1	2 11	10	9	8	7	6	5 4	3	2	1 0
Id																												Α	Α	A A
Rese	et 0x0	0000000		0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0 0
Id	RW	Field	Value Id	Va	alue						D	escri	ptio	n																
Α	RW	OVERSAMPLE									0	vers	amp	le c	onti	rol														
			Bypass	0							В	ypas	s ove	ersa	mp	ling														
			Over2x	1							0	vers	ampl	le 2	X															
			Over4x	2							0	vers	ampl	le 4	Х															
			Over8x	3							0	vers	ampl	le 8	x															
			Over16x	4							0	vers	ampl	le 1	.6x															
			Over32x	5							0	vers	ampl	le 3	2x															
			Over64x	6							0	vers	ampl	le 6	4x															
			Over128x	7							0	vers	amp	le 1	.28x															
			Over256x	8							0	vers	ampl	le 2	56x															

37.11.40 SAMPLERATE

Address offset: 0x5F8

Controls normal or continuous sample rate

Bit r	iumbe	er		31 30 29 28 27 26	25 24	4 23	22 2	1 20	19	18 1	7 16	15 :	14 1	3 12	11 10	9	8	7	6	5	4	3 2	1	0
Id														В	Δ	. A	Α	Α	Α	Α	Α /	A А	Α	Α
Res	et 0x0	0000000		0 0 0 0 0 0	0 0	0	0 0	0	0	0 (0 0	0	0 0	0	0 0	0	0	0	0	0	0 (0 0	0	0
Id	RW	Field	Value Id	Value		De	escript	tion																
Α	RW	CC		[802047]		Ca	pture	and	con	npar	e val	ue. S	amp	le rat	e is :	16 N	1Hz/	'CC						
В	RW	MODE				Se	lect m	ode	for	sam	ple ra	ate c	ontr	ol										
			Task	0	Rate is controlled from SAMPLE task																			
			Timers	1	Rate is controlled from local timer (use CC to control the rate)																			



37.11.41 RESULT.PTR

Address offset: 0x62C

Data pointer

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 1	16 1	.5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	۱ ۸	λ Δ	. 4	А	Α	Α	Α	Α	Α	Α	Α .	Δ.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	PTR		Data pointer																													

37.11.42 RESULT.MAXCNT

Address offset: 0x630

Maximum number of buffer words to transfer

Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0			
Id				A A A A A	. A A A A A A A			
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0			
Id RW Field	Value Id	Value	Description					
A RW MAXCNT Maximum number of buffer words to transfer								

37.11.43 RESULT.AMOUNT

Address offset: 0x634

Number of buffer words transferred since last START

Bit	numbe	er		31	30	29	28 2	27 2	6 2	5 2	4 23	3 22	2 21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2 :	1 ()
Id																				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۱ ۸	4 4	
Res	et 0x0	0000000		0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 ()
Id	RW	Field	Value Id	Va	lue						D	esci	ripti	on																				
Α	R	AMOUNT	NT Number of buffer words transferred since last START. This							7																								

register can be read after an END or STOPPED event.

37.12 Electrical specification

37.12.1 SAADC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
DNL	Differential non-linearity, 10-bit resolution	-0.95	<1		LSB
INL	Integral non-linearity, 10-bit resolution		1		LSB
V _{OS}	Differential offset error (calibrated), 10-bit resolution ^a		+-2		LSB
C _{EG}	Gain error temperature coefficient		0.02		%/∘C
f _{SAMPLE}	Maximum sampling rate			200	kHz
t _{ACQ,10k}	Acquisition time (configurable), source Resistance <= 10kOhm		3		μs
t _{ACQ,40k}	Acquisition time (configurable), source Resistance <= 40kOhm		5		μs
t _{ACQ,100k}	Acquisition time (configurable), source Resistance <= 100kOhm		10		μs
t _{ACQ,200k}	Acquisition time (configurable), source Resistance <= 200kOhm		15		μs
t _{ACQ,400k}	Acquisition time (configurable), source Resistance <= 400kOhm		20		μs
t _{ACQ,800k}	Acquisition time (configurable), source Resistance <= 800kOhm		40		μs
t _{CONV}	Conversion time		<2		μs
I _{ADC,CONV}	ADC current during ACQuisition and CONVersion		700		μΑ
I _{ADC,IDLE}	Idle current, when not sampling, excluding clock sources and		<5		μΑ
	regulator base currents ³³				
	regulator base currents ³³				

^a Digital output code at zero volt differential input.

When t_{ACQ} is 10us or longer, and if DC/DC is active, it will be allowed to work in refresh mode if no other resource is requiring a high quality power supply from 1V3. If t_{ACQ} is smaller than 10us and DC/DC is active,



Symbol	Description	Min.	Тур.	Max.	Units
E _{G1/6}	Error ^b for Gain = 1/6	-3		3	%
E _{G1/4}	Error ^b for Gain = 1/4	-3		3	%
E _{G1/2}	Error ^b for Gain = 1/2	-3		4	%
E _{G1}	Error ^b for Gain = 1	-3		4	%
C _{SAMPLE}	Sample and hold capacitance at maximum gain ³⁴		2.5		pF
R _{INPUT}	Input resistance		>1		ΜΩ
E _{NOB}	Effective number of bits, differential mode, 12-bit resolution,		9		Bit
	1/1 gain, 3 μs acquisition time, crystal HFCLK, 200 ksps				
S _{NDR}	Peak signal to noise and distortion ratio, differential mode, 12-		56		dB
	bit resolution, 1/1 gain, 3 µs acquisition time, crystal HFCLK, 200				
	ksps				
S _{FDR}	Spurious free dynamic range, differential mode, 12-bit		70		dBc
	resolution, 1/1 gain, 3 μs acquisition time, crystal HFCLK, 200				
	ksps				
R _{LADDER}	Ladder resistance		160		kΩ

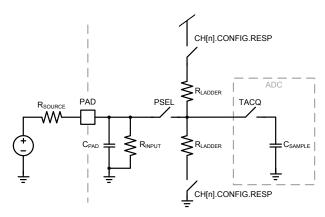


Figure 105: Model of SAADC input (one channel)

Note: SAADC average current calculation for a given application is based on the sample period, conversion and acquisition time (t_{conv} and t_{ACQ}) and conversion and idle current ($t_{ADC,CONV}$). For example, sampling at 4kHz gives a sample period of 250µs. The average current consumption would then be:

$$I_{\mathit{AVERAGE}} = \left(\frac{\left(t_{\mathit{CONV}} + t_{\mathit{ACQ}}\right)}{250}\right) \left(I_{\mathit{ADC},\mathit{CONV}}\right) + \left(\frac{250 - \left(t_{\mathit{CONV}} + t_{\mathit{ACQ}}\right)}{250}\right) \left(I_{\mathit{ADC},\mathit{IDLE}}\right)$$

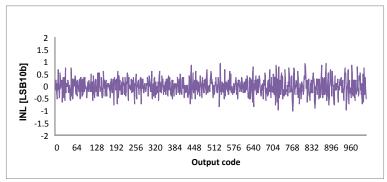


Figure 106: ADC INL vs Output Code

refresh mode will not be allowed, and it will remain in normal mode from the START task to the STOPPED event. So depending on t_{ACO} and other resources' needs, the appropriate base current needs to be taken into account.

^b Does not include temperature drift

³⁴ Maximum gain corresponds to highest capacitance.



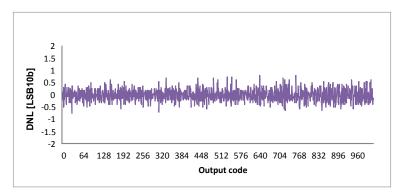


Figure 107: ADC DNL vs Output Code

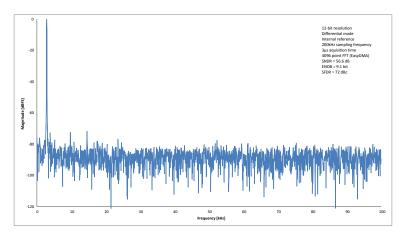


Figure 108: FFT of a 2.8 kHz sine at 200 ksps ()

37.13 Performance factors

Clock jitter, affecting sample timing accuracy, and circuit noise can affect ADC performance.

Jitter can be between START tasks or from START task to acquisition. START timer accuracy and startup times of regulators and references will contribute to variability. Sources of circuit noise may include CPU activity and the DC/DC regulator. Best ADC performance is achieved using START timing based on the TIMER module, HFXO clock source, and Constant Latency mode.



38 COMP — Comparator

The Comparator (COMP) compares the input voltage (VIN+) that is derived from an analog input pin selected via the PSEL register against a second input voltage (VIN-) that can be derived from multiple sources depending on operation mode.

Listed here are the main features for COMP:

- Input range from 0 V to VDD
- Single-ended mode
 - · Fully flexible hysteresis using a 64-level reference ladder
- Differential mode
 - Configurable 50 mV hysteresis
- Reference inputs:
 - VDD
 - External reference from AIN0 to AIN1 (between 0 V and VDD)
 - Internal references 1.2 V, 1.8 V and 2.4 V
- Three operation modes: low power, normal and high-speed
- · Single-pin capacitive sensor support
- Event generation on output changes
 - UP event on VIN- > VIN+
 - DOWN event on VIN- < VIN+
 - CROSS event on VIN+ and VIN- crossing
 - READY event on core and internal reference (if used) ready

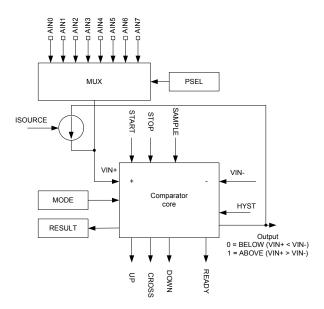


Figure 109: Comparator overview

Important: COMP cannot be used (STARTed) at the same time as LPCOMP. Only one comparator can be used at a time.

The COMP is started by triggering the START task, and stopped by triggering the STOP task. After a start-up time of t_{COMP,START} ³⁵ the COMP will generate a READY event to indicate that the comparator is ready

See t_{PROPDLY,LP}, t_{PROPDLY,N}, t_{PROPDLY,HS}, I_{COMP,LP}, I_{COMP,N} and I_{COMP,HS} in *Electrical parameters* for more information about COMP speed and power characteristics related to these different modes.



to use and the output of the COMP is correct. When the COMP module is started, events will be generated every time VIN+ crosses VIN-.

VIN- can be derived directly from AIN0 or AIN1 in differential mode, or VREF in single-ended mode. VUP and VDOWN thresholds can be set to implement a hysteresis on VIN- using the Reference Ladder. VREF can be derived from VDD, AIN0, AIN1 or internal 1.2V, 1.8V and 2.4V references.

An upward crossing will generate an UP event and a downward crossing will generate a DOWN event. The CROSS event will be generated every time there is a crossing, independent of direction.

An optional hysteresis on VIN+ and VIN- can be enabled when the module is used in differential mode through the HYST register. In single ended mode the two reference ladders (VUP and VDOWN, see *Figure 112: Comparator in single-ended mode* on page 395) will be used instead of the hysteresis mechanism configured in HYST.

This hysteresis is in the order of magnitude of 50 mV, and shall prevent noise on the signal to create unwanted events. See *Figure 113: Hysteresis example where VIN+ starts below VUP* on page 395 for illustration of the effect of an active hysteresis on a noisy input signal.

The COMP can be configured to operate in two main operation modes, differential mode and single-ended mode, see MODE register for more information.

The COMP can, for both main operation modes, operate in different speed and power consumption modes, see MODE register. High-speed mode will consume more power compared to low-power mode, and low-power mode will result in slower response time compared to high-speed mode.

The immediate value of the COMP can be sampled to the RESULT register by triggering the SAMPLE task.

A selectable current can be applied (ISOURCE register) on the currently selected AINx line. Enabling the block creates a feedback path around the comparator, forming a relaxation oscillator. The circuit will sink current from VIN+ when the comparator output is high, and source current into VIN+ when the comparator output is low. The frequency of the oscillator is dependent on the capacitance at the analog input pin, the reference voltages and the value of the current source. In this mode, only a capacitive sensor needs to be attached between the analog input pin and ground. With a selected current of 10 μ A, VUP-VDOWN equal to 1 V, and an external capacity of typically 10 pF, the resulting oscillation frequency is around 500 kHz.

The frequency of the oscillator can be calculated as

```
f OSC = I SOURCE / (2C · (VUP-VDOWN) )
```

38.1 Shared resources

The COMP shares analog resources with the SAADC and LPCOMP peripherals.

While it is possible to use SAADC at the same time as COMP or LPCOMP, COMP and LPCOMP are mutually exclusive: enabling one will automatically disable the other. In addition, when using SAADC and COMP or LPCOMP simultaneously, it is not possible to select the same analog input pin for both modules.

Important: The COMP peripheral shall not be disabled (by writing to the ENABLE register) before the peripheral has stopped. Failing to do so may result in unpredictable behaviour.

38.2 Differential mode

In differential mode, the reference input VIN- is derived directly from one of the AINx pins.

In this mode, the impedance on VIN-'s signal path is equal to the impedance on VIN+'s signal path. See $Z_{COMPVINP}$ and $Z_{COMPVINND}$ for more information. In differential mode, the PSEL, MODE and EXTREFSEL registers must be configured before the COMP is enabled via the ENABLE register. When HYST is turned on while in this mode, the Output of the comparator (and associated events) will change from ABOVE to BELOW whenever VIN+ becomes smaller than (VIN- - ($V_{DIFFHYST}$ / 2)). Similarly, it will change from BELOW to ABOVE whenever VIN+ becomes larger than (VIN- + ($V_{DIFFHYST}$ / 2)), as illustrated in *Figure 111: Hysteresis enabled in differential mode* on page 394.



Restriction: Depending on the device, not all the analog inputs may be available for each MUX.

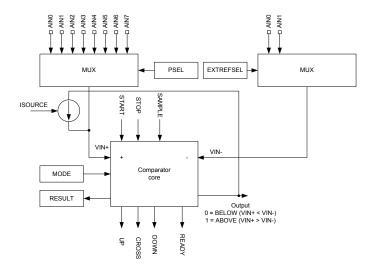


Figure 110: Comparator in differential mode

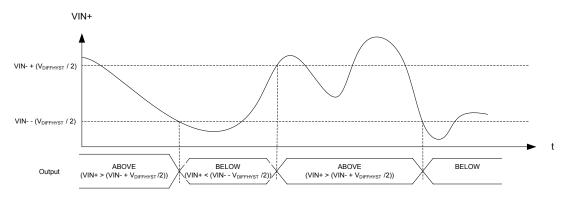


Figure 111: Hysteresis enabled in differential mode

38.3 Single-ended mode

In single-ended mode, VIN- is derived from the Reference Ladder.

The Reference Ladder uses the reference voltage VREF to derive two new voltage references, VUP and VDOWN. VUP and VDOWN are configured via THUP and THDOWN in the TH register. VREF can be sourced from any of the available references sources as illustrated in *Figure 112: Comparator in single-ended mode* on page 395. This is configured via EXTREFSEL and REFSEL.

When the comparator core detects that VIN+ > VIN-, i.e. ABOVE as per the RESULT register, VIN- will switch to VDOWN. When VIN- falls below VIN- again, VIN- will be switched back to VUP. By specifying VUP larger than VDOWN, a hysteresis as illustrated in *Figure 113: Hysteresis example where VIN+ starts below VUP* on page 395 and *Figure 114: Hysteresis example where VIN+ starts above VUP* on page 396 can be generated. In single-ended mode, the PSEL, MODE, EXTREFSEL, REFSEL and TH registers must be configured before the COMP is enabled via the ENABLE register.

Restriction: Depending on the device, not all the analog inputs may be available for each MUX.

Writing to the HYST register has no effect in single-ended mode, and the content of this register is ignored.



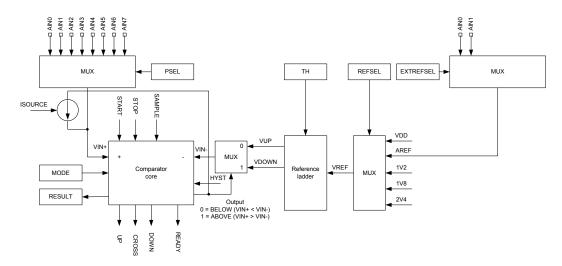


Figure 112: Comparator in single-ended mode

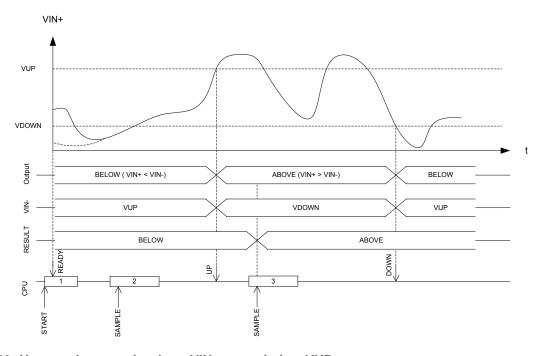


Figure 113: Hysteresis example where VIN+ starts below VUP



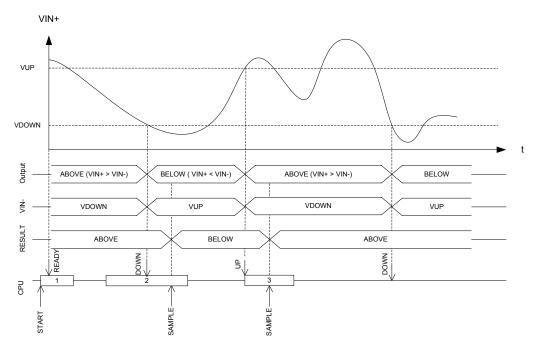


Figure 114: Hysteresis example where VIN+ starts above VUP

38.4 Pin configuration

The user can use the PSEL register to select one of the analog input pins, AINO through AINO, as input VIN +.

See *Figure 112: Comparator in single-ended mode* on page 395. Similarly the user can use the EXTREFSEL register to select one of the AINx analog input pins as reference input, in case AREF is selected in REFSEL. The selected analog pins will be acquired by the COMP when it is enabled via the ENABLE register.

Depending on the device, not all the analog inputs may be available for each MUX. See PSEL and EXTREFSEL register definition for more information about which analog pins are available on a particular device.

38.5 Registers

Table 91: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40013000	COMP	COMP	General purpose comparator	

Table 92: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start comparator
TASKS_STOP	0x004	Stop comparator
TASKS_SAMPLE	0x008	Sample comparator value
EVENTS_READY	0x100	COMP is ready and output is valid
EVENTS_DOWN	0x104	Downward crossing
EVENTS_UP	0x108	Upward crossing
EVENTS_CROSS	0x10C	Downward or upward crossing
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt



Register	Offset	Description
INTENCLR	0x308	Disable interrupt
RESULT	0x400	Compare result
ENABLE	0x500	COMP enable
PSEL	0x504	Pin select
REFSEL	0x508	Reference source select
EXTREFSEL	0x50C	External reference select
TH	0x530	Threshold configuration for hysteresis unit
MODE	0x534	Mode configuration
HYST	0x538	Comparator hysteresis enable
ISOURCE	0x53C	Current source select on analog input

38.5.1 SHORTS

Address offset: 0x200 Shortcut register

•	00	at regioter			
Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	READY_SAMPLE			Shortcut between READY event and SAMPLE task
					See EVENTS_READY and TASKS_SAMPLE
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
В	RW	READY_STOP			Shortcut between READY event and STOP task
					See EVENTS_READY and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
С	RW	DOWN_STOP			Shortcut between DOWN event and STOP task
					See EVENTS_DOWN and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
D	RW	UP_STOP			Shortcut between UP event and STOP task
					See EVENTS_UP and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
Ε	RW	CROSS_STOP			Shortcut between CROSS event and STOP task
					See EVENTS_CROSS and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut

38.5.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bitı	numbe	er		31	. 30	29	28	27	26 2	25	24 :	23 :	22 :	21 2	0 1	9 1	8 1	7 16	5 15	14	13	12	11 1	0 9	8	7	6	5	4	3 2	2 1	L 0
Id																														D (СВ	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 () (0 () (0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0 (
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	otior	1																	
Α	RW	READY									ı	Ena	ble	or d	lisa	ble	inte	erru	pt fo	or R	EAD	Y e	/ent									
											:	See	EV	ENT:	S_ <i>F</i>	REAL	ΟY															
			Disabled	0							ı	Disa	able	:																		
			Enabled	1							ı	Ena	ble																			
В	RW	DOWN									- 1	Ena	ble	or d	lisa	ble	inte	erru	pt fo	or D	OW	'N e	vent									
												See	EV	ENT:	S_E	OV	/N															



Bit r	numbe	er		31	. 30	29	28 2	27 2	26 2	5 24	4 23	3 22	21 2	0 1	9 1	8 1	7 16	15	14	13 :	12 1	1 10	9	8	7	6	5 4	1 3	2	1	0
Id																												D	С	В	Α
Res	et OxC	0000000		0	0	0	0	0	0 0	0	0	0	0 () (0 0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Va	alue						De	escri	ption	า																	
			Disabled	0							Di	isabl	e																		
			Enabled	1							En	nable	e																		
С	RW	UP									En	nable	e or d	lisa	ble	inte	erru	ot fo	or U	P ev	ent										
											Se	ee <i>E\</i>	/ENT	s_L	IP																
			Disabled	0							Di	isabl	e																		
			Enabled	1							En	nable	9																		
D	RW	CROSS									Er	nable	e or d	lisa	ble i	inte	erru	ot fo	or Cl	ROS	S ev	ent									
											Se	ee <i>E</i> V	/ENT	s_c	ROS	SS															
			Disabled	0							Di	isabl	е																		
			Enabled	1							En	nable	9																		

38.5.3 INTENSET

Address offset: 0x304

Enable interrupt

		•			
Bit	numb	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	READY			Write '1' to Enable interrupt for READY event
					See EVENTS_READY
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	DOWN			Write '1' to Enable interrupt for DOWN event
					See EVENTS_DOWN
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	UP			Write '1' to Enable interrupt for UP event
					See EVENTS_UP
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	CROSS			Write '1' to Enable interrupt for CROSS event
					See EVENTS_CROSS
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

38.5.4 INTENCLR

Address offset: 0x308

Disable interrupt

В	it nı	umbe	r	30	29	28	3 2	7 2	6 :	25	24	23	22	21	20	19	9 1	.8 :	17	16	15	14	1 1	3 1	2 1	11 1	.0	9	8	7	6	5	4	3	2	1 ()		
lo	ł																																			D	C I	В	4
R	ese	t 0x0	0000000		0	0	0	0	0) (0	0	0	0	0	0	0	0) (0	0	0	0	0	C) ()	0 (0	0	0	0	0	0	0	0	0 (0 ()
lo	i	RW	Field	Value Id	Va	lue								De	scr	ipti	on																						
Α		RW	READY								Wı	rite	'1'	to	Dis	ab	le i	nte	err	upt	fo	r R	EAI	ΟY	eve	nt													
														Se	e <i>E</i>	VEN	VTS.	_R	ΕAI	DΥ																			
				Clear	1									Dis	sab	le																							



Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			D C B A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW DOWN			Write '1' to Disable interrupt for DOWN event
			See EVENTS_DOWN
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW UP			Write '1' to Disable interrupt for UP event
			See EVENTS_UP
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW CROSS			Write '1' to Disable interrupt for CROSS event
			See EVENTS_CROSS
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

38.5.5 RESULT

Address offset: 0x400

Compare result

Bit	numbe	er		31 3	0 29	28	27	26	25	24	23 :	22 2	21 2	0 1	9 1	8 17	16	5 15	14	13	12	11 1	0 9	8	7	6	5	4	3	2 :	1 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Valu	е						Des	crip	otio	n																	
Α	R	RESULT									Res	ult	of la	st c	om	pare	e. D	ecis	ion	poi	nt S	AMI	PLE 1	task							
			Below	0							Inpi	ut v	olta	ge i	s be	low	the	e th	resl	nold	(VI	N+ <	· VII	V-)							
			Above	1							Inpi	ut v	olta	ge i	s ab	ove	the	e th	resl	nold	(VI	N+ >	· VII	۱-)							

38.5.6 ENABLE

Address offset: 0x500

COMP enable

В	it nı	umbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14 :	13 1	12 1	111	0 9	8	7	6	5	4	3	2	1 ()
lo	ł																																	Α ,	Ą
R	ese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 ()
le	ł	RW	Field	Value Id	Va	ue							De	scri	pti	on																			
Δ		RW	ENABLE										En	able	e or	dis	able	e CO	OM	>															
				Disabled							Dis	sabl	e																						
				Enabled	2								En	able	9																				

38.5.7 PSEL

Address offset: 0x504

Pin select

Bit	numbe	er		31	30	29	28	27	26	25	24	23 :	22 2	21 2	20 1	9 1	8 17	7 16	5 15	14	13	12 :	1 10	9	8	7	6	5	4	3	2	1 0
Id																															Α /	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	PSEL										Ana	log	pin	sel	ect																



Bit number	31	1 30 29 28 2	7 26 25 24	23 22 21 20	19 18 1	17 16 1	5 14 1	3 12 1	1 10	8 6	7	6 5	4	3 2	1 0
Id														А	A A
Reset 0x00000000	0	0 0 0 0	0 0 0	0 0 0 0	0 0	0 0 0	0 (0 0	0	0 0	0	0 0	0	0 0	0 0
Id RW Field Value	e Id Va	alue		Description											
Analo	ogInput0 0			AIN0 selecte	d as ana	alog inp	ut								
Analo	ogInput1 1			AIN1 selecte	d as ana	alog inp	ut								
Analo	ogInput2 2			AIN2 selecte	d as ana	alog inp	ut								
Analo	ogInput3 3			AIN3 selecte	d as ana	alog inp	ut								
Analo	ogInput4 4			AIN4 selecte	d as ana	alog inp	ut								
Analo	ogInput5 5			AIN5 selecte	d as ana	alog inp	ut								
Analo	ogInput6 6			AIN6 selecte	d as ana	alog inp	ut								
Analo	ogInput7 7			AIN7 selecte	d as ana	alog inp	ut								

38.5.8 REFSEL

Address offset: 0x508 Reference source select

Bit	numbe	er		33	1 30	29	28	8 27	7 2	6 25	5 24	4 2	3 22	2 21	20	19	18	17	7 16	15	14	13	12	11	10	9	8 7	(5	4	3	2	1	0
Id																																Α	Α	Α
Res	et 0x0	000004		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	C	0	0	0	1	0	0
Id	RW	Field	Value Id	V	alue							D	esci	ripti	on																			
Α	RW	REFSEL										R	efer	enc	e se	elec	t																	
			Int1V2	0								٧	REF	= in	ter	nal	1.2	۷	refe	erer	ice	(VD	D >:	= 1.7	7 V)									
			Int1V8	1								٧	REF	= in	ter	nal	1.8	۷	refe	erer	ice	(VD	D >:	= VR	EF ·	+ 0.	2 V)							
			Int2V4	2								٧	REF	= in	ter	nal	2.4	۷	refe	erer	ice	(VD	D >:	= VR	EF ·	+ 0.	2 V)							
			VDD	4								٧	REF	= V	DD																			
			ARef	7								٧	REF	= A	REF	(V	DD	>=	VRI	EF >	= A	REF	MIN	1)										

38.5.9 EXTREFSEL

Address offset: 0x50C External reference select

А
0 0 0 0

38.5.10 TH

Address offset: 0x530

Threshold configuration for hysteresis unit

Bit	numb	per		31 30 29 28 2	7 26 25 24 23 22 21 20	19 18 17 1	6 15	14 13	12	11 10	9	8	7	6	5	4	3 2	1	0
Id								В	В	ВВ	В	В			Α	Α	A A	Α.	Α
Res	et 0x	00000000		0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0	0 0	0 0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id	RW	/ Field	Value Id	Value	Description														
Α	RW	/ THDOWN		[63:0]	VDOWN = (THDOWN+1)	/64*	√REF											_
В	RW	/ THUP		[63:0]	VUP = (THU	P+1)/64*VRE	F												

38.5.11 MODE

Address offset: 0x534 Mode configuration



Bit n	umbe	er		31 3	0 29	28	27	26 25	5 24	23	22 2	21 20	19	18	17 1	l6 1	5 14	13	12	11 10	9	8	7	6 5	5 4	3	2	1 0
Id																						В						A A
Rese	t 0x0	0000000		0 (0 0	0	0	0 0	0	0	0	0 0	0	0	0	0 (0	0	0	0 0	0	0	0	0 (0	0	0	0 0
Id	RW	Field	Value Id	Valu	e					De	scrip	tion																
Α	RW	SP								Spe	eed a	and p	owe	er m	node	:												
			Low	0						Lov	v po	wer	mod	le														
			Normal	1						No	rmal	mod	de															
			High	2						Hig	sh sp	eed	mod	le														
В	RW	MAIN								Ma	in o	pera	tion	mo	de													
			SE	0						Sin	gle e	ende	d mo	ode														
			Diff	1						Dif	fere	ntial	mod	le														

38.5.12 HYST

Address offset: 0x538

Comparator hysteresis enable

Bit r	numb	er		33	1 30	29	28	27	26	5 25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	V	alue	:						De	scri	ptic	on																			
Α	RW	HYST										Со	mp	arat	tor I	nyst	tere	esis																
			NoHyst	0								Со	mp	arat	tor I	nyst	tere	esis	dis	abl	ed													
			Hyst50mV	1								Со	mp	arat	tor I	nyst	tere	esis	ena	able	ed													

38.5.13 ISOURCE

Address offset: 0x53C

Current source select on analog input

Bit	numb	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	LO	9	8	7	6	5	4	3	2	1	0
Id																																		Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•						De	scr	ipti	on																				
Α	RW	ISOURCE										Со	mp	ara	tor	hys	ter	esis	;																
			Off	0								Cu	rre	nt s	our	ce o	disa	ble	d																
			len2mA5	1								Cu	rre	nt s	our	ce e	ena	ble	d (+	-/- :	2.5	uA)													
			len5mA	2								Cu	rre	nt s	our	ce e	ena	ble	d (+	-/-!	5 u	A)													
			len10mA	3								Cu	rre	nt s	our	ce e	ena	ble	d (+	-/-	10 ι	ıA)													

38.6 Electrical specification

38.6.1 COMP Electrical Specification

Symbol De	escription	Min.	Тур.	Max.	Units
I _{COMP,LP} Co	ore run current in low power mode		2		μΑ
I _{COMP,N} Co	ore run current in normal mode		5		μΑ
I _{COMP,HS} Co	ore run current in high-speed mode		10		μΑ
t _{PROPDLY,LP} Pro	opagation delay, low power mode ^a		0.6		μS
t _{PROPDLY,N} Pro	opagation delay, normal mode ^a		0.2		μS
t _{PROPDLY,HS} Pro	opagation delay, high-speed mode ^a		0.1		μS
I _{SOURCE} Co	onfigurable input current provided by the output driven				μΑ
cu	rrent source.				
I _{SOURCE,A}			2.5		μΑ
I _{SOURCE,B}			5.0		μΑ
I _{SOURCE,C}			10.0		μΑ

^a Propagation delay is with 10mV overdrive.



Symbol	Description	Min.	Тур.	Max.	Units
V _{DIFFHYST}	Optional hysteresis applied to differential input		30		mV
V _{VDD-VREF}	Required difference between VDD and a selected VREF, VDD >	0.3			V
	VREF				
I _{INT_REF}	Current used by the internal bandgap reference when selected		13		μΑ
	as source for VREF				
t _{INT_REF} ,START	Startup time for the internal bandgap reference		50	80	μS
E _{INT_REF}	Internal bandgap reference error	-3		3	%
R _{LADDER}	Reference ladder resistance, ILADDER = VREF / RLADDER		550		kΩ
V _{INPUTOFFSET}	Input offset	-10		10	mV
D _{NLLADDER}	Differential non-linearity of reference ladder		<0.1		LSB
t _{COMP,START}	Startup time for the comparator core		3		μS

Total comparator run current must be calculated from the I_{COMP} , I_{INT_REF} , I_{SOURCE} and I_{LADDER} values for a given reference voltage.



39 LPCOMP — Low power comparator

LPCOMP compares an input voltage against a reference voltage.

Listed here are the main features of LPCOMP:

- 0 VDD input range
- Ultra low power
- Eight input options (AINO to AIN7)
- · Reference voltage options:
 - · Two external analog reference inputs, or
 - 15-level internal reference ladder (VDD/16)
- Optional hysteresis enable on input
- Wakeup source from OFF mode

In System ON, the LPCOMP can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the selected reference. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

Restriction: LPCOMP cannot be used (STARTed) at the same time as COMP. Only one comparator can be used at a time.

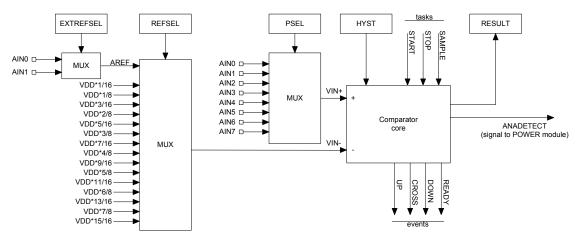


Figure 115: Low power comparator

The wakeup comparator (LPCOMP) compares an input voltage (VIN+), which comes from an analog input pin selected via the PSEL register against a reference voltage (VIN-) selected via the *REFSEL* on page 408 and *EXTREFSEL* registers.

The *PSEL*, *REFSEL*, and *EXTREFSEL* registers must be configured before the LPCOMP is enabled through the *ENABLE* register.

The *HYST* register allows enabling an optional hysteresis in the comparator core. This hysteresis is in the order of magnitude of 50 mV, and shall prevent noise on the signal to create unwanted events. See *Figure 116: Effect of hysteresis on a noisy input signal* on page 404 for illustration of the effect of an active hysteresis on a noisy input signal. It is disabled by default, and shall be configured before enabling LPCOMP as well.

The LPCOMP is started by triggering the START task. After a start-up time of $t_{LPCOMP,STARTUP}$ the LPCOMP will generate a READY event to indicate that the comparator is ready to use and the output of the LPCOMP is correct. The LPCOMP will generate events every time VIN+ crosses VIN-. More specifically, every time VIN+ rises above VIN- (upward crossing) an UP event is generated along with a CROSS event. Every time VIN+ falls below VIN- (downward crossing), a DOWN event is generated along with a CROSS event. When



hysteresis is enabled, the upward crossing level becomes (VIN- + VHYST/2), and the downward crossing level becomes (VIN- - VHYST/2).

The LPCOMP is stopped by triggering the STOP task.

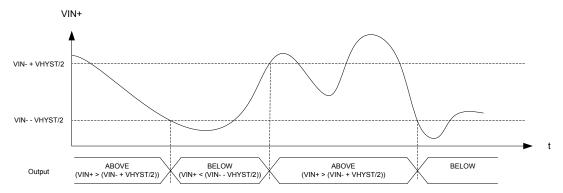


Figure 116: Effect of hysteresis on a noisy input signal

LPCOMP will be operational in both System ON and System OFF mode when it is enabled through the ENABLE register. See *POWER* — *Power supply* on page 78 for more information about power modes. Note that it is not allowed to go to System OFF when a READY event is pending to be generated.

All LPCOMP registers, including *ENABLE*, are classified as retained registers when the LPCOMP is enabled. However, when the device wakes up from System OFF, all LPCOMP registers will be reset.

The LPCOMP can wake up the system from System OFF by asserting the ANADETECT signal. The ANADETECT signal can be derived from any of the event sources that generate the UP, DOWN and CROSS events. In case of wakeup from System OFF, no events will be generated, only the ANADETECT signal. See the ANADETECT register (*ANADETECT* on page 408) for more information on how to configure the ANADETECT signal.

The immediate value of the LPCOMP can be sampled to *RESULT* on page 407 by triggering the SAMPLE task.

See *RESETREAS* on page 85 for more information on how to detect a wakeup from LPCOMP.

39.1 Shared resources

The LPCOMP shares resources with other peripherals.

The LPCOMP shares analog resources with SAADC and COMP. While it is possible to use SAADC at the same time as COMP or LPCOMP, COMP and LPCOMP are mutually exclusive: enabling one will automatically disable the other. In addition, when using SAADC and COMP or LPCOMP simultaneously, it is not possible to select the same analog input pin for both modules.

The LPCOMP peripheral shall not be disabled (by writing to the ENABLE register) before the peripheral has been stopped. Failing to do so may result in unpredictable behaviour.

39.2 Pin configuration

You can use the LPCOMP.PSEL register to select one of the analog input pins, AINO through AIN7, as the analog input pin for the LPCOMP.

See *GPIO* — *General purpose input/output* on page 111 for more information about the pins. Similarly, you can use *EXTREFSEL* on page 408 to select one of the analog reference input pins, AINO and AIN1, as input for AREF in case AREF is selected in *EXTREFSEL* on page 408. The selected analog pins will be acquired by the LPCOMP when it is enabled through *ENABLE* on page 407.



39.3 Registers

Table 93: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40013000	LPCOMP	LPCOMP	Low power comparator	

Table 94: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start comparator
TASKS_STOP	0x004	Stop comparator
TASKS_SAMPLE	0x008	Sample comparator value
EVENTS_READY	0x100	LPCOMP is ready and output is valid
EVENTS_DOWN	0x104	Downward crossing
EVENTS_UP	0x108	Upward crossing
EVENTS_CROSS	0x10C	Downward or upward crossing
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RESULT	0x400	Compare result
ENABLE	0x500	Enable LPCOMP
PSEL	0x504	Input pin select
REFSEL	0x508	Reference select
EXTREFSEL	0x50C	External reference select
ANADETECT	0x520	Analog detect configuration
HYST	0x538	Comparator hysteresis enable

39.3.1 SHORTS

Address offset: 0x200

Shortcut register

Dit.	number			24 20 20 20 27 26 25 24	22 22 24 20 40 40 47 46 45 44 42 42 44 40 0 0 7 6 5 4 2 2 4 0
	number			31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E D C B A
Res	et 0x00000				0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Fie	ld	Value Id	Value	Description
Α	RW REA	ADY_SAMPLE			Shortcut between READY event and SAMPLE task
					See EVENTS_READY and TASKS_SAMPLE
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
В	RW REA	ADY_STOP			Shortcut between READY event and STOP task
					See EVENTS_READY and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
С	RW DO	WN_STOP			Shortcut between DOWN event and STOP task
					See EVENTS_DOWN and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
D	RW UP	_STOP			Shortcut between UP event and STOP task
					See EVENTS_UP and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
E	RW CR	OSS_STOP			Shortcut between CROSS event and STOP task
					See EVENTS_CROSS and TASKS_STOP
			Disabled	0	Disable shortcut



Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10	0 9 8 7 6 5 4 3 2 1 0
Id					E D C B A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
	Enabled	1	Enable shortcut		

39.3.2 INTENSET

Address offset: 0x304

Enable interrupt

		mionapi			
Bit	numb	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Res	et 0x0	00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	READY			Write '1' to Enable interrupt for READY event
					See EVENTS_READY
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	DOWN			Write '1' to Enable interrupt for DOWN event
					See EVENTS_DOWN
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	UP			Write '1' to Enable interrupt for UP event
					See EVENTS_UP
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	CROSS			Write '1' to Enable interrupt for CROSS event
					See EVENTS_CROSS
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

39.3.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	umbe	r		31	30 2	9 :	28 2	27 :	26 2	5 2	24 2	3 22	2 2:	1 20	0 1	9 1	8 1	7 10	5 1	5 14	1 13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id																															0 0	В	Α
Rese	t 0x0	0000000		0	0	0	0	0	0 ()	0 (0 0	0	0	0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						C	esc	ript	tion	•																		
Α	RW	READY									٧	Vrite	e '1 '	' to	Dis	abl	e ir	nter	rup	t fo	r RI	AD	Y e	ent/									
											S	ee E	VE	NTS	R	EAL	ΟY																
			Clear	1							C	isab	ole																				
			Disabled	0							R	Read	: Di	isab	led	ı																	
			Enabled	1							R	Read	: Er	nabl	led																		
В	RW	DOWN									٧	Vrite	e '1'	' to	Dis	abl	e ir	nter	rup	t fo	r D	wc	N e	vent	:								
											S	ee E	VE	NTS	5_D	οи	/N																
			Clear	1							С	Disab	ole																				
			Disabled	0							R	Read	: Di	isab	led	ı																	
			Enabled	1							R	Read	: Er	nabl	led																		
С	RW	UP									٧	Vrite	e '1'	' to	Dis	abl	e ir	nter	rup	t fo	r U	P ev	ent/										
											S	ee E	VE	NTS	<u>5_</u> U	P																	



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW CROSS			Write '1' to Disable interrupt for CROSS event
			See EVENTS_CROSS
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

39.3.4 RESULT

Address offset: 0x400

Compare result

Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ld	RW	Field	Value Id	Va	lue							De	scri	pti	on																				
Α	R	RESULT										Re	sult	of	last	COI	np	are	. De	cis	on	poi	nt S	SAN	/IPLI	E ta	sk.								
			Bellow	0								Inp	ut	volt	age	is	oel	ow	the	re	ere	nce	e th	res	holo	V) b	IN+	< \	/IN	-).		De	ored	cate	ed.
			Below	0								Inp	ut	volt	age	is	oel	ow	the	re	ere	nce	e th	res	holo	V) b	IN+	< \	/IN	-).					
			Above	1								Inp	ut	volt	age	is	abo	ve	the	re	ere	nce	th	res	holo	V) b	IN+	> \	/IN	-).					

39.3.5 ENABLE

Address offset: 0x500 Enable LPCOMP

Bi	t nu	ımbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																																		Α	A
Re	eset	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id		RW	Field	Value Id	Val	ue							De	scr	pti	on																			
Α		RW	ENABLE										En	able	e or	dis	abl	e LF	со	MP	•														
				Disabled	0								Dis	abl	e																				
				Enabled	1								En	able	9																				

39.3.6 PSEL

Address offset: 0x504

Input pin select

Bit number		31	30 2	9 2	28 27	' 26	25	24	23 22	2 21 2	20 1	19 18	3 17	16	15 1	4 13	3 12	11 1	0 9	8	7	6	5	4 3	3 2	1	0
ld Reset 0x00000000		0	0 () (0 0	0	0	0	0 0	0	0 (0 0	0	0	0 (0 0	0	0 (0 0	0	0	0	0	0 (A 0 (. A	A 0
Id RW Field V	alue Id	Val	lue					1	Desc	riptio	n																
A RW PSEL								,	Analo	g pin	sel	ect															
A	nalogInput0	0						,	AINO	selec	ted	as a	nalo	g in	put												
A	nalogInput1	1						,	AIN1	selec	ted	as a	nalo	g in	put												
A	nalogInput2	2						,	AIN2	selec	ted	as a	nalo	g in	put												
A	nalogInput3	3						,	AIN3	selec	ted	as a	nalo	g in	put												
A	nalogInput4	4						,	AIN4	selec	ted	as a	nalo	g in	put												
A	nalogInput5	5						,	AIN5	selec	ted	as a	nalo	g in	put												
A	nalogInput6	6						,	AIN6	selec	ted	as a	nalo	g in	put												
A	nalogInput7	7						,	AIN7	selec	ted	as a	nalo	g in	put												



39.3.7 REFSEL

Address offset: 0x508 Reference select

Bit number		21 20 20 28 27 26 25 27	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		31 30 29 20 27 20 23 24	4 25 22 21 20 19 10 17 10 13 14 13 12 11 10 9 6 7 6 3 4 5 2 1 0
Reset 0x00000004		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW REFSEL			Reference select
	Ref1_8Vdd	0	VDD * 1/8 selected as reference
	Ref2_8Vdd	1	VDD * 2/8 selected as reference
	Ref3_8Vdd	2	VDD * 3/8 selected as reference
	Ref4_8Vdd	3	VDD * 4/8 selected as reference
	Ref5_8Vdd	4	VDD * 5/8 selected as reference
	Ref6_8Vdd	5	VDD * 6/8 selected as reference
	Ref7_8Vdd	6	VDD * 7/8 selected as reference
	ARef	7	External analog reference selected
	Ref1_16Vdd	8	VDD * 1/16 selected as reference
	Ref3_16Vdd	9	VDD * 3/16 selected as reference
	Ref5_16Vdd	10	VDD * 5/16 selected as reference
	Ref7_16Vdd	11	VDD * 7/16 selected as reference
	Ref9_16Vdd	12	VDD * 9/16 selected as reference
	Ref11_16Vdd	13	VDD * 11/16 selected as reference

VDD * 13/16 selected as reference

VDD * 15/16 selected as reference

39.3.8 EXTREFSEL

Ref13_16Vdd

Ref15_16Vdd

14

15

Address offset: 0x50C External reference select

Bit n	umbe	r		31	1 30	29	28	27	26	25	24	23	22	21 :	20	19	18	17 :	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 (0
Id																																	,	A
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 (O
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptio	n																			
Α	RW	EXTREFSEL										Ext	ern	al a	nal	og r	efe	ren	ce:	sele	ect													
			AnalogReference0	0								Us	e Al	N0 a	as e	xte	rna	l ar	nalo	g re	efe	ren	ce											
			AnalogReference1	1								Us	e Al	N1 a	as e	xte	rna	l ar	nalo	g re	efe	ren	ce											

39.3.9 ANADETECT

Address offset: 0x520

Analog detect configuration

Bit r	numbe	er		31	1 30	29	28	27 :	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							Des	scri	ptic	on																				
Α	RW	ANADETECT										Ana	alog	g de	tec	t cc	onfi	gur	atio	on															
			Cross	0								Ger	nera	ate	ΑN	ADI	ETE	СТ	on	cro	ssir	ıg, l	botl	n up	wa	rd o	ros	sin	g a	nd					
												dov	wnv	war	d cr	oss	ing																		
			Up	1								Ger	nera	ate	ΑN	ADI	ETE	СТ	on	upv	var	d cı	ross	ing	onl	У									
			Down	2								Ger	nera	ate	ΑN	ADI	ETE	СТ	on	dov	vnv	var	d cr	ossi	ng	onl	У								

39.3.10 HYST

Address offset: 0x538

Comparator hysteresis enable



Bit	numb	er		31 30	29	28 2	27 20	6 25	5 24	23	22 2	21 2	0 19	18	17	16	15 1	L4 1	3 12	11	10	9	8	7	6	5 4	4 3	2	1 0
Id																													Α
Res	et Ox	0000000		0 0	0	0 (0 0	0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0	0	0 0
Id	RW	Field	Value Id	Value						Des	crip	tio	1																
Α	RW	HYST								Cor	npa	rato	r hy	ster	esis	ena	ble												
			NoHyst	0						Cor	npa	rato	r hy	ster	esis	disa	able	d											
			Hyst50mV	1						Cor	npa	rato	r hy	ster	esis	disa	able	d (t	yp. 5	0 m	V)								

39.4 Electrical specification

39.4.1 LPCOMP Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{LPC}	Run current for low power comparator		0.5		μΑ
t _{LPCANADET}	Time from VIN crossing (>=50mV above threshold) to		5		μs
	ANADETECT signal generated.				
E _{REFLADDER}	Error in reference ladder threshold voltage	-30		30	mV
V _{HYST}	Optional hysteresis		30		mV



40 WDT — Watchdog timer

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up.

The watchdog timer is started by triggering the START task.

The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU. The watchdog is implemented as a down-counter that generates a TIMEOUT event when it wraps over after counting down to 0. When the watchdog timer is started through the START task, the watchdog counter is loaded with the value specified in the CRV register. This counter is also reloaded with the value specified in the CRV register when a reload request is granted.

The watchdog's timeout period is given by:

```
timeout [s] = ( CRV + 1 ) / 32768
```

When started, the watchdog will automatically force the 32.768 kHz RC oscillator on as long as no other 32.768 kHz clock source is running and generating the 32.768 kHz system clock, see chapter *CLOCK* — *Clock control* on page 101.

40.1 Reload criteria

The watchdog has eight separate reload request registers, which shall be used to request the watchdog to reload its counter with the value specified in the CRV register. To reload the watchdog counter, the special value 0x6E524635 needs to be written to all enabled reload registers.

One or more RR registers can be individually enabled through the RREN register.

40.2 Temporarily pausing the watchdog

By default, the watchdog will be active counting down the down-counter while the CPU is sleeping and when it is halted by the debugger. It is however possible to configure the watchdog to automatically pause while the CPU is sleeping as well as when it is halted by the debugger.

40.3 Watchdog reset

A TIMEOUT event will automatically lead to a watchdog reset.

See *Reset* on page 82 for more information about reset sources. If the watchdog is configured to generate an interrupt on the TIMEOUT event, the watchdog reset will be postponed with two 32.768 kHz clock cycles after the TIMEOUT event has been generated. Once the TIMEOUT event has been generated, the impending watchdog reset will always be effectuated.

The watchdog must be configured before it is started. After it is started, the watchdog's configuration registers, which comprise registers CRV, RREN, and CONFIG, will be blocked for further configuration.

The watchdog can be reset from several reset sources, see *Reset behavior* on page 83.

When the device starts running again, after a reset, or waking up from OFF mode, the watchdog configuration registers will be available for configuration again.



40.4 Registers

Table 95: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40010000	WDT	WDT	Watchdog timer	

Table 96: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start the watchdog
EVENTS_TIMEOUT	0x100	Watchdog timeout
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RUNSTATUS	0x400	Run status
REQSTATUS	0x404	Request status
CRV	0x504	Counter reload value
RREN	0x508	Enable register for reload request registers
CONFIG	0x50C	Configuration register
RR[0]	0x600	Reload request 0
RR[1]	0x604	Reload request 1
RR[2]	0x608	Reload request 2
RR[3]	0x60C	Reload request 3
RR[4]	0x610	Reload request 4
RR[5]	0x614	Reload request 5
RR[6]	0x618	Reload request 6
RR[7]	0x61C	Reload request 7

40.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	iumbe	r		31	. 30	29	28	8 27	7 2	26 2	5 2	24 2	3 2	22 2	21	20	19	18	3 1	7 1	5 1	5 1	4	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																					Α
Res	et 0x0	0000000		0	0	0	0	0	(0 () (0 (0	0	0	0	0	0	C) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							C)es	crip	otic	on																					
Α	RW	TIMEOUT										٧	Vrit	te '	1' t	to E	na	ble	in	teri	up	t fo	r T	IM	ΕO	UT	eve	ent									
												S	ee	EV	ΈN	TS_	TII	ME	οι	IT																	
			Set	1								Е	nal	ble																							
			Disabled	0								R	lea	d: [Disa	abl	ed																				
			Enabled	1								R	lea	d: E	Ena	ble	d																				

40.4.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	3	1 30 29 28	3 27 26 2	25 24 :	23 22	21 2	0 19	18	17 1	6 1	.5 14	13	12 1	1 10	9	8	7	6 5	5 4	3	2 :	1 0
ld																						Α
Reset 0x00000000	0	0 0 0	0 0	0 0	0 0	0 0	0	0	0 (0 (0 0	0	0 (0	0	0	0	0 (0	0	0 (0 0
ld RW Field	Value Id V	alue		- 1	Descri	iption	١															
A RW TIMEOU	т			,	Write	'1' to	Disa	ble	inte	rrup	ot fo	r TIN	ΛΕΟL	JT ev	ent/							
				:	See <i>E</i> \	/ENTS	S_TIN	MEC	UT													
	Clear 1			1	Disabl	e																
	Disabled 0			- 1	Read:	Disab	oled															
	Enabled 1				Read:	Enab	led															
	T Clear 1 Disabled 0	alue		: :	Write See <i>E\</i> Disabl Read:	'1' to <i>/ENTS</i> e Disab	Disa S_ <i>TIN</i> oled			rrup	ot fo	r TIN	ИEOU	JT ev	vent							



40.4.3 RUNSTATUS

Address offset: 0x400

Run status

Bitı	numbe	r		3:	1 30	29	28	8 27	7 20	6 2	5 24	4 2	3 2	2 2	1 2	0 1	9 1	.8 1	7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2	1 0	ı
Id																																		Α	
Res	et 0x0	0000000		0	0	0	0	0	0) (0) () (0) () (0 (0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	V	alue	2						D	esc	ript	tior	1																			l
Α	R	RUNSTATUS										Ir	ndic	ate	s w	het	the	r or	no	t th	e w	atc	ndo	g is	run	nin	g								
			NotRunning	0								W	Vato	chd	og i	not	rui	nnir	ng																
			Running	1								W	Vato	chd	og i	is rı	unn	ing																	

40.4.4 REQSTATUS

Address offset: 0x404

Request status

																									_							
	numbe	er		31	. 30	29	28	27	26	25	24 2	23	22 2	21 2	0 19	18	17	16	15 1	4 1	3 12	11	10	9				4	- 3	2	1	0
Id																													D			
Res	et 0x0	0000001		0	0	0	0	0	0	0	_	•	0 (0	0	0	0 () (0	0	0	0	0 () (0	0	0	0	0	1
Id	RW	Field	Value Id	Va	llue						ı	Des	scrip	tior	1																	
Α	R	RRO									ı	Rec	ques	t sta	itus	for	RR[C] re	gist	er												
			DisabledOrRequested	0							ı	RR[[0] re	egist	ter is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			${\sf EnabledAndUnrequested}$	1							ı	RR[[0] re	egist	ter is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
В	R	RR1									ı	Rec	ques	t sta	itus	for	RR[1] re	gist	er												
			DisabledOrRequested	0							ı	RR[[1] re	egist	ter is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			${\sf EnabledAndUnrequested}$	1							ı	RR[[1] re	egist	er is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
С	R	RR2									ı	Rec	ques	t sta	itus	for	RR[2] re	gist	er												
			DisabledOrRequested	0							ı	RR[[2] re	egist	ter is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			EnabledAndUnrequested	1							ı	RR[[2] re	egist	ter is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
D	R	RR3									ı	Rec	ques	t sta	atus	for	RR[3] re	gist	er												
			DisabledOrRequested	0							ı	RR[[3] re	egist	ter is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			${\sf EnabledAndUnrequested}$	1							ſ	RR[[3] re	egist	ter is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
E	R	RR4									ı	Rec	ques	t sta	itus	for	RR[4] re	gist	er												
			DisabledOrRequested	0							ı	RR[[4] re	egist	er is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			${\sf EnabledAndUnrequested}$	1							ı	RR[[4] re	egist	ter is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
F	R	RR5									ı	Rec	ques	t sta	atus	for	RR[5] re	gist	er												
			DisabledOrRequested	0							ı	RR[[5] re	egist	ter is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			EnabledAndUnrequested	1							ı	RR[[5] re	egist	ter is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
G	R	RR6									ı	Rec	ques	t sta	itus	for	RR[6] re	gist	er												
			DisabledOrRequested	0							ı	RR[[6] re	egist	ter is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			EnabledAndUnrequested	1							ı	RR[[6] re	egist	er is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					
Н	R	RR7									ı	Rec	ques	t sta	itus	for	RR[7	'] re	gist	er												
			DisabledOrRequested	0							ı	RR[[7] re	egist	er is	no	t en	able	ed, c	r ar	e alr	ead	ly re	que	estir	g re	eloa	d				
			EnabledAndUnrequested	1							ı	RR[[7] re	egist	ter is	en	able	d, a	nd a	are i	not y	et r	equ	esti	ing r	elo	ad					

40.4.5 CRV

Address offset: 0x504 Counter reload value

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16 :	15 1	L4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3 .	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A .	Α.	Α Α	A A	A	Α	Α	Α	Α	Α	Α	Α /	4 4	A A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	. 1	1	1	1	1	1	1	1 :	1 1	l 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	CRV		[0	x00	000	000	0	xFF	FFF	FFF	Со	unt	er r	elo	ad v	/alu	e in	nu	mb	er c	f cy	cles	of	the	32.7	768	kHz	2				

clock



40.4.6 RREN

Address offset: 0x508

Enable register for reload request registers

Bit r	numbe	er		31	30 2	29 2	28 2	7 26	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14 :	13 1	2 13	1 10	9	8	7	6	5	4 3	2	1	0
Id																										Н	G	F	E C	С С	В	Α
Res	et 0x0	0000001		0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	1
Id	RW	Field	Value Id	Va	lue						De	escr	ipti	on																		
Α	RW	RR0									En	nabl	e or	r dis	sabl	e RI	R[0]	re	gist	er												
			Disabled	0							Di	isab	le R	R[0)] re	gist	er															
			Enabled	1							En	nabl	e RF	R[0]] reg	giste	er															
В	RW	RR1									En	nabl	e or	r dis	sabl	e RI	R[1]	re	gist	er												
			Disabled	0							Di	isab	le R	R[1	.] re	gist	er															
			Enabled	1							En	nabl	e RF	R[1]] reg	giste	er															
С	RW	RR2									En	nabl	e or	r dis	sabl	e RI	R[2]	re	gist	er												
			Disabled	0							Di	isab	le R	R[2	?] re	gist	er															
			Enabled	1							En	nabl	e RF	R[2]] reg	giste	er															
D	RW	RR3									En	nabl	e or	r dis	sabl	e RI	R[3]	re	gist	er												
			Disabled	0							Di	isab	le R	R[3] re	gist	er															
			Enabled	1							En	nabl	e RF	R[3]] reg	giste	er															
Е	RW	RR4									En	nabl	e or	r dis	sabl	e RI	R[4]	re	gist	er												
			Disabled	0							Di	isab	le R	R[4	l] re	gist	er															
			Enabled	1							En	nabl	e RF	R[4]] reg	giste	er															
F	RW	RR5									En	nabl	e or	r dis	sabl	e RI	R[5]	re	gist	er												
			Disabled	0							Di	isab	le R	R[5] re	gist	er															
			Enabled	1							En	nabl	e RF	R[5]] reg	giste	er															
G	RW	RR6									En	nabl	e or	r dis	sabl	e RI	R[6]	re	gist	er												
			Disabled	0							Di	isab	le R	R[6	i] re	gist	er															
			Enabled	1							En	nabl	e RF	R[6]] reg	giste	er															
Н	RW	RR7									En	nabl	e or	r dis	sabl	e RI	R[7]	re	gist	er												
			Disabled	0							Di	isab	le R	R[7	'] re	gist	er															
			Enabled	1							En	nabl	e RF	R[7]] reg	giste	er															

40.4.7 CONFIG

Address offset: 0x50C Configuration register

Bit number		31	30 2	9 2	8 2	7 2	6 2	5 2	4 23	3 22	2 2:	1 20	0 1	9 1	8 1	7 1	6 1	5 1	4 13	12	11	10	9	8	7	6	5 4	3	2	1	0
Id																												С			Α
Reset 0x00000001		0	0 (0 (0 0) () (0	0	0	0	0	0) () () () (0 (0	0	0	0	0	0	0	0	0	0	0	0	1
Id RW Field	Value Id	Val	ue						D	esci	ript	ion	1																		
A RW SLEEP									Co	onfi	iguı	e tl	he v	wat	ch	gob	to	eith	er b	e p	aus	ed,	or k	ept	rur	nnin	g,				
									w	hile	th	e C	PU	is s	lee	pin	g														
	Pause	0							Pa	use	e w	atc	hdc	og v	vhi	e tl	ne (CPU	is s	leep	oing										
	Run	1							Ke	ep	the	e w	atcl	hdc	og r	unr	ing	g wh	ile t	he	CPL	l is s	lee	ping	5						
C RW HALT									Co	onfi	iguı	e tl	he v	wat	ch	gob	to	eith	er b	e p	aus	ed,	or k	ept	rur	nnin	g,				
									w	hile	th	e C	PU	is h	alt	ed l	oy t	he	deb	ıggı	er										
	Pause	0							Pa	use	e w	atc	hdc	og v	vhi	e tl	ne (CPU	is h	alte	d b	y th	e de	ebu	gge	r					
	Run	1							Ke	eep	the	e w	atcl	hdc	og r	unr	ing	g wh	ile t	he	CPL	l is h	alte	ed b	y t	he					
									de	ebu	gge	er																			

40.4.8 RR[0]

Address offset: 0x600 Reload request 0



Bit	nun	nbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	А А
Re	set ()0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	R	w	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	W	/	RR										Rel	oad	l re	que	st r	egi	stei	r															
				Reload	0x	6E5	246	35					Val	ue 1	to r	equ	ıest	ar	elo	ad d	of t	he v	wat	chc	log	tim	er								

40.4.9 RR[1]

Address offset: 0x604 Reload request 1

А		W	RR	Reload				535						load lue 1				_																		
_			D.D.										_																							-
Ic	d	RW	Field	Value Id	Va	lue							De	scri	ptic	n																				
R	lese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
lo	b				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	٨
В	it n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()

40.4.10 RR[2]

Address offset: 0x608 Reload request 2

Bit	numb	er		31	1 30	29	9 2	8 2	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Д		۸ ,	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A.	A A	4
Res	et Ox	00000000		0	0	0	()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	RW	Field	Value Id	Va	alue	•							Des	cri	otic	n																				
Α	W	RR											Rel	oad	red	que	st r	egi	stei	r																
			Reload	0.	6E!	- 2 4	ca	_					1/51	+	- r		ıest	- r	مام	٦d.	of +	ha		- a b a		+:										

40.4.11 RR[3]

Address offset: 0x60C Reload request 3

Bit	num	nbe	r		31	30	29	2	8 2	7	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id					Α	Α	Α	A	۱ ۸	Δ	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0)x0	0000000		0	0	0	C) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	R۱	w	Field	Value Id	Va	lue								De	scri	pti	on																				
Α	W	/	RR											Rel	oa	d re	que	estı	regi	ste	r																
				Reload	Λvi	6E5	24	63	5					Val	lue	to r	eui	IES	tai	elo	ha	of t	he	w/2	tch	dod	tin	nor									

40.4.12 RR[4]

Address offset: 0x610 Reload request 4

Bitı	numb	er		31	. 30	29	28	3 2	7 26	5 2	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Δ	A	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et 0x0	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue	:						De	scr	ipti	on																			
Α	W	RR										Re	loa	d re	qu	est i	regi	iste	r															
			Reload	Ох	6E5	524	635	;				Va	lue	to i	rea	uest	taı	relo	ad	of t	he	wat	cho	dog	tin	ner								

40.4.13 RR[5]

Address offset: 0x614 Reload request 5



Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	9 1	.8 1	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 /	4 A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et Ox	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	scrip	ptio	n																		
Α	W	RR										Rel	oad	l rec	ques	t re	gist	er															
			Reload	0x	6E5	246	35					Val	ue t	to re	eque	est	a rel	oad	d of	the	wa	tcho	dog	tim	ner								

40.4.14 RR[6]

Address offset: 0x618 Reload request 6

Bitı	numb	er		31	. 30	29	28	27	7 26	25	24	23	22	21	20 1	19 1	l8 1	7 1	5 15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α .	A A	. Δ	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	. 4	A A
Res	et Ox(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue	•						De	scrip	otic	n																		
Α	W	RR										Rel	oad	red	ques	st re	egist	er															
			Reload	0x	6E5	246	635					Val	ue t	o r	equ	est	a re	load	d of	the	wa	tcho	log	tim	er								

40.4.15 RR[7]

Address offset: 0x61C Reload request 7

Bit r	numb	er		31	. 30	29	28	3 27	7 26	5 2	5 2	4 2	3 2	2 21	. 20	19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	2	1 0
Id				Α	Α	Α	Α	. A	A	. 4	\ <i>A</i>	A A		4 A	Α	Α	Α	Α	Α	Α	Α	Α.	A /	A	Α	Α	Α	Α	Α	Α	A A	۱ ۱	A A
Res	et Ox	00000000		0	0	0	0	0	0	C) () () (0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	alue	•						D	esc	ript	ion																		
Α	W	RR										R	elo	ad r	equ	est	reg	iste	r														
			Reload	0x	6E5	524	635	5				٧	alu	e to	req	ues	t a	relo	ad	of t	he v	wato	hdo	g tii	ner								

40.5 Electrical specification

40.5.1 Watchdog Timer Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{WDT}	Run current for watchdog timer		0.3	2	μΑ
t _{WDT}	Time out interval	458 μs		36 h	



41 SWI — Software interrupts

A set of interrupts have been reserved for use as software interrupts.

41.1 Registers

Table 97: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40014000	SWI	SWI0	Software interrupt 0		
0x40015000	SWI	SWI1	Software interrupt 1		
0x40016000	SWI	SWI2	Software interrupt 2		
0x40017000	SWI	SWI3	Software interrupt 3		
0x40018000	SWI	SWI4	Software interrupt 4		
0x40019000	SWI	SWI5	Software interrupt 5		



42 NFCT — Near field communication tag

The NFCT peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106 kbps bit rate from the NFC Forum.

With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

Listed here are the main features for the NFC peripheral:

- NFC-A listen mode operation
 - 13.56 MHz input frequency
 - Bit rate 106 kbps
- Wake-on-field low power field detection (SENSE) mode
- Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum
- · Programmable frame timing controller
- · Integrated automatic collision resolution, CRC and parity functions

42.1 Overview

The NFC peripheral is an implementation of an NFC Forum compliant listening device NFC-A.

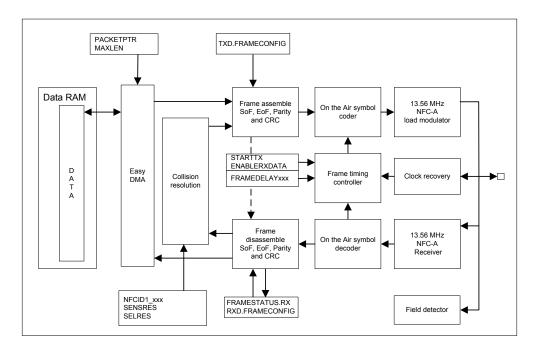


Figure 117: NFC block diagram

The NFC peripheral contains a 13.56 MHz AM receiver and a 13.56 MHz load modulator compatible with the NFC-A technology defined in the NFC Forum with 106 kbps data rate.

The received frames will be automatically disassembled and the data part of the frame transferred to RAM. When transmitting, the frame data will be transferred directly from RAM and transmitted with configurable frame type and delay timing. The system will be notified by an event whenever a complete frame is received or sent.

It also supports the collision detection and resolution ("anticollision") as defined by the NFC Forum.



Wake-on-field is supported in SENSE mode while the device is either in System OFF or System ON mode. When the antenna enters an NFC field, an event will be triggered notifying the system to activate the NFC functionality for incoming frames. In System ON, if the energy detected at the antenna increases beyond a threshold value, the module will generate a FIELDDETECTED event. The module will generate a FIELDLOST event when the quality or strength of the field no longer support NFC communication. Please refer to NFCT Electrical Specification on page 436 for the Low Power Field Detect threshold values.

In system OFF, the NFC Low Power Field Detect function can wake the system up through a reset. The NFC bit in register *RESETREAS* on page 85 will be set as cause of the wake-up.

If the system is put into system OFF mode while a field is already present, the NFC Low Power Field Detect function will wake the system up right away and generate a reset.

Note that as a consequence of reset, NFC is disabled, so the reset handler will have to activate NFC again and set it up properly.

The HFXO must be running before the NFC peripheral goes into ACTIVATED state. Note that the NFC peripheral calibration is automatically done on ACTIVATE task. The HFXO can be turned off when the NFC peripheral goes into SENSE mode. The shortcut FIELDDETECTED_ACTIVATE can be used when the HFXO is already running while in SENSE mode.

Outgoing data will be collected from RAM with the EasyDMA function and assembled according to the TXD.FRAMECONFIG register. Incoming data will be disassembled according to the RXD.FRAMECONFIG register and the data section in the frame will be written to RAM via the EasyDMA function.

The NFC peripheral includes a frame timing controller that can be used to accurately control the inter-frame delay between the incoming frame and a corresponding outgoing frame. It also includes optional CRC functionality.

The NFC peripheral has a set of different states. The module can change state by triggering a task, or when specific operations are finalized. Events and tasks allow software to keep track of and change the current state.

See Figure 117: NFC block diagram on page 417 and Figure 118: NFC state diagram on page 419 for more information.

Notes:

- FIELDLOST event will not be reflected in the state machine (for instance by going back to the DISABLE state), it is up to software to decide on the actions to take when a field lost occurs.
- FIELDLOST event is not generated in SENSE mode.
- FIELDDETECTED event is generated only on the transition from FIELDLOST event to energy detected by the NFC peripheral. So, sending SENSE task while field is still present does not generate FIELDDETECTED event.
- If the FIELDDETECTED event is cleared before sending the ACTIVATE task, then the FIELDDETECTED event shows up again after sending the ACTIVATE task. The shortcut FIELDDETECTED_ACTIVATE can be used to avoid this condition.



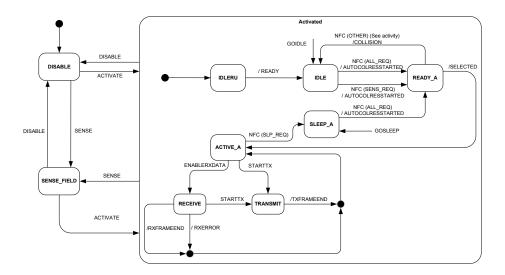


Figure 118: NFC state diagram

42.2 Pin configuration

NFC uses two pins to connect the antenna.

These pins are shared with GPIOs, and the PROTECT field in the NFCPINS register in *UICR* defines the usage of these pins and their protection level against excessive voltages. The content of the NFCPINS register is reloaded at every reset.

When NFCPINS.PROTECT=NFC, a protection circuit will be enabled on the dedicated pins, preventing the chip from being damaged in the presence of a strong NFC field. The GPIO function will be disabled on those pins as well.

When NFCPINS.PROTECT=Disabled, the device will not be protected against strong NFC field damages caught by a connected NFC antenna, and the NFCT peripheral will not operate as expected, as it will never leave the DISABLE state.

The pins dedicated to the NFC antenna function will have some limitation when the pins are configured for normal GPIO operation. The pin capacitance will be higher on those (refer to C_{PAD_NFC} in the GPIO *Electrical Specification* on page 154 below), and some increased leakage current between the two pins is to be expected if they are used in GPIO mode, and are driven to different logical values. To save power the two pins should always be set to the same logical value whenever entering one of the device power saving modes. Please refer to I_{NFC_LEAK} in $GPIO_Electrical_Specification$ on page 154 for details.

42.3 EasyDMA

The NFC peripheral implements EasyDMA for reading and writing of data packets from and to the Data RAM without CPU involvement.

The NFC EasyDMA utilizes one pointer called PACKETPTR for receiving and transmitting packets.

The EasyDMA can either read or write between the NFC peripheral and the RAM, but not at the same time. The event RXFRAMESTART indicates that the EasyDMA has started writing to the RAM for a receive frame and the event RXFRAMEND indicates that the EasyDMA has completed writing to the RAM. Similarly, the event TXFRAMESTART indicates that the EasyDMA has started reading from the RAM for a transmit frame and the event TXFRAMEND indicates that the EasyDMA has completed reading from the RAM. If a transmit and a receive operation is issued at the same time, the transmit operation would be prioritized.

Starting a transmit operation while the EasyDMA has already started writing a receive frame to the RAM will result in unpredictable behavior. Starting an EasyDMA operation whilst there is an ongoing EasyDMA operation may result in unpredictable behavior. It is recommended to wait for the TXFRAMEEND or



RXFRAMEND event for the respective ongoing transmit or receive before starting a new receive or transmit operation.

The MAXLEN register determines the maximum number of bytes that can be read from or written to the RAM. This feature can be used to secure that the NFC peripheral does not overwrite, or read beyond, the RAM assigned to a packet. Note that if the RXD.AMOUNT or TXD.AMOUNT register indicates longer data packets than set in MAXLEN, the frames sent to or received from the physical layer will be incomplete. In RX, the OVERRUN bit in the FRAMESTATUS.RX register will be set and an RXERROR event will be triggered in that situation.

Note that RXD.AMOUNT and TXD.AMOUNT define a frame length in bytes and bits excluding SoF, EoF and parity, but including CRC for RXD.AMOUNT only, make sure to take potential additional bits into account when setting MAXLEN.

Only sending task ENABLERXDATA ensures that a new value in PACKETPTR pointing to the RX buffer in Data RAM is taken into account.

If PACKETPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See Chapter *Memory* on page 23 for more information about the different memory regions.

The NFC peripherals normally do alternative receive and transmit frames. So, to prepare for the next frame, the PACKETPTR, MAXLEN, TXD.FRAMECONFIG and TXD.AMOUNT can be updated while the receive is in progress, and, similarly, the PACKETPTR, MAXLEN and RXD.FRAMECONFIG can be updated while the transmit is in progress. They can be updated and prepared for the next NFC frame immediately after the STARTED event of the current frame has been received. Updating the TXD.FRAMECONFIG and TXD.AMOUNT during the current transmit frame or updating RXD.FRAMECONFIG during current receive frame may cause unpredictable behaviour.

In accordance with *NFC Forum, NFC Digital Protocol Technical Specification*, the least a significant bit from the least significant byte is sent on air first. The bytes are stored in increasing order, starting at the lowest address in the EasyDMA buffer in RAM.

42.4 Collision resolution

The NFC peripheral implements an automatic collision resolution function as defined by the NFC Forum.

The SENSRES and SELRES registers need to be programmed upfront in order for the collision resolution to behave correctly. Depending on the NFCIDSIZE field in SENSRES, the following registers also need to be programmed upfront:

- NFCID1 LAST if NFCID1SIZE=NFCID1Single (ID = 4 bytes);
- NFCID1_2ND_LAST and NFCID1_LAST if NFCID1SIZE=NFCID1Double (ID = 7 bytes);
- NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST if NFCID1SIZE=NFCID1Triple (ID = 10 bytes);

Table 98: NFCID1 byte allocation (top sent first on air) on page 420 explains the position of the ID bytes in NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST, depending on the ID size, and as compared to the definition used in the NFC Forum, NFC Digital Protocol Technical Specification.

Table 98: NFCID1 byte allocation (top sent first on air)

	ID = 4 bytes	ID = 7 bytes	ID = 10 bytes
NFCID1_Q			nfcid1 ₀
NFCID1_R			nfcid1 ₁
NFCID1_S			nfcid1 ₂
NFCID1_T		nfcid1 ₀	nfcid1 ₃
NFCID1_U		nfcid1 ₁	nfcid1 ₄
NFCID1_V		nfcid1 ₂	nfcid1 ₅
NFCID1_W	nfcid1 ₀	nfcid1 ₃	nfcid1 ₆
NFCID1_X	nfcid1 ₁	nfcid1 ₄	nfcid1 ₇
NFCID1_Y	nfcid1 ₂	nfcid1 ₅	nfcid1 ₈
NFCID1 Z	nfcid13	nfcid1 ₆	nfcid1 ₉

Automatic collision resolution is enabled by default.



The hardware implementation can handle the states from IDLE to ACTIVE_A automatically as defined in the *NFC Forum, NFC Activity Technical Specification*, and the other states are to be handled by software. The software keeps track of the state through events. The collision resolution will trigger an AUTOCOLRESSTARTED event when it has started. Reaching the ACTIVE_A state is indicated by the SELECTED event.

If collision resolution fails, a COLLISION event is triggered. Note that errors occurring during automatic collision resolution may also cause ERROR and/or RXERROR events to be generated. Also, other events may get generated. It is recommended that the software ignores any event except COLLISION, SELECTED and FIELDLOST during automatic collision resolution. Software shall also make sure that any unwanted SHORT or PPI shortcut are disabled during automatic collision resolution.

A pre-defined set of registers, NFC.TAGHEADER0..3, containing a valid NFCID1 value, is available in *FICR*, and can be used by software to populate the NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST registers. Refer to the release notes of the NFC stack for more details on the format.

The automatic collision resolution will be restarted, if the packets are received with CRC or parity errors while in ACTIVE_A state.

The SLP_REQ is automatically handled by the NFC peripheral. However, this results in an ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS) since the SLP_REQ has no response. This error must be ignored until the SELECTED event is triggered and this error should be cleared by the software when the SELECTED event is triggered.

42.5 Frame timing controller

The NFC peripheral includes a frame timing controller that continuously keeps track of the number of the 13.56 MHz RF-carrier clock periods since the end of the EoF of the last received frame.

The NFC peripheral can be programmed to send a responding frame within a time window or at an exact count of RF carrier periods. In case of FRAMEDELAYMODE = Window a STARTTX task triggered before the frame timing controller counter is equal to FRAMEDELAYMIN will force the transmission to halt until the counter is equal to FRAMEDELAYMIN. If the counter is within FRAMEDELAYMIN and FRAMEDELAYMAX when the STARTTX task is triggered, the peripheral will start the transmission straight away. In case of FRAMEDELAYMODE = ExactVal, a STARTTX task, triggered before the frame delay counter is equal to FRAMEDELAYMAX, will halt the actual transmission start until the counter is equal to FRAMEDELAYMAX.

In case of FRAMEDELAYMODE = WindowGrid, the behaviour is similar to the FRAMEDELAYMODE = Window, but the actual transmission between FRAMEDELAYMIN and FRAMEDELAYMAX starts on a bit grid as defined for NFC-A Listen frames (slot duration of 128 RF carrier periods).

The FRAMEDELAYMIN and FRAMEDELAYMAX values shall only be updated before the STARTTX task is triggered. Failing to do so may cause unpredictable behaviour. An ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS) will be asserted if the frame timing controller counter reaches FRAMEDELAYMAX without any STARTTX task triggered. This may happen even when the response is not required as per *NFC Forum*, *NFC Digital Protocol Technical Specification*. Any commands handled by the automatic collision resolution that don't involve a response being generated may also result in an ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS).

The frame timing controller operation is illustrated in *Figure 119: Frame timing controller* (*FRAMEDELAYMODE=Window*) on page 422. The frame timing controller automatically adjusts the frame timing counter based on the last received data bit according to NFC-A technology in the *NFC Forum, NFC Digital Protocol Technical Specification*.



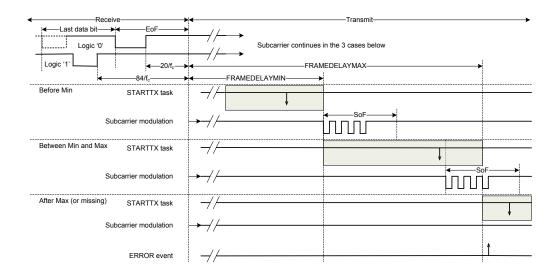


Figure 119: Frame timing controller (FRAMEDELAYMODE=Window)

42.6 Frame assembler

The NFC peripheral implements a frame assembler in hardware.

When the NFC peripheral is in the ACTIVE_A state, the software can decide to enter RX or TX mode. For RX, see *Frame disassembler* on page 423. For TX, the software must indicate the address of the source buffer in Data RAM and its size through programming the PACKETPTR and MAXCNT registers respectively, then issuing a TXSTART task.

MAXCNT must be set so that it matches the size of the frame to be sent.

The STARTED event indicates that the PACKETPTR and MAXCNT registers have been captured by the frame assembler's EasyDMA.

When asserting the STARTTX task, the frame assembler module will start reading TXD.AMOUNT.TXDATABYTES bytes (plus one additional byte if TXD.AMOUNT.TXDATABITS > 0) from the RAM position set by the PACKETPTR.

The NFC peripheral transmits the data as read from RAM, adding framing and the CRC calculated on the fly. The NFC peripheral will take (8*TXD.AMOUNT.TXDATABYTES + TXD.AMOUNT.TXDATABITS) bits and assemble a frame according to settings in TXD.FRAMECONFIG. Both short frames, standard frames and bit oriented SDD frames as specified in the NFC Forum, NFC Digital Protocol Technical Specification can be assembled by correct setting of the TXD.FRAMECONFIG register.

The bytes will be transmitted on air in the same order as they are read from RAM with a rising bit order within each byte (least significant bit first). That is, b0 will be transmitted on air before b1, and so on. The bits read from RAM will be coded into symbols as defined in the *NFC Forum*, *NFC Digital Protocol Technical Specification*.

Important: Some NFC Forum documents, such as *NFC Forum, NFC Digital Protocol Technical Specification*, define bit numbering in a byte from b1 (LSB) to b8 (MSB), while most other technical documents from the NFC Forum, and also the Nordic Semiconductor documentation, traditionally numbers them from b0 to b7. The present document uses the b0 to b7 numbering scheme. Be aware of this when comparing with the *NFC Forum, NFC Digital Protocol Technical Specification* to others.

The frame assembler can be configured in TXD.FRAMECONFIG to add Start of Frame (SoF) symbol, calculate and add parity bits, and calculate and add CRC to the data read from RAM when assembling the frame. The total frame will then be longer than what is defined by TXD.AMOUNT.TXDATABYTES and TXDATABITS. DISCARDMODE will select if the first bits in the first byte read from RAM or the last bits in the last byte read from RAM will be discarded if TXD.AMOUNT.TXDATABITS are not equal to zero. Note that if TXD.FRAMECONFIG.PARITY = Parity and TXD.FRAMECONFIG.DISCARDMODE=DiscardStart, a parity bit will be included after the non-complete first byte. No parity will be added after a non-complete last byte.



The Frame Assemble operation is illustrated in *Figure 120: Frame assemble* on page 423 for different settings in TXD.FRAMECONFIG. All shaded bits fields are added by the frame assembler. Some of these bits are optional and appearances are configured in TXD.FRAMECONFIG. Please note that the frames illustrated do not necessarily comply with the NFC specification. The figure is only to illustrate the behavior of the NFC peripheral.

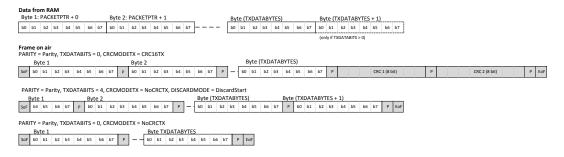


Figure 120: Frame assemble

The accurate timing for transmitting the frame on air is set using the frame timing controller settings.

42.7 Frame disassembler

The NFC peripheral implements a frame disassembler in hardware.

When the NFC peripheral is in the ACTIVE_A state, the software can decide to enter RX or TX mode. For TX, see *Frame assembler* on page 422. For RX, the software must indicate the address of the destination buffer in Data RAM and its size through programming the PACKETPTR and MAXCNT registers respectively, then issuing a ENABLERXDATA task.

The STARTED event indicates that the PACKETPTR and MAXCNT registers have been captured by the frame disassembler's EasyDMA.

When an incoming frame starts, the RXFRAMESTART event will get issued and data will be written to the buffer in Data RAM. The frame disassembler will verify and remove on the fly any parity bits and SoF and End of Frame (EoF) symbols based on RXD.FRAMECONFIG register configuration. It will, however, verify and transfer the CRC bytes into RAM, if the CRC is was enabled through RXD.FRAMECONFIG.

When an EoF symbol is detected, the NFC peripheral will assert the RXFRAMEEND event and write the RXD.AMOUNT register to indicate numbers of received bytes and bits in the data packet. The module does not interpret the content of the data received from the remote NFC device, except for SoF, EoF, parity and CRC checking, as described above. The Frame disassemble operation is illustrated in *Figure 121: Frame disassemble illustration* on page 423.

Per NFC specification, the time between end of frame to the next start of frame can be as short as $86 \mu s$, so care must be taken that PACKETPTR and MAXCNT are ready and ENABLERXDATA is issued on time after the end of previous frame. The use of a PPI shortcut from TXFRAMEEND to ENABLERXDATA is recommended.

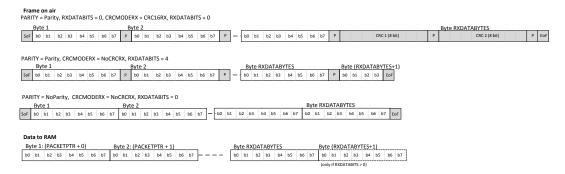


Figure 121: Frame disassemble illustration



42.8 Antenna interface

In ACTIVATED state, an amplitude regulator will adjust the voltage swing on the antenna pins to a value that is within the V_{swinq} limit.

Refer to NFCT Electrical Specification on page 436.

42.9 NFCT antenna recommendations

The NFCT antenna coil must be connected differential between NFC1 and NFC2 pins of the device.

Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56 MHz.

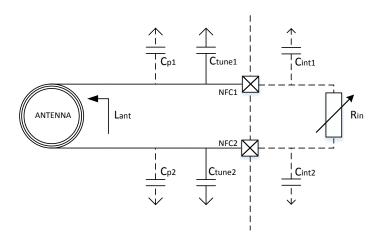


Figure 122: NFCT antenna recommendations

The required tuning capacitor value is given by the below equations:

$$C'_{tune} = \frac{1}{(2\pi \cdot 13.56 \text{ MHz})^2 \cdot L_{ant}} \quad where \ C'_{tune} = \frac{1}{2} \cdot (C_p + C_{int} + C_{tune})$$

$$and \ C_{tune1} = C_{tune2} = C_{tune} \qquad C_{p1} = C_{p2} = C_p \qquad C_{int1} = C_{int2} = C_{int}$$

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56 \text{ MHz})^2 \cdot L_{ant}} - C_p - C_{int}$$

An antenna inductance of $L_{ant} = 2 \mu H$ will give tuning capacitors in the range of 130 pF on each pin. For good performance, match the total capacitance on NFC1 and NFC2.

42.10 Battery protection

If the antenna is exposed to a strong NFC field, current may flow in the opposite direction on the supply due to parasitic diodes and ESD structures.

If the battery used does not tolerate return current, a series diode must be placed between the battery and the device in order to protect the battery.



42.11 References

NFC Forum, NFC Analog Specification version 1.0, www.nfc-forum.org

NFC Forum, NFC Digital Protocol Technical Specification version 1.1, www.nfc-forum.org

NFC Forum, NFC Activity Technical Specification version 1.1, www.nfc-forum.org

42.12 Registers

Table 99: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40005000	NFCT	NFCT	Near Field Communication Tag		

Table 100: Register Overview

Register	Offset	Description
TASKS_ACTIVATE	0x000	Activate NFC peripheral for incoming and outgoing frames, change state to activated
TASKS_DISABLE	0x004	Disable NFC peripheral
TASKS_SENSE	0x008	Enable NFC sense field mode, change state to sense mode
TASKS_STARTTX	0x00C	Start transmission of a outgoing frame, change state to transmit
TASKS_ENABLERXDATA	0x01C	Initializes the EasyDMA for receive.
TASKS_GOIDLE	0x024	Force state machine to IDLE state
TASKS_GOSLEEP	0x028	Force state machine to SLEEP_A state
EVENTS_READY	0x100	The NFC peripheral is ready to receive and send frames
EVENTS_FIELDDETECTED	0 0x104	Remote NFC field detected
EVENTS_FIELDLOST	0x108	Remote NFC field lost
EVENTS_TXFRAMESTAR	T 0x10C	Marks the start of the first symbol of a transmitted frame
EVENTS_TXFRAMEEND	0x110	Marks the end of the last transmitted on-air symbol of a frame
EVENTS_RXFRAMESTAR	T 0x114	Marks the end of the first symbol of a received frame
EVENTS_RXFRAMEEND	0x118	Received data have been checked (CRC, parity) and transferred to RAM, and EasyDMA has ended
		accessing the RX buffer
EVENTS_ERROR	0x11C	NFC error reported. The ERRORSTATUS register contains details on the source of the error.
EVENTS_RXERROR	0x128	NFC RX frame error reported. The FRAMESTATUS.RX register contains details on the source of the
		error.
EVENTS_ENDRX	0x12C	RX buffer (as defined by PACKETPTR and MAXLEN) in Data RAM full.
EVENTS_ENDTX	0x130	Transmission of data in RAM has ended, and EasyDMA has ended accessing the TX buffer
EVENTS_AUTOCOLRESST	Г 0x138	Auto collision resolution process has started
EVENTS_COLLISION	0x148	NFC Auto collision resolution error reported.
EVENTS_SELECTED	0x14C	NFC Auto collision resolution successfully completed
EVENTS_STARTED	0x150	EasyDMA is ready to receive or send frames.
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSTATUS	0x404	NFC Error Status register
FRAMESTATUS.RX	0x40C	Result of last incoming frames
CURRENTLOADCTRL	0x430	Current value driven to the NFC Load Control
FIELDPRESENT	0x43C	Indicates the presence or not of a valid field
FRAMEDELAYMIN	0x504	Minimum frame delay
FRAMEDELAYMAX	0x508	Maximum frame delay
FRAMEDELAYMODE	0x50C	Configuration register for the Frame Delay Timer
PACKETPTR	0x510	Packet pointer for TXD and RXD data storage in Data RAM
MAXLEN	0x514	Size of allocated for TXD and RXD data storage buffer in Data RAM
TXD.FRAMECONFIG	0x518	Configuration of outgoing frames
TXD.AMOUNT	0x51C	Size of outgoing frame
RXD.FRAMECONFIG	0x520	Configuration of incoming frames



Register	Offset	Description
RXD.AMOUNT	0x524	Size of last incoming frame
NFCID1_LAST	0x590	Last NFCID1 part (4, 7 or 10 bytes ID)
NFCID1_2ND_LAST	0x594	Second last NFCID1 part (7 or 10 bytes ID)
NFCID1_3RD_LAST	0x598	Third last NFCID1 part (10 bytes ID)
SENSRES	0x5A0	NFC-A SENS_RES auto-response settings
SELRES	0x5A4	NFC-A SEL_RES auto-response settings

42.12.1 SHORTS

Address offset: 0x200

Shortcut register

Bit	numbe	er		31	1 30 :	29	28 :	27 :	26 2	5 2	24 2	3 22	21	20	19 1	8 1	.7 1	6 1	5 14	4 13	3 12	11	10	9	8 7	' (5 5	4	3	2	1 0	ĺ
Id																															ВА	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0 (0 0	0	0	0	0 (0 () (0	0	0	0	0	0	0 () (0	0	0	0	0 0	ı
Id	RW	Field	Value Id	Va	alue						C	escr	iptic	on																		
Α	RW	FIELDDETECTED_ACTIVAT	E								S	hort	cut k	oetv	wee	n FII	ELD	DET	EC	ΓED	eve	nt a	nd A	ACT	IVAT	Έt	ask					
											S	ee <i>E</i>	VEN	TS_	FIEL	DDI	ETE	CTE	D a	nd 1	TASK	S_A	CTI	VAT	Έ							
			Disabled	0								isab	le sh	ort	cut																	
			Enabled	1							Е	nabl	e sh	orto	cut																	
В	RW	FIELDLOST_SENSE									S	hort	cut k	oetv	wee	n FII	ELD	LOS	T e	ven	t an	d SE	NSE	tas	sk							
											S	ee <i>E</i>	VEN	TS_	FIEL	DLC	OST	and	TA	SKS	_SE	NSE										
			Disabled	0							C	isab	le sh	ort	cut																	
			Enabled	1							Е	nabl	e sh	orto	cut																	

42.12.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit r	numbe	er		31	30	29	28 2	7 2	6 2	5 24	1 23	3 2	22 <u>2</u>	1 2	00 1	19 1	8 1	17 ^	16	15 1	14 1	3 1	2 1	1 1	0 9	8	7	6	5	4	3	2 -	1 0
Id																S					N			 . k									 3 A
	et 0x0	0000000		0	0	0	0 0) (0 0	0	0)	0 (0 (0	0	0	0	0 0			0	0				0			0 0
Id	RW	Field	Value Id	Va	lue						D	es	crip	tio	n																		
Α	RW	READY									Er	na	ble (or c	disa	ble	int	err	upt	for	RE	ADY	ev	ent									
											Se	ee	EVE	NT	'S I	REA	DΥ																
			Disabled	0									able		_																		
			Enabled	1							Er	na	ble																				
В	RW	FIELDDETECTED									Er	na	ble o	or c	disa	ble	int	err	upt	for	FIE	LDD	ETI	ECT	ED	eve	nt						
											Se	ee	EVE	NT	'S 1	FIEL	DD	ETE	ст	ED													
			Disabled	0									able		_																		
			Enabled	1							Er	na	ble																				
С	RW	FIELDLOST									Er	na	ble (or c	disa	ble	int	err	upt	for	FIE	LDL	os ⁻	Γev	ent								
											Se	ee	EVE	NT	'S I	FIEL	DLO	OST															
			Disabled	0									able		_																		
			Enabled	1							Er	na	ble																				
D	RW	TXFRAMESTART									Er	na	ble (or c	disa	ble	int	err	upt	for	TX	FRA	ME	STA	RT	eve	nt						
											Se	ee	EVE	NT	s	TXFI	RAI	MES	TA	RT													
			Disabled	0									able																				
			Enabled	1							Er	na	ble																				
E	RW	TXFRAMEEND									Er	na	ble (or c	disa	ble	int	err	upt	for	тх	FRA	ME	ENE) ev	ent							
											Se	66	EVE	NT	ς :	TXFI	RAI	MFF	NI)													
			Disabled	0									able																				
			Enabled	1									ble																				
F	RW	RXFRAMESTART									Er	na	ble o	or c	disa	able	int	err	upt	for	RX	FRA	ME	STA	RT	eve	nt						



Bitı	numb	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					TSR NMLK HGFEDCBA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
					See EVENTS_RXFRAMESTART
			Disabled	0	Disable
			Enabled	1	Enable
G	RW	RXFRAMEEND			Enable or disable interrupt for RXFRAMEEND event
					See EVENTS_RXFRAMEEND
			Disabled	0	Disable
			Enabled	1	Enable
Н	RW	ERROR			Enable or disable interrupt for ERROR event
					See EVENTS_ERROR
			Disabled	0	Disable
			Enabled	1	Enable
K	RW	RXERROR			Enable or disable interrupt for RXERROR event
					See EVENTS_RXERROR
			Disabled	0	Disable
			Enabled	1	Enable
L	RW	ENDRX			Enable or disable interrupt for ENDRX event
					See EVENTS_ENDRX
			Disabled	0	Disable
			Enabled	1	Enable
M	RW	ENDTX			Enable or disable interrupt for ENDTX event
					See EVENTS_ENDTX
			Disabled	0	Disable
			Enabled	1	Enable
N	RW	AUTOCOLRESSTARTED			Enable or disable interrupt for AUTOCOLRESSTARTED event
					See EVENTS_AUTOCOLRESSTARTED
			Disabled	0	Disable
			Enabled	1	Enable
R	RW	COLLISION			Enable or disable interrupt for COLLISION event
					See EVENTS_COLLISION
			Disabled	0	Disable
			Enabled	1	Enable
S	RW	SELECTED			Enable or disable interrupt for SELECTED event
					See EVENTS_SELECTED
			Disabled	0	Disable
			Enabled	1	Enable
Т	RW	STARTED			Enable or disable interrupt for STARTED event
					See EVENTS_STARTED
			Disabled	0	Disable
			Enabled	1	Enable

42.12.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
Id		TSR NMLK HGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW READY		Write '1' to Enable interrupt for READY event

See EVENTS_READY



Bit ı	numbe	er		31 30) 29	28 2	27 26	25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id									TSR NMLK HGFEDCB
Res	et 0x0	0000000		0 0	0	0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	9				Description
			Set	1					Enable
			Disabled	0					Read: Disabled
В	D\A/	FIELDDETECTED	Enabled	1					Read: Enabled Write '1' to Enable interrupt for FIELDDETECTED event
Б	NVV	FIELDDETECTED							See EVENTS_FIELDDETECTED
			Set	1					Enable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
С	RW	FIELDLOST							Write '1' to Enable interrupt for FIELDLOST event
									See EVENTS_FIELDLOST
			Set	1					Enable
			Disabled	0					Read: Disabled
D	D\A/	TXFRAMESTART	Enabled	1					Read: Enabled
U	NVV	IXFRAIVIESTANT							Write '1' to Enable interrupt for TXFRAMESTART event
									See EVENTS_TXFRAMESTART
			Set	1					Enable
			Disabled	0					Read: Disabled
E	D\A/	TXFRAMEEND	Enabled	1					Read: Enabled Write '1' to Enable interrupt for TXFRAMEEND event
_	NVV	TAFRAMEEND							
									See EVENTS_TXFRAMEEND
			Set	1					Enable
			Disabled Enabled	0					Read: Disabled Read: Enabled
F	RW	RXFRAMESTART	Eliablea	1					Write '1' to Enable interrupt for RXFRAMESTART event
			Set	1					See EVENTS_RXFRAMESTART Enable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
G	RW	RXFRAMEEND							Write '1' to Enable interrupt for RXFRAMEEND event
									See EVENTS_RXFRAMEEND
			Set	1					Enable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
Н	RW	ERROR							Write '1' to Enable interrupt for ERROR event
									See EVENTS_ERROR
			Set	1					Enable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
K	RW	RXERROR							Write '1' to Enable interrupt for RXERROR event
									See EVENTS_RXERROR
			Set	1					Enable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
L	RW	ENDRX							Write '1' to Enable interrupt for ENDRX event
									See EVENTS_ENDRX
			Set	1					Enable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
М	RW	ENDTX							Write '1' to Enable interrupt for ENDTX event
									See EVENTS_ENDTX
			Set	1					Enable



Bit	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			TSR NMLK HGFEDCBA
Res	set 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
N	RW AUTOCOLRESSTARTED		Write '1' to Enable interrupt for AUTOCOLRESSTARTED event
			See EVENTS_AUTOCOLRESSTARTED
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
R	RW COLLISION		Write '1' to Enable interrupt for COLLISION event
			See EVENTS COLLISION
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
S	RW SELECTED		Write '1' to Enable interrupt for SELECTED event
			See EVENTS_SELECTED
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
Т	RW STARTED		Write '1' to Enable interrupt for STARTED event
			See EVENTS_STARTED
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
		Lilabieu	1 Redu. Ellableu

42.12.4 INTENCLR

Address offset: 0x308

Disable interrupt

		·			
Bit	number	•		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					TSR NMLK HGFEDCBA
Res	et 0x00	000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	READY			Write '1' to Disable interrupt for READY event
					See EVENTS_READY
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	FIELDDETECTED			Write '1' to Disable interrupt for FIELDDETECTED event
					See EVENTS_FIELDDETECTED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	FIELDLOST			Write '1' to Disable interrupt for FIELDLOST event
					See EVENTS_FIELDLOST
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	TXFRAMESTART			Write '1' to Disable interrupt for TXFRAMESTART event
					See EVENTS_TXFRAMESTART
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled



Bit r	numb	er		3:	1 30	29	28	27 2	26 2	25 2	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id											TSR NMLK HGFEDCBA
Res		00000000					0	0	0	0 (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	V	alue						Description
Ε	RW	TXFRAMEEND									Write '1' to Disable interrupt for TXFRAMEEND event
											See EVENTS_TXFRAMEEND
			Clear	1							Disable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
F	RW	RXFRAMESTART									Write '1' to Disable interrupt for RXFRAMESTART event
											See EVENTS_RXFRAMESTART
			Clear	1							Disable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
G	RW	RXFRAMEEND									Write '1' to Disable interrupt for RXFRAMEEND event
											See EVENTS_RXFRAMEEND
			Clear	1							Disable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
Н	RW	ERROR									Write '1' to Disable interrupt for ERROR event
											See EVENTS_ERROR
			Clear	1							Disable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
K	RW	RXERROR									Write '1' to Disable interrupt for RXERROR event
											See EVENTS_RXERROR
			Clear	1							Disable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
L	RW	ENDRX									Write '1' to Disable interrupt for ENDRX event
											See EVENTS_ENDRX
			Clear	1							Disable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
М	RW	ENDTX									Write '1' to Disable interrupt for ENDTX event
			Clear	1							See EVENTS_ENDTX Disable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
N	RW	AUTOCOLRESSTARTED	2.102.00	-							Write '1' to Disable interrupt for AUTOCOLRESSTARTED event
			Clear	1							See EVENTS_AUTOCOLRESSTARTED
			Clear Disabled	1							Disable Read: Disabled
			Enabled	1							Read: Enabled
R	RW	COLLISION	Ellabica	_							Write '1' to Disable interrupt for COLLISION event
.,											
			Class	_							See EVENTS_COLLISION
			Clear	1							Disable Pead: Disabled
			Disabled Enabled	0							Read: Disabled Read: Enabled
S	R/M/	SELECTED	Lilableu	1							Write '1' to Disable interrupt for SELECTED event
J	11.44	SELECTED									
											See EVENTS_SELECTED
			Clear	1							Disable
			Disabled	0							Read: Disabled
_	DVA	STARTER	Enabled	1							Read: Enabled
Т	кW	STARTED									Write '1' to Disable interrupt for STARTED event



Bit number	31 30 29 28 27	26 25 24 23 22 21 20 19	18 17 16	5 15 14	13 12	11 10	9	8	7	6	5 4	4 3	2	1 0
Id		T S	R	N	М	L K			Н	G	F	E D	С	ВА
Reset 0x00000000	0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0	0 0	0 0	0 0	0	0	0	0	0	0 0	0	0 0
Id RW Field Value Id	Value	Description												
		See EVENTS_ST	ARTED											
Clear	1	Disable												
Disabled	0	Read: Disabled												
Enabled	1	Read: Enabled												

42.12.5 ERRORSTATUS

Address offset: 0x404 NFC Error Status register

Write a bit to '1' to clear it. Writing '0' has no effect.

Bit r	iumbe	r		3:	1 30	29	28	3 27	7 26	5 25	24	23	22	21	20 :	19 1	l8 1	7 1	6 15	5 14	13	12	11 1	0 9	8	7	6	5	4	3 :	2 1	L 0
Id																														D (С	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	V	alue	•						De	scri	ptic	n																	
Α	RW	FRAMEDELAYTIMEOUT										No	ST/	٩RT	TX t	ask	trig	ger	ed b	efo	re e	iqx	atio	n of	the	tim	e se	t in				
												FR	AMI	EDE	LAY	MA	Х															
С	RW	NFCFIELDTOOSTRONG										Fie	eld le	evel	is t	oo l	high	at	max	(loa	d re	esist	ance	:								
D	RW	NFCFIELDTOOWEAK										Fie	eld le	evel	is t	oo l	ow	at r	nin	load	l res	sista	nce									

42.12.6 FRAMESTATUS.RX

Address offset: 0x40C

Result of last incoming frames

Write a bit to '1' to clear it. Writing '0' has no effect.

Bit r	numbe	r		31	30 2	29 2	28 2	7 2	26 2	5 2	24 2	3 22	2 21	20	19	18	17	16	15 :	L4 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id																													С	В		Α
Res	et 0x0(0000000		0	0	0	0 (0	0 (0 (0 (0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	on																		
Α	RW	CRCERROR									Ν	lo va	alid I	End	of F	rar	ne o	dete	ecte	d												
			CRCCorrect	0							٧	'alid	CRC	de	tect	ed																
			CRCError	1							C	RC r	ecei	ivec	l do	es r	not	mat	ch	loca	l che	ck										
В	RW	PARITYSTATUS									Р	arity	/ sta	tus	of r	ece	eive	d fr	ame	è												
			ParityOK	0							F	ram	e re	ceiv	ed '	with	h pa	rity	Ok													
			ParityError	1							F	ram	e re	ceiv	ed '	with	h pa	rity	er	or												
С	RW	OVERRUN									C	ver	run (dete	ecte	d																
			NoOverrun	0							Ν	lo o	/erri	un c	lete	cte	d															
			Overrun	1							C	ver	run (erro	r																	

42.12.7 CURRENTLOADCTRL

Address offset: 0x430

Current value driven to the NFC Load Control

Bit	numbe	er		31	1 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 1	11 1	0 9	8	3 7	6	5	4	3	2	1	0
Id																													Α	Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	C	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																			
Α	R	CURRENTLOADCTRL										Cu	rrer	nt v	alue	e dr	ive	n to	th	e N	FC L	.oad	d Co	ntr	ol									_

42.12.8 FIELDPRESENT

Address offset: 0x43C



Indicates the presence or not of a valid field

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21 2	20	19	18	17 :	16 :	15 :	14 :	13	12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id																																	В	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	scri	ptio	n																			
Α	R	FIELDPRESENT										Ind	icat	es t	he	pre	ser	ice (or r	ot	of a	ı va	llid	fiel	d. A	vai	labl	e o	nly	in				
											1	the	act	tivat	ed	sta	te.																	
			NoField	0								No	vali	id fi	eld	det	ect	ed																
			FieldPresent	1							,	Val	id f	ield	de	tect	ed																	
В	R	LOCKDETECT										Ind	icat	es i	f th	ie lo	w l	eve	l ha	as lo	ock	ed 1	to t	he	field	t								
			NotLocked	0								Not	t lo	ckec	l to	fie	d																	
			Locked	1								Loc	kec	to	fiel	d																		

42.12.9 FRAMEDELAYMIN

Address offset: 0x504 Minimum frame delay

Bit	numbe	er		31	30	29	28 2	7 2	6 2	5 24	4 23	22	21	20	19	18	17 :	16 1	.5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2 :	1 0	
Id																			Δ,	4 Α	Δ /	A /	A	Α	Α	Α	Α	Α	Α	A	4 /	А А	
Res	et 0x0	0000480		0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0 () () () 1	0	0	1	0	0	0	0	0 (0 0	
Id	RW	Field	Value Id	Va	lue						D	escr	iptio	on																			
Α	RW	FRAMEDELAYMIN									М	inin	num	fra	me	del	av i	n nı	umb	oer	of 1	13.5	6 M	Hz	cloc	ks							

42.12.10 FRAMEDELAYMAX

Address offset: 0x508 Maximum frame delay

Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 :	16 15 14 13 12 11	10 9 8 7 6 5	4 3 2 1 0
Id				AAAAA	AAAAAA	
Reset 0x00001000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 1 0	0 0 0 0 0 0	00000
Id RW Field	Value Id	Value	Description			
A RW FRAMEDELAYMA	ΔX		Maximum frame delay	in number of 13 56	6 MHz clocks	

42.12.11 FRAMEDELAYMODE

Address offset: 0x50C

Configuration register for the Frame Delay Timer

Bit	numb	er		31 3	0 29	28	27	26 2	5 2	24 2	3 2	22 2	1 20	0 1	9 1	3 17	7 16	15	14	13	12	11	10	9	8 7	7 (6 5	5	4	3 2	1	. 0
Id																															Α	A A
Res	et 0x0	0000001		0 (0	0	0	0 () (0 (0 (0 (0 0	•	0	0	0	0	0	0	0	0	0	0	0 0) (0 (0	0 (0	0	1
Id	RW	Field	Value Id	Value							Description																					
Α	RW	FRAMEDELAYMODE									Configuration register for the Frame Delay Timer																					
			FreeRun	0						Transmission is independent of frame timer and will start when																						
										the STARTTX task is triggered. No timeout.																						
			Window	1						Frame is transmitted between FRAMEDELAYMIN and																						
				FRAMEDELAYMAX																												
			ExactVal	2							Frame is transmitted exactly at FRAMEDELAYMAX																					
			WindowGrid	3	3 Frame is transmitted on a bit grid between FRAM											M	EDE	LAY	/MI	N												
					and FRAMEDELAYMAX																											

42.12.12 PACKETPTR

Address offset: 0x510

Packet pointer for TXD and RXD data storage in Data RAM



Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 :	16 :	15 :	14 :	L3 1	12 1	.1 1	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α .	4 Δ	Α	Α	Α	Α	Α	Α	Α	A	А А
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	PTR										Pac	ket	ро	inte	r fo	r T	XD i	and	l RX	D d	ata	sto	rage	in	Dat	a R	٩M.	Thi	is			

address is a byte aligned RAM address.

42.12.13 MAXLEN

Address offset: 0x514

Size of allocated for TXD and RXD data storage buffer in Data RAM

Bit	number	31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A
Res	et 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field Value Id	Value	Description
Α	RW MAXLEN	[0257]	Size of allocated for TXD and RXD data storage buffer in Data
			RAM

42.12.14 TXD.FRAMECONFIG

Address offset: 0x518

Configuration of outgoing frames

Rit i	number			21 2	n 20	1201	ר דו	6 25	: 24	23.2	ר כי	1 20	10	10	17 1	16 1	15 1	1 13	112	11 1	0 0	Q	7	6	5	4 =	2	1	0
	lullibei			31 3	0 23	20 2	. / _	0 23	, 24	. 23 2	LZ Z	.1 20	13	10	1/1	.0 1		4 15	12	11.	.0 3	٥	,	U	_		_	D T	^
Id																										D 	С	В	A
Res	et 0x0000	00017		0 () 0	0	0 (0	0	0 (0 (0 0	0	0	0	0	0 () 0	0	0	0 0	0	0	0	0	1 (1	1	1
Id	RW Fi	eld	Value Id	Valu	е					Desc	crip	tion																	
Α	RW PA	ARITY								Addi	ing	parit	y or	no	t in t	he	frar	ne											
			NoParity	0						Parit	ty is	not	add	led	in TX	(fra	ame	S											
			Parity	1						Parit	ty is	add	ed 1	ΓX f	rame	es													
В	RW DI	SCARDMODE								Disc	ardi	ing u	nus	ed l	oits i	n st	tart	or a	t end	d of	a Fra	me							
			DiscardEnd	0						Unu	sed	bits	is d	isca	rded	d at	end	of	ram	e									
			DiscardStart	1						Unu	sed	bits	is di	isca	rdec	d at	sta	rt of	fran	ne									
С	RW SC	DF .								Addi	ing	SoF	or no	ot ii	n TX	fra	mes												
			NoSoF	0						Star	t of	Fran	ne s	yml	ool n	ot	add	ed											
			SoF	1						Star	t of	Fran	ne s	yml	ool a	dde	ed												
D	RW CF	RCMODETX								CRC	mo	de fo	or o	utgo	oing	fra	mes												
			NoCRCTX	0						CRC	is n	ot a	dde	d to	the	fra	me												
			CRC16TX	1						16 b	it C	RC a	dde	d to	the	fra	me	base	ed or	n all	the	data	rea	ad fi	om				
										RAN	1 th	at is	use	d in	the	fra	me												

42.12.15 TXD.AMOUNT

Address offset: 0x51C Size of outgoing frame

Bit	numbe	er		31	30	29 2	28 2	7 26	5 25	24	23	22	21 2	20 1	19 1	8 1	7 1	6 15	5 14	13	12 1	1 1	9	8	7	6	5	4	3 2	2 1	1 0
Id																					1	3 E	В	В	В	В	В	В	ВА	\ <i>A</i>	A A
Res	et 0x0	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0 (0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue						Des	scri	otio	n																	
A	RW	TXDATABITS		[0.	.7]						be The bits	incl e DI: s is o	ude SCA disc	d ir RDI ard	n the MO ed a	e fra DE f	ame field ne si	e (ex l in l tart	clud RAI or a	ding MEC	e re parit ONF e end	y bi IG.1	t). 'X se	elec	ts if	unı	use	d			
В	RW	TXDATABYTES		[0.	.257]						mbe			•		,				l be	incl	ude	d in	the	fra	me,	,			



42.12.16 RXD.FRAMECONFIG

Address offset: 0x520

Configuration of incoming frames

Bit n	umbe	er		31	30 2	9 2	8 27	7 26	25	24	23	22	21	20	19	18	17	16	15 1	4 1	3 1	2 1:	10	9	8	7	6	5 4	1 3	2	1	0
Id																												(В		Α
Rese	t 0x0	0000015		0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 1	0	1	0	1
Id	RW	Field	Value Id	Val	ue						De	scri	ptic	on																		
Α	RW	PARITY									Pa	rity	exp	ect	ed (or r	ot i	n R	X fr	ame	9											
			NoParity	0							Pa	rity	is n	ot e	expe	ecte	ed ii	n R	K fra	me	S											
			Parity	1							Pa	rity	is e	хре	cte	d ir	n RX	fra	me	5												
В	RW	SOF									So	F ex	pec	tec	or	not	t in	RX 1	fran	nes												
			NoSoF	0							Sta	art c	of Fr	am	ie sy	/ml	ool i	s n	ot e	кре	cted	l in	RX f	ram	ies							
			SoF	1							Sta	art o	of Fr	am	ie sy	/ml	ool i	s ex	крес	ted	in I	RX f	ram	es								
С	RW	CRCMODERX									CR	C m	ode	e fo	r in	con	ning	fra	me	S												
			NoCRCRX	0							CR	C is	not	ex	pec	ted	l in I	RX f	ran	ies												
			CRC16RX	1							Las	st 1	6 bit	ts ir	n RX	(fra	ame	is	CRC	CR	C is	che	cke	d ar	nd C	RCS	TA	ΓUS				
											up	dat	ed																			

42.12.17 RXD.AMOUNT

Address offset: 0x524

Size of last incoming frame

Bit	numbe	er		31	1 30	29	28	3 27	20	6 25	5 2	4 2	3 2	22	21	20	19	18	17	16	15	14	13	12	11	10 9	9	8 7	' E	5 5	5 4	3	2	1	0
Id																									В	В	3	ВЕ	E	3 B	3 E	В	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	(0 ()	0	0	0	0	0	0	0	0	0	0	0	0	0 ()	0 ((0) (0	0	0	0
Id	RW	Field	Value Id	Va	alue							D	es	cri	ptic	on																			
A	R	RXDATABITS										(i	ncl	luc ne	ding	CR ith	0 d	but lata	ex by	clud	, ling and	les	rity	and	l So	F/Ec	F f	tha ram are	ing).	d				
В	R	RXDATABYTES													er c					•						fran	ne ((incl	udi	ng (CRC	,			

42.12.18 NFCID1_LAST

Address offset: 0x590

Last NFCID1 part (4, 7 or 10 bytes ID)

Bit	numbe	er		31	. 30	29	28	3 27	7 26	5 25	5 24	4 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				D	D	D	D	D	D	D	D) C	. c	С	С	С	С	С	С	В	В	В	В	В	В	В	В	Α	Α	Α	Α	ΑА	Α Α	A A
Res	et 0x0	0006363		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1	1	0	0 0) 1	1
Id	RW	Field	Value Id	Va	lue							D	escri	ptic	on																			
Α	RW	NFCID1_Z										N	FCID	1 b	/te	Z (v	ery	las	t by	yte	sen	t)												
В	RW	NFCID1_Y										N	FCID	1 b	/te	Υ																		
С	RW	NFCID1_X										N	FCID	1 b	/te	X																		
D	RW	NFCID1 W										N	FCID	1 h	ıtο	۱۸/																		

42.12.19 NFCID1_2ND_LAST

Address offset: 0x594

Second last NFCID1 part (7 or 10 bytes ID)



Bit r	umbe	r		31 30	29	28	27	26 :	25 2	24 :	23 2	22 2	21 2	0 19	18	17	16	15	14	13 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id											С	C (c c	: C	С	С	С	В	В	ВЕ	8 B	В	В	В	Α	Α	Α	Α	А А	Α	Α
Res	t 0x0	0000000		0 0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value	•					ı	Des	crip	tion	ı																	
Α	RW	NFCID1_V								ı	NFC	ID1	byt	e V																	
В	RW	NFCID1_U								ı	NFC	ID1	byt	e U																	
С	RW	NFCID1_T								- 1	NFC	ID1	byt	e T																	

42.12.20 NFCID1_3RD_LAST

Address offset: 0x598

Third last NFCID1 part (10 bytes ID)

Bitı	numbe	er		3	1 30	29	28	8 27	7 26	5 25	5 24	1 23	3 22	2 21	. 20	19	18	17	16	15	14	13 :	12 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id												С	C	. c	С	С	С	С	С	В	В	В	В	3 E	В	В	Α	Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	٧	'alue	2						De	esc	ript	ion																		
Α	RW	NFCID1_S										NI	CII	D1 b	yte	S																	
В	RW	NFCID1_R										NI	CII	D1 b	yte	R																	
С	RW	NFCID1_Q										NI	CII	D1 k	yte	Q																	

42.12.21 SENSRES

Address offset: 0x5A0

NFC-A SENS_RES auto-response settings

Bit	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				EEEEDDDDCCBAAAA
Res	et 0x00000001		0 0 0 0 0 0 0 0	000000000000000000000000000000000000000
Id	RW Field	Value Id	Value	Description
Α	RW BITFRAMESDD			Bit frame SDD as defined by the b5:b1 of byte 1 in SENS_RES
				response in the NFC Forum, NFC Digital Protocol Technical
				Specification
		SDD00000	0	SDD pattern 00000
		SDD00001	1	SDD pattern 00001
		SDD00010	2	SDD pattern 00010
		SDD00100	4	SDD pattern 00100
		SDD01000	8	SDD pattern 01000
		SDD10000	16	SDD pattern 10000
В	RW RFU5			Reserved for future use. Shall be 0.
С	RW NFCIDSIZE			NFCID1 size. This value is used by the Auto collision resolution
				engine.
		NFCID1Single	0	NFCID1 size: single (4 bytes)
		NFCID1Double	1	NFCID1 size: double (7 bytes)
		NFCID1Triple	2	NFCID1 size: triple (10 bytes)
D	RW PLATFCONFIG			Tag platform configuration as defined by the b4:b1 of byte 2
				in SENS_RES response in the NFC Forum, NFC Digital Protocol
				Technical Specification
Ε	RW RFU74			Reserved for future use. Shall be 0.

42.12.22 SELRES

Address offset: 0x5A4

NFC-A SEL_RES auto-response settings



Bit	numbe	er		31	30 2	9	28 2	27 :	26 2	25 2	24 2	23 2	2 2	1 20	19	18	3 17	16	15	14	13	12	11 1	.0	Э	8 7	6	5	4	3	2	1 0
Id																										Е	D	D	С	С	В	A A
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Desc	rip	tion																		
Α	RW	RFU10									F	Rese	rve	d fo	r fu	tur	e us	e. S	hal	l be	0.											
В	RW	CASCADE									(Casc	ade	e bit	(co	ntro	olle	d by	ha	rdw	are	e, w	rite	has	no	effe	ct)					
			Complete	0							1	NFCI	D1	con	ple	te																
			NotComplete	1							1	NFCI	D1	not	con	nple	ete															
С	RW	RFU43									F	Rese	rve	d fo	r fu	tur	e us	e. S	hal	l be	0.											
D	RW	PROTOCOL									F	rot	осо	l as	defi	ine	d by	the	e b7	':b6	of	SEL	_RE	s re	spc	nse	in t	he				
											1	NFC	For	um,	NF	C D	igita	al Pi	oto	col	Te	chni	cal :	Spe	cifi	atio	n					
Е	RW	RFU7									F	Rese	rve	d fo	r fu	tur	e us	e. S	hal	l be	0.											

42.13 Electrical specification

42.13.1 NFCT Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
f _c	Frequency of operation		13.56		MHz
C _{MI}	Carrier modulation index	95			%
DR	Data Rate		106		kbps
f_s	Modulation sub-carrier frequency		f _c /16		MHz
V _{swing}	Peak differential Input voltage swing on NFC1 and NFC2			VDD	Vp
V _{sense}	Peak differential Field detect threshold level on NFC1-NFC2 ³⁶		1.0		Vp
I _{sense}	Current in SENSE STATE		100		nA
I _{activated}	Current in ACTIVATED STATE		480		μΑ
R _{in_min}	Minimum input resistance when regulating voltage swing			40	Ω
R _{in_max}	Maximum input resistance when regulating voltage swing	1.0			kΩ
R _{in_loadmod}	Input resistance when load modulating	8		22	Ω
I _{max}	Maximum input current on NFC pins			80	mA

42.13.2 NFCT Timing Parameters

Symbol	Description	Min.	Тур.	Max.	Units
t _{activate}	Time from task_ACTIVATE in SENSE or DISABLE state to ACTIVATE_A or IDLE state ³⁷			500	us
t _{sense}	Time from remote field is present in SENSE mode to FIELDDETECTED event is asserted			20	us

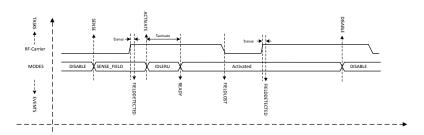


Figure 123: NFCT timing parameters (Shortcuts for FIELDDETECTED and FIELDLOST are disabled)

Input is high impedance in sense mode
 Does not account for voltage supply and oscillator startup times



43 PDM — Pulse density modulation interface

The pulse density modulation (PDM) module enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. The PDM module generates the PDM clock and supports single-channel or dual-channel (Left and Right) data input. Data is transferred directly to RAM buffers using EasyDMA.

Listed here are the main features for PDM:

- Up to two PDM microphones configured as a Left/Right pair using the same data input
- 16 kHz output sample rate, 16-bit samples
- EasyDMA support for sample buffering
- · HW decimation filters

The PDM module illustrated in *Figure 124: PDM module* on page 437 is interfacing up to two digital microphones with the PDM interface. It implements EasyDMA, which relieves real-time requirements associated with controlling the PDM slave from a low priority CPU execution context. It also includes all the necessary digital filter elements to produce PCM samples. The PDM module allows continuous audio streaming.

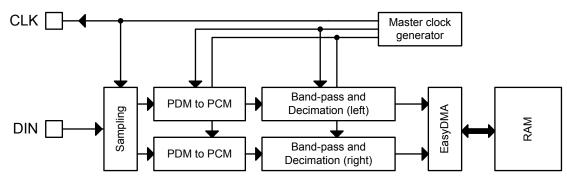


Figure 124: PDM module

43.1 Master clock generator

The FREQ field in the master clock's PDMCLKCTRL register allows adjusting the PDM clock's frequency.

The master clock generator does not add any jitter to the HFCLK source chosen. It is recommended (but not mandatory) to use the Xtal as HFCLK source.

43.2 Module operation

By default, bits from the left PDM microphone are sampled on PDM_CLK falling edge, bits for the right are sampled on the rising edge of PDM_CLK, resulting in two bitstreams. Each bitstream is fed into a digital filter which converts the PDM stream into 16-bit PCM samples, and filters and down-samples them to reach the appropriate sample rate.

The EDGE field in the MODE register allows swapping Left and Right, so that Left will be sampled on rising edge, and Right on falling.

The PDM module uses EasyDMA to store the samples coming out from the filters into one buffer in RAM.

Depending on the mode chosen in the OPERATION field in the MODE register, memory either contains alternating left and right 16-bit samples (Stereo), or only left 16-bit samples (Mono).

To ensure continuous PDM sampling, it is up to the application to update the EasyDMA destination address pointer as the previous buffer is filled.



The continuous transfer can be started or stopped by sending the START and STOP tasks. STOP becomes effective after the current frame has finished transferring, which will generate the STOPPED event. The STOPPED event indicates that all activity in the module are finished, and that the data is available in RAM (EasyDMA has finished transferring as well). Attempting to restart before receiving the STOPPED event may result in unpredictable behaviour.

43.3 Decimation filter

In order to convert the incoming data stream into PCM audio samples, a decimation filter is included in the PDM interface module.

The input of the filter is the two-channel PDM serial stream (with left channel on clock high, right channel on clock low), its output is 2×16 -bit PCM samples at a sample rate 64 times lower than the PDM clock rate.

The filter stage of each channel is followed by a digital volume control, to attenuate or amplify the output samples in a range of -20 dB to +20 dB around the default (reset) setting, defined by $G_{PDM,default}$. The gain is controlled by the GAINL and GAINR registers.

As an example, if the goal is to achieve 2500 RMS output samples (16 bit) with a 1 kHz 90 dBA signal into a -26 dBFS sensitivity PDM microphone, the user will have to sum the PDM module's default gain ($G_{PDM,default}$) and the gain introduced by the microphone and acoustic path of his implementation (an attenuation would translate into a negative gain), and adjust GAINL and GAINR by this amount. Assuming that only the PDM module influences the gain, GAINL and GAINR must be set to - $G_{PDM,default}$ dB to achieve the requirement.

With $G_{PDM,default}$ =3.2 dB, and as GAINL and GAINR are expressed in 0.5 dB steps, the closest value to program would be 3.0 dB, which can be calculated as:

```
GAINL = GAINR = (DefaultGain - (2 * 3))
```

Remember to check that the resulting values programmed into GAINL and GAINR fall within MinGain and MaxGain.

43.4 EasyDMA

Samples will be written directly to RAM, and EasyDMA must be configured accordingly.

The address pointer for the EasyDMA channel is set in SAMPLE.PTR register. If the destination address set in SAMPLE.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

DMA supports Stereo (Left+Right 16-bit samples) and Mono (Left only) data transfer, depending on setting in the OPERATION field in the MODE register. The samples are stored little endian.

Table 101: DMA sample storage

MODE.OPERATION	Bits per sample	Result stored per RAM word	Physical RAM allocated (32 bit words)	Result boundary indexes in RAM	Note
Stereo	32 (2x16)	L+R	ceil(SAMPLE.MAXCNT/2)	R0=[31:16]; L0=[15:0]	Default
Mono	16	2xL	ceil(SAMPLE.MAXCNT/2)	L1=[31:16]: L0=[15:0]	

The destination buffer in RAM consists of one block, the size of which is set in SAMPLE.MAXCNT register. Format is number of 16-bit samples. The physical RAM allocated is always:

```
(RAM allocation, in bytes) = SAMPLE.MAXCNT * 2;
```

(but the mapping of the samples depends on MODE.OPERATION.

If OPERATION=Stereo, RAM will contain a succession of Left and Right samples.

If OPERATION=Mono, RAM will contain a succession of mono samples.



For a given value of SAMPLE.MAXCNT, the buffer in RAM can contain half the stereo sampling time as compared to the mono sampling time.

The PDM acquisition can be started by the START task, after the SAMPLE.PTR and SAMPLE.MAXCNT registers have been written. When starting the module, it will take some time for the filters to start outputting valid data. Transients from the PDM microphone itself may also occur. The first few samples (typically around 50) might hence contain invalid values or transients. It is therefore advised to discard the first few samples after a PDM start.

As soon as the STARTED event is received, the firmware can write the next SAMPLE.PTR value (this register is double-buffered), to ensure continuous operation.

When the buffer in RAM is filled with samples, an END event is triggered. The firmware can start processing the data in the buffer. Meanwhile, the PDM module starts acquiring data into the new buffer pointed to by SAMPLE.PTR, and sends a new STARTED event, so that the firmware can update SAMPLE.PTR to the next buffer address.

43.5 Hardware example

Connect the microphone clock to CLK, and data to DIN.



Figure 125: Example of a single PDM microphone, wired as left



Figure 126: Example of a single PDM microphone, wired as right

Note that in a single-microphone (mono) configuration, depending on the microphone's implementation, either the left or the right channel (sampled at falling or rising CLK edge respectively) will contain reliable data. If two microphones are used, one of them has to be set as left, the other as right (L/R pin tied high or to GND on the respective microphone). It is strongly recommended to use two microphones of exactly the same brand and type so that their timings in left and right operation match.

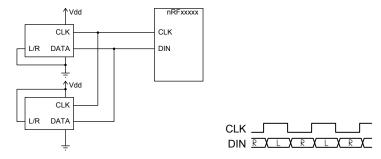


Figure 127: Example of two PDM microphones

43.6 Pin configuration

The CLK and DIN signals associated to the PDM module are mapped to physical pins according to the configuration specified in the PSEL.CLK and PSEL.DIN registers respectively. If the CONNECT field in any PSEL register is set to Disconnected, the associated PDM module signal will not be connected to the required physical pins, and will not operate properly.



The PSEL.CLK and PSEL.DIN registers and their configurations are only used as long as the PDM module is enabled, and retained only as long as the device is in System ON mode. See *POWER* — *Power supply* on page 78 for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register.

To ensure correct behaviour in the PDM module, the pins used by the PDM module must be configured in the GPIO peripheral as described in *Table 102: GPIO configuration before enabling peripheral* on page 440 before enabling the PDM module. This is to ensure that the pins used by the PDM module are driven correctly if the PDM module itself is temporarily disabled or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the PDM module is supposed to be connected to an external PDM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behaviour.

Table 102: GPIO configuration before enabling peripheral

PDM signal	PDM pin	Direction	Output value	Comment
CLK	As specified in PSEL.CLK	Output	0	
DIN	As specified in PSEL.DIN	Input	Not applicable	

43.7 Registers

Table 103: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001D000	PDM	PDM	Pulse Density Modulation (Digital	
			Microphone Interface)	

Table 104: Register Overview

Register	Offset	Description
TASKS_START	0x000	Starts continuous PDM transfer
TASKS_STOP	0x004	Stops PDM transfer
EVENTS_STARTED	0x100	PDM transfer has started
EVENTS_STOPPED	0x104	PDM transfer has finished
EVENTS_END	0x108	The PDM has written the last sample specified by SAMPLE.MAXCNT (or the last sample after a STOP
		task has been received) to Data RAM
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	PDM module enable register
PDMCLKCTRL	0x504	PDM clock generator control
MODE	0x508	Defines the routing of the connected PDM microphones' signals
GAINL	0x518	Left output gain adjustment
GAINR	0x51C	Right output gain adjustment
PSEL.CLK	0x540	Pin number configuration for PDM CLK signal
PSEL.DIN	0x544	Pin number configuration for PDM DIN signal
SAMPLE.PTR	0x560	RAM address pointer to write samples to with EasyDMA
SAMPLE.MAXCNT	0x564	Number of samples to allocate memory for in EasyDMA mode

43.7.1 INTEN

Address offset: 0x300 Enable or disable interrupt



Bit n	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				СВА
Rese	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW STARTED			Enable or disable interrupt for STARTED event
				See EVENTS_STARTED
		Disabled	0	Disable
		Enabled	1	Enable
В	RW STOPPED			Enable or disable interrupt for STOPPED event
				See EVENTS_STOPPED
		Disabled	0	Disable
		Enabled	1	Enable
С	RW END			Enable or disable interrupt for END event
				See EVENTS_END
		Disabled	0	Disable
		Enabled	1	Enable

43.7.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				СВА
Res	et 0x00000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW STARTED			Write '1' to Enable interrupt for STARTED event
				See EVENTS_STARTED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW STOPPED			Write '1' to Enable interrupt for STOPPED event
				See EVENTS_STOPPED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW END			Write '1' to Enable interrupt for END event
				See EVENTS_END
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

43.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	er		33	1 30	29	2	8 2	7 :	26	25	24	23	22	21	20	19	18	17	7 1	5 1	5 1	4 1	.3 :	12	11 :	LO	9	8	7	6	5	4	3	2	1 ()
Id																																			С	В	4
Res	et 0x0	0000000		0	0	0	(0 0	0	0	0	0	0	0	0	0	0	0	0	0	()	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (כ
Id	RW	Field	Value Id	V	alue								De	scr	ipti	on																					
Α	RW	STARTED											W	rite	'1'	to I	Disa	able	in	ter	rup	ot f	or S	TA	RTE	Dε	vei	nt									
													Se	e <i>E</i>	VΕN	ITS_	_ST	AR	TEL)																	
			Clear	1									Dis	sab	le																						
			Disabled	0									Re	ad:	Dis	abl	ed																				
			Enabled	1									Re	ad:	Ena	abl	ed																				
В	RW	STOPPED											W	rite	'1'	to I	Disa	able	in	ter	rup	ot f	or S	то	PPI	ED 6	eve	nt									



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 C B A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
			See EVENTS_STOPPED
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW END			Write '1' to Disable interrupt for END event
			See EVENTS_END
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

43.7.4 ENABLE

Address offset: 0x500

PDM module enable register

Bitı	numbe	er		31 30	29	28	27	26	25 2	24 2	3 2	2 2	1 20	0 19	18	17	16	15	14	13	12 1	1 1	9	8	7	6	5	4	3	2 1	. 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0 (0 (0 (0 (0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0
ld	RW	Field	Value Id	Value	2					C	esc	crip	tion	ı																	
Α	RW	ENABLE								Е	nat	ole d	or d	isab	le F	ND	l mo	odu	le												
			Disabled	0						C	isa	ble																			
			Enabled	1						Е	nat	ole																			

43.7.5 PDMCLKCTRL

Address offset: 0x504

PDM clock generator control

	Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21 2	20 1	19 1	l8 1	7 1	6 1	5 1	4 1	3 12	11	10	9	8	7 6	6 !	5 4	4 3	2	1	0
	Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	Δ Α	A A	A A	Δ Δ	Α	Α	Α	Α	Α .	Δ ,	Δ,	Δ /	A /	A	Α	. A
	Rese	et OxC	8400000		0	0	0	0	1	0	0	0	0	1	0	0	0	0 () (0 () (0	0	0	0	0	0	0 (0	0 (0	0	0	0
	Id	RW	Field	Value Id	Va	lue							De	scri	otio	n																		
Ī	Α	RW	FREQ										PD	M_(CLK	fre	que	ncy																
				1000K	0x	080	000	000					PD	M_0	CLK	= 3	2 M	Hz ,	/ 32	2 = 1	.00	00 N	lHz											
				Default	0x	084	000	000					PD	M_0	CLK	= 3	2 M	Hz ,	/ 31	= 1	.03	32 N	lHz											
				1067K	0x	088	000	000					PD	M_0	CLK	= 3	2 M	Hz ,	/ 30) = 1	.06	57 N	lHz											

43.7.6 MODE

Address offset: 0x508

Defines the routing of the connected PDM microphones' signals

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		В А
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW OPERATION		Mono or stereo operation
	Stereo	0 Sample and store one pair (Left + Right) of 16bit samples per
		RAM word R=[31:16]; L=[15:0]
	Mono	1 Sample and store two successive Left samples (16 bit each) per
		RAM word L1=[31:16]; L0=[15:0]
B RW EDGE		Defines on which PDM_CLK edge Left (or mono) is sampled
	LeftFalling	0 Left (or mono) is sampled on falling edge of PDM_CLK
	LeftRising	1 Left (or mono) is sampled on rising edge of PDM_CLK



43.7.7 GAINL

Address offset: 0x518

Left output gain adjustment

Bit numbe	_		21	20.2	0 20	27.	26.21	r 24	22.2	2 24 1	20 1	0 10	17	10	1 - 1	4 12	12	11 10		0	7	6 5	4	2	2 1	1 0
			31	3U Z	29 28	2/ 2	26 2:	5 24	23 2.	2 21 2	20 1	9 18	5 1/	16.	15 1	4 13	12	11 10	9	8				-		1 0
Id																						Д Д	A	Α	A A	A A
Reset 0x00	0000028		0	0 (0 0	0	0 0	0	0 0	0	0 (0	0	0	0 (0	0	0 0	0	0	0	0 1	. 0	1	0 (0 0
ld RW	Field	Value Id	Val	ue					Desc	riptio	n															
A RW	GAINL								Left o	outpu	t ga	in ad	ljust	mer	nt, in	0.5	dB s	steps,	aroı	und 1	he	defa	ault			
									mod	ule ga	in (s	see e	elect	rical	par	ame	ters)								
									0x00	-20 d	B ga	in a	djus	t												
									0x01	-19.5	dB	gain	adju	ıst												
									()																	
									0x27	-0.5	dB g	ain a	djus	it												
									0x28	0 dB	gain	adjı	ust													
									0x29	+0.5	dB g	gain a	adju	st												
									()																	
									0x4F	+19.5	dB	gain	adj	ust												
									0x50	+20 c	dB ga	ain a	ıdjus	t												
		MinGain	0x0	0					-20d	B gain	adj	ustn	nent	(mi	nim	um)										
		DefaultGain	0x2	8					0dB s	gain a	djus	tme	nt ('	2500	O RN	1S' re	qui	remei	nt)							
		MaxGain	0x5							B gair									,							
			0,10	_						- 5411		, 300														

43.7.8 GAINR

Address offset: 0x51C

Right output gain adjustment

Bit	numbe	r		33	1 30	29	28	27	26	5 25	5 24	23	22	21	20	19	18	17	7 16	5 15	5 14	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1	0
Id																												Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000028		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	1	0	1	0	0	0
Id	RW	Field	Value Id	V	alue							De	scr	ipti	on																				
Α	RW	GAINR										Rig	ht	out	put	t ga	in a	dju	ustn	ner	nt, i	n 0	.5 c	lB s	teps	, ar	oun	d t	he						
												de	fau	lt n	nod	lule	gai	n (:	see	ele	ectr	ical	pa	ran	nete	rs)									
			MinGain	0>	x00							-20)dE	ga	in a	dju	stn	nen	ıt (n	nin	imu	ım)													
			DefaultGain	0>	x28							0d	Вg	ain	adj	ust	me	nt (('25	00	RM	1S' ı	eq	uire	mei	nt)									
			MaxGain	0>	x50							+2	0dl	3 ga	in a	adju	ıstr	ner	nt (ı	max	xim	um)												
A	NVV	GAINN	DefaultGain	0>	x28							de -20 0d	fau OdB B g	lt n ga ain	nod in a adj	lule Idju Iust	gai stn me	n (: nen nt (see it (n ('25	ele nin 00	ectr imu RM	ical um) IS' i	pa	ran	nete	rs)	oun	ut	ile						

43.7.9 PSEL.CLK

Address offset: 0x540

Pin number configuration for PDM CLK signal

Bit r	numbe	er		31 30 29 28 27 2	26 25 2	4 23	22 2	1 20	19 1	18 1	7 16	15 1	L4 13	3 12	11 1	0 9	8	7	6	5 4	1 3	2	1 0
Id				В																A	A A	Α	A A
Res	et 0xF	FFFFFF		1 1 1 1 1 :	1 1 1	1 1	1 1	l 1	1	1 1	. 1	1	1 1	1	1 :	l 1	1	1	1	1 1	۱ 1	1	1 1
Id	RW	Field	Value Id	Value		De	scrip	tion															
Α	RW	PIN		[031]		Pin	num	ber															
В	RW	CONNECT				Co	nnect	tion															
			Disconnected	1		Dis	conn	ect															
			Connected	0		Co	nnect	t															

43.7.10 PSEL.DIN

Address offset: 0x544



Pin number configuration for PDM DIN signal

Bitı	numbe	er		31 30	29	28 2	27 2	6 25	5 24	23	22 2	21 2	20 19	9 18	3 17	16	15 3	14 1	3 12	11	10 !	9 8	7	6	5	4	3	2 1	0
Id				В																						Α	Α /	4 Α	A
Res	et OxF	FFFFFF		1 1	1	1	1 1	1	1	1	1	1	1 1	. 1	. 1	1	1	1 1	1	1	1	1 1	1	1	1	1	1 :	1 1	. 1
Id	RW	Field	Value Id	Value	!					De	scrip	otio	n																
Α	RW	PIN		[031]					Pin	nur	nbe	r																
В	RW	CONNECT								Coi	nne	ction	n																
			Disconnected	1						Dis	con	nect	t																
			Connected	0						Coi	nne	ct																	

43.7.11 SAMPLE.PTR

Address offset: 0x560

RAM address pointer to write samples to with EasyDMA

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW SAMPLEPTR		Address to write PDM samples to over DMA

43.7.12 SAMPLE.MAXCNT

Address offset: 0x564

Number of samples to allocate memory for in EasyDMA mode

Bit	number			31	30 2	29 2	8 27	7 26	25	24	23 2	22 2	1 2	0 19	18	17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	1 0
Id																			Α	A	Δ	A	Α	Α	Α	Α	Α	Α	A A	\ A	4 А
Res	et 0x00	000000		0	0	0 (0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Val	ue						Des	crip	tion	1																	
Α	RW	BUFFSIZE		[0	327	67]					Len	gth o	of D	MA	RA	Ма	lloc	atio	n in	nuı	nbe	r of	san	nple	es						

43.8 Electrical specification

43.8.1 PDM Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{PDM,stereo}	PDM module active current, stereo operation ³⁸		1.4		mA
$f_{\text{PDM,CLK}}$	PDM clock speed		1.032		MHz
t _{PDM,JITTER}	Jitter in PDM clock output			20	ns
T _{dPDM,CLK}	PDM clock duty cycle	40	50	60	%
t _{PDM,DATA}	Decimation filter delay			5	ms
t _{PDM,cv}	Allowed clock edge to data valid			125	ns
t _{PDM,ci}	Allowed (other) clock edge to data invalid	0			ns
t _{PDM,s}	Data setup time at f _{PDM,CLK} =1.024 MHz	65			ns
t _{PDM,h}	Data hold time at f _{PDM,CLK} =1.024 MHz	0			ns
G _{PDM,default}	Default (reset) absolute gain of the PDM module		3.2		dB

³⁸ Average current including PDM and DMA transfers, excluding clock and power supply base currents



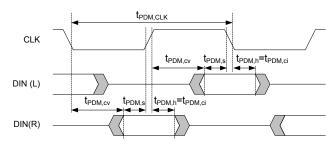


Figure 128: PDM timing diagram



44 I²S — Inter-IC sound interface

The I²S (Inter-IC Sound) module, supports the original two-channel I²S format, and left or right-aligned formats. It implements EasyDMA for sample transfer directly to and from RAM without CPU intervention.

The I²S peripheral has the following main features:

- Master and Slave mode
- Simultaneous bi-directional (TX and RX) audio streaming
- Original I²S and left- or right-aligned format
- 8, 16 and 24-bit sample width
- Low-jitter Master Clock generator
- Various sample rates

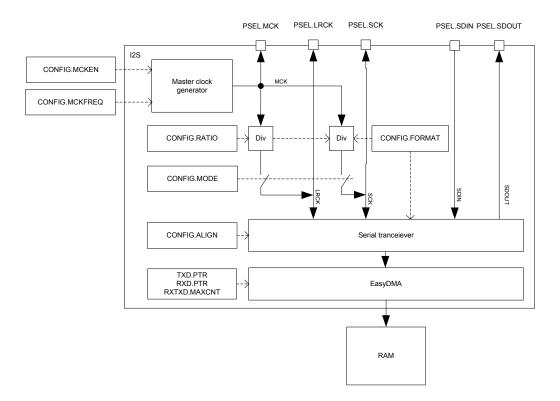


Figure 129: I²S master

44.1 Mode

The I²S protocol specification defines two modes of operation, Master and Slave.

The I²S mode decides which of the two sides (Master or Slave) shall provide the clock signals LRCK and SCK, and these signals are always supplied by the Master to the Slave.

44.2 Transmitting and receiving

The I²S module supports both transmission (TX) and reception (RX) of serial data. In both cases the serial data is shifted synchronously to the clock signals SCK and LRCK.



TX data is written to the SDOUT pin on the falling edge of SCK, and RX data is read from the SDIN pin on the rising edge of SCK. The most significant bit (MSB) is always transmitted first.

TX and RX are available in both Master and Slave modes and can be enabled/disabled independently in the CONFIG.TXEN on page 456 and CONFIG.RXEN on page 456.

Transmission and/or reception is started by triggering the START task. When started and transmission is enabled (in *CONFIG.TXEN* on page 456), the TXPTRUPD event will be generated for every *RXTXD.MAXCNT* on page 459 number of transmitted data words (containing one or more samples). Similarly, when started and reception is enabled (in *CONFIG.RXEN* on page 456), the RXPTRUPD event will be generated for every *RXTXD.MAXCNT* on page 459 received data words.

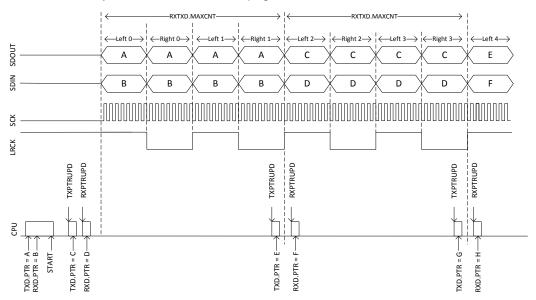


Figure 130: Transmitting and receiving. CONFIG.FORMAT = Aligned, CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo, RXTXD.MAXCNT = 1.

44.3 Left right clock (LRCK)

The Left Right Clock (LRCK), often referred to as "word clock", "sample clock" or "word select" in I²S context, is the clock defining the frames in the serial bit streams sent and received on SDOUT and SDIN, respectively.

In I2S mode, each frame contains one left and right sample pair, with the left sample being transferred during the low half period of LRCK followed by the right sample being transferred during the high period of LRCK.

In Aligned mode, each frame contains one left and right sample pair, with the left sample being transferred during the high half period of LRCK followed by the right sample being transferred during the low period of LRCK.

Consequently, the LRCK frequency is equivalent to the audio sample rate.

When operating in Master mode, the LRCK is generated from the MCK, and the frequency of LRCK is then given as:

```
LRCK = MCK / CONFIG.RATIO
```

LRCK always toggles around the falling edge of the serial clock SCK.

44.4 Serial clock (SCK)

The serial clock (SCK), often referred to as the serial bit clock, pulses once for each data bit being transferred on the serial data lines SDIN and SDOUT.



When operating in Master mode the SCK is generated from the MCK, and the frequency of SCK is then given as:

```
SCK = 2 * LRCK * CONFIG.SWIDTH
```

The falling edge of the SCK falls on the toggling edge of LRCK.

When operating in Slave mode SCK is provided by the external I²S master.

44.5 Master clock (MCK)

The master clock (MCK) is the clock from which LRCK and SCK are derived when operating in Master mode.

The MCK is generated by an internal MCK generator. This generator always needs to be enabled when in Master mode, but the generator can also be enabled when in Slave mode. Enabling the generator when in slave mode can be useful in the case where the external Master is not able to generate its own master clock.

The MCK generator is enabled/disabled in the register *CONFIG.MCKEN* on page 457, and the generator is started or stopped by the START or STOP tasks.

In Master mode the LRCK and the SCK frequencies are closely related, as both are derived from MCK and set indirectly through *CONFIG.RATIO* on page 457 and *CONFIG.SWIDTH* on page 458.

When configuring these registers, the user is responsible for fulfilling the following requirements:

1. SCK frequency can never exceed the MCK frequency, which can be formulated as:

```
CONFIG.RATIO >= 2 * CONFIG.SWIDTH
```

2. The MCK/LRCK ratio shall be a multiple of 2 * CONFIG.SWIDTH, which can be formulated as:

```
Integer = (CONFIG.RATIO / (2 * CONFIG.SWIDTH))
```

The MCK signal can be routed to an output pin (specified in PSEL.MCK) to supply external I²S devices that require the MCK to be supplied from the outside.

When operating in Slave mode, the I²S module does not use the MCK and the MCK generator does not need to be enabled.

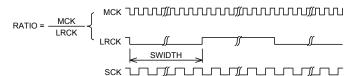


Figure 131: Relation between RATIO, MCK and LRCK.

Table 105: Configuration examples

Desired LRCK [Hz]	CONFIG.SWIDTH	CONFIG.RATIO	CONFIG.MCKFREQ	MCK [Hz]	LRCK [Hz]	LRCK error [%]
16000	16Bit	32X	32MDIV63	507936.5	15873.0	-0.8
16000	16Bit	64X	32MDIV31	1032258.1	16129.0	0.8
16000	16Bit	256X	32MDIV8	4000000.0	15625.0	-2.3
32000	16Bit	32X	32MDIV31	1032258.1	32258.1	0.8
32000	16Bit	64X	32MDIV16	2000000.0	31250.0	-2.3
32000	16Bit	256X	32MDIV4	8000000.0	31250.0	-2.3
44100	16Bit	32X	32MDIV23	1391304.3	43478.3	-1.4
44100	16Bit	64X	32MDIV11	2909090.9	45454.5	3.1
44100	16Bit	256X	32MDIV3	10666666.7	41666.7	-5.5

44.6 Width, alignment and format

The CONFIG.SWIDTH register primarily defines the sample width of the data written to memory. In master mode, it then also sets the amount of bits per frame. In Slave mode it controls padding/trimming if required. Left, right, transmitted, and received samples always have the same width. The CONFIG.FORMAT register specifies the position of the data frames with respect to the LRCK edges in both Master and Slave modes.



When using I²S format, the first bit in a half-frame (containing one left or right sample) gets sampled on the second rising edge of the SCK after a LRCK edge. When using Aligned mode, the first bit in a half-frame gets sampled on the first rising edge of SCK following a LRCK edge.

For data being received on SDIN the sample value can be either right or left-aligned inside a half-frame, as specified in *CONFIG.ALIGN* on page 458. *CONFIG.ALIGN* on page 458 affects only the decoding of the incoming samples (SDIN), while the outgoing samples (SDOUT) are always left-aligned (or justified).

When using left-alignment, each half-frame starts with the MSB of the sample value (both for data being sent on SDOUT and received on SDIN).

When using right-alignment, each half-frame of data being received on SDIN ends with the LSB of the sample value, while each half-frame of data being sent on SDOUT starts with the MSB of the sample value (same as for left-alignment).

In Master mode, the size of a half-frame (in number of SCK periods) equals the sample width (in number of bits), and in this case the alignment setting does not care as each half-frame in any case will start with the MSB and end with the LSB of the sample value.

In slave mode, however, the sample width does not need to equal the frame size. This means you might have extra or fewer SCK pulses per half-frame than what the sample width specified in *CONFIG.SWIDTH* requires.

In the case where we use **left-alignment** and the number of SCK pulses per half-frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits after the LSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0.

In the case where we use **left-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

Data sent and received on SDOUT and SDIN will be truncated with the LSBs being removed first.

In the case where we use **right-alignment** and the number of SCK pulses per frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits before the MSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0 (same behavior as for left-alignment).

In the case where we use **right-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

- Data received on SDIN will be sign-extended to "sample width" number of bits before being written to memory.
- Data sent on SDOUT will be truncated with the LSBs being removed first (same behavior as for leftalignment).

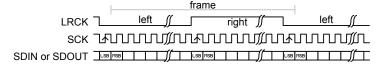


Figure 132: I²S format. CONFIG.SWIDTH equalling half-frame size.

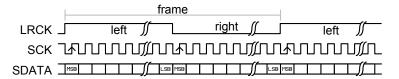


Figure 133: Aligned format. CONFIG.SWIDTH equalling half-frame size.



44.7 EasyDMA

The I²S module implements EasyDMA for accessing internal Data RAM without CPU intervention.

The source and destination pointers for the TX and RX data are configured in *TXD.PTR* on page 459 and *RXD.PTR* on page 459. The memory pointed to by these pointers will only be read or written when TX or RX are enabled in *CONFIG.TXEN* on page 456 and *CONFIG.RXEN* on page 456.

The addresses written to the pointer registers *TXD.PTR* on page 459 and *RXD.PTR* on page 459 are double-buffered in hardware, and these double buffers are updated for every *RXTXD.MAXCNT* on page 459 words (containing one or more samples) read/written from/to memory. The events TXPTRUPD and RXPTRUPD are generated whenever the TXD.PTR and RXD.PTR are transferred to these double buffers.

If *TXD.PTR* on page 459 is not pointing to the Data RAM region when transmission is enabled, or *RXD.PTR* on page 459 is not pointing to the Data RAM region when reception is enabled, an EasyDMA transfer may result in a HardFault and/or memory corruption. See *Memory* on page 23 for more information about the different memory regions.

Due to the nature of I²S, where the number of transmitted samples always equals the number of received samples (at least when both TX and RX are enabled), one common register *RXTXD.MAXCNT* on page 459 is used for specifying the sizes of these two memory buffers. The size of the buffers is specified in a number of 32-bit words. Such a 32-bit memory word can either contain four 8-bit samples, two 16-bit samples or one right-aligned 24-bit sample sign extended to 32 bit.

In stereo mode (CONFIG.CHANNELS=Stereo), the samples are stored as "left and right sample pairs" in memory. Figure Figure 134: Memory mapping for 8 bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo. on page 450, Figure 136: Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo. on page 451 and Figure 138: Memory mapping for 24 bit stereo. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo. on page 451 show how the samples are mapped to memory in this mode. The mapping is valid for both RX and TX.

In mono mode (CONFIG.CHANNELS=Left or Right), RX sample from only one channel in the frame is stored in memory, the other channel sample is ignored. Illustrations *Figure 135: Memory mapping for 8 bit mono.* CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left. on page 451, Figure 137: Memory mapping for 16 bit mono, left channel only. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left. on page 451 and Figure 139: Memory mapping for 24 bit mono, left channel only. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left. on page 452 show how RX samples are mapped to memory in this mode.

For TX, the same outgoing sample read from memory is transmitted on both left and right in a frame, resulting in a mono output stream.

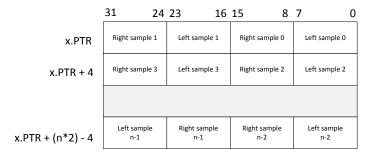


Figure 134: Memory mapping for 8 bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo.



	31 24	23 16	15 8	7 0
x.PTR	Left sample 3	Left sample 2	Left sample 1	Left sample 0
x.PTR + 4	Left sample 7	Left sample 6	Left sample 5	Left sample 4
x.PTR + n - 4	Left sample n-1	Left sample n-2	Left sample n-3	Left sample n-4

Figure 135: Memory mapping for 8 bit mono. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left.

	31 16	15	0
x.PTR	Right sample 0	Left sample 0	
x.PTR + 4	Right sample 1	Left sample 1	
x.PTR + (n*4) - 4	Right sample n - 1	Left sample n - 1	

Figure 136: Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo.

	31 16	15 0
x.PTR	Left sample 1	Left sample 0
x.PTR + 4	Left sample 3	Left sample 2
x.PTR + (n*2) - 4	Left sample n - 1	Left sample n - 2

Figure 137: Memory mapping for 16 bit mono, left channel only. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left.

	31	23 0
x.PTR	Sign ext.	Left sample 0
x.PTR + 4	Sign ext.	Right sample 0
x.PTR + (n*8) - 8	Sign ext.	Left sample n - 1
x.PTR + (n*8) - 4	Sign ext.	Right sample n - 1

Figure 138: Memory mapping for 24 bit stereo. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo.



	31	23 0
x.PTR	Sign ext.	Left sample 0
x.PTR + 4	Sign ext.	Left sample 1
x.PTR + (n*4) - 4	Sign ext.	Left sample n - 1

Figure 139: Memory mapping for 24 bit mono, left channel only. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left.

44.8 Module operation

Described here is a typical operating procedure for the I²S module.

1. Configure the I²S module using the CONFIG registers

```
// Enable reception
NRF I2S->CONFIG.RXEN = (I2S CONFIG RXEN RXEN Enabled <<
                                        I2S_CONFIG_RXEN_RXEN_Pos);
// Enable transmission
NRF I2S->CONFIG.TXEN = (I2S CONFIG TXEN TXEN Enabled <<
                                        I2S CONFIG TXEN TXEN Pos);
// Enable MCK generator
NRF_I2S->CONFIG.MCKEN = (I2S_CONFIG_MCKEN_MCKEN_Enabled <<</pre>
                                        12S CONFIG MCKEN MCKEN Pos);
// MCKFREQ = 4 MHz
NRF_12S->CONFIG.MCKFREQ = 12S_CONFIG_MCKFREQ_MCKFREQ_32MDIV8 <<
                                        12S CONFIG MCKFREQ MCKFREQ Pos;
// Ratio = 256
NRF I2S->CONFIG.RATIO = I2S CONFIG RATIO RATIO 256X <<
                                       12S CONFIG RATIO RATIO Pos;
// MCKFREQ = 4 MHz and Ratio = 256 gives sample rate = 15.625 ks/s
// Sample width = 16 bit
NRF I2S->CONFIG.SWIDTH = I2S CONFIG SWIDTH SWIDTH 16Bit <<
                                        12S CONFIG SWIDTH SWIDTH Pos;
// Alignment = Left
NRF I2S->CONFIG.ALIGN = I2S CONFIG ALIGN ALIGN Left <<
                                       12S CONFIG ALIGN ALIGN Pos;
// Format = I2S
NRF I2S->CONFIG.FORMAT = I2S CONFIG FORMAT FORMAT I2S <<
                                        12S CONFIG FORMAT FORMAT Pos;
// Use stereo
NRF I2S->CONFIG.CHANNELS = I2S CONFIG CHANNELS CHANNELS Stereo <<
                                        12S CONFIG CHANNELS CHANNELS Pos;
```

2. Map IO pins using the PINSEL registers



3. Configure TX and RX data pointers using the TXD, RXD and RXTXD registers

```
NRF_I2S->TXD.PTR = my_tx_buf;
NRF_I2S->RXD.PTR = my_rx_buf;
NRF_I2S->TXD.MAXCNT = MY_BUF_SIZE;
```

4. Enable the I²S module using the ENABLE register

```
NRF_I2S->ENABLE = 1;
```

5. Start audio streaming using the START task

```
NRF_I2S->TASKS_START = 1;
```

6. Handle received and transmitted data when receiving the TXPTRUPD and RXPTRUPD events

```
if (NRF_I2S->EVENTS_TXPTRUPD != 0)
{
    NRF_I2S->TXD.PTR = my_next_tx_buf;
    NRF_I2S->EVENTS_TXPTRUPD = 0;
}

if (NRF_I2S->EVENTS_RXPTRUPD != 0)
{
    NRF_I2S->RXD.PTR = my_next_rx_buf;
    NRF_I2S->EVENTS_RXPTRUPD = 0;
}
```

44.9 Pin configuration

The MCK, SCK, LRCK, SDIN and SDOUT signals associated with the I²S module are mapped to physical pins according to the pin numbers specified in the PSEL.x registers.

These pins are acquired whenever the I²S module is enabled through the register *ENABLE* on page 456.

When a pin is acquired by the I²S module, the direction of the pin (input or output) will be configured automatically, and any pin direction setting done in the GPIO module will be overridden. The directions for the various I²S pins are shown below in *Table 106: GPIO configuration before enabling peripheral (master mode)* on page 453 and *Table 107: GPIO configuration before enabling peripheral (slave mode)* on page 454.

To secure correct signal levels on the pins when the system is in OFF mode, and when the I²S module is disabled, these pins must be configured in the GPIO peripheral directly.

Table 106: GPIO configuration before enabling peripheral (master mode)

I ² S signal	I ² S pin	Direction	Output value	Comment
MCK	As specified in PSEL.MCK	Output	0	
LRCK	As specified in PSEL.LRCK	Output	0	



I ² S signal	I ² S pin	Direction	Output value	Comment
SCK	As specified in PSEL.SCK	Output	0	
SDIN	As specified in PSEL.SDIN	Input	Not applicable	
SDOUT	As specified in PSEL.SDOUT	Output	0	

Table 107: GPIO configuration before enabling peripheral (slave mode)

I ² S signal	I ² S pin	Direction	Output value	Comment
MCK	As specified in PSEL.MCK	Output	0	
LRCK	As specified in PSEL.LRCK	Input	Not applicable	
SCK	As specified in PSEL.SCK	Input	Not applicable	
SDIN	As specified in PSEL.SDIN	Input	Not applicable	
SDOUT	As specified in PSEL.SDOUT	Output	0	

44.10 Registers

Table 108: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40025000	I2S	125	Inter-IC Sound Interface		

Table 109: Register Overview

Register	Offset	Description
TASKS_START	0x000	Starts continuous I2S transfer. Also starts MCK generator when this is enabled.
TASKS_STOP	0x004	Stops I2S transfer. Also stops MCK generator. Triggering this task will cause the {event:STOPPED}
		event to be generated.
EVENTS_RXPTRUPD	0x104	The RXD.PTR register has been copied to internal double-buffers. When the I2S module is started
		and RX is enabled, this event will be generated for every RXTXD.MAXCNT words that are received on
		the SDIN pin.
EVENTS_STOPPED	0x108	12S transfer stopped.
EVENTS_TXPTRUPD	0x114	The TDX.PTR register has been copied to internal double-buffers. When the I2S module is started
		and TX is enabled, this event will be generated for every RXTXD.MAXCNT words that are sent on the
		SDOUT pin.
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable I2S module.
CONFIG.MODE	0x504	I2S mode.
CONFIG.RXEN	0x508	Reception (RX) enable.
CONFIG.TXEN	0x50C	Transmission (TX) enable.
CONFIG.MCKEN	0x510	Master clock generator enable.
CONFIG.MCKFREQ	0x514	Master clock generator frequency.
CONFIG.RATIO	0x518	MCK / LRCK ratio.
CONFIG.SWIDTH	0x51C	Sample width.
CONFIG.ALIGN	0x520	Alignment of sample within a frame.
CONFIG.FORMAT	0x524	Frame format.
CONFIG.CHANNELS	0x528	Enable channels.
RXD.PTR	0x538	Receive buffer RAM start address.
TXD.PTR	0x540	Transmit buffer RAM start address.
RXTXD.MAXCNT	0x550	Size of RXD and TXD buffers.
PSEL.MCK	0x560	Pin select for MCK signal.
PSEL.SCK	0x564	Pin select for SCK signal.
PSEL.LRCK	0x568	Pin select for LRCK signal.
PSEL.SDIN	0x56C	Pin select for SDIN signal.
PSEL.SDOUT	0x570	Pin select for SDOUT signal.

44.10.1 INTEN

Address offset: 0x300 Enable or disable interrupt



Bit r	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F C B
Res	et 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
В	RW RXPTRUPD			Enable or disable interrupt for RXPTRUPD event
				See EVENTS_RXPTRUPD
		Disabled	0	Disable
		Enabled	1	Enable
С	RW STOPPED			Enable or disable interrupt for STOPPED event
				See EVENTS_STOPPED
		Disabled	0	Disable
		Enabled	1	Enable
F	RW TXPTRUPD			Enable or disable interrupt for TXPTRUPD event
				See EVENTS_TXPTRUPD
		Disabled	0	Disable
		Enabled	1	Enable

44.10.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31 3	30 29	9 28	27	26 2	5 24	23 2	22 21	L 20	19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4 3	2	1 (
Id																										F		С	В
Res	et 0x0	0000000		0	0 0	0	0	0 0	0	0	0 0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0 0	0	0 (
Id	RW	Field	Value Id	Valu	ıe					Des	cript	ion																	
В	RW	RXPTRUPD								Writ	te '1'	to E	nab	le i	nte	rru	pt f	or F	RXPT	RU	PD e	ven	t						
										See	EVEI	NTS_	RXF	PTR	UPL)													
			Set	1						Enal	ble																		
			Disabled	0						Read	d: Di	sabl	ed																
			Enabled	1						Read	d: En	able	d																
С	RW	STOPPED								Writ	te '1'	to E	nab	le i	nte	rru	pt f	or S	TOP	PEI	D ev	ent							
										See	EVEI	NTS_	STO	PP	ED														
			Set	1						Enal	ble																		
			Disabled	0						Read	d: Di	sabl	ed																
			Enabled	1						Read	d: En	able	d																
F	RW	TXPTRUPD								Writ	te '1'	to E	nab	le i	nte	rru	pt f	or T	XPT	RU	PD e	ven	t						
										See	EVEI	NTS_	TXP	TR	UPE)													
			Set	1						Enal	ble																		
			Disabled	0						Read	d: Di	sabl	ed																
			Enabled	1						Read	d: En	able	d																

44.10.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bitı	numbe	er		31	. 30	29	2	8 27	7 2	26 2	5 2	24 2	23 2	22 :	21 :	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																															F			С	В	
Res	et 0x0	0000000		0	0	0	0	0) (0 () (0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue								Desc	crip	otio	n																				
В	RW	RXPTRUPD										١	Vrit	te '	1' t	o D	isak	ole	inte	erru	upt	for	RX	PTF	RUP	D e	ven	t								
												5	ee	EV	EN	rs_	RXP	TR	UPI)																
			Clear	1									Disa	ble	9																					
			Disabled	0								F	Read	d: [Disa	ble	d																			
			Enabled	1								F	Read	d: E	na	ble	d																			
С	RW	STOPPED										١	Vrit	te '	1' t	o D	isat	ole	inte	erru	upt	for	ST	OPF	PED	eve	ent									



	numbe	er		3	1 30	29	28	3 27	26	25	24	23 2	22 2	21 20) 19	18	17	16	15	14 1	.3 1	12 11	. 10	9	8	7	6	_	4 3	3 2	1	0
ld Res	et OxO	0000000		0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0 0	0	0	0	0		F 0	0 (: В • О	0
Id	RW	Field	Value Id	٧	alue							Des	crip	tion																		
												See	EVE	ENTS	_ST	OPF	PED															
			Clear	1								Disa	ble																			
			Disabled	0								Read	d: D	isab	led																	
			Enabled	1								Read	d: E	nabl	ed																	
F	RW	TXPTRUPD										Writ	te '1	1' to	Disa	ble	int	erru	ıpt 1	for T	ΧP	TRUI	D e	ven	t							
												See	EVE	ENTS	_TX	PTF	RUP	D														
			Clear	1								Disa	ble																			
			Disabled	0								Read	d: D	isab	led																	
			Enabled	1								Read	d: E	nabl	ed																	

44.10.4 ENABLE

Address offset: 0x500 Enable I2S module.

Bit	nun	mber	•		31 30 29 28 27 26 25 24 23	3 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id						A
Res	et C	0x00	000000		0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	R	w	Field	Value Id	Value De	escription
Α	R	RW	ENABLE		En	nable I2S module.
				Disabled	0 Dis	isable
				Enabled	1 En	nable

44.10.5 CONFIG.MODE

Address offset: 0x504

I2S mode.

Bit n	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 1	18 1	17 :	16	15	14	13	12 1	1 1) 9	8	7	6	5	4	3	2	1 0
Id																																	Α
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	n																		
Α	RW	MODE										I2S	mo	ode.																			
			Master	0								Ma	ste	r m	ode	. SC	K a	nd	LRC	CK g	gene	erat	ed	from	int	ern	al n	nast	er				
												clcd	ok (MC	K) a	nd	out	put	on	pii	ns d	efir	ned	by F	SEL	.xxx							
			Slave	1								Sla	ve r	noc	le. S	SCK	and	d LF	RCK	ge	ner	ate	d by	ext	erna	al m	ast	er a	nd				
												rec	eive	ed c	n p	ins	def	ine	d b	y P	SEL	ххх											

44.10.6 CONFIG.RXEN

Address offset: 0x508 Reception (RX) enable.

Bit number	31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A
Reset 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
A RW RXEN		Reception (RX) enable.
Disabled	0	Reception disabled and now data will be written to the RXD.PTR
		address.
Enabled	1	Reception enabled.

44.10.7 CONFIG.TXEN

Address offset: 0x50C



Transmission (TX) enable.

Bit number		31 30 2	9 28 2	7 26	25 24	4 23	22 21	20	19 1	L8 17	7 16	15	14 1	3 12	11 10	9	8	7	6	5	4 3	2	1	0
Id																								Α
Reset 0x00000001		0 0 0	0 0 (0 0	0 0	0	0 0	0	0	0 0	0	0	0 0	0	0 0	0	0	0	0	0	0 0	0	0	1
ld RW Field	Value Id	Value				De	scripti	on																
A RW TXEN						Tra	nsmis	sion	(TX) ena	ble.													
	Disabled	0				Tra	nsmis	sion	ı disa	abled	d and	d no	w da	ta w	ll be	eac	l fro	m t	he					
						RXI	D.TXD	add	Iress															
	Enabled	1				Tra	nsmis	sion	ena	bled	١.													

44.10.8 CONFIG.MCKEN

Address offset: 0x510

Master clock generator enable.

Bitı	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 :	16	15	14 :	13 1	12 1	1 1) 9	8	7	6	5	4	3	2 :	1 0
Id																																	Α
Res	et 0x0	000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 (0 1
Id	RW	Field	Value Id	Va	alue	!						De	scri	ptic	n																		
Α	RW	MCKEN										M	aste	r clo	ck	gen	era	tor	en	abl	e.												
			Disabled	0								M	aste	r clo	ck	gen	era	tor	dis	abl	ed a	and	PSE	L.N	ICK	not							
												со	nne	ctec	l(av	aila	ble	as	GΡ	10).													
			Enabled	1								M	aste	r clo	ck	gen	era	tor	rur	nnir	ng a	nd	MC	Κοι	tpu	t on	PS	EL.N	ИСК	ζ.			

44.10.9 CONFIG.MCKFREQ

Address offset: 0x514

Master clock generator frequency.

	numbe	er		3:	1 3	0 29	28	27	26	25	24	23 :	22 :	21 20) 19	9 18	3 17	16	15	14	13 1	2 11	10	9	8	7	6	5	4 :	3 2	1	0
Id				Α	Δ	A	Α	Α	Α	Α	Α	Α	Α	A A	Α	\ A	Α	Α	Α	Α	A A	A A	Α	Α	Α	Α	Α	Α	Α /	A A	Α	Α
Res	et 0x2	20000000		0	0) 1	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	V	alu	e						Des	crip	otion																		
Α	RW	MCKFREQ										Ma	ster	cloc	k g	ene	rato	or fr	equ	enc	y.											
			32MDIV2	0:	x80	000	000)				32 [ИΗ	z / 2	= 1	6.0	МН	Z														
			32MDIV3	0:	x50	000	000)				32 [ИΗ	z/3	= 1	0.66	666	567	МН	z												
			32MDIV4	0:	x40	000	000)				32 [ИΗ	z / 4	= 8	.0 N	1Hz															
			32MDIV5	0:	x30	000	000)				32 [ИΗ	z / 5	= 6	.4 N	1Hz															
			32MDIV6	0	x28	000	000)				32 [ИΗ	z / 6	= 5	.333	333	33 N	ЛHz													
			32MDIV8	0	x20	000	000)				32 [ИΗ	z / 8	= 4	.0 N	1Hz															
			32MDIV10	0	x18	000	000)				32 [ИΗ	z / 10) = 1	3.2	МН	Z														
			32MDIV11	0	x16	000	000)				32 [ИΗ	z / 11	L = 1	2.90	909	909	МН	z												
			32MDIV15	0	x11	000	000)				32 [ИΗ	z / 15	5 = 1	2.13	333	333	МН	z												
			32MDIV16	0	x10	000	000)				32 [ИΗ	z / 16	5 = 1	2.0	МН	Z														
			32MDIV21	0	x0C	000	000)				32 [ИΗ	z / 21	L =	1.52	2380	095														
			32MDIV23	0:	хОВ	000	000)				32 [ИΗ	z / 23	3 =	1.39	9130	043	МН	z												
			32MDIV30	0:	x08	800	000)				32 [ИΗ	z / 30) =	1.06	666	567	МН	z												
			32MDIV31	0:	x08	400	000)				32 [ИΗ	z / 31	L =	1.03	322	581	МН	z												
			32MDIV32	0:	x08	000	000)				32 [ИΗ	z / 32	2 =	1.0	МН	Z														
			32MDIV42	0	x06	000	000)				32 [ИΗ	z / 42	2 =	0.76	519	048	МН	z												
			32MDIV63	0	x04	100	000)				32 [ИΗ	z / 63	3 =	0.50	79	365	МН	z												
			32MDIV125	0	x02	0C0	000)				32 [ИΗ	z / 12	25 =	0.2	256	МН	Z													

44.10.10 CONFIG.RATIO

Address offset: 0x518 MCK / LRCK ratio.



Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	1 0
Id			A A A	A A
Reset 0x00000006		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	L O
Id RW Field	Value Id	Value	Description	
A RW RATIO			MCK / LRCK ratio.	
	32X	0	LRCK = MCK / 32	
	48X	1	LRCK = MCK / 48	
	64X	2	LRCK = MCK / 64	
	96X	3	LRCK = MCK / 96	
	128X	4	LRCK = MCK / 128	
	192X	5	LRCK = MCK / 192	
	256X	6	LRCK = MCK / 256	
	384X	7	LRCK = MCK / 384	
	512X	8	LRCK = MCK / 512	

44.10.11 CONFIG.SWIDTH

Address offset: 0x51C

Sample width.

Bit n	umbe	r		31	1 30	29	28	3 27	7 26	6 2	5 2	24 2	23 2	22 2	21 2	0 1	L9 1	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id																																		,	A A	4
Rese	t 0x0	0000001		0	0	0	0	0	0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 1	L
Id	RW	Field	Value Id	Va	alue	:							Des	crip	tio	n																				
Α	RW	SWIDTH										9	Sam	ple	wi	dth																				
			8Bit	0								8	3 bit	t.																						
			16Bit	1								1	16 b	it.																						
			24Bit	2								2	24 b	it.																						

44.10.12 CONFIG.ALIGN

Address offset: 0x520

Alignment of sample within a frame.

Bit	nuı	mbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																																			Α
Res	et	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	F	RW	Field	Value Id	Va	lue							De	scri	ptio	on																			
Α	F	RW	ALIGN										Ali	gnn	nen	t of	sar	npl	e w	ithi	n a	fra	me												
				Left	0								Lef	t-al	ign	ed.																			
				Right	1								Rig	ht-	alig	ned	١.																		

44.10.13 CONFIG.FORMAT

Address offset: 0x524

Frame format.

Bit r	numbe	er		31 3	29	28	3 27	26	25	24	23 2	22 2	21 2) 19	18	17	16 :	15 1	4 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1 0
Id																														Α
Res	et OxO	0000000		0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0	0	0 0
Id	RW	Field	Value Id	Valu	е						Des	crip	tion																	
Α	RW	FORMAT									Fran	ne f	orm	at.																
			I2S	0							Orig	gina	l I2S	for	nat.															
			Aligned	1							Alte	rna	te (I	eft-	or r	ight	-alig	nec	d) fo	rma	t.									

44.10.14 CONFIG.CHANNELS

Address offset: 0x528 Enable channels.



Bit num	nber			31	. 30	29	28	27	26	25	24	23	22	21	20	19 1	L8 1	17 1	16 :	15 :	14 1	L3 1	.2 1	1 1	9	8 (7	6	5	4	3	2	1	0
Id																																	Α	Α
Reset 0	0x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0
Id R	W	Field	Value Id	Va	alue							De	scri	ptic	n																			
A R	W	CHANNELS										Ena	able	cha	ann	els.																		
			Stereo	0								Ste	rec	١.																				
			Left	1								Lef	t or	ıly.																				
			Right	2								Rig	ht d	only																				

44.10.15 RXD.PTR

Address offset: 0x538

Receive buffer RAM start address.

Bit	numb	per		31	. 30	29	28	8 27	7 20	5 25	5 24	1 23	22	21	20	19	18	17	16	15	14	L3 1	L2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	. Α	. Α	A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α .	Δ Δ	A	Α	Α	Α	Α	Α	Α .	Δ.	4 А
Res	et 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	/ Field	Value Id	Va	lue							De	scr	iptio	on																		
Α	RW	/ PTR										Re	cei	/e b	uffe	er D	ata	RA	M s	tar	t ac	dre	ss.	Whe	n r	ecei	ving	g, w	ord	ls			
												со	nta	inin	g sa	mp	les	wil	be	wr	itte	n to	thi	s ad	dre	ss.	his	ado	dres	SS			
												is	a w	ord	alig	nec	l Da	ata I	RAN	Лa	ddr	255											

44.10.16 TXD.PTR

Address offset: 0x540

Transmit buffer RAM start address.

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21 2	20 1	9 18	3 17	16	15	14	13 1	2 13	. 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	A A	A	Α	Α	Α	Α	A	4 A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							De	scri	ptio	n																	
Α	RW	PTR										Tra	nsn	nit b	uffe	r Da	ıta F	RAN	1 sta	art a	ddr	ess.	Whe	en ti	rans	smi	ttin	ıg,				
												wo	rds	con	taini	ing s	am	ples	wi	ll be	feto	hed	fro	m th	nis a	addı	res	s. T	his			
												ado	dres	s is	a wo	ord a	aligr	ned	Dat	a R	AM a	addr	ess.									

44.10.17 RXTXD.MAXCNT

Address offset: 0x550

Size of RXD and TXD buffers.

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1
Id				AAAAA	A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A RW MAXCNT			Size of RXD and TXD	buffers in number of 32 bit v	words.

44.10.18 PSEL.MCK

Address offset: 0x560

Pin select for MCK signal.

Bit r	umbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Rese	t OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect



44.10.19 PSEL.SCK

Address offset: 0x564
Pin select for SCK signal.

Bit r	numbe	er		31	. 30	29	28	27	26	25	24 :	23 2	22 :	21 2	20 :	19 :	18 :	17 1	16 1	5 1	4 1	3 12	11	10	9	8	7	6 5	5 4	3	2	1	0
Id				С																									Δ	A	Α	Α	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	. 1	1	1	1	1	1	1 :	l 1	. 1	1	1	1
Id	RW	Field	Value Id	Va	llue						ı	Des	crip	otio	n																		
Α	RW	PIN		[0.	31]						ı	Pin	nur	nbe	er																		
С	RW	CONNECT									(Con	nec	ctio	n																		
			Disconnected	1							ı	Disc	con	nec	t																		
			Connected	0							(Con	nec	ct																			

44.10.20 PSEL.LRCK

Address offset: 0x568

Pin select for LRCK signal.

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7	6 5 4 3 2 1 0
С	A A A A A
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1
Value Id Value Description	
[031] Pin number	
Connection	
Disconnected 1 Disconnect	
Connected 0 Connect	
Value Id Value Description [031] Pin number Connection Connection Disconnected 1 Disconnect	1111

44.10.21 PSEL.SDIN

Address offset: 0x56C

Pin select for SDIN signal.

Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

44.10.22 PSEL.SDOUT

Address offset: 0x570

Pin select for SDOUT signal.

Bit	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect



44.11 Electrical specification

44.11.1 I2S timing specification

Symbol	Description	Mi	in.	Тур.	Max.	Units
t _{S_SDIN}	SDIN setup time before SCK rising	20	1			ns
t _{H_SDIN}	SDIN hold time after SCK rising	15				ns
t _{S_SDOUT}	SDOUT setup time after SCK falling	40	1			ns
t _{H_SDOUT}	SDOUT hold time before SCK falling	6				ns
t _{SCK_LRCK}	SCLK falling to LRCK edge	-5		0	5	ns
f_{MCK}	MCK frequency				4000	kHz
f _{LRCK}	LRCK frequency				48	kHz
f _{SCK}	SCK frequency				2000	kHz
DC _{CK}	Clock duty cycle (MCK, LRCK, SCK)	45			55	%

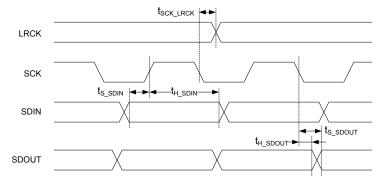


Figure 140: I2S timing diagram



45 MWU — Memory watch unit

The Memory watch unit (MWU) can be used to generate events when a memory region is accessed by the CPU. The MWU can be configured to trigger events for access to Data RAM and Peripheral memory segments. The MWU allows an application developer to generate memory access events during development for debugging or during production execution for failure detection and recovery.

Listed here are the main features for MWU:

- Six memory regions, four user-configurable and two fixed regions in peripheral address space
- Flexible configuration of regions with START and END addresses
- Generate events on CPU read and/or write to a defined region of Data RAM or peripheral memory address space
- Programmable maskable or non-maskable (NMI) interrupt on events
- Peripheral interfaces can be watched for read and write access using subregions of the two fixed memory regions

Table 110: Memory regions

Memory region	START address	END address
REGION[03]	Configurable	Configurable
PREGION[0]	0x4000000	0x4001FFFF
PREGION[1]	0x40020000	0x4003FFFF

Each MWU region is defined by a start address and an end address, configured by the START and END registers respectively. These addresses are byte aligned and inclusive. The END register value has to be greater or equal to the START register value. Each region is associated with a pair of events that indicate that either a write access or a read access from the CPU has been detected inside the region.

For regions containing subregions (see below), a set of status registers PERREGION[0..1].SUBSTATWA and PERREGION[0..1].SUBSTATRA indicate which subregion(s) caused the EVENT_PREGION[0..1].WA and EVENT_PREGION[0..1].RA respectively.

The MWU is only able to detect memory accesses in the Data RAM and Peripheral memory segments from the CPU, see *Memory* on page 23 for more information about the different memory segments. EasyDMA accesses are not monitored by the MWU. The MWU requires two HCLK cycles to detect and generate the event.

The peripheral regions, PREGION[0...1], are divided into 32 equally sized subregions, SR[0...31]. All subregions are excluded in the main region by default, and any can be included by specifying them in the SUBS register. When a subregion is excluded from the main region, the memory watch mechanism will not trigger any events when that subregion is accessed.

Subregions in PREGION[0..1] cannot be individually configured for read or write access watch. Watch configuration is only possible for a region as a whole. The PRGNiRA and PRGNiWA (i=0..1) fields in the REGIONEN register control watching read and write access.

REGION[0..3] can be individually enabled for read and/or write access watching through their respective RGNiRA and RGNiWA (i=0..3) fields in the REGIONEN register.

REGIONENSET and REGIONENCLR allow respectively enabling and disabling one or multiple REGIONs or PREGIONs watching in a single write access.

45.1 Registers

Table 111: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40020000	MWU	MWU	Memory Watch Unit	



Table 112: Register Overview

Register	Offset	Description
EVENTS_REGION[0].WA	A 0x100	Write access to region 0 detected
EVENTS_REGION[0].RA	0x104	Read access to region 0 detected
EVENTS_REGION[1].WA	A 0x108	Write access to region 1 detected
EVENTS_REGION[1].RA	0x10C	Read access to region 1 detected
EVENTS_REGION[2].WA	A 0x110	Write access to region 2 detected
EVENTS_REGION[2].RA	0x114	Read access to region 2 detected
EVENTS_REGION[3].WA	A 0x118	Write access to region 3 detected
EVENTS_REGION[3].RA	0x11C	Read access to region 3 detected
EVENTS_PREGION[0].W	/A 0x160	Write access to peripheral region 0 detected
EVENTS_PREGION[0].R.	A 0x164	Read access to peripheral region 0 detected
EVENTS_PREGION[1].W	/A 0x168	Write access to peripheral region 1 detected
EVENTS_PREGION[1].R.	A 0x16C	Read access to peripheral region 1 detected
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
NMIEN	0x320	Enable or disable non-maskable interrupt
NMIENSET	0x324	Enable non-maskable interrupt
NMIENCLR	0x328	Disable non-maskable interrupt
PERREGION[0].SUBSTA	7 1 0x400	Source of event/interrupt in region 0, write access detected while corresponding subregion was
		enabled for watching
PERREGION[0].SUBSTA	T/ 0x404	Source of event/interrupt in region 0, read access detected while corresponding subregion was
		enabled for watching
PERREGION[1].SUBSTA	7 1 0x408	Source of event/interrupt in region 1, write access detected while corresponding subregion was
		enabled for watching
PERREGION[1].SUBSTA	T/ 0x40C	Source of event/interrupt in region 1, read access detected while corresponding subregion was
		enabled for watching
REGIONEN	0x510	Enable/disable regions watch
REGIONENSET	0x514	Enable regions watch
REGIONENCLR	0x518	Disable regions watch
REGION[0].START	0x600	Start address for region 0
REGION[0].END	0x604	End address of region 0
REGION[1].START	0x610	Start address for region 1
REGION[1].END	0x614	End address of region 1
REGION[2].START	0x620	Start address for region 2
REGION[2].END	0x624	End address of region 2
REGION[3].START	0x630	Start address for region 3
REGION[3].END	0x634	End address of region 3
PREGION[0].START	0x6C0	Reserved for future use
PREGION[0].END	0x6C4	Reserved for future use
PREGION[0].SUBS	0x6C8	Subregions of region 0
PREGION[1].START	0x6D0	Reserved for future use
PREGION[1].END	0x6D4	Reserved for future use
PREGION[1].SUBS	0x6D8	Subregions of region 1

45.1.1 INTEN

Address offset: 0x300 Enable or disable interrupt

Bitı	numbe	er		31	1 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 1	.1 10	9	8	7	6	5	4	3	2 :	1 0
Id								L	K	J	1																Н	G	F	Ε	D	C E	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	V	alue	•						De	scri	otic	n																		
Α	RW	REGION0WA										Ena	ble	or	dis	able	e in	teri	rup	t fo	r RE	GIO	ON[()].W	A e	/ent	:						
												See	e EV	EN	TS_	REC	310	N[0	J. N	/A													
			Disabled	0								Dis	able	ē																			



Bit	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
В	RW REGIONORA	Enabled	1 Enable Enable or disable interrupt for REGION[0].RA event See EVENTS_REGION[0].RA
		Disabled	0 Disable
С	RW REGION1WA	Enabled	1 Enable Enable or disable interrupt for REGION[1].WA event
			See EVENTS_REGION[1].WA
		Disabled	0 Disable
_	DW DECIONADA	Enabled	1 Enable
D	RW REGION1RA		Enable or disable interrupt for REGION[1].RA event See EVENTS_REGION[1].RA
		Disabled	0 Disable
		Enabled	1 Enable
E	RW REGION2WA		Enable or disable interrupt for REGION[2].WA event
			See EVENTS_REGION[2].WA
		Disabled	0 Disable
F	RW REGION2RA	Enabled	1 Enable
F	RW REGIONZKA		Enable or disable interrupt for REGION[2].RA event See EVENTS_REGION[2].RA
		Disabled	0 Disable
		Enabled	1 Enable
G	RW REGION3WA		Enable or disable interrupt for REGION[3].WA event
		Disabled	See EVENTS_REGION[3].WA 0 Disable
		Enabled	1 Enable
Н	RW REGION3RA		Enable or disable interrupt for REGION[3].RA event
			See EVENTS_REGION[3].RA
		Disabled	0 Disable
	RW PREGIONOWA	Enabled	1 Enable
'	KW PREGIONOWA		Enable or disable interrupt for PREGION[0].WA event See EVENTS_PREGION[0].WA
		Disabled	0 Disable
		Enabled	1 Enable
J	RW PREGIONORA		Enable or disable interrupt for PREGION[0].RA event
		Disabled	See EVENTS_PREGION[0].RA 0 Disable
		Enabled	1 Enable
K	RW PREGION1WA		Enable or disable interrupt for PREGION[1].WA event
			See EVENTS_PREGION[1].WA
		Disabled	0 Disable
L	RW PREGION1RA	Enabled	1 Enable Enable or disable interrupt for PREGION[1].RA event
L	WW PREGIONIKA		See EVENTS_PREGION[1].RA See EVENTS_PREGION[1].RA
		Disabled	0 Disable
		Enabled	1 Enable

45.1.2 INTENSET

Address offset: 0x304 Enable interrupt



	number			26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld Bos	et 0x00000000			H G F E D C B A 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
A	RW REGIONOWA	30000		Write '1' to Enable interrupt for REGION[0].WA event
				See EVENTS_REGION[0].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW REGIONORA			Write '1' to Enable interrupt for REGION[0].RA event
				See EVENTS_REGION[0].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW REGION1WA			Write '1' to Enable interrupt for REGION[1].WA event
				See EVENTS_REGION[1].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW REGION1RA			Write '1' to Enable interrupt for REGION[1].RA event
				See EVENTS_REGION[1].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E	RW REGION2WA			Write '1' to Enable interrupt for REGION[2].WA event
				See EVENTS_REGION[2].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW REGION2RA			Write '1' to Enable interrupt for REGION[2].RA event
				See EVENTS_REGION[2].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW REGION3WA			Write '1' to Enable interrupt for REGION[3].WA event
				See EVENTS_REGION[3].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW REGION3RA			Write '1' to Enable interrupt for REGION[3].RA event
				See EVENTS_REGION[3].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
I	RW PREGIONOWA			Write '1' to Enable interrupt for PREGION[0].WA event
				See EVENTS_PREGION[0].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
J	RW PREGIONORA			Write '1' to Enable interrupt for PREGION[0].RA event
				See EVENTS_PREGION[0].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
K	RW PREGION1WA			Write '1' to Enable interrupt for PREGION[1].WA event



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		LKJI	H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
			See EVENTS_PREGION[1].WA
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
L RW PREGION1RA			Write '1' to Enable interrupt for PREGION[1].RA event
			See EVENTS_PREGION[1].RA
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

45.1.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
d		L	K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
d RW Field	Value Id	Value	Description
A RW REGIONOWA			Write '1' to Disable interrupt for REGION[0].WA event
			See EVENTS_REGION[0].WA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW REGIONORA			Write '1' to Disable interrupt for REGION[0].RA event
			See EVENTS_REGION[0].RA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
RW REGION1WA			Write '1' to Disable interrupt for REGION[1].WA event
			See EVENTS_REGION[1].WA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
RW REGION1RA			Write '1' to Disable interrupt for REGION[1].RA event
			See EVENTS_REGION[1].RA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
RW REGION2WA			Write '1' to Disable interrupt for REGION[2].WA event
			See EVENTS_REGION[2].WA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
RW REGION2RA			Write '1' to Disable interrupt for REGION[2].RA event
			See EVENTS_REGION[2].RA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
6 RW REGION3WA	Lilabica	1	Write '1' to Disable interrupt for REGION[3].WA event
, REGIONOVA			
			See EVENTS_REGION[3].WA
	Clear	1	Disable



Bit r	number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L K J I	HGFEDCBA
Res	set 0x00000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
	[Disabled	0	Read: Disabled
	E	Enabled	1	Read: Enabled
Н	RW REGION3RA			Write '1' to Disable interrupt for REGION[3].RA event
				See EVENTS_REGION[3].RA
	(Clear	1	Disable
		Disabled	0	Read: Disabled
	E	Enabled	1	Read: Enabled
1	RW PREGIONOWA			Write '1' to Disable interrupt for PREGION[0].WA event
				See EVENTS_PREGION[0].WA
	(Clear	1	Disable
	[Disabled	0	Read: Disabled
	E	Enabled	1	Read: Enabled
J	RW PREGIONORA			Write '1' to Disable interrupt for PREGION[0].RA event
				See EVENTS_PREGION[0].RA
	(Clear	1	Disable
	(Disabled	0	Read: Disabled
	E	Enabled	1	Read: Enabled
K	RW PREGION1WA			Write '1' to Disable interrupt for PREGION[1].WA event
				See EVENTS_PREGION[1].WA
		Clear	1	Disable
]	Disabled	0	Read: Disabled
	E	Enabled	1	Read: Enabled
L	RW PREGION1RA			Write '1' to Disable interrupt for PREGION[1].RA event
				See EVENTS_PREGION[1].RA
		Clear	1	Disable
	[Disabled	0	Read: Disabled
	E	Enabled	1	Read: Enabled

45.1.4 NMIEN

Address offset: 0x320

Enable or disable non-maskable interrupt

Bitı	numbe	r		31 30	29	28 2	7 2	6 25	5 24	23 22 2	21 20	19 1	.8 1	7 16	15	14 :	13 12	2 11	. 10	9	8	7 6	5	4	3	2 1	L 0
Id						l	L I	K J	-1												- 1	H G	F	Ε	D	C E	3 A
Res	et 0x0(0000000		0 0	0	0 (0 (0 0	0	0 0 0	0 0	0 (0 (0	0	0	0 0	0	0	0	0 (0	0	0	0	0 0	0 (
Id	RW	Field	Value Id	Value	:					Descrip	tion																
Α	RW	REGION0WA								Enable	or dis	able	nor	n-ma	skal	ole i	nteri	rupt	for I	REG	ION	[0].\	VA				
										event																	
										See EVE	ENTS_	REG	ION	[0].v	VA												
			Disabled	0						Disable																	
			Enabled	1						Enable																	
В	RW	REGIONORA								Enable	or dis	able	nor	n-ma	skal	ole i	nteri	rupt	for I	REG	ION	[0].F	RA				
										event																	
										See EVE	ENTS_	REG	ION	[0].R	A												
			Disabled	0						Disable																	
			Enabled	1						Enable																	
С	RW	REGION1WA								Enable	or dis	able	nor	n-ma	skal	ole i	nteri	rupt	for I	REG	ION	[1].\	VA				
										event																	
										See EVE	ENTS_	REG	ION	[1].v	VA												
			Disabled	0						Disable																	
			Enabled	1						Enable																	



Rit r	numbe	r		31 30	29 28	27	26.2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	idilibe			31 30	25 20		ΣΟ 2 Κ .		H G F E D C B A
	-t 0x0	000000		0 0	0 0				0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value	•				Description
D		REGION1RA							Enable or disable non-maskable interrupt for REGION[1].RA
									event
									See EVENTS DECION[4] DA
			Disabled	0					See EVENTS_REGION[1].RA Disable
			Enabled	1					Enable
E	RW	REGION2WA	Lilabica	-					Enable or disable non-maskable interrupt for REGION[2].WA
_									event
			Disabled	0					See EVENTS_REGION[2].WA
			Disabled Enabled	0					Disable Enable
F	RW/	REGION2RA	Lilabieu	1					Enable or disable non-maskable interrupt for REGION[2].RA
•	11.00	REGIONZINA							event
				_					See EVENTS_REGION[2].RA
			Disabled	0					Disable
G	D\A/	REGION3WA	Enabled	1					Enable Enable or disable non-maskable interrupt for REGION[3].WA
G	NVV	REGIONSWA							event
				_					See EVENTS_REGION[3].WA
			Disabled	0					Disable
ш	D\A/	REGION3RA	Enabled	1					Enable Enable or disable non-markable interrupt for RECION(2) PA
Н	I VV	REGIONSKA							Enable or disable non-maskable interrupt for REGION[3].RA event
				_					See EVENTS_REGION[3].RA
			Disabled	0					Disable
1	D\A/	PREGIONOWA	Enabled	1					Enable Finable as disable non markable intervent for PRECIONIO WA
'	NVV	PREGIONOWA							Enable or disable non-maskable interrupt for PREGION[0].WA event
				_					See EVENTS_PREGION[0].WA
			Disabled	0					Disable
	D\A/	DDECIONODA	Enabled	1					Enable
J	KVV	PREGION0RA							Enable or disable non-maskable interrupt for PREGION[0].RA event
									See EVENTS_PREGION[0].RA
			Disabled	0					Disable
14	DIA	PDECIONAVA	Enabled	1					Enable
K	RW	PREGION1WA							Enable or disable non-maskable interrupt for PREGION[1].WA
									event
									See EVENTS_PREGION[1].WA
			Disabled	0					Disable
			Enabled	1					Enable
L	RW	PREGION1RA							Enable or disable non-maskable interrupt for PREGION[1].RA
									event
									See EVENTS_PREGION[1].RA
			Disabled	0					Disable
			Enabled	1					Enable

45.1.5 NMIENSET

Address offset: 0x324

Enable non-maskable interrupt



Bit	number		31 30 29	28 27	7 26	25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				L	. K	J I	H G F E D C B A
Res	set 0x00000000			0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value				Description
Α	RW REGIONOWA						Write '1' to Enable non-maskable interrupt for REGION[0].WA
							event
							See EVENTS_REGION[0].WA
		Set	1				Enable
		Disabled Enabled	0 1				Read: Disabled Read: Enabled
В	RW REGIONORA	Enabled	1				Write '1' to Enable non-maskable interrupt for REGION[0].RA
U	NW REGIONORA						event
		C-1	1				See EVENTS_REGION[0].RA
		Set Disabled	1				Enable Read: Disabled
		Enabled	1				Read: Enabled
С	RW REGION1WA	Enabled	1				Write '1' to Enable non-maskable interrupt for REGION[1].WA
-							event
		C-t	1				See EVENTS_REGION[1].WA
		Set Disabled	1 0				Enable Read: Disabled
		Enabled	1				Read: Enabled
D	RW REGION1RA	Enabled	•				Write '1' to Enable non-maskable interrupt for REGION[1].RA
							event
							Con EVENTS DECION[4] DA
		Set	1				See EVENTS_REGION[1].RA Enable
		Disabled	0				Read: Disabled
		Enabled	1				Read: Enabled
E	RW REGION2WA						Write '1' to Enable non-maskable interrupt for REGION[2].WA
							event
							See EVENTS_REGION[2].WA
		Set	1				Enable
		Disabled	0				Read: Disabled
		Enabled	1				Read: Enabled
F	RW REGION2RA						Write '1' to Enable non-maskable interrupt for REGION[2].RA
							event
							See EVENTS_REGION[2].RA
		Set	1				Enable
		Disabled	0				Read: Disabled
		Enabled	1				Read: Enabled
G	RW REGION3WA						Write '1' to Enable non-maskable interrupt for REGION[3].WA
							event
							See EVENTS_REGION[3].WA
		Set	1				Enable
		Disabled	0				Read: Disabled
		Enabled	1				Read: Enabled
Н	RW REGION3RA						Write '1' to Enable non-maskable interrupt for REGION[3].RA
							event
							See EVENTS_REGION[3].RA
		Set	1				Enable
		Disabled	0				Read: Disabled
		Enabled	1				Read: Enabled
I	RW PREGIONOWA						Write '1' to Enable non-maskable interrupt for PREGION[0].WA
							event
							See EVENTS_PREGION[0].WA



Bit num	ber		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			LKJI	HGFEDCBA
Reset 0	x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id R\	V Field	Value Id	Value	Description
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
J RV	V PREGIONORA			Write '1' to Enable non-maskable interrupt for PREGION[0].RA
				event
				See EVENTS_PREGION[0].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
K RV	V PREGION1WA			Write '1' to Enable non-maskable interrupt for PREGION[1].WA
				event
				See EVENTS PREGION[1].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
L RV	V PREGION1RA			Write '1' to Enable non-maskable interrupt for PREGION[1].RA
				event
				See EVENTS DECION[1] DA
		Set	1	See EVENTS_PREGION[1].RA Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
		Lilableu	1	Neau. Lilabieu

45.1.6 NMIENCLR

Address offset: 0x328

Disable non-maskable interrupt

Bit nui	mbe	r		31	. 30	29	28 2	27 2	6 2	5 2	4 23	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id								LI	K J		ı																Н	G	F E	D	С	В	Α
Reset	0x0	0000000		0	0	0	0	0 (0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0
ld F	RW	Field	Value Id	Va	alue						D	escr	ripti	on																			
A F	RW	REGION0WA									W	/rite	e '1'	to I	Disa	able	no	n-n	nas	kab	le i	nter	rup	t fo	r R	EGI]NC	0].\	NΑ				
											ev	vent	t																				
											Se	-е <u>F</u>	VEN	VTS	RE	GIO	ONI	01. V	VA.														
			Clear	1								isab						•															
			Disabled	0							Re	ead:	: Dis	sabl	led																		
			Enabled	1							Re	ead:	: En	abl	ed																		
B F	RW	REGIONORA									W	/rite	e '1'	to I	Disa	able	no	n-n	nas	kab	le i	nter	rup	t fo	r R	EGI) NC	0].[RA				
											ev	vent	t																				
											Se	эр <u>F</u>	VEN	JTS	RF	GIO	אונו	11 R	24														
			Clear	1								isab				0,0	,,,,	<i>,</i> ,,,,															
			Disabled	0									: Dis	sabl	led																		
			Enabled	1							Re	ead	: En	able	ed																		
C F	RW	REGION1WA									W	/rite	e '1'	to I	Disa	able	no	n-n	nas	kab	le i	nter	rup	t fo	r R	EGI	ואכ	1].\	NΑ				
											ev	vent	t																				
											Se	эр <u>F</u>	VEN	JTS	RF	GIO	אור.	11 V	1/Δ														
			Clear	1								isab		ي		0,0	,,,[-	.,	•/.														
			Disabled	0							_		: Dis	abl	led																		
			Enabled	1									: En																				
D F	RW	REGION1RA									W	/rite	e '1'	to I	Disa	able	no	n-n	nas	kab	le i	nter	rup	ot fo	r R	EGI) NC	1].F	RA				
												vent																					
											_			ıTC			2015																
											56	ee E	VEN	v / S_	_KE	GIC	ב]או <i>ע</i>	ı J. K	A														



	numbe	er			4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				LKJI	
		0000000 Field	Value Id	Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	IVVV	riciu	Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW	REGION2WA		-	Write '1' to Disable non-maskable interrupt for REGION[2].WA
					event
					See EVENTS_REGION[2].WA
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	REGION2RA			Write '1' to Disable non-maskable interrupt for REGION[2].RA
					event
					C EVENTS DECIONAL DA
			Clear	1	See EVENTS_REGION[2].RA
			Disabled	0	Disable Read: Disabled
			Enabled	1	Read: Enabled
G	RW	REGION3WA	Lilableu	1	Write '1' to Disable non-maskable interrupt for REGION[3].WA
•	11.00	REGIONSWA			event
					See EVENTS_REGION[3].WA
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	REGION3RA			Write '1' to Disable non-maskable interrupt for REGION[3].RA
					event
					See EVENTS_REGION[3].RA
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
I	RW	PREGIONOWA			Write '1' to Disable non-maskable interrupt for PREGION[0].WA
					event
					See EVENTS PREGION[0].WA
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
J	RW	PREGIONORA			Write '1' to Disable non-maskable interrupt for PREGION[0].RA
					event
					See EVENTS_PREGION[0].RA
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
K	RW	PREGION1WA			Write '1' to Disable non-maskable interrupt for PREGION[1].WA
					event
					See EVENTS_PREGION[1].WA
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
L	RW	PREGION1RA			Write '1' to Disable non-maskable interrupt for PREGION[1].RA
					event
					See EVENTS_PREGION[1].RA
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled



45.1.7 PERREGION[0].SUBSTATWA

Address offset: 0x400

Source of event/interrupt in region 0, write access detected while corresponding subregion was enabled for watching

wa	tCHII	119																											
Bit r	numbe	er		31 30	29 2	8 2	7 26	25	24	3 22 21 20 19 1	8	17 :	16	15	1	4	13	12	11	10	9	8	7	6	5	4	3	2	1
Id				f e	d (c b	а	Z	Υ	WVUTS	S	R	Q	Р	C)	N	M	L	K	J	1	Н	G	F	Ε	D	С	В
Res	et 0x0	0000000		0 0	0 (0	0	0	0	00000	0	0	0	0	C	כ	0	0	0	0	0	0	0	0	0	0	0	0	0
ld	RW	Field	Value Id	Value						escription																			
Α	RW	SR0								ubregion 0 in reg	gio	n 0	(v	vrit	e '	'1'	to o	cle	ar)										
			NoAccess	0						o write access o	CCI	urre	ed	in t	thi	is s	subi	reg	gion										
			Access	1						rite access(es) o	oco	urr	ec	l in	th	iis	sub	re	gio	1									
В	RW	SR1								ubregion 1 in reg	gio	n 0	(v	vrit	e '	'1'	to o	cle	ar)										
			NoAccess	0						o write access o	CCI	urre	ed	in t	thi	is s	subi	reg	gion										
			Access	1						rite access(es) o	oco	urr	ed	l in	th	iis	sub	re	gio	1									
С	RW	SR2								ubregion 2 in reg	gio	n 0	(v	vrit	e '	'1'	to o	cle	ar)										
			NoAccess	0						o write access o	CCI	urre	ed	in t	thi	is s	subi	reg	gion										
			Access	1						rite access(es) o	oco	urr	ed	l in	th	iis	sub	re	gio	1									
D	RW	SR3								ubregion 3 in reg	gio	n 0	(v	vrit	e '	'1'	to o	cle	ar)										
			NoAccess	0						o write access o	CCI	urre	ed	in t	thi	is s	subi	reg	gion										
			Access	1						rite access(es) o	oco	urr	ed	l in	th	iis	sub	re	gio	า									
E	RW	SR4								ubregion 4 in reg	gio	n 0	(v	vrit	e '	1'	to o	cle	ar)										
			NoAccess	0						o write access o	CCI	urre	ed	in t	thi	is s	subi	reg	gion										
			Access	1						rite access(es) o	oco	urr	ed	lin	th	iis	sub	re	gio	1									
F	RW	SR5								ubregion 5 in reg	gio	n 0	(v	vrit	e '	'1'	to o	cle	ar)										
			NoAccess	0						o write access o	CCI	urre	ed	in t	thi	is s	subi	reg	gion										
			Access	1						rite access(es) o	oco	urr	ed	l in	th	iis	sub	re	gio	1									
G	RW	SR6								ubregion 6 in reg	gio	n 0	(v	vrit	e '	'1'	to o	cle	ar)										
			NoAccess	0						o write access o	CCI	urre	ed	in t	thi	is s	subi	res	, gion										
			Access	1						rite access(es) o																			
Н	RW	SR7								ubregion 7 in reg									_										
			NoAccess	0						o write access o	_		•																
			Access	1						rite access(es) o																			
	RW/	SR8	recess	-						ubregion 8 in reg									-	•									
•		3110	NoAccess	0						o write access o	_		•																
			Access	1						rite access(es) o																			
J	D\A/	SR9	Access	-						ubregion 9 in reg									_										
,	11.00	31.3	NoAccess	0						o write access o	_		•																
			Access	1																									
V	D\A/	SR10	Access	1						rite access(es) o									-										
K	KVV	2K10	No Access	0						ubregion 10 in re	_																		
			NoAccess							o write access o								-											
	DIA	CD11	Access	1						rite access(es) o																			
L	KVV	SR11	N = A =====	0						ıbregion 11 in re	-																		
			NoAccess	0						o write access o																			
			Access	1						rite access(es) o									-										
M	RW	SR12								ubregion 12 in re	•									•									
			NoAccess	0						o write access o																			
			Access	1						rite access(es) o									_										
N	RW	SR13								ubregion 13 in re	_																		
			NoAccess	0						o write access o																			
			Access	1						rite access(es) o									-										
0	RW	SR14								ubregion 14 in re	-																		
			NoAccess	0						o write access o	CCI	urre	ed	in t	thi	is s	subi	reg	gion										
			Access	1						rite access(es) o	occ	urr	ec	l in	th	iis	sub	re	gio	١									
Р	RW	SR15								ubregion 15 in re	egi	on	0 (wri	ite	· '1	l' to	cl	ear)									
			NoAccess	0						o write access o	CCI	urre	ed	in t	thi	is s	subi	reg	gion										
			Access	1						rite access(es) o	oco	urr	ed	l in	th	is	sub	re	gio	1									
Q	RW	SR16								ıbregion 16 in re	egi	on	0 (wri	ite	· '1	l' to	cl	ear	1									



Bitı	numbe	er		31 30	29 2	8 27	7 26	25 24	1 23	22 21	. 20	19 1	8 17	16 1	L5 1	4 13	12 :	1 10	9	8	7 6	5 5	4	3 2	1	0
Id				f e	d c	b	а	Z Y	Х	w v	U	Т 9	S R	Q	P (N	М	L K	J	1.1	H (i F	Ε	D C	В	Α
Res	et 0x0	0000000		0 0	0 0	0	0	0 0	0	0 0	0	0 (0 0	0	0 (0	0	0 0	0	0 () (0	0	0 0	0	0
Id	RW	Field	Value Id	Value					Des	script	ion															
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
R	RW	SR17							Sub	oregio	n 17	' in re	egion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
S	RW	SR18							Sub	regio	n 18	in re	egion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
Т	RW	SR19							Sub	oregio	n 19	in re	egion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
U	RW	SR20							Sub	regio	n 20) in re	egion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
٧	RW	SR21							Sub	oregio	n 21	. in re	egion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
W	RW	SR22							Sub	oregio	n 22	! in re	gion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
Χ	RW	SR23							Sub	oregio	n 23	in re	gion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
Υ	RW	SR24							Sub	oregio	n 24	in re	egion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
Z	RW	SR25							Sub	oregio	n 25	in re	gion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
а	RW	SR26							Sub	oregio	n 26	in re	egion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
b	RW	SR27							Sub	oregio	n 27	' in re	egion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
С	RW	SR28							Sub	oregio	n 28	in re	egion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	ccur	red i	n th	is su	breg	ion								
d	RW	SR29							Sub	oregio	n 29	in re	egion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
e	RW	SR30							Sub	oregio	n 30) in re	egion	0 (v	rite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								
f	RW	SR31							Sub	oregio	n 31	in re	egion	0 (v	vrite	'1' t	o cle	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	n thi	s sub	regi	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is su	breg	ion								

45.1.8 PERREGION[0].SUBSTATRA

Address offset: 0x404

Source of event/interrupt in region 0, read access detected while corresponding subregion was enabled for watching



The Control	Bit r	numbe	er		31 30	29 28	27 26	25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
No Wilsing Wilsing Workers Subregion () minigon () (with "1" to clarge () monorable construction () (with "1" to clarge () monorable construction () (with "1" to clarge () monorable construction () monorable construc									
AR W SRD NoAccess 0 Accessor on the subregion of centure 1'to clearly when subregion (accessed in this subregion of the	Res	et 0x0	0000000		0 0	0 0	0 0	0 (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
No.	Id	RW	Field	Value Id	Value				Description
Rev	Α	RW	SR0						Subregion 0 in region 0 (write '1' to clear)
No.				NoAccess	0				No read access occurred in this subregion
No.				Access	1				Read access(es) occurred in this subregion
Maccess 1	В	RW	SR1						Subregion 1 in region 0 (write '1' to clear)
C RW SR2 NoAccess 0 No medial access occurred in this subregion D RW SR3 SR3 Subregion 2 in region 0 (write "1" to clear) D RW SR3 No read access occurred in this subregion E RW SR4 No read access courred in this subregion E RW SR4 Subregion 3 in region 0 (write "1" to clear) F RW SR4 Subregion 5 in region 0 (write "1" to clear) F RW SR5 Inception 0 (write "1" to clear) F RW SR5 Inception 0 (write "1" to clear) G RW SR6 Inception 0 (write "1" to clear) G RW SR6 Inception 0 (write "1" to clear) Moncess 0 No read access occurred in this subregion Moncess 1 Read access(se) occurred in this subregion Moncess 0 No read access occurred in this subregion Moncess 1 Read access(se) occurred in this subregion Moncess 1 Read access(se) occurred in this subregion				NoAccess	0				No read access occurred in this subregion
No read access occurred in this subregion Access 1 Read access[es] occurred in this subregion Read ac				Access	1				Read access(es) occurred in this subregion
No.	С	RW	SR2						Subregion 2 in region 0 (write '1' to clear)
No				NoAccess	0				No read access occurred in this subregion
No Access				Access	1				Read access(es) occurred in this subregion
Read access(es) occurred in this subregion Subregion Air region (write '1' to clear) NoAccess No Read access (excurred in this subregion No Re	D	RW	SR3						Subregion 3 in region 0 (write '1' to clear)
E RW SR4 Security Subregion 1 in region 0 (write "1" to clear) F RW SR5 1 Read accesses occurred in this subregion F RW SR5 NoAccess 1 Read accesses occurred in this subregion G RW SR6 1 Read accesses occurred in this subregion G RW SR6 1 Read accesses occurred in this subregion G RW SR7 Image: Region 0 (write "1" to clear) MCCess 1 Read access (es) occurred in this subregion MCCESS 1 Read access (es) occurred in this subregion MCCESS 1 Read access (es) occurred in this subregion MCCESS 1 Read access (es) occurred in this subregion MCCESS 1 Read access occurred in this subregion MCCESS 1 Read access occurred in this subregion MCCESS 0 No read access occurred in this subregion MCCESS 1 Read access occurred in this subregion MCCESS 1 Read access occurred in this subregion				NoAccess	0				No read access occurred in this subregion
No.				Access	1				Read access(es) occurred in this subregion
	Е	RW	SR4						Subregion 4 in region 0 (write '1' to clear)
F				NoAccess	0				No read access occurred in this subregion
No.				Access	1				Read access(es) occurred in this subregion
Access	F	RW	SR5						Subregion 5 in region 0 (write '1' to clear)
G RW S86 Subregion 6 in region 0 (write '1' to clear) No No Access 0 No read access cocurred in this subregion H RW S87 Subregion 7 in region 0 (write '1' to clear) I RW S87 Subregion 7 in region 0 (write '1' to clear) I RW S88 1 Read access(es) occurred in this subregion I RW S88 Subregion 8 in region 0 (write '1' to clear) J RW S88 Subregion 8 in region 0 (write '1' to clear) J RW S89 Subregion 8 in region 0 (write '1' to clear) J RW S89 Subregion 9 in region 0 (write '1' to clear) J RW S89 Subregion 10 in region 0 (write '1' to clear) J RW S810 Subregion 10 in region 0 (write '1' to clear) J RW S810 Subregion 10 in region 0 (write '1' to clear) J RW S810 Subregion 10 in region 0 (write '1' to clear) J RW S810 Subregion 10 in region 0 (write '1' to clear) J R				NoAccess	0				No read access occurred in this subregion
No Access 1				Access	1				Read access(es) occurred in this subregion
Rev	G	RW	SR6						Subregion 6 in region 0 (write '1' to clear)
H				NoAccess	0				No read access occurred in this subregion
NoAccess NoAccess No No read access occurred in this subregion				Access	1				Read access(es) occurred in this subregion
RW SR8	Н	RW	SR7						Subregion 7 in region 0 (write '1' to clear)
RW SR8				NoAccess	0				No read access occurred in this subregion
No Access 1 Read access(es) occurred in this subregion				Access	1				Read access(es) occurred in this subregion
Read access(es) occurred in this subregion Subregion Subregion Noread access (es) occurred in this subregion Noread Noread access occurred in this subregion Noread access occurred in Noread access o	1	RW	SR8						Subregion 8 in region 0 (write '1' to clear)
Subregion 9 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion				NoAccess	0				No read access occurred in this subregion
NoAccess 1 Read access(es) occurred in this subregion K RW SR10 Subregion 10 in region 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion K RW SR11 Subregion 10 in region 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion L RW SR11 Subregion 11 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion M RW SR12 Subregion 11 in region 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion				Access	1				Read access(es) occurred in this subregion
Access 1 Read access(es) occurred in this subregion	J	RW	SR9						Subregion 9 in region 0 (write '1' to clear)
K RW SR10 NoAccess 0 No No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion				NoAccess	0				No read access occurred in this subregion
NoAccess 0 No Fead access occurred in this subregion Access 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion NoAccess 0 No Fead access occurred in this subregion NoAccess 0 No Fead access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No Fead access occurred in this subregion NoAccess 0 No Fead access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion				Access	1				Read access(es) occurred in this subregion
L RW SR11 Subregion 11 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion M RW SR12 Subregion 12 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion No read access occurred in this subregion Access 1 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 2 Subregion 17 in region 0 (write '1' to clear) No read access occurred in this subregion Access 3 Subregion 17 in region 0 (write '1' to clear) No read access occurred in this subregion Access 3 Subregion 17 in region 0 (write '1' to clear) No read access occurred in this subregion Access 3 Read access(es) occurred in this subregion Access 3 Read access(es) occurred in this subregion Access 4 Read access(es) occurred in this subregion Access 5 Read access(es) occurred in this subregion Access 5 Read access(es) occurred in this subregion Access 6 Read access(es) occurred in this subregion Access 6 Read access(es) occurred in this subregion Access 6 Read access(es) occurred in thi	K	RW	SR10						Subregion 10 in region 0 (write '1' to clear)
L RW SR11 Subregion 11 in region 0 (write '1' to clear) NoAccess 1 Read access occurred in this subregion RRW SR12 Subregion 12 in region 0 (write '1' to clear) NoAccess 1 Read access occurred in this subregion No RW SR12 Subregion 12 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Read access(es) occurred in this subregion Read access(es) occurred in this subregion Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion				NoAccess	0				No read access occurred in this subregion
NOAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion M RW SR12 Subregion 12 in region 0 (write '1' to clear) NOACCESS 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NOACCESS 1 Read access occurred in this subregion NOACCESS 1 Read access occurred in this subregion NOACCESS 1 Read access(es) occurred in this subregion				Access	1				Read access(es) occurred in this subregion
M RW SR12 NoAccess 0 No No read access occurred in this subregion N RW SR13 NoAccess 0 No Read access occurred in this subregion N RW SR13 NoAccess 0 No Read access occurred in this subregion N RW SR13 NoAccess 0 No Read access occurred in this subregion N RW SR14 NoAccess 0 No Read access occurred in this subregion N RW SR15 NoAccess 0 No Read access occurred in this subregion N RW SR14 NoAccess 0 No Read access occurred in this subregion N NoAccess 0 No Read access occurred in this subregion N No Read access occurred in this subregion R RW SR16 NoAccess 1 Read access occurred in this subregion N No Read acce	L	RW	SR11						Subregion 11 in region 0 (write '1' to clear)
M RW SR12 Subregion 12 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion				NoAccess	0				No read access occurred in this subregion
No Access 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion No RW SR13 No Access 0 No read access occurred in this subregion 0 (write '1' to clear) No Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion No RW SR14 No Access 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion P RW SR15 No RCCESS 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion No Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion No Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion				Access	1				Read access(es) occurred in this subregion
N RW SR13 N ACCESS 1 Read access(es) occurred in this subregion N N RW SR13 N NACCESS 0 NO No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion	M	RW	SR12						Subregion 12 in region 0 (write '1' to clear)
N RW SR13 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access occurred in this subregion Read access occurred in this subregion NoAccess 1 Read access occurred in this subregion Read access occurred in this subregion NoAccess 1 Read access occurred in this subregion				NoAccess	0				No read access occurred in this subregion
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 14 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion No read access occurred in this subregion Access 1 Read access occurred in this subregion No read access occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access occurred in this subregion				Access	1				Read access(es) occurred in this subregion
Access 1 Read access(es) occurred in this subregion O RW SR14 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion P RW SR15 NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion	N	RW	SR13						Subregion 13 in region 0 (write '1' to clear)
O RW SR14 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion NoAccess 1 Read access occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 NoAccess 0 No read access occurred in this subregion Read access occurred in this subregion NoAccess 1 Read access occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion				NoAccess	0				No read access occurred in this subregion
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion P RW SR15 Subregion 15 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 16 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 17 in region 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion R RW SR17 Subregion 17 in region 0 (write '1' to clear) NoAccess 1 Read access occurred in this subregion R Read access occurred in this subregion				Access	1				Read access(es) occurred in this subregion
P RW SR15 NoAccess 0 No No read access occurred in this subregion Q RW SR16 NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Subregion 15 in region 0 (write '1' to clear) Read access occurred in this subregion Subregion 16 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Read access(es) occurred in this subregion Read access(es) occurred in this subregion Subregion 17 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion	0	RW	SR14						Subregion 14 in region 0 (write '1' to clear)
P RW SR15 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Q RW SR16 NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion Read access occurred in this subregion Read access occurred in this subregion				NoAccess	0				No read access occurred in this subregion
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Q RW SR16 Subregion 16 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion R RW SR17 Subregion 17 in region 0 (write '1' to clear) NoAccess 1 No read access occurred in this subregion R Read access occurred in this subregion				Access	1				Read access(es) occurred in this subregion
Access 1 Read access(es) occurred in this subregion Q RW SR16 Subregion 16 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion R RW SR17 Subregion 17 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access occurred in this subregion Read access occurred in this subregion Read access occurred in this subregion	Р	RW	SR15						Subregion 15 in region 0 (write '1' to clear)
Q RW SR16 Subregion 16 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 17 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access occurred in this subregion Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion				NoAccess	0				No read access occurred in this subregion
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion R RW SR17 Subregion 17 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion				Access	1				Read access(es) occurred in this subregion
Access 1 Read access(es) occurred in this subregion R RW SR17 Subregion 17 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion	Q	RW	SR16						Subregion 16 in region 0 (write '1' to clear)
R RW SR17 Subregion 17 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion				NoAccess	0				No read access occurred in this subregion
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion				Access	1				Read access(es) occurred in this subregion
Access 1 Read access(es) occurred in this subregion	R	RW	SR17						Subregion 17 in region 0 (write '1' to clear)
* * * * * * * * * * * * * * * * * * * *				NoAccess	0				No read access occurred in this subregion
S RW SR18 Subregion 18 in region 0 (write '1' to clear)				Access	1				Read access(es) occurred in this subregion
	S	RW	SR18						Subregion 18 in region 0 (write '1' to clear)



Bit r	numbe	er		31 30	29	28	27 2	6 2	25 24	1 2	3 22 21 20	0 19 1	8 17	16	5 15	14	13	12	1:	1 10	9	8	7	6	5	4	3 2	2 1	L O
Id											x w v u																		
	et OxO	0000000									0 0 0 0																		
Id		Field	Value Id	Value							escription			Ĭ			Ť												
			NoAccess	0							lo read acc		ccurre	ed	in tl	his	sub	reg	ior	1									
			Access	1							lead access							-											
Т	RW	SR19									ubregion 1																		
			NoAccess	0							lo read acc		-																
			Access	1							lead access							_											
U	RW	SR20								S	ubregion 2	20 in r	egion	0	(wri	ite	'1' t	o cl	- lea	r)									
			NoAccess	0							lo read acc		-																
			Access	1							lead access							_											
٧	RW	SR21								S	ubregion 2	21 in r	egion	0 0	(wri	ite	'1' t	o cl	lea	r)									
			NoAccess	0						Ν	lo read acc	ess o	ccurre	ed	in th	his	sub	reg	ior	1									
			Access	1						R	lead access	s(es) c	ccuri	red	in t	hi	sub	re	gio	n									
W	RW	SR22								S	ubregion 2	22 in r	egion	0	(wri	te	'1' t	o cl	lea	r)									
			NoAccess	0						Ν	lo read acc	ess o	ccurre	ed	in tl	his	sub	reg	ior	1									
			Access	1						R	lead access	s(es) c	ccuri	red	in t	hi	sub	re	gio	n									
Χ	RW	SR23								S	ubregion 2	23 in r	egion	0	(wri	ite	'1' t	o cl	lea	r)									
			NoAccess	0						Ν	lo read acc	ess o	ccurr	ed	in tl	his	sub	reg	ior	1									
			Access	1						R	lead access	s(es) c	ccuri	red	in t	hi	sub	re	gio	n									
Υ	RW	SR24								S	ubregion 2	24 in r	egion	0	(wri	te	'1' t	o cl	lea	r)									
			NoAccess	0						١	lo read acc	ess o	ccurre	ed	in tl	his	sub	reg	ior	ı									
			Access	1						R	lead access	s(es) c	ccuri	red	in t	hi	sub	re	gio	n									
Z	RW	SR25								S	ubregion 2	25 in r	egion	0	(wri	ite	'1' t	o cl	lea	r)									
			NoAccess	0						Ν	lo read acc	ess o	ccurre	ed	in tl	his	sub	reg	ior	1									
			Access	1						R	lead access	s(es) c	ccuri	red	in t	hi	sub	re	gio	n									
а	RW	SR26								S	ubregion 2	26 in r	egion	0	(wri	te	'1' t	o cl	lea	r)									
			NoAccess	0						١	lo read acc	ess o	ccurr	ed	in tl	his	sub	reg	ior	1									
			Access	1						R	lead access	s(es) c	ccuri	red	in t	hi	sub	re	gio	n									
b	RW	SR27								S	ubregion 2	27 in r	egion	0	(wri	te	'1' t	o cl	lea	r)									
			NoAccess	0						١	lo read acc	ess o	ccurr	ed	in tl	his	sub	reg	ior	1									
			Access	1						R	lead access	s(es) c	ccuri	red	in t	hi	suk	re	gio	n									
С	RW	SR28								S	ubregion 2	28 in r	egion	0	(wri	te	'1' t	o cl	lea	r)									
			NoAccess	0						١	lo read acc	ess o	ccurre	ed	in tl	his	sub	reg	ior	1									
			Access	1						R	lead access	s(es) c	ccuri	red	in t	hi	suk	re	gio	n									
d	RW	SR29								S	ubregion 2	29 in r	egion	0	(wri	te	'1' t	o cl	lea	r)									
			NoAccess	0							lo read acc							_											
			Access	1							lead access								-										
е	RW	SR30									ubregion 3		-																
			NoAccess	0							lo read acc							_											
			Access	1							lead access																		
f	RW	SR31									ubregion 3		-																
			NoAccess	0							lo read acc							_											
			Access	1						R	lead access	s(es) c	ccuri	red	in t	hi	sut	re	gio	n									

45.1.9 PERREGION[1].SUBSTATWA

Address offset: 0x408

Source of event/interrupt in region 1, write access detected while corresponding subregion was enabled for watching

Bit	numb	er		31	1 30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 1	8 1	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				f	е	d	С	b	а	Z	Υ	Х	W	V	U 1	Γ 5	S R	. a	P	0	Ν	М	L	K	J	l	Н	G	F	Ε	D	С	ВА
Res	et 0x(00000000		0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																													
Α	RW	SRO										Sub	regi	ion	0 in	re	gion	1 (writ	e '1	' to	clea	ar)										
			NoAccess	0								No	writ	e a	cces	s o	ccui	rec	in 1	this	suk	reg	ion										
			Access	1								Wri	te a	cce	ss(e	s) c	occu	rre	d in	thi	s su	bre	gior	1									



Rit r	numbe	or .		31 30	29 28	27	26.2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	iumbe	-1							X W V U T S R Q P O N M L K J I H G F E D C B A
	et 0x0	0000000							0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value					Description
В		SR1							Subregion 1 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
С	RW	SR2		_					Subregion 2 in region 1 (write '1' to clear)
·		5112	NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
D	R\M	SR3	7100033	•					Subregion 3 in region 1 (write '1' to clear)
	11.00	31(3	NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
E	R\//	SR4	Access	_					Subregion 4 in region 1 (write '1' to clear)
_	11.00	314	NoAccess	0					
				1					No write access occurred in this subregion
Е	D\A/	CDE	Access	1					Write access(es) occurred in this subregion
г	KVV	SR5	NaAssass	0					Subregion 5 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
	DIA	cnc.	Access	1					Write access(es) occurred in this subregion
G	кW	SR6	NaAssass	0					Subregion 6 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Н	RW	SR7		_					Subregion 7 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
ı	RW	SR8							Subregion 8 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
J	RW	SR9							Subregion 9 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
K	RW	SR10							Subregion 10 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
L	RW	SR11							Subregion 11 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
М	RW	SR12							Subregion 12 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
N	RW	SR13							Subregion 13 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
0	RW	SR14							Subregion 14 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Р	RW	SR15							Subregion 15 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Q	RW	SR16							Subregion 16 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
R	RW	SR17							Subregion 17 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
S	RW	SR18							Subregion 18 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Т	RW	SR19							Subregion 19 in region 1 (write '1' to clear)



Bit r	numbe	er		31 30) 20	9 28	3 2	7 21	6 2	5 2	4 :	23 22 21 :	20 19	18	3 17	1	6 1	5 1	4 1	13 1	12	11 1	LO	9 :	3 7	7 6	5	4	3	2	1	0
Id												X W V																				
	at OvO	0000000										0 0 0																				
Id		Field	Value Id	Value			Ŭ					Descriptio		Ŭ	Ŭ					•	Ů	٠	•					Ů	Ŭ	Ŭ	Ů	Ü
		Ticiu	NoAccess	0								No write a		00	cur	rei	d in	th	ic c	uhr	reg	ion										
			Access	1								Write acce									_											
U	RW	SR20	7,66633	-								Subregion		•																		
Ŭ		31120	NoAccess	0								No write a			_		•					,										
			Access	1								Write acce									_											
V	R\M	SR21	Access	_								Subregion																				
٧	IVV	31/21	NoAccess	0								No write a			_																	
			Access	1								Write acce									Ŭ											
W	D\A/	SR22	Access	1										•																		
VV	KVV	SKZZ	No Access	0								Subregion			_		•															
			NoAccess									No write a									_											
v/	D) 4 /	cn22	Access	1								Write acce																				
Х	RW	SR23		_								Subregion			_		•															
			NoAccess	0								No write a																				
			Access	1								Write acce																				
Υ	RW	SR24		_								Subregion			_		•															
			NoAccess	0								No write a									_											
			Access	1								Write acce																				
Z	RW	SR25										Subregion			_		•															
			NoAccess	0							1	No write a	access	00	cur	re	d in	th	is s	ubr	reg	ion										
			Access	1							١	Write acce	ess(es) o	ccui	rre	d ir	ı tł	nis s	sub	re	gion										
а	RW	SR26									9	Subregion	26 in	re	gior	า 1	(w	rite	e '1	' to	cl	ear)										
			NoAccess	0							1	No write a	access	00	cur	re	d in	th	is s	ubr	reg	ion										
			Access	1							١	Write acce	ess(es) o	ccu	rre	d ir	ı tł	nis s	sub	re	gion										
b	RW	SR27										Subregion	27 in	re	gior	า 1	(w	rite	· '1	' to	cl	ear)										
			NoAccess	0							1	No write a	access	00	cur	re	d in	th	is s	ubr	reg	ion										
			Access	1							١	Write acce	ess(es) o	ccui	rre	d ir	ı th	nis s	sub	re	gion										
C	RW	SR28									9	Subregion	28 in	re	gior	า 1	(w	rite	e '1	' to	cl	ear)										
			NoAccess	0							ſ	No write a	access	00	cur	re	d in	th	is s	ubr	reg	ion										
			Access	1							١	Write acce	ess(es) o	ccui	rre	d ir	t t	nis s	sub	re	gion										
d	RW	SR29									9	Subregion	29 in	re	gior	า 1	(w	rite	e '1	' to	cl	ear)										
			NoAccess	0							ı	No write a	access	00	cur	re	d in	th	is s	ubr	reg	ion										
			Access	1							١	Write acce	ess(es) o	ccu	rre	d ir	ı th	is s	sub	re	gion										
е	RW	SR30									9	Subregion	30 in	re	gior	ո 1	(w	rite	· '1	' to	cl	ear)										
			NoAccess	0							ı	No write a	access	00	cur	re	d in	th	is s	ubr	reg	ion										
			Access	1							١	Write acce	ess(es) o	ccui	rre	d ir	ı th	is s	sub	re	gion										
f	RW	SR31									9	Subregion	31 in	re	gior	า 1	(w	rite	e '1	' to	cl	ear)										
			NoAccess	0								No write a			-																	
			Access	1								Nrite acce									_											

45.1.10 PERREGION[1].SUBSTATRA

Address offset: 0x40C

Source of event/interrupt in region 1, read access detected while corresponding subregion was enabled for watching

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 :	21 2	0 1	19 1	8 1	7 16	5 15	14	13	12	11 :	10 9	9 8	3 7	6	5	4	3	2	1 0
Id				f	е	d	С	b	а	Z	Υ	Х	W	۷١	J	Т 9	S F	R O	P	0	Ν	М	L	Κ.		Н	G	F	Ε	D	С	В А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0	0 () (0 0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	llue							De	scrip	otio	n																	
Α	RW	SR0										Sub	reg	ion	0 ir	n reg	gior	1 (writ	e '1	' to	clea	ır)									
			NoAccess	0								No	rea	d ac	ces	s oc	cur	red	in t	his	subi	egi	on									
			Access	1								Rea	ad a	cces	s(e	es) o	ccu	rrec	lin	this	sub	regi	on									
В	RW	SR1										Sub	reg	ion	1 ir	n reg	gior	1 (writ	e '1	' to	clea	ır)									
			NoAccess	0								No	rea	d ac	ces	s oc	cur	red	in t	his	subi	egi	on									
			Access	1								Rea	ad a	cces	s(e	es) o	ccu	rrec	lin	this	sub	regi	on									



Bit n	umber		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Rese	et 0x000000	00	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
С	RW SR2		Subregion 2 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
D	RW SR3		Subregion 3 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
E	RW SR4		Subregion 4 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
F	RW SR5		Subregion 5 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
G	RW SR6		Subregion 6 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
Н	RW SR7		Subregion 7 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
I	RW SR8		Subregion 8 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
J	RW SR9		Subregion 9 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
K	RW SR10		Subregion 10 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
L	RW SR11		Subregion 11 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
М	RW SR12		Subregion 12 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
N	RW SR13		Subregion 13 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
0	RW SR14		Subregion 14 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
Р	RW SR15		Subregion 15 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
Q	RW SR16		Subregion 16 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
R	RW SR17		Subregion 17 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
S	RW SR18		Subregion 18 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
Т	RW SR19		Subregion 19 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
			Subregion 20 in region 1 (write '1' to clear)



Bit ı	number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				X W V U T S R Q P O N M L K J I H G F E D C B A
Res	set 0x00000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
٧	RW SR21		:	Subregion 21 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
W	RW SR22		:	Subregion 22 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
Χ	RW SR23		3	Subregion 23 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
Υ	RW SR24		;	Subregion 24 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
Z	RW SR25		;	Subregion 25 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
а	RW SR26		!	Subregion 26 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
b	RW SR27		:	Subregion 27 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
С	RW SR28		;	Subregion 28 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
d	RW SR29		:	Subregion 29 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
e	RW SR30		:	Subregion 30 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion
f	RW SR31			Subregion 31 in region 1 (write '1' to clear)
		NoAccess	0	No read access occurred in this subregion
		Access	1	Read access(es) occurred in this subregion

45.1.11 REGIONEN

Address offset: 0x510

Enable/disable regions watch

Bit r	iumbe	er		31	30 2	29 2	28 27	7 26	5 25	5 24	23	22	21 2	20 1	19 1	18 1	7 1	6 1	.5 1	L4 1	.3 1	2 11	. 10	9	8	7	6	5	4 3	3 2	1	0
Id							L	. K	J	-1																Н	G	F	E [) С	В	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0) (0	0	0 (0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Val	lue						De	scri	ptio	n																		
Α	RW	RGN0WA									Ena	able	/dis	abl	e w	rite	acc	ess	w	atcł	n in	regi	on[C)]								
			Disable	0							Dis	able	e wr	ite	acc	ess	wat	ch	in 1	this	reg	ion										
			Enable	1							Ena	able	wri	te a	ассе	ess	wat	ch i	n t	his	regi	on										
В	RW	RGNORA									Ena	able	/dis	abl	e re	ad	acce	ess	wa	tch	in r	egic	n[0]	l								
			Disable	0							Dis	able	e rea	ad a	ссе	ss '	wato	ch i	n t	his	regi	on										
			Enable	1							Ena	able	rea	d a	cce	ss v	/atc	h ir	n th	nis r	egic	n										
С	RW	RGN1WA									Ena	able	/dis	abl	e w	rite	acc	ess	w	atcl	n in	regi	on[1	.]								
			Disable	0							Dis	able	e wr	ite	acc	ess	wat	ch	in t	this	reg	ion										
			Enable	1							Ena	able	wri	te a	ассе	ess	wat	ch i	n t	his	regi	on										
D	RW	RGN1RA									Ena	able	/dis	abl	e re	ad	acce	ess	wa	itch	in r	egic	n[1]	l								



Bitı	numb	er		33	1 30	29	28 2	7 2	6 2	5 24	1 23	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 :	2 1	1 0
Id								LI	K J	-1																	Н	G	F	Ε	D (C E	3 A
Res	et 0x0	0000000		0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () 0
Id	RW	Field	Value Id	V	alue						D	esc	ripti	on																			
			Disable	0							Di	isak	ole re	ead	acc	ess	wa	tch	in 1	this	re	gio	n										
			Enable	1							Er	nab	le re	ead	acc	ess	wat	ch	in t	his	reg	ior	1										
Е	RW	RGN2WA									Er	nab	le/d	isal	ole v	writ	e ac	ces	s w	/ato	h i	n re	egic	n[2	2]								
			Disable	0							Di	isat	ole w	vrite	e ac	ces	s wa	atch	in	thi	s re	gic	n										
			Enable	1							Er	nab	le w	rite	acc	cess	wa	tch	in	this	re	gio	n										
F	RW	RGN2RA									Er	nab	le/d	isal	ole r	eac	d ac	ces	s w	atc	n in	re	gio	ո[2]								
			Disable	0							Di	isak	ole re	ead	acc	ess	wa	tch	in	this	re	gio	n										
			Enable	1							Er	nab	le re	ead	acc	ess	wat	ch	in t	his	reg	ior	1										
G	RW	RGN3WA									Er	nab	le/d	isal	ole v	writ	e ac	ces	s w	/ato	h i	n re	egic	n[3	3]								
			Disable	0							Di	isat	ole w	vrite	e ac	ces	s wa	atch	in	thi	s re	gic	n										
			Enable	1							Er	nab	le w	rite	acc	cess	wa	tch	in	this	re	gio	n										
Н	RW	RGN3RA									Er	nab	le/d	isal	ole r	eac	dac	ces	s w	atc	n in	re	gio	า[3]								
			Disable	0							Di	isak	ole re	ead	acc	ess	wa	tch	in	this	re	gio	n										
			Enable	1							Er	nab	le re	ead	acc	ess	wat	ch	in t	his	reg	ior	1										
I	RW	PRGN0WA									Er	nab	le/d	isal	ole v	writ	e ac	ces	s w	/ato	h i	n P	REG	ilO	N[0]							
			Disable	0							Di	isat	ole w	vrite	e ac	ces	s wa	atch	in	thi	s PI	REG	SIOI	V									
			Enable	1							Er	nab	le w	rite	acc	cess	wa	tch	in	this	PR	EG	101	I									
J	RW	PRGNORA									Er	nab	le/d	isal	ole r	eac	dac	ces	s w	atc	n in	PF	REG	101	(0]۱								
			Disable	0							Di	isak	ole re	ead	acc	ess	wa	tch	in	this	PR	EG	ION	I									
			Enable	1							Er	nab	le re	ead	acc	ess	wat	ch	in t	his	PR	EGI	ON										
K	RW	PRGN1WA									Er	nab	le/d	isal	ole v	writ	e ac	ces	s w	/ato	h i	n P	REG	ilO	N[1	.]							
			Disable	0							Di	isat	ole w	vrite	e ac	ces	s wa	atch	in	thi	s PI	REG	SIOI	V									
			Enable	1							Er	nab	le w	rite	acc	cess	wa	tch	in	this	PR	EG	ION	I									
L	RW	PRGN1RA									Er	nab	le/d	isal	ole r	eac	dac	ces	s w	atc	n in	PF	REG	101	N[1]								
			Disable	0							Di	isat	ole r	ead	acc	ess	wa	tch	in	this	PR	EG	ION	ı									
			Enable	1							Er	nab	le re	ead	acc	ess	wat	ch	in t	his	PR	EGI	ON										

45.1.12 REGIONENSET

Address offset: 0x514 Enable regions watch

Bit	numbe	r		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				L K J I	HGFEDCBA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	RGN0WA			Enable write access watch in region[0]
			Set	1	Enable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
В	RW	RGNORA			Enable read access watch in region[0]
			Set	1	Enable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
С	RW	RGN1WA			Enable write access watch in region[1]
			Set	1	Enable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
D	RW	RGN1RA			Enable read access watch in region[1]
			Set	1	Enable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
Е	RW	RGN2WA			Enable write access watch in region[2]
			Set	1	Enable write access watch in this region
			Disabled	0	Write access watch in this region is disabled



Bit	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L K J	I H G F E D C B A
Res	set 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Enabled	1	Write access watch in this region is enabled
F	RW RGN2RA			Enable read access watch in region[2]
		Set	1	Enable read access watch in this region
		Disabled	0	Read access watch in this region is disabled
		Enabled	1	Read access watch in this region is enabled
G	RW RGN3WA			Enable write access watch in region[3]
		Set	1	Enable write access watch in this region
		Disabled	0	Write access watch in this region is disabled
		Enabled	1	Write access watch in this region is enabled
Н	RW RGN3RA			Enable read access watch in region[3]
		Set	1	Enable read access watch in this region
		Disabled	0	Read access watch in this region is disabled
		Enabled	1	Read access watch in this region is enabled
T	RW PRGNOWA			Enable write access watch in PREGION[0]
		Set	1	Enable write access watch in this PREGION
		Disabled	0	Write access watch in this PREGION is disabled
		Enabled	1	Write access watch in this PREGION is enabled
J	RW PRGNORA			Enable read access watch in PREGION[0]
		Set	1	Enable read access watch in this PREGION
		Disabled	0	Read access watch in this PREGION is disabled
		Enabled	1	Read access watch in this PREGION is enabled
K	RW PRGN1WA			Enable write access watch in PREGION[1]
		Set	1	Enable write access watch in this PREGION
		Disabled	0	Write access watch in this PREGION is disabled
		Enabled	1	Write access watch in this PREGION is enabled
L	RW PRGN1RA			Enable read access watch in PREGION[1]
		Set	1	Enable read access watch in this PREGION
		Disabled	0	Read access watch in this PREGION is disabled
		Enabled	1	Read access watch in this PREGION is enabled

45.1.13 REGIONENCLR

Address offset: 0x518 Disable regions watch

Bitı	numbe	er		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				L K J I	H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	RGN0WA			Disable write access watch in region[0]
			Clear	1	Disable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
В	RW	RGNORA			Disable read access watch in region[0]
			Clear	1	Disable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
С	RW	RGN1WA			Disable write access watch in region[1]
			Clear	1	Disable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
D	RW	RGN1RA			Disable read access watch in region[1]
			Clear	1	Disable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled



Bit	numbe	er		31 30 2	29 28 2	7 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					ı	L K	J I	HGFEDCBA
Res	et 0x0	0000000		0 0	0 0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
Ε	RW	RGN2WA						Disable write access watch in region[2]
			Clear	1				Disable write access watch in this region
			Disabled	0				Write access watch in this region is disabled
			Enabled	1				Write access watch in this region is enabled
F	RW	RGN2RA						Disable read access watch in region[2]
			Clear	1				Disable read access watch in this region
			Disabled	0				Read access watch in this region is disabled
			Enabled	1				Read access watch in this region is enabled
G	RW	RGN3WA						Disable write access watch in region[3]
			Clear	1				Disable write access watch in this region
			Disabled	0				Write access watch in this region is disabled
			Enabled	1				Write access watch in this region is enabled
Н	RW	RGN3RA						Disable read access watch in region[3]
			Clear	1				Disable read access watch in this region
			Disabled	0				Read access watch in this region is disabled
			Enabled	1				Read access watch in this region is enabled
1	RW	PRGN0WA						Disable write access watch in PREGION[0]
			Clear	1				Disable write access watch in this PREGION
			Disabled	0				Write access watch in this PREGION is disabled
			Enabled	1				Write access watch in this PREGION is enabled
J	RW	PRGNORA						Disable read access watch in PREGION[0]
			Clear	1				Disable read access watch in this PREGION
			Disabled	0				Read access watch in this PREGION is disabled
			Enabled	1				Read access watch in this PREGION is enabled
K	RW	PRGN1WA						Disable write access watch in PREGION[1]
			Clear	1				Disable write access watch in this PREGION
			Disabled	0				Write access watch in this PREGION is disabled
			Enabled	1				Write access watch in this PREGION is enabled
L	RW	PRGN1RA						Disable read access watch in PREGION[1]
			Clear	1				Disable read access watch in this PREGION
			Disabled	0				Read access watch in this PREGION is disabled
			Enabled	1				Read access watch in this PREGION is enabled

45.1.14 REGION[0].START

Address offset: 0x600 Start address for region 0

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW START		Start address for region

45.1.15 REGION[0].END

Address offset: 0x604 End address of region 0

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
ld RW Field Value Id	Value Description
A RW END	End address of region.



45.1.16 REGION[1].START

Address offset: 0x610 Start address for region 1

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW START	Start address for region

45.1.17 REGION[1].END

Address offset: 0x614 End address of region 1

E	Bit n	umb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
1	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	А А
F	Rese	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
ı	d	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
1	١	RW	END		End a							d ac	ddress of region.																						

45.1.18 REGION[2].START

Address offset: 0x620 Start address for region 2

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 1	16 1	L5 1	4 1	3 1	2 11	. 10	9	8	7	6	5	4	3	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A .	Δ ,	Α Δ	A	Α	Α	Α	Α	Α	Α	Α	A	4 Δ	АА
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	START										Sta	rt a	ddr	ess	for	reg	ion															

45.1.19 REGION[2].END

Address offset: 0x624 End address of region 2

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW END		End address of region.

45.1.20 REGION[3].START

Address offset: 0x630 Start address for region 3

Bit nun	mbe	r		31	30	29	28	27 :	26	25 :	24	23 :	22 2	21 2	20 1	9 1	8 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α,	4 <i>A</i>	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	А А
Reset (0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
ld R	RW	Field	Value Id	Val	lue							Des	crip	otio	n																		
A R	RW	START										Star	t ac	ddre	ess	for i	egio	on															

45.1.21 REGION[3].END

Address offset: 0x634 End address of region 3



Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22 :	21	20	19	18	17	16	15	14	13	12 :	11 :	10	9	8	7	6	5	4	3 2	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	A A	Α Δ	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cri	otic	n																			
Α	RW	END										Enc	l ad	dre	SS (of re	egic	on.																

45.1.22 PREGION[0].START

Address offset: 0x6C0

Reserved for future use

Bit r	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	А А
Res	et Ox(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	pti	on																			
	_											_			,	٠.																		_

A R START Reserved for future use

45.1.23 PREGION[0].END

Address offset: 0x6C4

Reserved for future use

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A R END		Reserved for future use

45.1.24 PREGION[0].SUBS

Address offset: 0x6C8 Subregions of region 0

Bit r	numbe	er		31	30 2	29 2	28 27	7 26	25	24	23	22 2	21 2	20 1	9 1	8 1	7 16	5 15	14	13	12 1	.1 10	9	8	7	6	5	4 3	2	1	0
Id				f	e	d	c b	а	Z	Υ	Х	W	V	U 1	Г 9	S R	R C	P	О	N	М	L K	J	1	н	G	F	E D	С	В	Α
Res	et OxO	0000000		0	0	0	0 0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	lue						De	scrip	otio	n																	
Α	RW	SR0									Inc	clude	or	excl	lude	e su	bre	gion	ni O	n re	gion										
			Exclude	0							Exc	clude	9																		
			Include	1							Inc	clude	2																		
В	RW	SR1									Inc	clude	or	excl	lude	e su	bre	gion	1 ir	n re	gion										
			Exclude	0							Exc	clude	9																		
			Include	1							Inc	clude	2																		
С	RW	SR2									Inc	clude	or	excl	lude	e su	bre	gion	2 ir	n re	gion										
			Exclude	0							Exc	clude	9																		
			Include	1							Inc	clude	:																		
D	RW	SR3									Inc	clude	or	excl	lude	e su	bre	gion	ıi E	n re	gion										
			Exclude	0							Exc	clude	9																		
			Include	1							Inc	clude	•																		
Ε	RW	SR4									Inc	clude	or	excl	lude	e su	bre	gion	4 ir	n re	gion										
			Exclude	0							Exc	clude	e																		
			Include	1							Inc	clude	•																		
F	RW	SR5									Inc	clude	or	excl	lude	e su	bre	gion	ni Z	n re	gion										
			Exclude	0							Exc	clude	9																		
			Include	1							Inc	clude	•																		
G	RW	SR6									Inc	clude	or	excl	lude	e su	bre	gion	6 ir	n re	gion										
			Exclude	0							Exc	clude	9																		
			Include	1							Inc	clude	•																		



Bit r	numbe	er		31 30	29 28	27	26 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et OxO	0000000							0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
Н	RW	SR7							Include or exclude subregion 7 in region
			Exclude	0					Exclude
			Include	1					Include
I	RW	SR8							Include or exclude subregion 8 in region
			Exclude	0					Exclude
			Include	1					Include
J	RW	SR9							Include or exclude subregion 9 in region
			Exclude	0					Exclude
.,			Include	1					Include
K	RW	SR10	Fredrick	0					Include or exclude subregion 10 in region
			Exclude	0					Exclude
L	D\A/	SR11	Include	1					Include Include or exclude subregion 11 in region
_	KVV	2411	Exclude	0					Exclude Exclude
			Include	1					Include
М	RW	SR12	meidde	-					Include or exclude subregion 12 in region
		31112	Exclude	0					Exclude
			Include	1					Include
N	RW	SR13							Include or exclude subregion 13 in region
			Exclude	0					Exclude
			Include	1					Include
0	RW	SR14							Include or exclude subregion 14 in region
			Exclude	0					Exclude
			Include	1					Include
Р	RW	SR15							Include or exclude subregion 15 in region
			Exclude	0					Exclude
			Include	1					Include
Q	RW	SR16							Include or exclude subregion 16 in region
			Exclude	0					Exclude
			Include	1					Include
R	RW	SR17		_					Include or exclude subregion 17 in region
			Exclude	0					Exclude
_	D\A/	SR18	Include	1					Include
S	KVV	2819	Exclude	0					Include or exclude subregion 18 in region Exclude
			Include	1					Include
Т	RW	SR19	meidde	_					Include or exclude subregion 19 in region
•		5.125	Exclude	0					Exclude
			Include	1					Include
U	RW	SR20							Include or exclude subregion 20 in region
			Exclude	0					Exclude
			Include	1					Include
V	RW	SR21							Include or exclude subregion 21 in region
			Exclude	0					Exclude
			Include	1					Include
W	RW	SR22							Include or exclude subregion 22 in region
			Exclude	0					Exclude
			Include	1					Include
Х	RW	SR23							Include or exclude subregion 23 in region
			Exclude	0					Exclude
			Include	1					Include
Υ	RW	SR24		_					Include or exclude subregion 24 in region
			Exclude	0					Exclude
-	Divi	CDOF	Include	1					Include
Z	КW	SR25							Include or exclude subregion 25 in region



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
Exclude	0 Exclude
Include	1 Include
a RW SR26	Include or exclude subregion 26 in region
Exclude	0 Exclude
Include	1 Include
b RW SR27	Include or exclude subregion 27 in region
Exclude	0 Exclude
Include	1 Include
c RW SR28	Include or exclude subregion 28 in region
Exclude	0 Exclude
Include	1 Include
d RW SR29	Include or exclude subregion 29 in region
Exclude	0 Exclude
Include	1 Include
e RW SR30	Include or exclude subregion 30 in region
Exclude	0 Exclude
Include	1 Include
f RW SR31	Include or exclude subregion 31 in region
Exclude	0 Exclude
Include	1 Include

45.1.25 PREGION[1].START

Address offset: 0x6D0

Reserved for future use

Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2 :	1 0
ld		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	A A	А А
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
ld RW Field V	/alue Id	Va	lue							De	scri	ptic	on																			
A R START										Res	serv	/ed	for	fut	ure	use	e															

45.1.26 PREGION[1].END

Address offset: 0x6D4

Reserved for future use

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	A A
Res	et 0x	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Δ	R	END										Res	on	haı	for	fut	ıro	1156																

45.1.27 PREGION[1].SUBS

Address offset: 0x6D8 Subregions of region 1

Bit r	numb	er		31	. 30	29	28	3 27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				f	е	d	С	b	а	Z	Υ	Х	W	٧	U	Т	S	R	Q	Р	О	N	M	L	K	J	1	н	G	F	Е	D C	В	Α
Res	et 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	SR0										Ind	lud	e oı	r ex	cluc	de s	ubr	egi	on	0 in	ı re	gioi	า										
			Exclude	0								Ex	clud	le																				



Bit n	umbe	er		31 30	29 28	27	26 25	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b	a Z	Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	t 0x0	0000000		0 0	0 0	0	0 0	0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value					Description
			Include	1					Include
В	RW	SR1							Include or exclude subregion 1 in region
			Exclude	0					Exclude
			Include	1					Include
С	RW	SR2							Include or exclude subregion 2 in region
			Exclude	0					Exclude
			Include	1					Include
D	RW	SR3							Include or exclude subregion 3 in region
			Exclude	0					Exclude
			Include	1					Include
E	RW	SR4							Include or exclude subregion 4 in region
			Exclude	0					Exclude
			Include	1					Include
F	RW	SR5							Include or exclude subregion 5 in region
			Exclude	0					Exclude
			Include	1					Include
G	RW	SR6							Include or exclude subregion 6 in region
			Exclude	0					Exclude
	D) 4 /	507	Include	1					Include
Н	RW	SR/	5 1 1						Include or exclude subregion 7 in region
			Exclude	0					Exclude
	D\A/	CDO	Include	1					Include
1	KVV	SR8	Exclude	0					Include or exclude subregion 8 in region Exclude
			Include	1					Include
J	D\A/	SR9	include	1					Include or exclude subregion 9 in region
,	11.00	31(9	Exclude	0					Exclude
			Include	1					Include
K	RW	SR10	meidde	-					Include or exclude subregion 10 in region
		SKID	Exclude	0					Exclude
			Include	1					Include
L	RW	SR11							Include or exclude subregion 11 in region
			Exclude	0					Exclude
			Include	1					Include
М	RW	SR12							Include or exclude subregion 12 in region
			Exclude	0					Exclude
			Include	1					Include
N	RW	SR13							Include or exclude subregion 13 in region
			Exclude	0					Exclude
			Include	1					Include
0	RW	SR14							Include or exclude subregion 14 in region
			Exclude	0					Exclude
			Include	1					Include
Р	RW	SR15							Include or exclude subregion 15 in region
			Exclude	0					Exclude
			Include	1					Include
Q	RW	SR16							Include or exclude subregion 16 in region
			Exclude	0					Exclude
			Include	1					Include
R	RW	SR17							Include or exclude subregion 17 in region
			Exclude	0					Exclude
			Include	1					Include
S	RW	SR18							Include or exclude subregion 18 in region
			Exclude	0					Exclude
			Include	1					Include



Bit	numb	er		31 30	29	28	27 20	6 2	5 24	2	3 22 21 2	20 19	18	17	16	15	14	13	3 12	2 1	1 10	9	8	7	6 !	5 4	4 3	3 2	2 1	. 0
Id				f e	d	С	b a	1 2	Z Y	>	(W V I	U T	S	R	Q	Р	0	N	М	1 L	. K	J	ī	Н	G I	FI	E [) (В	8 A
Res	et 0x0	0000000		0 0	0	0	0 0) (0 0	c	000	0 0	0	0	0	0	0	0	0	C	0 (0	0	0	0 (0 (0 () (0	0
Id		Field	Value Id	Value						D	escriptio	n																		
Т	RW	SR19								lr	clude or	exclu	de	sub	re	gion	19	in	reg	ior	1									
			Exclude	0						E	kclude																			
			Include	1						Ir	clude																			
U	RW	SR20								lr	clude or	exclu	de	sub	reg	gion	20) in	reg	ior	n									
			Exclude	0						E:	kclude																			
			Include	1						lr	ıclude																			
V	RW	SR21								lr	clude or	exclu	de	sub	re	gion	21	. in	reg	ior	n									
			Exclude	0						E	kclude																			
			Include	1						Ir	ıclude																			
W	RW	SR22								Ir	clude or	exclu	de	sub	re	gion	22	! in	reg	ior	ı									
			Exclude	0						E	kclude																			
			Include	1						lr	ıclude																			
Χ	RW	SR23								lr	clude or	exclu	de	sub	re	gion	23	in	reg	ior	1									
			Exclude	0						E	kclude																			
			Include	1						lr	ıclude																			
Υ	RW	SR24								lr	clude or	exclu	de	sub	re	gion	24	in	reg	ior	n									
			Exclude	0						E:	kclude																			
			Include	1						Ir	ıclude																			
Z	RW	SR25								lr	iclude or	exclu	de	sub	re	gion	25	in	reg	ior	1									
			Exclude	0						E	kclude																			
			Include	1							ıclude																			
а	RW	SR26									iclude or	exclu	de	sub	re	gion	26	in	reg	ior	1									
			Exclude	0							kclude																			
			Include	1							ıclude																			
b	RW	SR27									iclude or	exclu	de	sub	re	gion	27	' in	reg	ior	1									
			Exclude	0							kclude																			
			Include	1							iclude																			
С	RW	SR28									iclude or	exclu	ide	sub	re	gion	28	in	reg	ior	1									
			Exclude	0							kclude																			
	D\4/	CD20	Include	1							iclude						20													
d	RW	SR29	Fuelude	0							iclude or	exciu	ae	sub	re	gion	29	ın	reg	gior	1									
			Exclude Include	1							kclude iclude																			
e	D\A/	SR30	include	1							iclude iclude or	ovelu	de	cub	ror	ion	30	l in	roc	ior	,									
٦	IL AA	31130	Exclude	0							kclude or	CXCIU	ue	งนม	ıe	51011	50	, 111	ıeg	iUI	'									
			Include	1							iclude																			
f	B/V	SR31	include	1							iclude iclude or	evelu	ndo	cub	rer	ion	21	in	rec	ior	1									
	ΝVV	JUST	Exclude	0							kclude or	exciu	ue	งนม	ı e	51011	31	. 111	reg	,101										
			Include	1							iclude																			
			meiuue	1						II	iciuue																			



46 EGU — Event generator unit

The Event generator unit (EGU) provides support for inter-layer signaling. This means support for atomic triggering of both CPU execution and hardware tasks from both firmware (by CPU) and hardware (by PPI). This feature can, for instance, be used for triggering CPU execution at a lower priority execution from a higher priority execution, or to handle a peripheral's ISR execution at a lower priority for some of its events. However, triggering any priority from any priority is possible.

Listed here are the main EGU features:

- · Enables SW triggering of interrupts
- 6 EGU instances separate interrupt vectors
- Up to 16 separate event flags per interrupt for multiplexing

The EGU implements a set of tasks which can individually be triggered to generate the corresponding event, i.e., the corresponding event for TASKS_TRIGGER[n] is EVENTS_TRIGGERED[n].

Table 113: EGU configuration

EGU instance	Number of event flags
0-5	16

46.1 Registers

Table 114: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40014000	EGU	EGU0	Event Generator Unit 0	
0x40015000	EGU	EGU1	Event Generator Unit 1	
0x40016000	EGU	EGU2	Event Generator Unit 2	
0x40017000	EGU	EGU3	Event Generator Unit 3	
0x40018000	EGU	EGU4	Event Generator Unit 4	
0x40019000	EGU	EGU5	Event Generator Unit 5	

Table 115: Register Overview

Register	Offset	Description
TASKS_TRIGGER[0]	0x000	Trigger 0 for triggering the corresponding TRIGGERED[0] event
TASKS_TRIGGER[1]	0x004	Trigger 1 for triggering the corresponding TRIGGERED[1] event
TASKS_TRIGGER[2]	0x008	Trigger 2 for triggering the corresponding TRIGGERED[2] event
TASKS_TRIGGER[3]	0x00C	Trigger 3 for triggering the corresponding TRIGGERED[3] event
TASKS_TRIGGER[4]	0x010	Trigger 4 for triggering the corresponding TRIGGERED[4] event
TASKS_TRIGGER[5]	0x014	Trigger 5 for triggering the corresponding TRIGGERED[5] event
TASKS_TRIGGER[6]	0x018	Trigger 6 for triggering the corresponding TRIGGERED[6] event
TASKS_TRIGGER[7]	0x01C	Trigger 7 for triggering the corresponding TRIGGERED[7] event
TASKS_TRIGGER[8]	0x020	Trigger 8 for triggering the corresponding TRIGGERED[8] event
TASKS_TRIGGER[9]	0x024	Trigger 9 for triggering the corresponding TRIGGERED[9] event
TASKS_TRIGGER[10]	0x028	Trigger 10 for triggering the corresponding TRIGGERED[10] event
TASKS_TRIGGER[11]	0x02C	Trigger 11 for triggering the corresponding TRIGGERED[11] event
TASKS_TRIGGER[12]	0x030	Trigger 12 for triggering the corresponding TRIGGERED[12] event
TASKS_TRIGGER[13]	0x034	Trigger 13 for triggering the corresponding TRIGGERED[13] event
TASKS_TRIGGER[14]	0x038	Trigger 14 for triggering the corresponding TRIGGERED[14] event
TASKS_TRIGGER[15]	0x03C	Trigger 15 for triggering the corresponding TRIGGERED[15] event
EVENTS_TRIGGERED[0]	0x100	Event number 0 generated by triggering the corresponding TRIGGER[0] task
EVENTS_TRIGGERED[1]	0x104	Event number 1 generated by triggering the corresponding TRIGGER[1] task
EVENTS_TRIGGERED[2]	0x108	Event number 2 generated by triggering the corresponding TRIGGER[2] task
EVENTS_TRIGGERED[3]	0x10C	Event number 3 generated by triggering the corresponding TRIGGER[3] task
EVENTS_TRIGGERED[4]	0x110	Event number 4 generated by triggering the corresponding TRIGGER[4] task



Register	Offset	Description
EVENTS_TRIGGERED	[5] 0x114	Event number 5 generated by triggering the corresponding TRIGGER[5] task
EVENTS_TRIGGERED	0[6] 0x118	Event number 6 generated by triggering the corresponding TRIGGER[6] task
EVENTS_TRIGGERED	[7] 0x11C	Event number 7 generated by triggering the corresponding TRIGGER[7] task
EVENTS_TRIGGERED	0[8] 0x120	Event number 8 generated by triggering the corresponding TRIGGER[8] task
EVENTS_TRIGGERED	0[9] 0x124	Event number 9 generated by triggering the corresponding TRIGGER[9] task
EVENTS_TRIGGERED	0[10] 0x128	Event number 10 generated by triggering the corresponding TRIGGER[10] task
EVENTS_TRIGGERED	[11] 0x12C	Event number 11 generated by triggering the corresponding TRIGGER[11] task
EVENTS_TRIGGERED	0[12] 0x130	Event number 12 generated by triggering the corresponding TRIGGER[12] task
EVENTS_TRIGGERED	0[13] 0x134	Event number 13 generated by triggering the corresponding TRIGGER[13] task
EVENTS_TRIGGERED	0[14] 0x138	Event number 14 generated by triggering the corresponding TRIGGER[14] task
EVENTS_TRIGGERED	[15] 0x13C	Event number 15 generated by triggering the corresponding TRIGGER[15] task
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt

46.1.1 INTEN

Address offset: 0x300 Enable or disable interrupt

	abic c	n disable interru	ρι		
Bit	number			31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					P O N M L K J I H G F E D C B A
Res	et 0x000	00000		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW Fi	ield	Value Id	Value	Description
Α	RW TI	RIGGERED0			Enable or disable interrupt for TRIGGERED[0] event
					See EVENTS_TRIGGERED[0]
			Disabled	0	Disable
			Enabled	1	Enable
В	RW TI	RIGGERED1			Enable or disable interrupt for TRIGGERED[1] event
					See EVENTS_TRIGGERED[1]
			Disabled	0	Disable
			Enabled	1	Enable
С	RW TI	RIGGERED2			Enable or disable interrupt for TRIGGERED[2] event
					See EVENTS_TRIGGERED[2]
			Disabled	0	Disable
			Enabled	1	Enable
D	RW TI	RIGGERED3			Enable or disable interrupt for TRIGGERED[3] event
					See EVENTS_TRIGGERED[3]
			Disabled	0	Disable
			Enabled	1	Enable
E	RW TI	RIGGERED4			Enable or disable interrupt for TRIGGERED[4] event
					See EVENTS_TRIGGERED[4]
			Disabled	0	Disable
			Enabled	1	Enable
F	RW TI	RIGGERED5			Enable or disable interrupt for TRIGGERED[5] event
					See EVENTS_TRIGGERED[5]
			Disabled	0	Disable
			Enabled	1	Enable
G	RW TI	RIGGERED6			Enable or disable interrupt for TRIGGERED[6] event
					See EVENTS_TRIGGERED[6]
			Disabled	0	Disable
			Enabled	1	Enable
Н	RW TI	RIGGERED7			Enable or disable interrupt for TRIGGERED[7] event
					See EVENTS_TRIGGERED[7]
			Disabled	0	Disable



Bit r	numbe	er		31 30	29 2	28 2	7 26	25 24	4 23	3 22 21	1 2	0 19	1	8 17	7 1	5 15	5 1	4 :	13 1	2 1	1 1) 9	8 (7	6	5 5	4	3	2	1	0
Id																Р	(o	N N	1	L K	J	- 1	Н	C	i F	Ε	D	С	В	Α
Res	et 0x0	0000000		0 0	0	0 0	0	0 0	0	0 0	0	0	c	0	0	0	(0	0 0) (0 0	0	0	0	c	0	0	0	0	0	0
Id	RW	Field	Value Id	Value					D	escript	tion	1																			
			Enabled	1					Er	nable																					
I	RW	TRIGGERED8							Er	nable o	or d	isab	le	inte	rru	pt f	or	TR	IGGI	ERE	D[8] ev	ven	t							
									Se	ee <i>EVEI</i>	NTS	S_TR	RIG	GER	ED	[8]															
			Disabled	0					Di	isable																					
			Enabled	1					Er	nable																					
J	RW	TRIGGERED9							Er	nable o	or d	isab	le	inte	rru	pt f	or	TR	IGGI	ERE	D[9] ev	ven	t							
									Se	ee <i>EVEI</i>	NTS	S_TR	RIG	GER	ED	[9]															
			Disabled	0					Di	isable																					
			Enabled	1					Er	nable																					
K	RW	TRIGGERED10							Er	nable o	or d	isab	le	inte	rru	pt f	or	TR	IGGI	ERE	D[1	0] 6	eve	nt							
									Se	ee <i>EVEI</i>	NTS	S_TR	RIG	GER	ED	[10]														
			Disabled	0					Di	isable																					
			Enabled	1					Er	nable																					
L	RW	TRIGGERED11							Er	nable o	or d	isab	le	inte	rru	pt f	or	TR	IGGI	ERE	D[1	1] 6	eve	nt							
									Se	ee <i>EVEI</i>	NTS	S_TR	RIG	GER	ED	[11]														
			Disabled	0					Di	isable																					
			Enabled	1					Er	nable																					
М	RW	TRIGGERED12							Er	nable o	or d	isab	le	inte	rru	pt f	or	TR	IGGI	ERE	D[1	2] 6	eve	nt							
									Se	ee <i>EVEI</i>	NTS	S_TR	RIG	GER	ED	[12]														
			Disabled	0					Di	isable																					
			Enabled	1					Er	nable																					
N	RW	TRIGGERED13							Er	nable o	or d	isab	le	inte	rru	pt f	or	TR	IGGI	ERE	D[1	.3] €	eve	nt							
									Se	ee <i>EVEI</i>	NTS	S_TR	RIG	GER	ED	[13]														
			Disabled	0					Di	isable																					
			Enabled	1					Er	nable																					
0	RW	TRIGGERED14							Er	nable o	or d	isab	le	inte	rru	pt f	or	TR	IGGI	ERE	D[1	4] 6	eve	nt							
									Se	ee <i>EVEI</i>	NTS	S_TR	RIG	GER	ED	[14]														
			Disabled	0					Di	isable																					
			Enabled	1					Er	nable																					
Р	RW	TRIGGERED15							Er	nable o	or d	isab	le	inte	rru	pt f	or	TR	IGGI	ERE	D[1	5] €	eve	nt							
									Se	ee <i>EVEI</i>	NTS	S_TR	RIG	GER	ED	[15]														
			Disabled	0						isable																					
			Enabled	1						nable																					

46.1.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	iumbe	r		31	. 30 :	29	28 2	27 2	26 2	25 2	24 2	23 22	2 21	20	19	L8 1	L7 1	16 1	15 :	14 1	.3 1	2 11	10	9	8	7	6	5	4 3	2	1	0
Id																			Р	0 1	N N	1 L	K	J	1	Н	G	F	E C	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	lue						0	Desc	ripti	on																		
Α	RW	TRIGGERED0									٧	Vrite	e '1'	to E	nab	le ir	nter	rup	ot fo	or T	RIG	SER	D[0)] ev	/ent							
											S	ee E	VEN	ITS_	TRI	GGE	REL	D[0 _]	1													
			Set	1							Е	nab	le																			
			Disabled	0							F	Read	: Dis	able	ed																	
			Enabled	1							F	Read	: Ena	able	d																	
В	RW	TRIGGERED1									٧	Vrite	e '1'	to E	nab	le ir	nter	rup	ot fo	or T	RIG	SERI	ED[1	.] ev	/ent							
											S	ee E	VEN	ITS_	TRI	GGE	REL	D[1]	1													
			Set	1							E	nab	le																			



Bit r	number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 C
Id				P O N M L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW TRIGGERED2			Write '1' to Enable interrupt for TRIGGERED[2] event
				See EVENTS_TRIGGERED[2]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW TRIGGERED3			Write '1' to Enable interrupt for TRIGGERED[3] event
				See EVENTS_TRIGGERED[3]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E	RW TRIGGERED4			Write '1' to Enable interrupt for TRIGGERED[4] event
		Cat	1	See EVENTS_TRIGGERED[4]
		Set Disabled	1 0	Enable Read: Disabled
		Enabled	1	Read: Enabled
F	RW TRIGGERED5	Ellableu	1	Write '1' to Enable interrupt for TRIGGERED[5] event
	NW TRIOGENEDS			write 1 to thable interrupt for middenta[5] event
				See EVENTS_TRIGGERED[5]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW TRIGGERED6			Write '1' to Enable interrupt for TRIGGERED[6] event
				See EVENTS_TRIGGERED[6]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW TRIGGERED7			Write '1' to Enable interrupt for TRIGGERED[7] event
				See EVENTS_TRIGGERED[7]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
ı	RW TRIGGERED8			Write '1' to Enable interrupt for TRIGGERED[8] event
				See EVENTS_TRIGGERED[8]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
J	RW TRIGGERED9			Write '1' to Enable interrupt for TRIGGERED[9] event
		C-+	4	See EVENTS_TRIGGERED[9] Enable
		Set	1	
		Disabled Enabled	1	Read: Disabled Read: Enabled
V	RW TRIGGERED10	Enabled	1	
K	WAN LUIGGEVENTO			Write '1' to Enable interrupt for TRIGGERED[10] event
				See EVENTS_TRIGGERED[10]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
L	RW TRIGGERED11			Write '1' to Enable interrupt for TRIGGERED[11] event
				See EVENTS_TRIGGERED[11]
		Set	1	Enable
		Disabled	0	Read: Disabled



Bit	numbe	er		31	30	29 2	28 2	7 26	25	24 23	3 22	2 21 2	20	19	18	17	16	15	14	13	12	11 1	.0 9	8	7	6	5 4	4 3	2	1	0
Id																		Р	О	N	М	L	K J	-1	Н	G	F	E D	С	В	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0 0	0 0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	lue					D	escr	riptio	n																		
			Enabled	1						Re	ead	: Enal	ble	d																	
М	RW	TRIGGERED12								W	Vrite	'1' to	οЕ	nab	le	inte	rru	pt f	or '	TRIC	GGE	RED	[12]	eve	nt						
										Se	ee <i>E</i>	VEN1	rs_	TRI	GG	ERE	D[1	12]													
			Set	1						Er	nabl	le																			
			Disabled	0						Re	ead	: Disa	ble	ed																	
			Enabled	1						Re	ead	: Enal	ble	d																	
N	RW	TRIGGERED13								W	Vrite	'1' to	o E	nab	le	inte	rru	pt f	or '	TRIC	GGE	RED	[13]	eve	nt						
										Se	ee <i>E</i>	VENT	rs	TRI	GG	ERE	D[1	13]													
			Set	1							nabl		Ī																		
			Disabled	0						Re	ead	: Disa	ble	ed																	
			Enabled	1						Re	ead:	: Enal	ble	d																	
0	RW	TRIGGERED14								W	Vrite	'1' to	o E	nab	le	inte	rru	pt f	or '	TRIC	GGE	REC	[14]	eve	nt						
										Se	ee E	VENT	rs_	TRI	GG	ERE	D[1	14]													
			Set	1						Er	nabl	le																			
			Disabled	0						Re	ead	: Disa	ble	ed																	
			Enabled	1						Re	ead	: Enal	ble	d																	
Р	RW	TRIGGERED15								W	Vrite	'1' to	οЕ	nab	le	inte	rru	pt f	or '	TRIC	GGE	RED	[15]	eve	nt						
										Se	ee <i>E</i>	VEN7	rs_	TRI	GG	ERE	D[1	15]													
			Set	1						Er	nabl	le																			
			Disabled	0						Re	ead	: Disa	ble	ed																	
			Enabled	1						Re	ead	: Enal	ble	d																	

46.1.3 INTENCLR

Address offset: 0x308

Disable interrupt

Dioabio interrupt			
Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			PONMLKJIHGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW TRIGGEREDO			Write '1' to Disable interrupt for TRIGGERED[0] event
			See EVENTS_TRIGGERED[0]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW TRIGGERED1			Write '1' to Disable interrupt for TRIGGERED[1] event
			See EVENTS_TRIGGERED[1]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW TRIGGERED2			Write '1' to Disable interrupt for TRIGGERED[2] event
			See EVENTS_TRIGGERED[2]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW TRIGGERED3			Write '1' to Disable interrupt for TRIGGERED[3] event
			See EVENTS TRIGGERED[3]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW TRIGGERED4			Write '1' to Disable interrupt for TRIGGERED[4] event



Bit r	numbe	er		31 30	29	28 2	7 26	5 25 2	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									PONMLKJIHGFEDCBA
Rese		0000000				0 (0 0	0 (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			Clear	1					See EVENTS_TRIGGERED[4] Disable
			Clear Disabled	1					Disable Read: Disabled
			Enabled	1					Read: Enabled
F	RW	TRIGGERED5	Lilableu	1					Write '1' to Disable interrupt for TRIGGERED[5] event
•		MIGGENESS							
				_					See EVENTS_TRIGGERED[5]
			Clear Disabled	1					Disable Read: Disabled
			Enabled	1					Read: Enabled
G	RW	TRIGGERED6	Lilabica	_					Write '1' to Disable interrupt for TRIGGERED[6] event
•		GGENESG							
				_					See EVENTS_TRIGGERED[6]
			Clear	1					Disable Disable
			Disabled Enabled	0					Read: Disabled Read: Enabled
Н	D\A/	TRIGGERED7	Enableu	1					Write '1' to Disable interrupt for TRIGGERED[7] event
П	IV V V	INIGGENED/							Write 1 to disable interrupt for integered[7] event
									See EVENTS_TRIGGERED[7]
			Clear	1					Disable
			Disabled	0					Read: Disabled
	D\A/	TDICCEDEDO	Enabled	1					Read: Enabled
1	RW	TRIGGERED8							Write '1' to Disable interrupt for TRIGGERED[8] event
									See EVENTS_TRIGGERED[8]
			Clear	1					Disable
			Disabled	0					Read: Disabled
	DVA	TNICCENERO	Enabled	1					Read: Enabled
J	RW	TRIGGERED9							Write '1' to Disable interrupt for TRIGGERED[9] event
									See EVENTS_TRIGGERED[9]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
K	RW	TRIGGERED10							Write '1' to Disable interrupt for TRIGGERED[10] event
									See EVENTS_TRIGGERED[10]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
L	RW	TRIGGERED11							Write '1' to Disable interrupt for TRIGGERED[11] event
									See EVENTS_TRIGGERED[11]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
М	RW	TRIGGERED12							Write '1' to Disable interrupt for TRIGGERED[12] event
									See EVENTS_TRIGGERED[12]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
N	RW	TRIGGERED13							Write '1' to Disable interrupt for TRIGGERED[13] event
									See EVENTS_TRIGGERED[13]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
0	RW	TRIGGERED14							Write '1' to Disable interrupt for TRIGGERED[14] event
									See EVENTS_TRIGGERED[14]



Bitı	numb	er		31	1 30	29	28	27	26	25 :	24 2	23 22	2 21	20	19	18	17 :	16 :	15 1	L4 1	3 12	11	10	9	8	7	6	5 -	4 3	2	1	0
Id																			Р	0 1	I M	L	K	J	1	Н	G	F	E C	С	В	Α
Res	Reset 0x00000000			0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	alue							Desc	ripti	on																		
			Clear	1							[Disab	ole																			
			Disabled	0							F	Read	: Dis	sabl	ed																	
			Enabled	1							F	Read	: En	able	ed																	
Р	RW	TRIGGERED15									١	Vrite	e '1'	to [Disa	ble	inte	rru	pt f	or T	RIGO	GERI	ED[:	15]	eve	nt						
											9	See E	VEN	NTS_	TRI	GG	ERE	D[1	5]													
			Clear	1							[Disab	ole																			
			Disabled	0							F	Read	: Dis	sabl	ed																	
			Enabled	1							F	Read	: En	able	ed																	

46.2 Electrical specification

46.2.1 EGU Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
$t_{\text{EGU,EVT}}$	Latency between setting an EGU event flag and the system		1		cycles
	setting an interrupt				



47 PWM — Pulse width modulation

The PWM module enables the generation of pulse width modulated signals on GPIO. The module implements an up or up-and-down counter with four PWM channels that drive assigned GPIOs.

Three PWM modules can provide up to 12 PWM channels with individual frequency control in groups of up to four channels. Furthermore, a built-in decoder and EasyDMA capabilities make it possible to manipulate the PWM duty cycles without CPU intervention. Arbitrary duty-cycle sequences are read from Data RAM and can be chained to implement ping-pong buffering or repeated into complex loops.

Listed here are the main features of one PWM module:

- Fixed PWM base frequency with programmable clock divider
- Up to four PWM channels with individual polarity and duty-cycle values
- Edge or center-aligned pulses across PWM channels
- Multiple duty-cycle arrays (sequences) defined in Data RAM
- · Autonomous and glitch-free update of duty cycle values directly from memory through EasyDMA
- · Change of polarity, duty-cycle, and base frequency possibly on every PWM period
- Data RAM sequences can be repeated or connected into loops

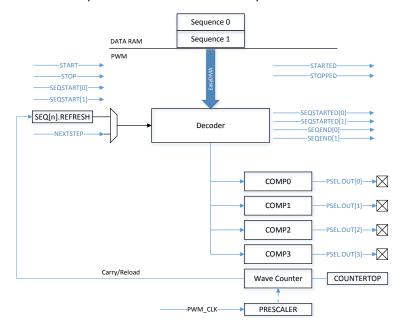


Figure 141: PWM Module

47.1 Wave counter

The wave counter is responsible for generating the pulses at a duty-cycle that depends on the compare values, and at a frequency that depends on COUNTERTOP.

There is one common 15-bit counter with four compare channels. Thus, all four channels will share the same period (PWM frequency), but can have individual duty-cycle and polarity. The polarity is set by the value read from RAM (see *Figure 144: Decoder memory access modes* on page 499), while the MODE register controls if the counter counts up, or up and down. The timer top value is controlled by the COUNTERTOP register. This register value in conjunction with the selected PRESCALER of the PWM_CLK will result in a given PWM period. A COUNTERTOP value smaller than the compare setting will result in a state where no PWM edges are generated. Respectively, OUT[n] is held high, given that the polarity is set to FallingEdge. All the compare registers are internal and can only be configured through the decoder presented later.

COUNTERTOP can be safely written at any time. It will get sampled following a START task. If DECODER.LOAD is anything else than WaveForm, it will also get sampled following a STARTSEQ[n] task,



and when loading a new value from RAM during a sequence playback. If DECODER.LOAD=WaveForm, the register value is ignored, and taken from RAM instead (see *Decoder with EasyDMA* on page 499 below).

Figure 142: PWM up counter example - FallingEdge polarity on page 497 shows the counter operating in up (MODE=PWM_MODE_Up) mode with three PWM channels with the same frequency but different duty cycle. The counter is automatically reset to zero when COUNTERTOP is reached and OUT[n] will invert. OUT[n] is held low if the compare value is 0 and held high respectively if set to COUNTERTOP given that the polarity is set to FallingEdge. Running in up counter mode will result in pulse widths that are edge-aligned. See the code example below:

```
uint16 t pwm seq[4] = {PWM CH0 DUTY, PWM CH1 DUTY, PWM CH2 DUTY,
PWM CH3 DUTY);
NRF PWM0->PSEL.OUT[0] = (first pin << PWM PSEL OUT PIN Pos)
                        (PWM PSEL OUT CONNECT Connected <<
                                                  PWM PSEL OUT CONNECT Pos);
NRF PWM0->PSEL.OUT[1] = (second pin << PWM PSEL OUT PIN Pos) |
                        (PWM PSEL OUT CONNECT Connected <<
                                                 PWM_PSEL_OUT_CONNECT_Pos);
                      = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
NRF PWM0->ENABLE
NRF PWM0->MODE
                      = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
NRF PWM0->PRESCALER = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                  PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM COUNTERTOP COUNTERTOP Pos); //1 msec
NRF PWM0->LOOP
                    = (PWM LOOP CNT Disabled << PWM LOOP CNT Pos);
NRF PWM0->DECODER
                   = (PWM DECODER LOAD Individual << PWM DECODER LOAD Pos)
                      (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF PWM0->SEQ[0].PTR = ((uint32_t)(pwm_seq) << PWM_SEQ_PTR_PTR_Pos);
NRF PWM0->SEQ[0].CNT = ((sizeof(pwm seq) / sizeof(uint16_t)) < < 
                                                 PWM SEQ CNT CNT Pos);
NRF_PWM0 \rightarrow SEQ[0].REFRESH = 0;
NRF PWM0 -> SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

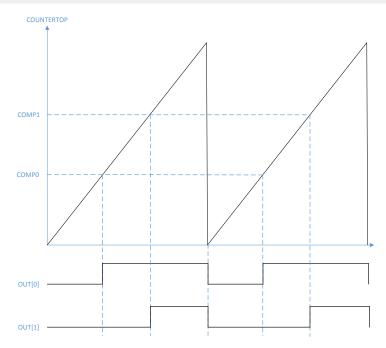


Figure 142: PWM up counter example - FallingEdge polarity

In up counting mode, the following formula can be used to compute PWM period and step size:

```
PWM period: T<sub>PWM</sub> (U<sub>p</sub>) = T<sub>PWM</sub> C<sub>LK</sub> * COUNTERTOP
```

Step width/Resolution: $T_{\text{steps}} = T_{\text{PWM_CLK}}$



Figure 143: PWM up-and-down counter example on page 498 shows the counter operating in up and down mode with (MODE=PWM_MODE_UpAndDown) two PWM channels with the same frequency but different duty cycle and output polarity. The counter starts decrementing to zero when COUNTERTOP is reached and will invert the OUT[n] when compare value is hit for the second time. This results in a set of pulses that are center- aligned.

```
uint16 t pwm seq[4] = {PWM CHO DUTY, PWM CH1 DUTY, PWM CH2 DUTY,
 PWM CH3 DUTY);
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |</pre>
                                                                      (PWM PSEL OUT CONNECT Connected <<
                                                                                                                                              PWM PSEL OUT CONNECT Pos);
NRF PWM0->PSEL.OUT[1] = (second pin << PWM PSEL OUT PIN Pos) |
                                                                      (PWM PSEL OUT CONNECT Connected <<
                                                                                                                                             PWM PSEL OUT CONNECT Pos);
NRF PWM0->ENABLE
                                                               = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
                                                               = (PWM MODE UPDOWN UpAndDown << PWM MODE UPDOWN Pos);
NRF PWM0->MODE
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                                                                                                                             PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
                                                               = (PWM LOOP CNT Disabled << PWM LOOP CNT Pos);
NRF
          PWM0->LOOP
NRF PWM0->DECODER
                                                          = (PWM DECODER LOAD Individual << PWM DECODER LOAD Pos)
                                                               (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF_PWM0->SEQ[0].PTR = ((uint32_t)(pwm_seq) << PWM_SEQ PTR PTR Pos);
NRF_PWM0 - SEQ[0].CNT = ((sizeof(pwm_seq) / sizeof(uint16_t)) < < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < colspan="2">(sizeof(uint16_t)) < col
                                                                                                                                             PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0 \rightarrow SEQ[0].REFRESH = 0;
NRF PWM0 -> SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

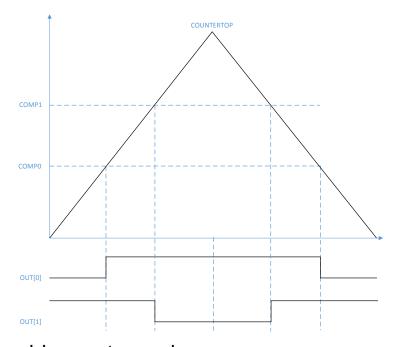


Figure 143: PWM up-and-down counter example

In up-and-down counting modes, the following formula can be used to compute PWM period and step size:

```
T_{PWM}(Up And Down) = T_{PWM} CLK * 2 * COUNTERTOP
```

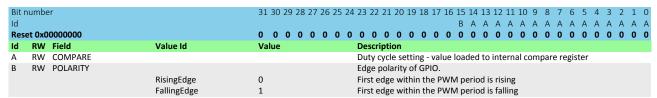
Step width/Resolution: $T_{\text{Steps}} = T_{\text{PWM CLK}} * 2$



47.2 Decoder with EasyDMA

The decoder uses EasyDMA to take PWM parameters stored in Data RAM by ways of EasyDMA and updates the internal compare registers of the wave counter based on the mode of operation.

The mentioned PWM parameters are organized into a sequence containing at least one half word (16 bit). Its most significant bit[15] denotes the polarity of the OUT[n] while bit[14:0] is the 15-bit compare value. See below for further details of these RAM defined registers.



The DECODER register controls how the RAM content is interpreted and loaded to the internal compare registers. The LOAD field can be used to control if the RAM values are loaded to all compare channels - or alternatively to update a group or all channels with individual values. *Figure 144: Decoder memory access modes* on page 499 illustrates how the parameters stored in RAM are organized and routed to the various compare channels in the different modes.

A special mode of operation is available when DECODER.LOAD is set to WaveForm. In this mode, up to three PWM channels can be enabled - OUT[0] to OUT[2]. In RAM, four values are loaded at a time: the first, second and third location are used to load the values, and the fourth RAM location is used to load the COUNTERTOP register. This way one can have up to three PWM channels with a frequency base that changes on a per PWM period basis. This mode of operation is useful for arbitrary wave form generation in applications such as LED lighting.

The register SEQ[n].REFRESH=N (one per sequence n=0 or 1) will instruct a new RAM stored pulse width value on every (N+1)th PWM period. Setting the register to zero will result in a new duty cycle update every PWM period as long as the minimum PWM period is observed.

Note that registers SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored when DECODER.MODE=NextStep . The next value is loaded upon receiving every NEXTSTEP task.

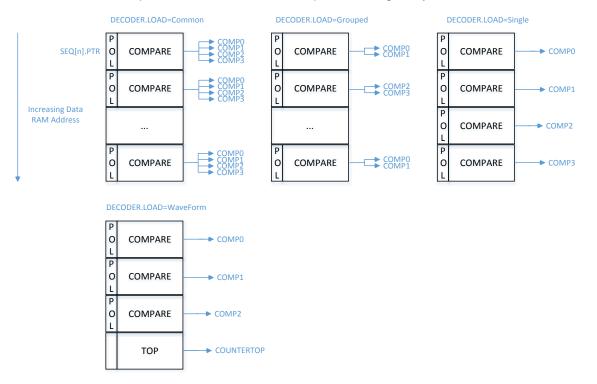


Figure 144: Decoder memory access modes



SEQ[n].PTR is the pointer used to fetch COMPARE values from RAM. If the SEQ[n].PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

After the SEQ[n].PTR is set to the desired RAM location, the SEQ[n].CNT register must be set to the number of 16-bit half words in the sequence. It is important to observe that the Grouped and Single modes require one half word per group or one half word per channel respectively, and thus increases RAM size occupation. If PWM generation was not running yet at that point, sending the SEQSTART[n] task will load the first value from RAM, then start the PWM generation. A SEQSTARTED[n] event is generated as soon as the EasyDMA has read the first PWM parameter from RAM and the wave counter has started executing it. When LOOP.CNT=0, sequence n=0 or 1 is played back once. After the last value in the sequence has been loaded and started executing, a SEQEND[n] event is generated. The PWM generation will then continue with the last loaded value. See *Figure 145: Simple sequence example* on page 501 for an example of such simple playback.

To completely stop the PWM generation and force the associated pins to a defined state, a STOP task can be fired at any time. A STOPPED event is generated when the PWM generation has stopped at the end of currently running PWM period, and the pins go into their idle state as defined in GPIO->OUT. PWM generation can then only be restarted through a SEQSTART[n] task. SEQSTART[n] will resume PWM generation after having loaded the first value from the RAM buffer defined in the SEQ[n].PTR register.

The table below provides indication of when specific registers get sampled by the hardware. Care should be taken when updating these registers to avoid values to be applied earlier than expected.

Table 116: When to safely update PWM registers

Register	Taken into account by hardware	Recommended (safe) update
SEQ[n].PTR	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[n].CNT	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[0].ENDDELAY	When sending the SEQSTART[0] task	Before starting sequence [0] through a SEQSTART[0] task
	Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the	When no more value from sequence [0] gets loaded from RAM (indicated by the SEQEND[0] event)
	PWMPERIODEND event)	At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired)
SEQ[1].ENDDELAY	When sending the SEQSTART[1] task	Before starting sequence [1] through a SEQSTART[1] task
	Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the	When no more value from sequence [1] gets loaded from RAM (indicated by the SEQEND[1] event)
	PWMPERIODEND event)	At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired)
SEQ[0].REFRESH	When sending the SEQSTART[0] task	Before starting sequence [0] through a SEQSTART[0] task
	Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired)
SEQ[1].REFRESH	When sending the SEQSTART[1] task	Before starting sequence [1] through a SEQSTART[1] task
	Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired)
COUNTERTOP	In DECODER.LOAD=WaveForm: this register is ignored.	Before starting PWM generation through a SEQSTART[n] task
	In all other LOAD modes: at the end of current PWM period (indicated by the PWMPERIODEND event)	After a STOP task has been issued, and the STOPPED event has been received.
MODE	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
DECODER	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
PRESCALER	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
LOOP	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
PSEL.OUT[n]	Immediately	Before enabling the PWM instance through the ENABLE register

Important: SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored at the end of a complex sequence, indicated by a LOOPSDONE event. The reason for this is that the last value loaded from RAM is maintained until further action from software (restarting a new sequence, or stopping PWM generation).



Figure 145: Simple sequence example on page 501 depicts the source code used for configuration and timing details in a sequence where only sequence 0 is used and only run once with a new PWM duty cycle for each period.

```
NRF PWM0->PSEL.OUT[0] = (first pin << PWM_PSEL_OUT_PIN_Pos)
                           (PWM PSEL OUT CONNECT Connected <<
                                                      PWM PSEL OUT CONNECT Pos);
NRF PWM0->ENABLE
                        = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
                        = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
NRF PWM0->MODE
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                                      PWM PRESCALER PRESCALER Pos);
NRF_PWM0->COUNTERTOP = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec NRF_PWM0->LOOP = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF PWM0->DECODER
                      = (PWM DECODER LOAD Common << PWM DECODER LOAD Pos)
                        (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF PWM0->SEQ[0].PTR = ((uint32 t)(seq0 ram) << PWM SEQ PTR PTR Pos);
NRF PWM0->SEQ[0].CNT = ((sizeof(seq0 ram) / sizeof(\overline{uint16 t})) < \overline{<})
                                                      PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[0].REFRESH = 0;
NRF PWM0->SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

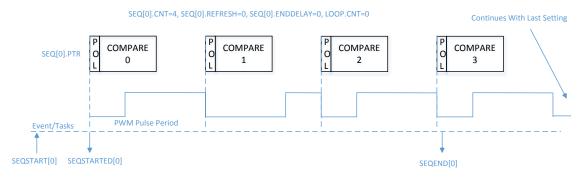


Figure 145: Simple sequence example

A more complex example is shown in *Figure 146: Example using two sequences* on page 502, where LOOP.CNT>0. In this case, an automated playback takes place, consisting of SEQ[0], delay 0, SEQ[1], delay 1, then again SEQ[0], etc. The user can choose to start a complex playback with SEQ[0] or SEQ[1] through sending the SEQSTART[0] or SEQSTART[1] task.

The complex playback always ends with delay 1.

The two sequences 0 and 1 are defined with address of values tables in Data RAM (pointed by SEQ[n].PTR) and respective buffer size (SEQ[n].CNT). The rate at which a new value is loaded is defined individually for each sequence by SEQ[n].REFRESH . The chaining of sequence 1 following sequence 0 is implicit, the LOOP.CNT register allows the chaining of sequence 1 to sequence 0 for a determined number of times. In other words, it allows to repeat a complex sequence a number of times in a fully automated way.

In the example below, sequence 0 is defined with SEQ[0].REFRESH set to one - that means that a new PWM duty cycle is pushed every second PWM period. This complex sequence is started with the SEQSTART[0] task, so SEQ[0] is played first. Since SEQ[0].ENDDELAY=1 there will be one PWM period delay between last period on sequence 0 and the first period on sequence 1. Since SEQ[1].ENDDELAY=0 there is no delay 1, so SEQ[0] would be started immediately after the end of SEQ[1]. However, as LOOP.CNT is one, the playback stops after having played only once SEQ[1], and both SEQEND[1] and LOOPSDONE are generated (their order is not guaranteed in this case).



```
NRF PWM0->PSEL.OUT[0] = (first pin << PWM PSEL OUT PIN Pos)
                       (PWM PSEL OUT CONNECT Connected <<
                                              PWM PSEL OUT CONNECT Pos);
NRF PWM0->ENABLE
                    = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_
   PWM0->MODE
                    = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                              PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM COUNTERTOP COUNTERTOP Pos); //1 msec
                   = (1 \ll PWM LOOP CNT Pos);
NRF PWM0->LOOP
NRF PWM0->DECODER
                  = (PWM DECODER LOAD Common << PWM DECODER LOAD Pos) |
                    (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF PWM0->SEQ[0].PTR = ((uint32 t)(seq0 ram) << PWM SEQ PTR PTR Pos);
PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[0].REFRESH = 1;
NRF PWM0->SEQ[0].ENDDELAY = 1;
NRF PWM0->SEQ[1].PTR = ((uint32 t)(seq1 ram) << PWM SEQ PTR PTR Pos);
NRF PWM0->SEQ[1].CNT = ((sizeof(seq1 ram) / sizeof(uint16 t)) <<
                                              PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[1].REFRESH = 0;
NRF PWM0->SEQ[1].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

SEQ[0].CNT=2, SEQ[1].CNT=3, SEQ[0].REFRESH=1, SEQ[1].REFRESH=0, SEQ[0].ENDDELAY=1, SEQ[1].ENDDELAY=0, LOOP.CNT=1

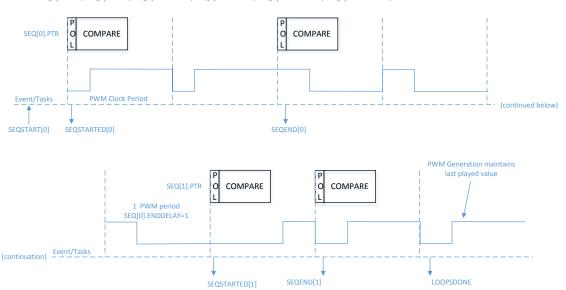


Figure 146: Example using two sequences

The decoder can also be configured to asynchronously load a new PWM duty cycle. If the DECODER.MODE register is set to NextStep - then the NEXTSTEP task will cause an update of the internal compare registers on the next PWM period.

The figures below provide an overview of each part of an arbitrary sequence, in various modes (LOOP.CNT=0 and LOOP.CNT>0). In particular are represented:

- Initial and final duty cycle on the PWM output(s)
- Chaining of SEQ[0] and SEQ[1] if LOOP.CNT>0
- · Influence of registers on the sequence
- · Events fired during a sequence
- DMA activity (loading of next value and applying it to the output(s))

Note that the single-shot example applies also to SEQ[1], only SEQ[0] is represented for simplicity.



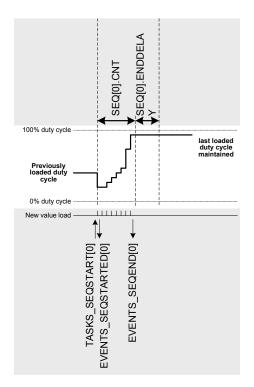


Figure 147: Single shot (LOOP.CNT=0)

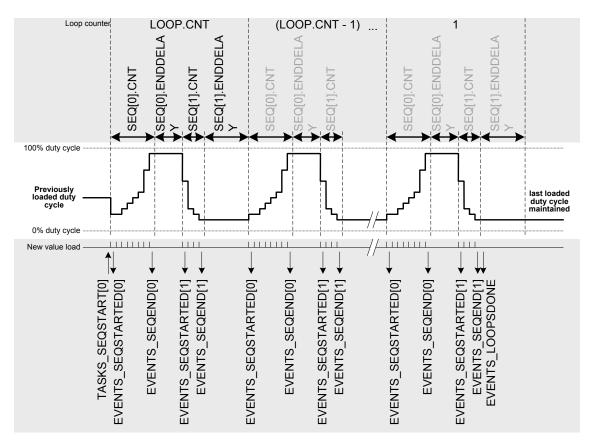


Figure 148: Complex sequence (LOOP.CNT>0) starting with SEQ[0]



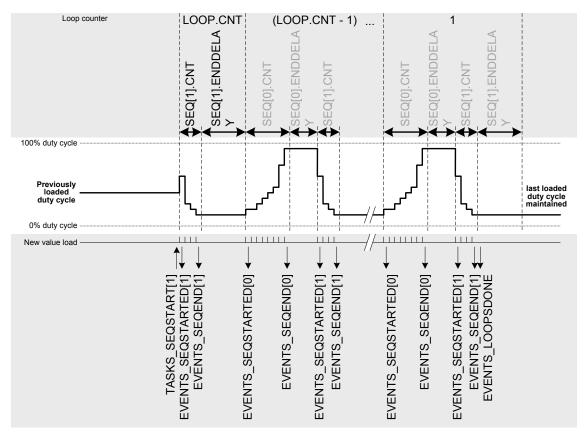


Figure 149: Complex sequence (LOOP.CNT>0) starting with SEQ[1]

Note that if a sequence is in use in a simple or complex sequence, it must have a length of SEQ[n].CNT > 0.

47.3 Limitations

The previous compare value will be repeated if the PWM period is selected to be shorter than the time it takes for the EasyDMA to fetch from RAM and update the internal compare registers.

This is to ensure a glitch-free operation even if very short PWM periods are chosen.

47.4 Pin configuration

The OUT[n] (n=0..3) signals associated to each channel of the PWM module are mapped to physical pins according to the configuration specified in the respective PSEL.OUT[n] registers. If a PSEL.OUT[n].CONNECT is set to Disconnected, the associated PWM module signal will not be connected to any physical pins.

The PSEL.OUT[n] registers and their configurations are only used as long as the PWM module is enabled and PWM generation is active (wave counter started), and retained only as long as the device is in System ON mode, see *POWER* chapter for more information about power modes.

To ensure correct behaviour in the PWM module, the pins used by the PWM module must be configured in the GPIO peripheral as described in *Table 117: Recommended GPIO configuration before starting PWM generation* on page 505 before enabling the PWM module. The pins' idle state is defined by the OUT registers in the GPIO module. This is to ensure that the pins used by the PWM module are driven correctly, if PWM generation is stopped through a STOP task, the PWM module itself is temporarily disabled, or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected IOs as long as the PWM module is supposed to be connected to an external PWM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behaviour.



Table 117: Recommended GPIO configuration before starting PWM generation

PWM signal	PWM pin	Direction	Output value	Comment
OUT[n]	As specified in PSEL.OUT[n]	Output	0	Idle state defined in GPIO->OUT
	(n=0, 3)			

47.5 Registers

Table 118: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x4001C000	PWM	PWM0	Pulse Width Modulation Unit 0		
0x40021000	PWM	PWM1	Pulse Width Modulation Unit 1		
0x40022000	PWM	PWM2	Pulse Width Modulation Unit 2		

Table 119: Register Overview

Register	Offset	Description
TASKS_STOP	0x004	Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence
		playback
TASKS_SEQSTART[0]	0x008	Loads the first PWM value on all enabled channels from sequence 0, and starts playing that
		sequence at the rate defined in SEQ[0]REFRESH and/or DECODER.MODE. Causes PWM generation to
		start it was not running.
TASKS_SEQSTART[1]	0x00C	Loads the first PWM value on all enabled channels from sequence 1, and starts playing that
		sequence at the rate defined in SEQ[1]REFRESH and/or DECODER.MODE. Causes PWM generation to
		start it was not running.
TASKS_NEXTSTEP	0x010	Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep.
		Does not cause PWM generation to start it was not running.
EVENTS_STOPPED	0x104	Response to STOP task, emitted when PWM pulses are no longer generated
EVENTS_SEQSTARTED[0	0] 0x108	First PWM period started on sequence 0
EVENTS_SEQSTARTED[1	1] 0x10C	First PWM period started on sequence 1
EVENTS_SEQEND[0]	0x110	Emitted at end of every sequence 0, when last value from RAM has been applied to wave counter
EVENTS_SEQEND[1]	0x114	Emitted at end of every sequence 1, when last value from RAM has been applied to wave counter
EVENTS_PWMPERIODE	N 0x118	Emitted at the end of each PWM period
EVENTS_LOOPSDONE	0x11C	Concatenated sequences have been played the amount of times defined in LOOP.CNT
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	PWM module enable register
MODE	0x504	Selects operating mode of the wave counter
COUNTERTOP	0x508	Value up to which the pulse generator counter counts
PRESCALER	0x50C	Configuration for PWM_CLK
DECODER	0x510	Configuration of the decoder
LOOP	0x514	Amount of playback of a loop
SEQ[0].PTR	0x520	Beginning address in Data RAM of this sequence
SEQ[0].CNT	0x524	Amount of values (duty cycles) in this sequence
SEQ[0].REFRESH	0x528	Amount of additional PWM periods between samples loaded into compare register
SEQ[0].ENDDELAY	0x52C	Time added after the sequence
SEQ[1].PTR	0x540	Beginning address in Data RAM of this sequence
SEQ[1].CNT	0x544	Amount of values (duty cycles) in this sequence
SEQ[1].REFRESH	0x548	Amount of additional PWM periods between samples loaded into compare register
SEQ[1].ENDDELAY	0x54C	Time added after the sequence
PSEL.OUT[0]	0x560	Output pin select for PWM channel 0
PSEL.OUT[1]	0x564	Output pin select for PWM channel 1
PSEL.OUT[2]	0x568	Output pin select for PWM channel 2
PSEL.OUT[3]	0x56C	Output pin select for PWM channel 3



47.5.1 SHORTS

Address offset: 0x200 Shortcut register

Bit r	numbe	er		31 30	29	28 2	27 :	26 2	25 :	24 2	23	22 :	21 2	20 1	9 1	8 17	7 10	5 15	5 14	13	12	11	10	9	8	7	6 5	4	3	2	1 (
Id																												Ε	D	С	ВА
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0 0
Id	RW	Field	Value Id	Value							Des	scrip	ptio	n																	
Α	RW	SEQENDO_STOP								9	Sho	ortcı	ut b	etw	eer	SEC	QEN	ND[()] e	ven	t an	d S	ГОР	tas	sk						
										9	See	e <i>EV</i>	EN7	rs_s	EQI	ND	[0]	and	TA	SKS	_ST	ОР									
			Disabled	0						[Disa	able	e sh	orto	ut																
			Enabled	1						E	Ena	able	sho	ortci	ut																
В	RW	SEQEND1_STOP								5	Sho	ortcı	ut b	etw	eer	SEC	QEN	ND[:	1] e	ven	t an	d S	ГОР	tas	sk						
										9	See	e <i>EV</i>	EN7	rs_s	EQI	ND	[1]	and	TA	SKS	_ST	ОР									
			Disabled	0						[Disa	able	e sh	orto	ut																
			Enabled	1						E	Ena	able	sho	ortci	ut																
С	RW	LOOPSDONE_SEQSTARTO								5	Sho	ortcı	ut b	etw	eer	LO	OP:	SDO	NE	eve	nt a	and	SEC	QST.	ART	[0]	task				
										9	See	e <i>EV</i>	EN7	rs_L	.00	PSD	ON	E ar	nd 7	ASI	(S_S	EQS	TΑ	RT[0]						
			Disabled	0						[Disa	able	e sh	orto	ut																
			Enabled	1						E	Ena	able	shc	ortci	ut																
D	RW	LOOPSDONE_SEQSTART1								9	Sho	ortci	ut b	etw	eer	LO	OP:	SDO	NE	eve	nt a	and	SEC	QST.	ART	[1]	task				
										9	See	e <i>EV</i>	EN7	rs_L	.00	PSD	ON	<i>E</i> ar	nd 7	ASI	(S_S	EQ	TA	RT[1]						
			Disabled	0						[Disa	able	e sh	orto	ut																
			Enabled	1						E	Ena	able	sho	ortci	ut																
E	RW	LOOPSDONE_STOP								9	Sho	ortci	ut b	etw	eer	LO	OP:	SDO	NE	eve	nt a	and	STC	OP t	ask						
										9	See	e <i>EV</i>	EN7	rs_L	.00	PSD	ON	<i>E</i> ar	nd 7	ASI	(S_S	TOI	,								
			Disabled	0						[Disa	able	e sh	orto	ut																
			Enabled	1						E	Ena	able	shc	ortci	ut																

47.5.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bitı	numbe	er		31	30 29	9 28	27 2	6 25	5 24	23 22	2 21	20	19 1	18 1	17 1	6 1	.5 14	4 13	3 12	11	10	9	8	7 (6	5 4	1 3	2	1 (
Id																								Н	Ĝ	F E	D	С	В
Res	et 0x0	0000000		0	0 0	0 (0 (0 0	0	0 0	0	0	0	0	0 0) (0 0	0	0	0	0	0	0	0 (0	0 0	0	0	0 0
Id	RW	Field	Value Id	Val	ue					Desc	ripti	on																	
В	RW	STOPPED								Enab	le oi	r dis	able	int	erru	ıpt	for S	STO	PPE	D ev	vent								
										See E	VEN	NTS_	STO	PPE	D														
			Disabled	0						Disab	ole																		
			Enabled	1						Enab	le																		
С	RW	SEQSTARTED0								Enab	le oi	r dis	able	int	erru	ıpt	for S	SEQ	STA	RTE	D[0] ev	ent						
										See E	VEN	NTS_	SEQ	STA	RTE	D[0]												
			Disabled	0						Disab	ole																		
			Enabled	1						Enab	le																		
D	RW	SEQSTARTED1								Enab	le oi	r dis	able	int	erru	ıpt	for S	SEQ	STA	RTE	D[1] ev	ent						
										See E	VEN	NTS_	SEQ	STA	RTE	D[1]												
			Disabled	0						Disab	ole																		
			Enabled	1						Enab	le																		
E	RW	SEQEND0								Enab	le oi	r dis	able	int	erru	ıpt	for s	SEQ	END	[0]	eve	nt							
										See E	VEN	NTS_	SEQ	ENL	D[0]														
			Disabled	0						Disab	ole																		
			Enabled	1						Enab	le																		
F	RW	SEQEND1								Enab	le o	r dis	able	int	erru	ıpt	for s	SEQ	END	[1]	eve	nt							



Bitı	numbe	er		31	30 29	9 28	27	26 2	5 2	4 23 :	22 2	21 20	19	18	17 :	16 1	L5 1	4 1	.3 12	2 11	10	9	8	7	6	5	4 3	2	1 0
Id																								Н	G	F	E D) C	В
Res	et 0x0	0000000		0	0 0	0	0	0 (0 (0 0	0 (0 0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0 0	0	0 0
Id	RW	Field	Value Id	Val	ue					Des	crip	tion																	
										See	EVE	ENTS_	_SE	QEN	ID[1	1													
			Disabled	0						Disa	able																		
			Enabled	1						Ena	ble																		
G	RW	PWMPERIODEND								Ena	ble	or di	sabl	le ir	iterr	upt	for	PW	/MP	ERIC	DEI	ND	evei	nt					
										See	EVE	ENTS_	_PV	VMI	PERI	ODI	END)											
			Disabled	0						Disa	able																		
			Enabled	1						Ena	ble																		
Н	RW	LOOPSDONE								Ena	ble	or di	sabl	le ir	terr	upt	for	LO	OPS	DON	IE ev	/en	t						
										See	EVE	ENTS_	_LO	OPS	SDOI	V <i>E</i>													
			Disabled	0						Disa	able																		
			Enabled	1						Ena	ble																		

47.5.3 INTENSET

Address offset: 0x304

Enable interrupt

Reset 0.00000000	Lilable interrupt			
Review	Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
New Field Value Id Value Value Value Description Write '1' to Enable interrupt for STOPPED event See EVENTS_STOPPED	Id			HGFEDCB
RW STOPPED	Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Set	ld RW Field	Value Id	Value	Description
Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled C RW SEQSTARTED0 Set 1 Enable Disabled 0 Read: Disabled Enable Set 1 Enable Disabled 0 Read: Disabled Enable Set 1 Enable Disabled 0 Read: Disabled Enable Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Mrite '1' to Enable interrupt for SEQSTARTED[0] event See EVENTS_SEQSTARTED[1] Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled ENABLE ENABLE Disabled 0 Read: Disabled Enable Disabled 0 Read: Enabled Finable Disabled 0 Read: Enabled Enable Disabled 1 Read: Enabled Finable Disabled 0 Read: Disabled Enable Disabled 1 Read: Enabled See EVENTS_SEQEND[1] Enable Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND Write '1' to Enable interrupt for PWMPERIODEND	B RW STOPPED			Write '1' to Enable interrupt for STOPPED event
Disabled 0 Read: Disabled 1 Read: Enabled C RW SEQSTARTEDO				See EVENTS_STOPPED
Enabled 1 Read: Enabled Read: Enabled		Set	1	Enable
Write '1' to Enable interrupt for SEQSTARTED[0] event		Disabled	0	Read: Disabled
Set		Enabled	1	Read: Enabled
Set	C RW SEQSTARTEDO			Write '1' to Enable interrupt for SEQSTARTED[0] event
Set				See EVENTS SEOSTARTEDIOI
Read: Enabled 1 Read: Enabled Write '1' to Enable interrupt for SEQSTARTED[1] event See EVENTS_SEQSTARTED[1] Set 1 Enable Read: Enabled Read: Enabled		Set	1	
D RW SEQSTARTED1 Set 1 Enable Disabled 0 Read: Disabled Enable 0 Read: Enabled ENUMBRICAN SEQENDO Set 1 Enable 0 Read: Enabled ENUMBRICAN SEQENDO Set 1 Enable 0 Read: Enabled ENUMBRICAN SEQENDO Set 1 Enable 0 Read: Disabled Disabled 0 Read: Disabled Enable 0 Read: Disabled FRAM SEQENDO Set 1 Enable 0 Read: Disabled Enable 0 Read: Disabled Enable 0 Read: Enabled FRAM SEQENDI Write '1' to Enable interrupt for SEQEND[0] event See EVENTS_SEQEND[0] Set 1 Read: Enabled FRAM SEQENDI Write '1' to Enable interrupt for SEQEND[1] event See EVENTS_SEQEND[1] Set 1 Enable See EVENTS_SEQEND[1] Set 1 Read: Enabled FRAM PWMPERIODEND FRAM PWMPERIODEND Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND		Disabled	0	Read: Disabled
See EVENTS_SEQSTARTED[1] Set 1 Enable Read: Disabled 0 Read: Disabled Enabled 1 Read: Enabled ENUM SEQENDO Set 1 Enable See EVENTS_SEQEND[0] Set 1 Enable Disabled 0 Read: Disabled Enable Poisabled 1 Read: Enabled Enable Poisabled 0 Read: Disabled Enable Enable Poisabled 1 Read: Enabled Enable Enable Poisabled 1 Read: Enabled Enable Poisabled 1 Read: Enabled Enable Poisabled 1 Read: Enabled FOUNT ENABLE POISABLED POISABLE POISABLED POISAB		Enabled	1	Read: Enabled
Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled ENUM SEQENDO Set 1 Enable Disabled 0 Read: Enabled See EVENTS_SEQEND[0] Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled FNUM SEQEND1	D RW SEQSTARTED1			Write '1' to Enable interrupt for SEQSTARTED[1] event
Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled ENUM SEQENDO Set 1 Enable Disabled 0 Read: Enabled See EVENTS_SEQEND[0] Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled FNUM SEQEND1				See EVENTS SEOSTARTED[1]
Enabled 1 Read: Enabled E RW SEQENDO Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled F RW SEQEND1 Set 1 Enable Enabled 1 Read: Enabled Write '1' to Enable interrupt for SEQEND[0] event See EVENTS_SEQEND[0] F RW SEQEND1 Set 1 Read: Enabled See EVENTS_SEQEND[1] Set 1 Enable Disabled 0 Read: Disabled Enable Disabled 1 Read: Enabled Write '1' to Enable interrupt for SEQEND[1] event See EVENTS_SEQEND[1] Set 1 Enable Read: Enabled Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND		Set	1	——————————————————————————————————————
Write '1' to Enable interrupt for SEQEND[0] event See EVENTS_SEQEND[0] Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled FRW SEQEND1 Write '1' to Enable interrupt for SEQEND[1] event See EVENTS_SEQEND[1] Set 1 Enable Enable Disabled 0 Read: Disabled Enable Read: Enabled Write '1' to Enable interrupt for SEQEND[1] event See EVENTS_SEQEND[1] Set 1 Enable Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND		Disabled	0	Read: Disabled
See EVENTS_SEQEND[0] Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled F RW SEQEND1 Set 1 Enable See EVENTS_SEQEND[1] Set 1 Enable Disabled 0 Read: Disabled Read: Disabled Finable Write '1' to Enable interrupt for SEQEND[1] event See EVENTS_SEQEND[1] Set 1 Enable Read: Disabled Finabled 1 Read: Enabled Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND		Enabled	1	Read: Enabled
Set 1 Enable Disabled 0 Read: Disabled FRW SEQEND1 Set 1 Mrite '1' to Enable interrupt for SEQEND[1] event See EVENTS_SEQEND[1] Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable interrupt for SEQEND[1] event See EVENTS_SEQEND[1] Enable Write '1' to Enable interrupt for PWMPERIODEND Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND	E RW SEQENDO			Write '1' to Enable interrupt for SEQEND[0] event
Set 1 Enable Disabled 0 Read: Disabled FRW SEQEND1 Set 1 Mrite '1' to Enable interrupt for SEQEND[1] event See EVENTS_SEQEND[1] Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable interrupt for SEQEND[1] event See EVENTS_SEQEND[1] Enable Write '1' to Enable interrupt for PWMPERIODEND Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND				See EVENTS SECENDIOI
Enabled 1 Read: Enabled F RW SEQEND1 See EVENTS_SEQEND[1] event See EVENTS_SEQEND[1] Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled G RW PWMPERIODEND Enabled Write '1' to Enable interrupt for SEQEND[1] event Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND		Set	1	
F RW SEQEND1 Write '1' to Enable interrupt for SEQEND[1] event See EVENTS_SEQEND[1] Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled G RW PWMPERIODEND Write '1' to Enable interrupt for SEQEND[1] event See EVENTS_PWMPERIODEND Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND		Disabled	0	Read: Disabled
See EVENTS_SEQEND[1] Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled G RW PWMPERIODEND Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND		Enabled	1	Read: Enabled
Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled G RW PWMPERIODEND Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND	F RW SEQEND1			Write '1' to Enable interrupt for SEQEND[1] event
Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled G RW PWMPERIODEND Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND				See EVENTS SECEND[1]
Enabled 1 Read: Enabled G RW PWMPERIODEND Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND		Set	1	
G RW PWMPERIODEND Write '1' to Enable interrupt for PWMPERIODEND event See EVENTS_PWMPERIODEND		Disabled	0	Read: Disabled
See EVENTS_PWMPERIODEND		Enabled	1	Read: Enabled
	G RW PWMPERIODEND			Write '1' to Enable interrupt for PWMPERIODEND event
				See EVENTS PWMPERIODEND
Set 1 Enable		Set	1	
Disabled 0 Read: Disabled				
Enabled 1 Read: Enabled				Read: Enabled
H RW LOOPSDONE Write '1' to Enable interrupt for LOOPSDONE event	H RW LOOPSDONE			Write '1' to Enable interrupt for LOOPSDONE event



Bit number		31 30 29 28 27	26 25 24	23 22 2	21 20 :	19 18	3 17	16 1	5 14	13 1	2 11	10 9	8	7	6	5	4	3 2	1	0
Id														Н	G	F	Е	D C	В	
Reset 0x00000000		0 0 0 0	0 0 0	0 0	0 0	0 0	0	0 0	0	0	0 0	0 (0	0	0	0	0	0 0	0	0
ld RW Field	Value Id	Value		Descrip	tion															
				See <i>EV</i>	ENTS_	LOOF	SDO	NE												_
	Set	1		Enable																
	Disabled	0		Read: [isable	d														
	Enabled	1		Read: E	nable	d														

47.5.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit	number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
ld				H G F E D C B
Res	et 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW Field	Value Id	Value	Description
В	RW STOPPED			Write '1' to Disable interrupt for STOPPED event
				See EVENTS_STOPPED
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW SEQSTARTED0			Write '1' to Disable interrupt for SEQSTARTED[0] event
				See EVENTS_SEQSTARTED[0]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW SEQSTARTED1			Write '1' to Disable interrupt for SEQSTARTED[1] event
				See EVENTS_SEQSTARTED[1]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E	RW SEQENDO			Write '1' to Disable interrupt for SEQEND[0] event
				See EVENTS_SEQEND[0]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW SEQEND1			Write '1' to Disable interrupt for SEQEND[1] event
				See EVENTS_SEQEND[1]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW PWMPERIODEND			Write '1' to Disable interrupt for PWMPERIODEND event
				See EVENTS_PWMPERIODEND
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW LOOPSDONE			Write '1' to Disable interrupt for LOOPSDONE event
				See EVENTS_LOOPSDONE
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

47.5.5 ENABLE

Address offset: 0x500



PWM module enable register

Bit	numl	ber	•		31	30 :	29	28	27	26	25	24	23	3 22	2 2:	L 20	19	9 18	3 17	16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																				Α
Res	et O	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RV	N	Field	Value Id	Val	ue							D	escr	ript	ion																				
Α	RV	٧	ENABLE										Er	nabl	le c	r d	isab	le	PWI	M r	nod	ule														
				Disabled	0								Di	isab	led																					
				Enabled	1								Er	nabl	le																					

47.5.6 MODE

Address offset: 0x504

Selects operating mode of the wave counter

Bit	numb	er		31 30	29 2	28 2	7 26	25	24	23	22	21 2	20 1	9 1	8 17	7 16	15	14	13	L2 1	.1 10	9	8	7	6	5	4	3	2 1	. 0
Id																														Α
Res	et Ox	00000000		0 0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Value						Des	scrip	ptio	n																	
Α	RW	UPDOWN								Sel	ects	up	or ι	ир а	nd c	low	n as	wa	ve c	our	iter i	nod	le							
			Up	0						Up	cou	ınte	r - e	dge	alig	gned	d PV	VM	dut	/-cy	cle									
			UpAndDown	1						Up	and	d do	wn	cou	nter	- C6	ente	er al	igne	d P	WM	dut	у су	cle						

47.5.7 COUNTERTOP

Address offset: 0x508

Value up to which the pulse generator counter counts

Bit	numbe	er		31 30	29 2	28 27	7 26	25 2	24 2	3 2	2 21	20	19	18 1	7 16	5 15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																	Α	Α .	4 Δ	A	Α	Α	Α	Α	Α	Α	А А	. A	Α
Res	et 0x0	00003FF		0 0	0 (0 0	0	0	0 (0 0	0	0	0	0 0	0	0	0	0	0 0	0	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Value					D)esc	ripti	on																	
Α	RW	COUNTERTOP		[3327	767]				٧	alue	e up	to v	vhic	h the	e pu	lse į	gene	erato	or co	unt	er c	oun	ts.	This	;				
									re	egis	ter i	s igr	ore	d wh	en	DEC	ODE	R.N	IODI	E=W	ave	For	m a	nd (only	/			
									V	alue	es fro	om F	RAN	l will	he	use	d												

47.5.8 PRESCALER

Address offset: 0x50C

Configuration for PWM_CLK

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Id		A A	Α
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
Id RW Field	Value Id	Value Description	
A RW PRESCALER		Pre-scaler of PWM_CLK	
	DIV_1	0 Divide by 1 (16MHz)	
	DIV_2	1 Divide by 2 (8MHz)	
	DIV_4	2 Divide by 4 (4MHz)	
	DIV_8	3 Divide by 8 (2MHz)	
	DIV_16	4 Divide by 16 (1MHz)	
	DIV_32	5 Divide by 32 (500kHz)	
	DIV_64	6 Divide by 64 (250kHz)	
	DIV_128	7 Divide by 128 (125kHz)	

47.5.9 DECODER

Address offset: 0x510

Configuration of the decoder



Bit number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B A A A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW LOAD			How a sequence is read from RAM and spread to the compare
			register
	Common	0	1st half word (16-bit) used in all PWM channels 03
	Grouped	1	1st half word (16-bit) used in channel 01; 2nd word in channel
			23
	Individual	2	1st half word (16-bit) in ch.0; 2nd in ch.1;; 4th in ch.3
	WaveForm	3	1st half word (16-bit) in ch.0; 2nd in ch.1;; 4th in
			COUNTERTOP
B RW MODE			Selects source for advancing the active sequence
	RefreshCount	0	SEQ[n].REFRESH is used to determine loading internal compare
			registers
	NextStep	1	NEXTSTEP task causes a new value to be loaded to internal
			compare registers

47.5.10 LOOP

Address offset: 0x514

Amount of playback of a loop

Bit	number		31 3	0 29	9 2	8 27	7 26	25	24	23	22 :	21 2	20 1	9 1	8 17	7 16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id																	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А	. 4	A A
Res	et 0x00000000		0	0 0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW Field	Value Id	Valu	ie						Des	crip	otio	n																		
Α	RW CNT									Am	our	nt of	pla	yba	ck c	of pa	itte	rn c	ycle	es											
		Disabled	0							Loc	pin	g di	sabl	ed	(sto	p at	the	en	d of	the	e se	que	enc	e)							

47.5.11 SEQ[0].PTR

Address offset: 0x520

Beginning address in Data RAM of this sequence

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Beginning address in Data RAM of this sequence

47.5.12 SEQ[0].CNT

Address offset: 0x524

Amount of values (duty cycles) in this sequence

Bitı	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW CNT			Amount of values (duty cycles) in this sequence
		Disabled	0	Sequence is disabled, and shall not be started as it is empty

47.5.13 SEQ[0].REFRESH

Address offset: 0x528

Amount of additional PWM periods between samples loaded into compare register



Bit	numl	per		31	1 30	29	28	3 27	7 26	25	24	23	22	21	20	19 :	18 1	7 1	5 15	5 14	13	12	11 1	.0 9	9 8	3 7	' 6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α /	4 Α	. A	Α	Α	Α	A	Δ ,	Δ ,	A /	A	Α	Α	Α	Α	А А
Re	set 0	00000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0 1
Id	RV	/ Field	Value Id	Va	alue	:						De	scri	ptic	on																	
Α	RV	/ CNT										An	nou	nt o	f ac	dditi	ona	I PV	/M	peri	ods	bet	wee	n s	amı	oles	loa	ded	ı			
												int	:о сс	mp	are	reg	iste	r (lo	ad	eve	ry R	EFRE	SH.	CN.	T+1	PW	M					
												pe	riod	s)																		
			Continuous	0								Up	dat	e ev	ery	PW	/M	oerio	od													

47.5.14 SEQ[0].ENDDELAY

Address offset: 0x52C

Time added after the sequence

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20	19 18 17 16 15	5 14 13 12 11 10	9 8 7 6 5	5 4 3 2 1 0
Id			АААА	AAAAA	. A A A A A .	AAAAA	A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0 0
Id RW Field	Value Id	Value	Description				
A RW CNT			Time added	after the sequer	nce in PWM period	ds	

47.5.15 SEQ[1].PTR

Address offset: 0x540

Beginning address in Data RAM of this sequence

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Beginning address in Data RAM of this sequence

47.5.16 SEQ[1].CNT

Address offset: 0x544

Amount of values (duty cycles) in this sequence

Bitı	numb	er		31 30	29	28 2	7 26	25	24	23	22	21 2	0 19	9 18	3 17	16	15	14	13	12 :	1 1	9	8	7	6	5	4	3 2	2 1	. 0
Id																		Α	Α	Α	Α Α	A	Α	Α	Α	Α	Α	A A	Α Δ	A A
Res	et Ox	0000000		0 0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value						De	scrip	ptio	n																	
Α	RW	CNT								Am	nour	nt of	valu	ıes	(dut	у су	cles	s) ir	thi	s se	que	nce								
			Disabled	0						Sec	quer	nce i	s dis	sabl	ed,	and	sha	all n	ot k	e si	arte	d a	s it i	s er	npt	У				

47.5.17 SEQ[1].REFRESH

Address offset: 0x548

Amount of additional PWM periods between samples loaded into compare register

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000001		$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value Description
A RW CNT		Amount of additional PWM periods between samples loaded
		into compare register (load every REFRESH.CNT+1 PWM
		periods)
	Continuous	0 Update every PWM period

47.5.18 SEQ[1].ENDDELAY

Address offset: 0x54C



Time added after the sequence

Bi	t nui	mbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0	l
Id													Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	А А	
Re	eset	0x0	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	l
Id	F	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				l
Α	F	RW	CNT										Tin	ne a	add	ed a	afte	r th	ie s	eau	ien	ce i	n P	WΝ	1 pe	erio	ds									

47.5.19 PSEL.OUT[0]

Address offset: 0x560

Output pin select for PWM channel 0

Bit	numbe	er		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	ААААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

47.5.20 PSEL.OUT[1]

Address offset: 0x564

Output pin select for PWM channel 1

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	ААААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

47.5.21 PSEL.OUT[2]

Address offset: 0x568

Output pin select for PWM channel 2

Bit	numb	er		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	ААААА
Re	et 0xl	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

47.5.22 PSEL.OUT[3]

Address offset: 0x56C

Output pin select for PWM channel 3

E	Bit n	umb	er		31 30 29	9 28 27	26 2	5 24	23 2	22 21	20	19 1	8 17	7 16	15	14 1	3 12	11 1	0 9	8	7	6	5	4	3 2	2 1	0
1	d				В																			Α	A A	A	Α
F	Rese	t Oxl	FFFFFFF		1 1 1	. 1 1	1 1	. 1	1	1 1	1	1 :	1 1	1	1	1 1	1	1	l 1	1	1	1	1	1	1 1	1	1
ı	ld	RW	Field	Value Id	Value				Des	cripti	ion																
1	Д	RW	PIN		[031]				Pin r	numb	oer																



Bitı	numbe	er		31 30	29 2	28 2	7 26	25	24	23	22 2	1 20	19	18 3	l7 1	6 15	14	13 1	12 11	. 10	9	8	7	6	5	4	3 2	1	0
Id				В																						A	4 А	Α	Α
Res	et OxF	FFFFFF		1 1	1	1 1	1	1	1	1	1 1	l 1	1	1	1 :	l 1	1	1	1 1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Value						Des	cript	tion																	
В	RW	CONNECT								Con	nect	ion																	
			Disconnected	1						Disc	onn	ect																	
			Connected	0						Con	nect	t																	

47.6 Electrical specification

47.6.1 PWM Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{PWM,16MHz}	PWM run current, Prescaler set to DIV_1 (16 MHz), excluding		200		μΑ
	DMA and GPIO				
I _{PWM,8MHz}	PWM run current, Prescaler set to DIV_2 (8 MHz), excluding		150		μΑ
	DMA and GPIO				
I _{PWM,125kHz}	PWM run current, Prescaler set to DIV_128 (125 kHz), excluding		150		μΑ
	DMA and GPIO				



48 SPI — Serial peripheral interface master

The SPI master provides a simple CPU interface which includes a TXD register for sending data and an RXD register for receiving data. This section is added for legacy support for now.

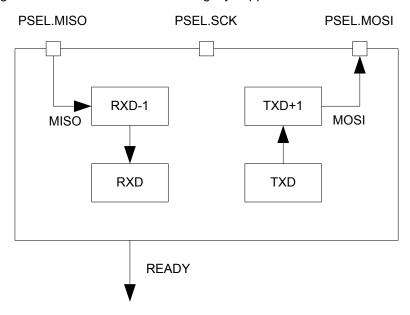


Figure 150: SPI master

RXD-1 and TXD+1 illustrate the double buffered version of RXD and TXD respectively.

48.1 Functional description

The TXD and RXD registers are double-buffered to enable some degree of uninterrupted data flow in and out of the SPI master.

The SPI master does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master. The SPI master supports SPI modes 0 through 3.

Table 120: SPI modes

Mode	Clock polarity	Clock phase
	CPOL	СРНА
SPI_MODE	0 (Leading)	0 (Active High)
SPI_MODE	0 (Leading)	1 (Active Low)
SPI_MODE	1 (Trailing)	0 (Active High)
SPI_MODE	1 (Trailing)	1 (Active Low)

48.1.1 SPI master mode pin configuration

The different signals SCK, MOSI, and MISO associated with the SPI master are mapped to physical pins.

This mapping is according to the configuration specified in the PSELSCK, PSELMOSI, and PSELMISO registers respectively. If a value of 0xFFFFFFF is specified in any of these registers, the associated SPI master signal is not connected to any physical pin. The PSELSCK, PSELMOSI, and PSELMISO registers and their configurations are only used as long as the SPI master is enabled, and retained only as long as the device is in ON mode. PSELSCK, PSELMOSI, and PSELMISO must only be configured when the SPI master is disabled.

To secure correct behavior in the SPI, the pins used by the SPI must be configured in the GPIO peripheral as described in *Table 121: GPIO configuration* on page 515 prior to enabling the SPI. The SCK must



always be connected to a pin, and that pin's input buffer must always be connected for the SPI to work. This configuration must be retained in the GPIO for the selected IOs as long as the SPI is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 121: GPIO configuration

SPI master signal	SPI master pin	Direction	Output value
SCK	As specified in PSELSCK	Output	Same as CONFIG.CPOL
MOSI	As specified in PSELMOSI	Output	0
MISO	As specified in PSELMISO	Input	Not applicable

48.1.2 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.

Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 24 for details on peripherals and their IDs.

48.1.3 SPI master transaction sequence

An SPI master transaction is started by writing the first byte, which is to be transmitted by the SPI master, to the TXD register.

Since the transmitter is double buffered, the second byte can be written to the TXD register immediately after the first one. The SPI master will then send these bytes in the order they are written to the TXD register.

The SPI master is a synchronous interface, and for every byte that is sent, a different byte will be received at the same time; this is illustrated in *Figure 151: SPI master transaction* on page 516. Bytes that are received will be moved to the RXD register where the CPU can extract them by reading the register. The RXD register is double buffered in the same way as the TXD register, and a second byte can therefore be received at the same time as the first byte is being extracted from RXD by the CPU. The SPI master will generate a READY event every time a new byte is moved to the RXD register. The double buffered byte will be moved from RXD-1 to RXD as soon as the first byte is extracted from RXD. The SPI master will stop when there are no more bytes to send in TXD and TXD+1.



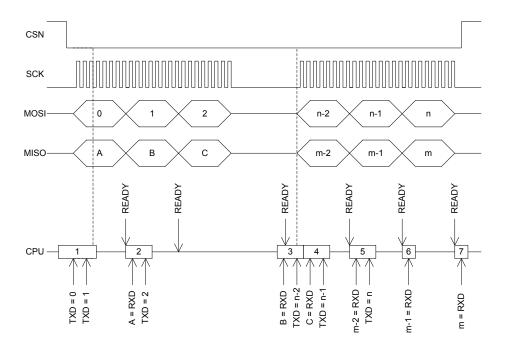


Figure 151: SPI master transaction

The READY event of the third byte transaction is delayed until B is extracted from RXD in occurrence number 3 on the horizontal lifeline. The reason for this is that the third event is generated first when C is moved from RXD-1 to RXD after B is read.

The SPI master will move the incoming byte to the RXD register after a short delay following the SCK clock period of the last bit in the byte. This also means that the READY event will be delayed accordingly, see *Figure 152: SPI master transaction* on page 516. Therefore, it is important that you always clear the READY event, even if the RXD register and the data that is being received is not used.

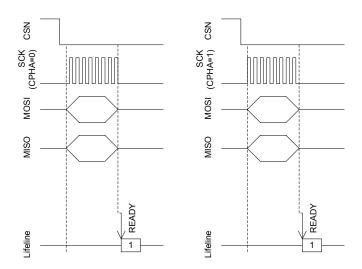


Figure 152: SPI master transaction



48.2 Registers

Table 122: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	SPI	SPI0	SPI master 0		Deprecated
0x40004000	SPI	SPI1	SPI master 1		Deprecated
0x40023000	SPI	SPI2	SPI master 2		Deprecated

Table 123: Register Overview

Register	Offset	Description	
EVENTS_READY	0x108	TXD byte sent and RXD byte received	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
ENABLE	0x500	Enable SPI	
PSELSCK	0x508	Pin select for SCK	Deprecated
PSELMOSI	0x50C	Pin select for MOSI	Deprecated
PSELMISO	0x510	Pin select for MISO	Deprecated
PSEL.SCK	0x508	Pin select for SCK	
PSEL.MOSI	0x50C	Pin select for MOSI	
PSEL.MISO	0x510	Pin select for MISO	
RXD	0x518	RXD register	
TXD	0x51C	TXD register	
FREQUENCY	0x524	SPI frequency	
CONFIG	0x554	Configuration register	

48.2.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	1	5 14	1 13	3 12	2 11	. 10	9	8	7	6	5	4	3	2 1	0
Id																																,	4	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	alue							Des	cri	ptic	on																			
Α	RW	READY										Wri	te	'1' t	o E	nal	ole	int	err	upt	fo	RE	ΑD	Y ev	ent	:								
												See	EV	'EN	TS_	RE	4D	Υ																
			Set	1								Ena	ble	:																				
			Disabled	0								Rea	ıd:	Disa	able	ed																		
			Enabled	1								Rea	ıd:	Ena	ble	d																		

48.2.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	er		31	. 30	29	28	8 27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 :	2 1	. 0
Id																																,	4	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							De	scr	pti	on																			
Α	RW	READY										Wı	rite	'1' 1	to [Disa	ble	int	terr	upt	for	RE	٩DY	ev	ent									
												Se	e <i>E</i> ۱	/EN	TS_	RE	AD	Y																
			Clear	1								Dis	abl	e																				
			Disabled	0								Re	ad:	Dis	abl	ed																		
			Enabled	1								Re	ad:	Ena	able	ed																		



48.2.3 ENABLE

Address offset: 0x500

Enable SPI

Bit	numbe	er		31 30	29	28	27	26 :	25 2	24 2	23 2	2 2	1 20	19	18	17	16	15 1	4 1	3 12	11	10 9	9 8	7	6	5	4	3	2	1 0
Id																												Α	Α	А А
Res	et 0x0	0000000		0 0	0	0	0	0	0 (0	0 (0 0	0	0	0	0	0	0	0 0	0	0	0 () (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value	е					C	Desc	crip	tion																	
Α	RW	ENABLE								Е	nat	ole d	or d	sab	le S	ΡI														
			Disabled	0							Disa	ble	SPI																	
			Enabled	1						Е	nak	ole S	SPI																	

48.2.4 PSELSCK (Deprecated)

Address offset: 0x508 Pin select for SCK

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 18	3 17	16	15	14	13	12 1	.1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	ΑА	A	Α	Α	Α	Α	Α	A .	ДД	Α	Α	Α	Α	Α	Α	Α .	Δ ,	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																	
Α	RW	PSELSCK		[0	31]						Pin	nur	nbe	r co	nfig	urat	tion	for	SPI	SCI	(sig	nal									
			Disconnected	0x	FFF	FFF	FF					Dis	con	nec	t																	

48.2.5 PSELMOSI (Deprecated)

Address offset: 0x50C Pin select for MOSI

Bit	number			31	30	29	28	27	26	25	24	23	22	21 :	20 :	19 1	18 :	17 1	.6 1	15 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	Δ.	A A	A A	A	Α	Α	Α	Α	Α	Α	Α	Α /	4 А	Α	Α
Res	et OxFFFFF	FFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	1	1	1	1	1	1	1	1	1	1 1	1	1
Id	RW Field	d	Value Id	Va	lue							De	scri	ptio	n																		
Α	RW PSEI	LMOSI		[0.	31]							Pin	nu	mbe	er c	onfi	iguı	atio	n f	or S	PI I	NOS	l się	nal									
			Disconnected	٥	FFFI							D:c	con																				

48.2.6 PSELMISO (Deprecated)

Address offset: 0x510 Pin select for MISO

Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18 1	L7 1	.6 1	5 1	4 1	3 12	2 11	. 10	9	8	7	6	5	4	3 2	1	. 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A ,	Δ.	A A	A /	A	Α	Α	Α	Α	Α	Α	Α	Α	ΑА	. 4	A A
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	1	1	1	1	1	1	1	1	1 1	. 1	1
Id RW Field	Value Id	Va	lue							De	scri	ptic	n																		
A RW PSELMISO		[0.	31]							Pin	nu	mb	er c	onf	igur	atio	n f	or S	PIN	ЛISC) się	gnal									,
	Disconnected	0x	FFFF	FFF	FF					Dis	con	nec	t																		

48.2.7 PSEL.SCK

Address offset: 0x508 Pin select for SCK

Bit	numbe	er		31	L 30	29	28	27	' 26	25	24	23	22	21	20 1	19 1	.8 1	7 16	5 15	14	13	L2 1	.1 10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A .	ДД	A	Α	Α	Α	Α .	Д А	Α	Α	Α	Α	Α	Α	A A	λ /	A A
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1 1	1	1	1	1	1	1	1 1	L 1	l 1
Id	RW	Field	Value Id	Va	alue	:						De	scri	otic	n																	
Α	RW	PSELSCK		[0	31]						Pin	nuı	nbe	er co	onfi	gura	itio	n foi	SPI	SCI	sig	nal									
			Disconnected	0x	FFF	FFF	FF					Dis	con	nec	t																	



48.2.8 PSEL.MOSI

Address offset: 0x50C Pin select for MOSI

Bit	numb	er		31	1 30	29	9 2	8 2	7 2	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 :	1 0
Id				Α	Α	Α	. 4	Α Α	Δ.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	4 A
Res	et 0xl	FFFFFFF		1	1	1	1	L 1	L	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	1 1
Id	RW	Field	Value Id	Va	alue	•							De	scri	ptic	on																			
Α	RW	PSELMOSI		[0	31	.]							Pin	nu	mb	er d	con	figu	ırat	ion	for	SP	М	OSI	sigr	nal									

48.2.9 PSEL.MISO

Address offset: 0x510 Pin select for MISO

Bit	numb	er		30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A	A A A A A A A A A A A A A A A A A A A
Res	et 0x	FFFFFFF		1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	ue	Description
Α	RW	PSELMISO		31]	Pin number configuration for SPI MISO signal
			Disconnected	FFFFFF	Disconnect

48.2.10 RXD

Address offset: 0x518

RXD register

Bi	it n	umbe	er		31 30	29 2	28 27	7 26	25 2	24 2	3 2	2 21	20	19	18	17 :	16 :	L5 1	14 1	.3 1	2 1:	10	9	8	7	6	5	4	3 2	2 1	0
Id																									Α	Α	Α	Α .	A A	A A	Α
R	ese	t OxC	0000000		0 0	0	0 0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Id	ı	RW	Field	Value Id	Value						esc	ripti	on																		
Α		R	RXD							F	X da	ata r	ece	ived	l. De	oub	le b	uff	ere	d											

48.2.11 TXD

Address offset: 0x51C

TXD register

Bit number		31 30 29 28 27 2	$6\ 25\ 24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0$
Id			A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW TXD			TX data to send. Double buffered

48.2.12 FREQUENCY

Address offset: 0x524

SPI frequency

Bit	numbe	r		31	30	29	28	27	26	25	24	23 :	22 :	21 :	20 1	19 :	18	17	16	15	14	13	12 1	11 1	10	9	8	7 6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	A	Α.	Δ,	4 4	A	Α	Α	Α	А А
Res	et 0x0	4000000		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	FREQUENCY										SPI	ma	ste	da	ta r	rate	•															
			K125	0x0	020	000	000					125	kb	ps																			
			K250	0x0	040	000	000					250	kb	ps																			
			K500	0x0	080	000	000					500	kb	ps																			
			M1	0x	100	000	000					1 M	lbps	5																			



Bit number		31	. 30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	8 1	7 16	5 15	5 14	13	12	11	10	9	8	7	6	5 4	4 3	2	1	0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ ,	A /	A	Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	A A	ДД	A	Α	Α
Reset 0x04000000		0	0	0	0	0	1	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0
ld RW Field	Value Id	Va	lue							Des	crip	otio	n																		
	M2	0х	200	000	000					2 N	1bp:	S																			
	M4	0х	400	000	000					4 N	1bp:	S																			
	M8	0х	800	000	000					8 N	1bp:	S																			

48.2.13 CONFIG

Address offset: 0x554 Configuration register

Bit r	iumbe	er		31	30 2	9 2	28 2	7 2	6 25	24	23	22 2	21 2	0 1	9 18	8 1	7 10	5 15	5 14	1 13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id																														С	В	Α
Res	et 0x0	0000000		0	0 ()	0 0) (0	0	0	0	0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Val	lue						Des	crip	tion	1																		
Α	RW	ORDER									Bit	ord	er																			
			MsbFirst	0							Mo	st si	gnif	icar	nt b	it sl	nift	ed c	out	firs	t											
			LsbFirst	1							Lea	st si	gnif	icar	nt b	it sl	nift	ed c	out	firs	t											
В	RW	СРНА									Seri	ial c	lock	(SC	CK) p	oha	se															
			Leading	0							San	nple	on	lead	ding	g ed	ge	of c	loc	k, sl	nift	seri	al d	ata	on t	rai	ling					
											edg	ge																				
			Trailing	1							San	nple	on	trai	ling	ed	ge (of cl	locl	c, sł	ift:	seri	al da	ata	on l	eac	ling					
											edg	ge																				
С	RW	CPOL									Seri	ial c	lock	(SC	CK) p	oola	rity	,														
			ActiveHigh	0							Acti	ive l	high																			
			ActiveLow	1							Acti	ive l	ow																			

48.3 Electrical specification

48.3.1 SPI master interface

Symbol	Description	Min.	Тур.	Max.	Units
f _{SPI}	Bit rates for SPI ³⁹			8 ⁴⁰	Mbps
I _{SPI,2Mbps}	Run current for SPI, 2 Mbps			50	μΑ
I _{SPI,8Mbps}	Run current for SPI, 8 Mbps			50	μΑ
I _{SPI,IDLE}	Idle current for SPI (STARTed, no CSN activity)		<1		μΑ
t _{SPI,START,LP}	Time from writing TXD register to transmission started, low		t _{SPI,START}	,CI	μs
	power mode		+		
			t _{START_H}	IN	
t _{SPI,START,CL}	Time from writing TXD register to transmission started, constant		1		μs
	latency mode				

48.3.2 Serial Peripheral Interface (SPI) Master timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{SPI,CSCK,8Mbps}	SCK period at 8Mbps		125		ns
t _{SPI,CSCK,4Mbps}	SCK period at 4Mbps		250		ns
t _{SPI,CSCK,2Mbps}	SCK period at 2Mbps		500		ns
t _{SPI,RSCK,LD}	SCK rise time, low drive ^a			t _{RF,25pF}	
t _{SPI,RSCK,HD}	SCK rise time, high drive ^a			t _{HRF,25pF}	
t _{SPI,FSCK,LD}	SCK fall time, low drive ^a			t _{RF,25pF}	
t _{SPI,FSCK,HD}	SCK fall time, high drive ^a			t _{HRF,25pF}	

Higher bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.
 The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.

 $^{^{\}rm a}~{\rm At}~25{\rm pF}~{\rm load},$ including GPIO capacitance, see GPIO spec.



Symbol	Description	Min.	Тур.	Max.	Units
t _{SPI,WHSCK}	SCK high time ^a	(0.5*t _{CS}	ck)		
		- t _{RSCK}			
t _{SPI,WLSCK}	SCK low time ^a	(0.5*t _{CS}	ck)		
		$-t_{\text{FSCK}}$			
t _{SPI,SUMI}	MISO to CLK edge setup time	19			ns
t _{SPI,HMI}	CLK edge to MISO hold time	18			ns
t _{SPI,VMO}	CLK edge to MOSI valid			59	ns
t _{SPI,HMO}	MOSI hold time after CLK edge	20			ns

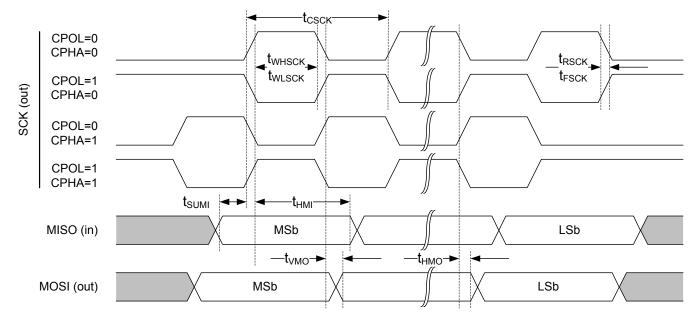


Figure 153: SPI master timing diagram



49 TWI — I²C compatible two-wire interface

The TWI master is compatible with I²C operating at 100 kHz and 400 kHz.

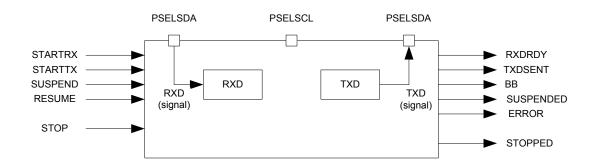


Figure 154: TWI master's main features

49.1 Functional description

This TWI master is not compatible with CBUS. The TWI transmitter and receiver are single buffered.

See, Figure 154: TWI master's main features on page 522.

A TWI setup comprising one master and three slaves is illustrated in *Figure 155: A typical TWI setup comprising one master and three slaves* on page 522. This TWI master is only able to operate as the only master on the TWI bus.

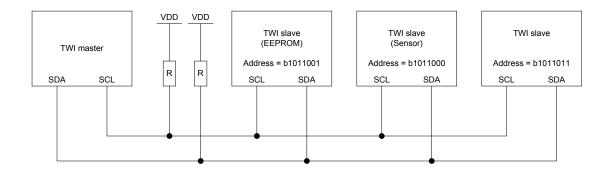


Figure 155: A typical TWI setup comprising one master and three slaves

This TWI master supports clock stretching performed by the slaves. The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

49.2 Master mode pin configuration

The different signals SCL and SDA associated with the TWI master are mapped to physical pins according to the configuration specified in the PSELSCL and PSELSDA registers respectively.

If a value of 0xFFFFFFF is specified in any of these registers, the associated TWI master signal is not connected to any physical pin. The PSELSCL and PSELSDA registers and their configurations are only used



as long as the TWI master is enabled, and retained only as long as the device is in ON mode. PSELSCL and PSELSDA must only be configured when the TWI is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table 124: GPIO configuration* on page 523.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 124: GPIO configuration

TWI master signal	TWI master pin	Direction	Drive strength	Output value
SCL	As specified in PSELSCL	Input	SOD1	Not applicable
SDA	As specified in PSELSDA	Input	SOD1	Not applicable

49.3 Shared resources

The TWI shares registers and other resources with other peripherals that have the same ID as the TWI.

Therefore, you must disable all peripherals that have the same ID as the TWI before the TWI can be configured and used. Disabling a peripheral that has the same ID as the TWI will not reset any of the registers that are shared with the TWI. It is therefore important to configure all relevant TWI registers explicitly to secure that it operates correctly.

The Instantiation table in *Instantiation* on page 24 shows which peripherals have the same ID as the TWI.

49.4 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes that are written to the TXD register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave. A TXDSENT event will be generated each time the TWI master has clocked out a TXD byte, and the associated ACK/NACK bit has been clocked in from the slave.

The TWI master transmitter is single buffered, and a second byte can only be written to the TXD register after the previous byte has been clocked out and the ACK/NACK bit clocked in, that is, after the TXDSENT event has been generated.

If the CPU is prevented from writing to TXD when the TWI master is ready to clock out a byte, the TWI master will stretch the clock until the CPU has written a byte to the TXD register.

A typical TWI master write sequence is illustrated in *Figure 156: The TWI master writing data to a slave* on page 524. Occurrence 3 in the figure illustrates delayed processing of the TXDSENT event associated with TXD byte 1. In this scenario the TWI master will stretch the clock to prevent writing erroneous data to the slave.



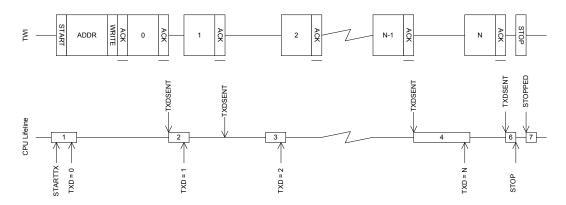


Figure 156: The TWI master writing data to a slave

The TWI master write sequence is stopped when the STOP task is triggered whereupon the TWI master will generate a stop condition on the TWI bus.

49.5 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1).

The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

The TWI master will generate a RXDRDY event every time a new byte is received in the RXD register.

After receiving a byte, the TWI master will delay sending the ACK/NACK bit by stretching the clock until the CPU has extracted the received byte, that is, by reading the RXD register.

The TWI master read sequence is stopped by triggering the STOP task. This task must be triggered before the last byte is extracted from RXD to ensure that the TWI master sends a NACK back to the slave before generating the stop condition.

A typical TWI master read sequence is illustrated in *Figure 157: The TWI master reading data from a slave* on page 525. Occurrence 3 in this figure illustrates delayed processing of the RXDRDY event associated with RXD byte B. In this scenario the TWI master will stretch the clock to prevent the slave from overwriting the contents of the RXD register.



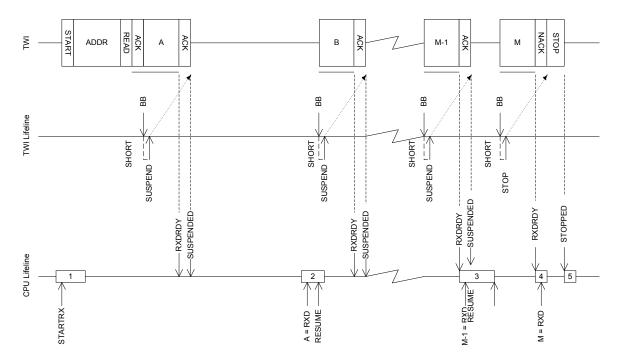


Figure 157: The TWI master reading data from a slave

49.6 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes one byte to the slave followed by reading M bytes from the slave. Any combination and number of transmit and receive sequences can be combined in this fashion. Only one shortcut to STOP can be enabled at any given time.

The figure below illustrates a repeated start sequence where the TWI master writes one byte, followed by reading M bytes from the slave without performing a stop in-between.

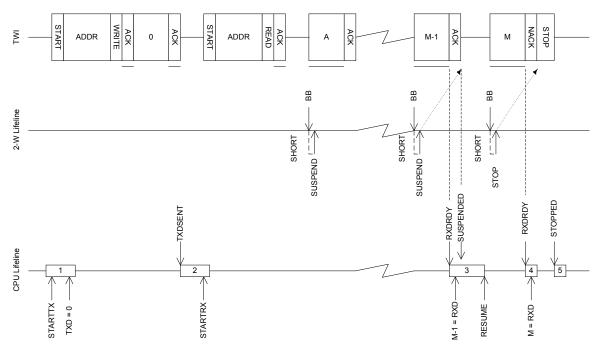


Figure 158: A repeated start sequence, where the TWI master writes one byte, followed by reading M bytes from the slave without performing a stop in-between



To generate a repeated start after a read sequence, a second start task must be triggered instead of the STOP task, that is, STARTRX or STARTTX. This start task must be triggered before the last byte is extracted from RXD to ensure that the TWI master sends a NACK back to the slave before generating the repeated start condition.

49.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

49.8 Registers

Table 125: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	TWI	TWI0	Two-wire interface master 0		Deprecated
0x40004000	TWI	TWI1	Two-wire interface master 1		Deprecated

Table 126: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start TWI receive sequence
TASKS_STARTTX	0x008	Start TWI transmit sequence
TASKS_STOP	0x014	Stop TWI transaction
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_RXDREADY	0x108	TWI RXD byte received
EVENTS_TXDSENT	0x11C	TWI TXD byte sent
EVENTS_ERROR	0x124	TWI error
EVENTS_BB	0x138	TWI byte boundary, generated before each byte that is sent or received
EVENTS_SUSPENDED	0x148	TWI entered the suspended state
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4C4	Error source
ENABLE	0x500	Enable TWI
PSELSCL	0x508	Pin select for SCL
PSELSDA	0x50C	Pin select for SDA
RXD	0x518	RXD register
TXD	0x51C	TXD register
FREQUENCY	0x524	TWI frequency
ADDRESS	0x588	Address used in the TWI transfer

49.8.1 SHORTS

Address offset: 0x200

Shortcut register

Е	tit number		31 3	30 29	28 2	7 26	25 2	24 2	3 22	21	20 1	9 18	17	16 1	15 14	13	12	11 1	0 9	8	7	6	5 4	4 3	2	1	O .
1	d																									В	A
F	Reset 0x00000000		0	0 0	0 (0 0	0	0	0 0	0	0 (0 0	0	0	0 0	0	0	0 (0 0	0	0	0	0	0 0	0	0	O
b	d RW Field	Value Id	Valu	ıe				0)esci	iptic	n																

A RW BB_SUSPEND

Shortcut between BB event and SUSPEND task



Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			В А
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
			See EVENTS_BB and TASKS_SUSPEND
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut
B RW BB_STOP			Shortcut between BB event and STOP task
			See EVENTS_BB and TASKS_STOP
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut

49.8.2 INTENSET

Address offset: 0x304

Enable interrupt

		у и поттарт																															
	numb	er		3:	1 30	29	28 2	27 2	6 25	5 24	1 2	3 22	2 21 2	0 1			.7 1	6 1			13 1	2 :	11 1					5 5	5 4	3			0
Id															F					Ε)	(Α	
Res		00000000		0			0	0 (0	0			0		0 0) (0 (כ	0	0	0	0	0 () () () () (0 () (0	0	0	0
Id		Field	Value Id	V	alue								riptio																				
Α	RW	STOPPED									W	Vrite	e '1' to	En	nable	e in	iter	rup	ot fo	or S	TOI	PE	D e	ven	t								
											S	ee E	VENT	s_s	TOF	PE	D																
			Set	1							Е	nab	le																				
			Disabled	0							R	ead	: Disa	ble	d																		
			Enabled	1							R	ead	: Enat	oled	ł																		
В	RW	RXDREADY									W	Vrite	e '1' to	En	nable	e in	iter	rup	ot fo	or F	RXDI	RE/	ADY	eve	nt								
											S	ee E	VENT	S F	RXDI	RE/	ADY																
			Set	1								nab		_																			
			Disabled	0							R	ead	: Disa	ble	d																		
			Enabled	1							R	ead	: Enat	oled	ł																		
С	RW	TXDSENT									W	Vrite	e '1' to	En	nable	e in	iter	rup	ot fo	or 1	XDS	SEN	IT e	/en	t								
											S	ee E	VENT	· S_1	TXDS	EΝ	IT																
			Set	1								nab		Ī																			
			Disabled	0							R	ead	: Disa	ble	d																		
			Enabled	1							R	ead	: Enab	oled	ł																		
D	RW	ERROR									W	Vrite	e '1' to	En	nable	e in	iter	rup	ot fo	or E	RRC	OR	eve	nt									
											S	ee E	VENT	S_E	RRC	DR																	
			Set	1							Е	nab	le																				
			Disabled	0							R	ead	: Disa	ble	d																		
			Enabled	1							R	ead	: Enak	oled	ł																		
Ε	RW	ВВ									W	Vrite	e '1' to	En	nable	e in	iter	rup	ot fo	or E	ВВ е	ver	nt										
											S	ee E	VENT	S_E	3 <i>B</i>																		
			Set	1							Е	nab	le																				
			Disabled	0							R	ead	: Disa	ble	d																		
			Enabled	1							R	ead	: Enat	oled	ł																		
F	RW	SUSPENDED									W	Vrite	e '1' to	En	nable	e in	iter	rup	ot fo	or S	USF	PEN	IDE) ev	en	t							
											S	ee E	VENT	s_s	SUSF	EΝ	IDE	D															
			Set	1							Е	nab	le																				
			Disabled	0							R	ead	: Disa	ble	d																		
			Enabled	1							R	ead	: Enak	oled	ł																		

49.8.3 INTENCLR

Address offset: 0x308 Disable interrupt



Bit	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F E D C B A
Res	set 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW STOPPED			Write '1' to Disable interrupt for STOPPED event
				See EVENTS_STOPPED
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW RXDREADY			Write '1' to Disable interrupt for RXDREADY event
				See EVENTS_RXDREADY
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW TXDSENT			Write '1' to Disable interrupt for TXDSENT event
				See EVENTS_TXDSENT
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW ERROR			Write '1' to Disable interrupt for ERROR event
				See EVENTS_ERROR
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Ε	RW BB			Write '1' to Disable interrupt for BB event
				See EVENTS_BB
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW SUSPENDED			Write '1' to Disable interrupt for SUSPENDED event
				See EVENTS_SUSPENDED
		Clear	1	_ Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

49.8.4 ERRORSRC

Address offset: 0x4C4

Error source

	numbe	er		31	30 2	9 2	28 2	27 2	26 2	5 2	24 23	22	21 20) 1:	9 18	3 17	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
ld Res	et 0x0	0000000		0	0 ()	0 (0	0 0) (0 0	0	0 0	O	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		3 A 0 0
Id	RW	Field	Value Id	Va	lue						De	scri	ption																			
Α	RW	OVERRUN									Ov	erru	ın err	or																		
													byte re fro							•				-			by					
			NotPresent	0							Rea	ad: ı	no ov	err	un	осс	ure	d														
			Present	1							Rea	ad: d	overr	un	осс	ure	d															
			Clear	1							Wr	rite:	clear	er	ror	on v	writ	ing	'1'													
В	RW	ANACK									NA	CK r	receiv	/ed	aft	er s	end	ling	the	e ad	ldre	ess (wri	te '	1' tc	clo	ear))				
			NotPresent	0							Rea	ad: e	error	no	t pr	ese	nt															
			Present	1							Rea	ad: e	error	pre	eser	nt																
			Clear	1							Wr	rite:	clear	er	ror	on v	writ	ing	'1'													
С	RW	DNACK									NA	CK r	receiv	/ed	aft	er s	end	ling	ac	lata	by	te (writ	e '1	' to	cle	ear)					
			NotPresent	0							Rea	ad:	error	no	t pr	ese	nt															



Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			СВА
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
	Present	1	Read: error present
	Clear	1	Write: clear error on writing '1'

49.8.5 ENABLE

Address offset: 0x500

Enable TWI

Bit r	numbe	r		33	1 30	29	28	3 27	7 26	5 25	5 24	1 23	22	21	20	19	18	17	16	15	14	13	3 12	2 11	. 10	9	8	7	6	5	4	3 2	2 1	. 0
Id																																A A	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0
Id	RW	Field	Value Id	V	alue	•						De	scr	ipti	on																			
Α	RW	ENABLE										En	abl	e o	dis	abl	e T	WI																
			Disabled	0								Di	sab	le T	WI																			
			Enabled	5								En	abl	e T	ΝI																			

49.8.6 PSELSCL

Address offset: 0x508
Pin select for SCL

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21 :	20 1	19 1	.8 1	7 16	15	14	13	12 :	11 10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A .	4 <i>A</i>	A	Α	Α	Α	Α	ДД	Α	Α	Α	Α	Α	Α	A A	\ A	A A
Res	et Oxl	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1 1	1	1	1	1	1	1	1 :	L 1	1
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																	
Α	RW	PSELSCL		[0.	31							Pin	nu	mbe	er co	onfi	gura	itio	n for	٠TW	/I SC	L si	gnal									
			Disconnected	0x	FFF	FFF	FF					Dis	con	nec	t																	

49.8.7 PSELSDA

Address offset: 0x50C Pin select for SDA

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A	
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value	Description
A RW PSELSDA		[031]	Pin number configuration for TWI SDA signal
	Disconnected	0xFFFFFFF	Disconnect

49.8.8 RXD

Address offset: 0x518

RXD register

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A R RXD			RXD register		

49.8.9 TXD

Address offset: 0x51C

TXD register



Bit number 31 30 29 28 27 26 25 24 2	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	$A \; A \; $
Reset 0x00000000 0 0 0 0 0 0 0 0 0 0 0	$ \begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0$
Id RW Field Value Id Value D	Description
A RW TXD	TXD register

49.8.10 FREQUENCY

Address offset: 0x524

TWI frequency

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23 2	2 2	1 2	0 19	18	17	16	15	14	13	12 1	.1 1	0 9	9 8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α .	A A	A /	A A	Α	Α	Α	Α	Α	Α	A	4 Α	Δ Α	4 4	A	A	Α	Α	Α	Α	А А
Res	et 0x0	4000000		0	0	0	0	0	1	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 () (0 (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue	!						Des	crip	tior	1																	
Α	RW	FREQUENCY										TWI	ma	stei	r clo	ck f	req	uen	су													
			K100	0x	019	800	000					100	kbp	S																		
			K250	0x	040	0000	000					250	kbp	S																		

49.8.11 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

Bit nu	mber		31 3	0 29	28 2	7 26	25	24	23 2	2 21	L 20	19	18	17 1	16 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4 3	2	1	0
Id																								Α	Α	A A	A	Α	Α
Reset	0x00000000		0	0	0 0	0 0	0	0	0 (0 0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0 0	0	0	0
ld I	RW Field	Value Id	Valu	e					Desc	ript	ion																		
Δ	RW ADDRESS								hhΔ	ress	IISE	d in	the	T\//	l tra	nsf	er												

49.9 Electrical specification

49.9.1 TWI interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWI}	Bit rates for TWI ⁴¹	100		400	kbps
I _{TWI,100kbps}	Run current for TWI, 100 kbps		50		μΑ
I _{TWI,400kbps}	Run current for TWI, 400 kbps		50		μΑ
t _{TWI,START,LP}	Time from STARTRX/STARTTX task to transmission started, Low		t _{TWI,STAI}	RT,C	μs
	power mode		+		
			t _{START_H}	FIN	
t _{TWI,START,CL}	Time from STARTRX/STARTTX task to transmission started,		1.5		μs
	Constant latency mode				

49.9.2 Two Wire Interface (TWI) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWI,SCL,100kbps}	SCL clock frequency, 100 kbps		100		kHz
f _{TWI,SCL,250kbps}	SCL clock frequency, 250 kbps		250		kHz
f _{TWI,SCL,400kbps}	SCL clock frequency, 400 kbps		400		kHz
t _{TWI,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t _{TWI,HD_DAT}	Data hold time after negative edge on SCL – all modes	500			ns
t _{TWI,HD_STA,100kbps}	TWI master hold time for START and repeated START condition,	10000			ns
	100 kbps				

Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Symbol	Description	Min.	Тур.	Max.	Units
t _{TWI,HD_STA,250kbps}	TWI master hold time for START and repeated START condition,	4000			ns
	250kbps				
t _{TWI,HD_STA,400kbps}	TWI master hold time for START and repeated START condition,	2500			ns
	400 kbps				
$t_{TWI,SU_STO,100kbps}$	TWI master setup time from SCL high to STOP condition, 100	5000			ns
	kbps				
$t_{TWI,SU_STO,250kbps}$	TWI master setup time from SCL high to STOP condition, 250	2000			ns
	kbps				
$t_{TWI,SU_STO,400kbps}$	TWI master setup time from SCL high to STOP condition, 400	1250			ns
	kbps				
t _{TWI,BUF,100kbps}	TWI master bus free time between STOP and START conditions,	5800			ns
	100 kbps				
t _{TWI,BUF,250kbps}	TWI master bus free time between STOP and START conditions,	2700			ns
	250 kbps				
t _{TWI,BUF,400kbps}	TWI master bus free time between STOP and START conditions,	2100			ns
	400 kbps				

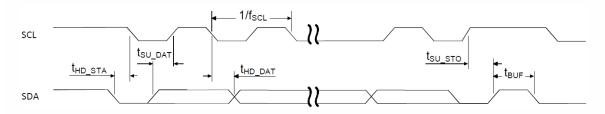


Figure 159: TWI timing diagram, 1 byte transaction



50 UART — Universal asynchronous receiver/ transmitter

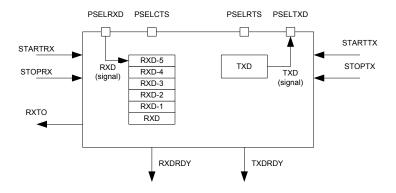


Figure 160: UART configuration

50.1 Functional description

Listed here are the main features of UART.

The UART implements support for the following features:

- Full-duplex operation
- · Automatic flow control
- Parity checking and generation for the 9th data bit

As illustrated in *Figure 160: UART configuration* on page 532, the UART uses the TXD and RXD registers directly to transmit and receive data. The UART uses one stop bit.

50.2 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UART are mapped to physical pins according to the configuration specified in the PSELRXD, PSELCTS, PSELRTS, and PSELTXD registers respectively.

If a value of 0xFFFFFFFF is specified in any of these registers, the associated UART signal will not be connected to any physical pin. The PSELRXD, PSELCTS, PSELRTS, and PSELTXD registers and their configurations are only used as long as the UART is enabled, and retained only for the duration the device is in ON mode. PSELRXD, PSELCTS, PSELRTS and PSELTXD must only be configured when the UART is disabled.

To secure correct signal levels on the pins by the UART when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Pin configuration* on page 532.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 127: GPIO configuration

UART pin	Direction		Output value	
RXD	2	Input	•	Not applicable
CTS		Input	Ī	Not applicable
RTS		Output		1
TXD		Output		1



50.3 Shared resources

The UART shares registers and other resources with other peripherals that have the same ID as the UART.

Therefore, you must disable all peripherals that have the same ID as the UART before the UART can be configured and used. Disabling a peripheral that has the same ID as the UART will not reset any of the registers that are shared with the UART. It is therefore important to configure all relevant UART registers explicitly to ensure that it operates correctly.

See the Instantiation table in *Instantiation* on page 24 for details on peripherals and their IDs.

50.4 Transmission

A UART transmission sequence is started by triggering the STARTTX task.

Bytes are transmitted by writing to the TXD register. When a byte has been successfully transmitted the UART will generate a TXDRDY event after which a new byte can be written to the TXD register. A UART transmission sequence is stopped immediately by triggering the STOPTX task.

If flow control is enabled a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in *Figure 161: UART transmission* on page 533. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended. For more information, see *Suspending the UART* on page 534.

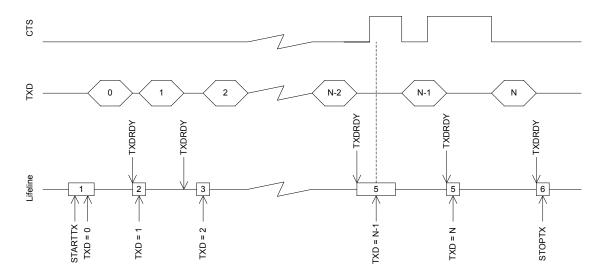


Figure 161: UART transmission

50.5 Reception

A UART reception sequence is started by triggering the STARTRX task.

The UART receiver chain implements a FIFO capable of storing six incoming RXD bytes before data is overwritten. Bytes are extracted from this FIFO by reading the RXD register. When a byte is extracted from the FIFO a new byte pending in the FIFO will be moved to the RXD register. The UART will generate an RXDRDY event every time a new byte is moved to the RXD register.

When flow control is enabled, the UART will deactivate the RTS signal when there is only space for four more bytes in the receiver FIFO. The counterpart transmitter is therefore able to send up to four bytes after the RTS signal is deactivated before data is being overwritten. To prevent overwriting data in the FIFO, the counterpart UART transmitter must therefore make sure to stop transmitting data within four bytes after the RTS line is deactivated.



The RTS signal will first be activated again when the FIFO has been emptied, that is, when all bytes in the FIFO have been read by the CPU, see *Figure 162: UART reception* on page 534.

The RTS signal will also be deactivated when the receiver is stopped through the STOPRX task as illustrated in *Figure 162: UART reception* on page 534. The UART is able to receive four to five additional bytes if they are sent in succession immediately after the RTS signal has been deactivated. This is possible because the UART is, even after the STOPRX task is triggered, able to receive bytes for an extended period of time dependent on the configured baud rate. The UART will generate a receiver timeout event (RXTO) when this period has elapsed.

To prevent loss of incoming data the RXD register must only be read one time following every RXDRDY event.

To secure that the CPU can detect all incoming RXDRDY events through the RXDRDY event register, the RXDRDY event register must be cleared before the RXD register is read. The reason for this is that the UART is allowed to write a new byte to the RXD register, and therefore can also generate a new event, immediately after the RXD register is read (emptied) by the CPU.

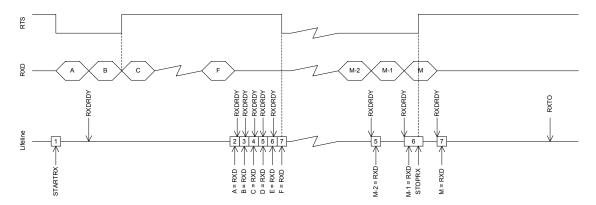


Figure 162: UART reception

As indicated in occurrence 2 in the figure, the RXDRDY event associated with byte B is generated first after byte A has been extracted from RXD.

50.6 Suspending the UART

The UART can be suspended by triggering the SUSPEND task.

SUSPEND will affect both the UART receiver and the UART transmitter, i.e. the transmitter will stop transmitting and the receiver will stop receiving. UART transmission and reception can be resumed, after being suspended, by triggering STARTTX and STARTRX respectively.

Following a SUSPEND task, an ongoing TXD byte transmission will be completed before the UART is suspended.

When the SUSPEND task is triggered, the UART receiver will behave in the same way as it does when the STOPRX task is triggered.

50.7 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.



50.8 Using the UART without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

50.9 Parity configuration

When parity is enabled, the parity will be generated automatically from the even parity of TXD and RXD for transmission and reception respectively.

50.10 Registers

Table 128: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40002000	UART	UART0	Universal Asynchronous Receiver/		Deprecated
			Transmitter		

Table 129: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS_STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_SUSPEND	0x01C	Suspend UART
EVENTS_CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_RXDRDY	0x108	Data received in RXD
EVENTS_TXDRDY	0x11C	Data sent from TXD
EVENTS_ERROR	0x124	Error detected
EVENTS_RXTO	0x144	Receiver timeout
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x480	Error source
ENABLE	0x500	Enable UART
PSELRTS	0x508	Pin select for RTS
PSELTXD	0x50C	Pin select for TXD
PSELCTS	0x510	Pin select for CTS
PSELRXD	0x514	Pin select for RXD
RXD	0x518	RXD register
TXD	0x51C	TXD register
BAUDRATE	0x524	Baud rate
CONFIG	0x56C	Configuration of parity and hardware flow control

50.10.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number	31 3	30 29 28 27 26 25 24	23 22 21 20 19 18 17 1	.6 15 14 13 12	11 10 9 8 7	6 5 4 3 2 1 0
Id						ВА
Reset 0x00000000	0	0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0	0 0 0 0 0 0
Id RW Field V	/alue Id Valu		Description			

A RW CTS_STARTRX

Shortcut between CTS event and STARTRX task



Bit	numb	er		31	L 30	29	28 2	27 2	26 2	5 2	4 2	3 22	2 21	20	19	18	17 1	L6 1	15 1	4 1	3 1	2 1:	10	9	8	7	6	5	4	3 2	2 1	0
Id																													В	4		
Res	et 0x(0000000		0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	alue						D	esci	ripti	on																		
											S	ee E	VEN	VTS_	CTS	an	d T/	1 <i>5K</i> .	s_s	TAR	TR)	(
			Disabled	0							D	isab	le s	hor	tcut																	
			Enabled	1							E	nab	le sł	nort	cut																	
В	RW	NCTS_STOPRX									S	hort	cut	bet	wee	n N	ICTS	ev	ent	and	ST	OPF	X ta	sk								
											S	ee E	VEN	NTS_	NC	TS a	nd	TAS	KS_	STC	PR.	X										
			Disabled	0							D	isab	le s	hor	tcut																	
			Enabled	1							Е	nab	le sh	nort	cut																	

50.10.2 INTENSET

Address offset: 0x304

Enable interrupt

		у интоггарт																															
Bit	numb	er		31	L 30	29	28 2	27 2	26 2	5 24	4 2	23 :	22 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4 3	3 2	1	0
Id																	F								Ε		D				C	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 0	0) (0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	alue						D)es	scripti	on																			
Α	RW	CTS									٧	۷ri	ite '1'	to E	Enab	le i	inte	rrı	ıpt	for	CTS	ev	ent										
											S	ee	e EVEN	ITS_	CTS																		
			Set	1							Ε	na	able																				
			Disabled	0							R	Rea	ad: Dis	abl	ed																		
			Enabled	1							R	Rea	ad: Ena	able	ed																		
В	RW	NCTS									٧	۷ri	ite '1'	to E	Enab	le i	inte	rru	ıpt	for	NCT	S e	ver	nt									
											S	ee	e EVEN	ITS	NC	TS																	
			Set	1									able	-																			
			Disabled	0							R	Rea	ad: Dis	abl	ed																		
			Enabled	1							R	Rea	ad: Ena	able	ed																		
С	RW	RXDRDY									٧	۷ri	ite '1'	to E	nab	le i	inte	rru	ıpt	for	RXC	RD	Y e	ven	t								
											S	iee	e EVEN	ITS_	RXL	ORE	ΟY																
			Set	1									able																				
			Disabled	0							R	Rea	ad: Dis	abl	ed																		
			Enabled	1							R	Rea	ad: Ena	able	ed																		
D	RW	TXDRDY									٧	۷ri	ite '1'	to E	Enab	le i	inte	rru	ıpt	for	TXD	RD	Y e	ven	t								
											S	ee	e EVEN	ITS_	TXL	DRE	ΟY																
			Set	1							Ε	na	able																				
			Disabled	0							R	Rea	ad: Dis	abl	ed																		
			Enabled	1							R	Rea	ad: Ena	able	ed																		
Ε	RW	ERROR									٧	۷ri	ite '1'	to E	Enab	le i	inte	rru	ıpt	for	ERR	OR	ev	ent									
											S	iee	e EVEN	ITS_	ERF	ROF	?																
			Set	1									able																				
			Disabled	0							R	Rea	ad: Dis	abl	ed																		
			Enabled	1							R	Rea	ad: Ena	able	ed																		
F	RW	RXTO									٧	۷ri	ite '1'	to E	Enab	le i	inte	rru	ıpt	for	RXT	0 6	evei	nt									
											S	ee	e EVEN	ITS	RXT	0																	
			Set	1									able																				
			Disabled	0							R	Rea	ad: Dis	abl	ed																		
			Enabled	1							R	Rea	ad: Ena	able	ed																		

50.10.3 INTENCLR

Address offset: 0x308 Disable interrupt



Bit	numbe	er		31	30	29	28	27 2	6 2	25 2	4 2	23	22 2	21	20	19	1	3 17	1	6	15	14	13	12	11	10	9	8	3 7	6	5 5	5 4	4	3 :	2	1 (
Id																		F									Ε		D					(2 1	ВА
Res	et 0x0	0000000		0	0	0	0	0 () (0 0) (0	0	0	0	0	0	0	()	0	0	0	0	0	0	0	(0	() () (0	0 () (0 (
Id	RW	Field	Value Id	Val	ue						0	Des	scrip	tic	n																					
Α	RW	CTS									٧	۸r	ite '1	1' t	о [Disa	ıbl	e in	ter	rru	pt 1	for	СТ	S e	ver	nt										
											S	See	e EVE	EN	TS_	СТ	S																			
			Clear	1								Dis	able																							
			Disabled	0							F	Rea	ad: D)isa	ble	ed																				
			Enabled	1							F	Rea	ad: E	na	ble	d																				
В	RW	NCTS									٧	۸r	ite '1	1' t	0 [Disa	bl	e in	ter	rru	pt i	or	NC	TS	ev	ent										
											S	See	e <i>EVE</i>	EN:	TS_	NC	TS																			
			Clear	1							0	Dis	able																							
			Disabled	0							F	Rea	ad: D)isa	ble	ed																				
			Enabled	1							F	Rea	ad: E	na	ble	d																				
С	RW	RXDRDY									٧	۸r	ite '1	1' t	о [Disa	bl	e in	ter	rru	pt 1	or	RX	DR	DY	eve	ent									
											S	See	e EVE	EN	TS_	RX	DF	DY																		
			Clear	1									able																							
			Disabled	0							F	Rea	ad: D)isa	ble	ed																				
			Enabled	1							F	Rea	ad: E	na	ble	d																				
D	RW	TXDRDY									٧	۸r	ite '1	1' t	о [Disa	bl	e in	ter	rru	pt 1	for	ΤX	DRI	DY	eve	ent									
											S	See	e <i>EVE</i>	EN:	TS_	ТX	DF	DY																		
			Clear	1							0	Dis	able																							
			Disabled	0							F	Rea	ad: D)isa	ble	ed																				
			Enabled	1							F	Rea	ad: E	na	ble	d																				
Ε	RW	ERROR									٧	۸r	ite '1	1' t	о [Disa	bl	e in	ter	rru	pt 1	for	ER	RO	R e	ver	nt									
											S	See	e EVE	EN	TS_	ER	RC)R																		
			Clear	1								Dis	able																							
			Disabled	0							F	Rea	ad: D)isa	ble	ed																				
			Enabled	1							F	Rea	ad: E	na	ble	d																				
F	RW	RXTO									٧	۸r	ite '1	1' t	0 [Disa	bl	e in	ter	rru	pt i	or	RX	то	ev	ent										
											S	See	e <i>EVE</i>	EN:	TS_	RX	TC)																		
			Clear	1							0	Dis	able																							
			Disabled	0							F	Rea	ad: D)isa	ble	ed																				
			Enabled	1							F	Rea	ad: E	na	ble	d																				

50.10.4 ERRORSRC

Address offset: 0x480

Error source

Bitı	numbe	er		31	30 :	29	28 2	27 :	26 2	25 2	24 :	23 22	2 21	20	19	18	17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																														D (В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	ue						- 1	Desc	ripti	on																		
Α	RW	OVERRUN									(Over	run	erro	or																	
											,	A sta	rt bi	t is	rece	eive	ed v	vhil	e tł	ne p	revi	ous	dat	a sti	II lie	es ir	n RX	D.				
											((Prev	ious	da	ta is	s los	st.)															
			NotPresent	0							ı	Read	: err	or r	not	pre	sen	t														
			Present	1							1	Read	: err	or p	ores	ent	t															
В	RW	PARITY									-	Parit	y err	or																		
												A cha	aract	er v	with	n ha	nd n	arit	v is	rec	eive	i he	f HV	V na	ritv	che	-ck	ic				
															••••		iu p	uiii	yı			.u, i		• pu	,	Cit	CICI	.5				
											(enab	led.																			
			NotPresent	0							ı	Read	: err	or r	not	pre	sen	t														
			Present	1							-	Read	: err	or p	ores	ent	t															
С	RW	FRAMING									-	Fram	ing	erro	or o	ccu	rred	t														



Bit number		31	30	29	28	27	26	25	24	23 2	22	21	20	19	18	17	16	5 1	5 1	4 1	3 1	2 1	.1 1	LO	9	8	7	6	5 4	3	2	1	0
Id																														D	С	В	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) () (0 () (0	0	0	0	0	0	0 (0	0	0	0
Id RW Field	Value Id	Va	lue							Des	cri	pti	on																				
										A va	alic	d st	ор I	bit i	is n	ot	det	ect	ed	on	the	se	ria	da	ta	nρι	ıt a	fter	all				
										bits	in	a c	har	act	er l	hav	e b	ee	n re	ece	ive	d.											
	NotPresent	0								Rea	ıd:	err	or r	not	pre	ese	nt																
	Present	1								Rea	ıd:	err	or p	ores	sen	t																	
D RW BREAK										Brea	ak	cor	ndit	ion																			
										The	se	rial	l da	ıta i	npı	ut i	s '0	' fc	or lo	ong	er t	haı	n th	ne I	eng	gth o	of a	da	ta				
										fran	ne	. (T	he (dat	a fr	am	ie le	eng	th	is 1	.0 b	its	wit	hoı	ut p	arit	y b	it, a	ınd				
										11 k	bits	s wi	th	par	ity	bit	.).																
	NotPresent	0								Rea	ıd:	err	or r	not	pre	ese	nt																
	Present	1								Rea	ıd:	err	or p	ores	sen	t																	

50.10.5 ENABLE

Address offset: 0x500

Enable UART

Bit nu	umbe	r		33	1 30	29	28	3 2	7 20	6 2	5 2	4 2	2 2	22 2	21 :	20	19	18	17	16	15	14	13	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																																	Α	Α	А А
Rese	t 0x0	000000		0	0	0	0	0	0) (0 0) (0 (0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	9						C)es	crip	tio	n																			
Α	RW	ENABLE										Е	nal	ble	or	disa	able	e U	AR	Г															
			Disabled	0								C	Disa	ble	UA	ART																			
			Enabled	4								Е	nal	ble	UA	RT																			

50.10.6 PSELRTS

Address offset: 0x508 Pin select for RTS

Bit r	numbe	er		31	1 30	29	28	27	26	25	24	23	22 2	21 2	20 1	.9 1	.8 1	7 1	5 15	14	13	12	11 1	0 9	9 1	3 7	7 6	5 5	5 4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A	Δ ,	4 <i>A</i>	Α Α	Α	Α	Α	Α	Α /	A A	Δ,	4 /	A /	\ A	A	Α	Α	A A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	. 1	1	1	1	1	1 :	1 :	1 :	1 :	1 1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	alue	•						Des	crip	tio	n																	
Α	RW	PSELRTS		[0	31	.]						Pin	nun	nbe	er co	nfi	gura	itio	n fo	r UA	RT	RTS	sigr	ıal								
			Disconnected	0x	(FFF	FFF	FF					Dis	conr	nec	t																	

50.10.7 PSELTXD

Address offset: 0x50C

Pin select for TXD

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	L9 1	8 1	7 1	6 1	5 14	13	12	11	10	9	8 7	7 6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	A A	4 <i>A</i>	Α Δ	A A	Α	Α	Α	Α	Α	A A	4 Δ	A	Α	Α ,	Α,	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	1	1	1	1	1	1	1	1 1	L 1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																	
Α	RW	PSELTXD		[0.	.31]							Pin	nur	nbe	er co	onfi	gur	atio	n fo	or U	ART	ΤXΙ) sig	nal								
			Disconnected	0x	FFFI	FFI	FF					Dis	coni	nec	t																	

50.10.8 PSELCTS

Address offset: 0x510 Pin select for CTS



Bitı	numbe	er		31	L 30	29	28	27	26	25	24	23	22	21 :	20 1	19 1	l8 1	7 1	6 15	14	13	12	11 1	0 9	9 8	3 7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A .	A A	\ A	A	Α	Α	Α	A	A /	۱ ۸	A A	A	Α	Α	Α	Α	АА
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	۱ 1	. 1	1	1	1	1 1	L 1	ι :	l 1	. 1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	alue							De	scri	ptio	n																	
Α	RW	PSELCTS		[0	31]						Pin	nuı	mbe	er co	onfi	gura	atio	n fo	r U/	ART	CTS	sign	al								
			Disconnected	0>	FFF	FFF	FF					Dis	con	nec	t																	

50.10.9 PSELRXD

Address offset: 0x514
Pin select for RXD

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	PSELRXD		[0.	31							Pin	nu	mb	er c	onf	igu	rati	on	for	UA	RT	RXE) się	gna	I								
			Disconnected	0x	FFF	FFF	FF					Dis	con	neo	t																			

50.10.10 RXD

Address offset: 0x518

RXD register

Bit	numb	er		31	1 30 2	9 2	28 27	7 26	25	24	23 :	22 2	21 2	0 1	9 1	3 17	' 16	15	14 :	13 1	2 11	10	9	8	7	6	5	4 3	2	1	0
Id																									Α	Α	A	A A	A	Α	Α
Re	set 0x	00000000		0	0	0	0 0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	alue						Des	crip	tio	n																	
Α	R	RXD									RX (data	red	ceiv	ed i	n pr	evic	us 1	tran	sfer	s, do	uble	e bu	ffer	ed						

50.10.11 TXD

Address offset: 0x51C

TXD register

Bit r	umbe	er		31	L 30	29	28 2	7 26	25	24	23	22	21 2	20 :	19 1	18 :	17 1	.6 1	.5 1	4 13	12	11	10	9 :	8 7	' 6	5	4	3	2	1 0
Id																									A	Α	A	Α	Α	Α.	А А
Res	t 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0 (0 0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue						Des	scri	otio	n																	
Α	W	TXD									ТΧ	data	a to	be	trai	nsf	erre	d													

50.10.12 BAUDRATE

Address offset: 0x524

Baud rate

Rit r	numbe	or		31 30 29 28 27 2	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id	idilibe	-1			A A A A A A A A A A A A A A A A A A A
Res	et 0x0	4000000		0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	BAUDRATE			Baud rate
			Baud1200	0x0004F000	1200 baud (actual rate: 1205)
			Baud2400	0x0009D000	2400 baud (actual rate: 2396)
			Baud4800	0x0013B000	4800 baud (actual rate: 4808)
			Baud9600	0x00275000	9600 baud (actual rate: 9598)
			Baud14400	0x003B0000	14400 baud (actual rate: 14414)
			Baud19200	0x004EA000	19200 baud (actual rate: 19208)
			Baud28800	0x0075F000	28800 baud (actual rate: 28829)
			Baud38400	0x009D5000	38400 baud (actual rate: 38462)
			Baud57600	0x00EBF000	57600 baud (actual rate: 57762)



Bit number	31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	$A \ A \ A \ A \ A \ A \ A \ A$	A A A A A A A A A A A A A A A A A A A
Reset 0x04000000	0 0 0 0 0 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
Baud76800	0x013A9000	76800 baud (actual rate: 76923)
Baud115200	0x01D7E000	115200 baud (actual rate: 115942)
Baud230400	0x03AFB000	230400 baud (actual rate: 231884)
Baud250000	0x04000000	250000 baud
Baud460800	0x075F7000	460800 baud (actual rate: 470588)
Baud921600	0x0EBED000	921600 baud (actual rate: 941176)
Baud1M	0x10000000	1Mega baud

50.10.13 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

Bit	numbe	er		31	30 2	29	28 2	27 2	26 2	25 2	24 2	23 2	2 2	21 2	0 1	9 1	8 1	7 1	5 1!	5 14	13	12	11	10	9	8	7	6 !	5 4	4 3	3 2	1	0
Id																															3 B	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 0) (0 () (0	0	0	0	0	0	0	0	0)	0 (0 (0 (0 (0	0
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	tion	ı																		
Α	RW	HWFC									ŀ	Haro	dwa	are f	low	v со	ntr	ol															
			Disabled	0							[Disa	ble	d																			
			Enabled	1								Enal	oled	b																			
В	RW	PARITY									ı	Pari	ty																				
			Excluded	0x0)						1	Excl	ude	par	ity	bit																	
			Included	0x	7						ı	nclu	ıde	par	ity	bit																	

50.11 Electrical specification

50.11.1 UART electrical specification

Symbol	Description	Min.	Тур.	Max.	Units
f _{UART}	Baud rate for UART ⁴² .			1000	kbps
I _{UART1M}	Run current at max baud rate.		55		μΑ
I _{UART115k}	Run current at 115200 bps.		55		μΑ
I _{UART1k2}	Run current at 1200 bps.		55		μΑ
I _{UART,IDLE}	Idle current for UART		1		μΑ
t _{UART,CTSH}	CTS high time	1			μs
t _{UART,START,LP}	Time from STARTRX/STARTTX task to transmission started, low		t _{UART,STAR}	т	μs
	power mode		+		
			t _{START_HFI}	N	
t _{UART,START,CL}	Time from STARTRX/STARTTX task to transmission started,		1		μs
	constant latency mode				

Higher baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.



51 Mechanical specifications

The mechanical specifications for the packages show the dimensions in millimeters.

51.1 QFN48 6 x 6 mm package

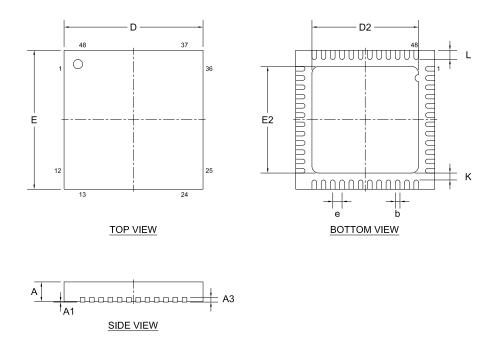


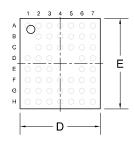
Figure 163: QFN48 6 x 6 mm package

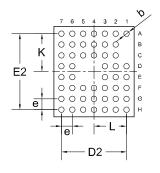
Table 130: QFN48 dimensions in millimeters

Package	Α	A1	А3	b	D, E	D2, E2	е	K	L	
	0.80	0.00		0.15		4.50		0.20	0.35	Min.
QFN48 (6x6)	0.85	0.02	0.2	0.20	6.0	4.60	0.4		0.40	Nom.
	0.90	0.05		0.25		4.70			0.45	Max.



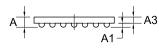
51.2 WLCSP package





TOP VIEW

BOTTOM VIEW



SIDE VIEW

Figure 164: WLCSP package

Table 131: WLCSP packet dimensions in millimeters

Package	Α	A1	А3	b	D	E	D2	E2	е	K	L	
	0.351	0.13		0.19								Min.
WLCSP (3.0 × 3.2)	0.375	0.15	0.225	0.20	2.956	3.226	2.4	2.8	0.4	1.4	1.2	Nom.
	0.399	0.17		0.25								Max.



52 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

52.1 IC marking

The nRF52832 IC package is marked like described below.

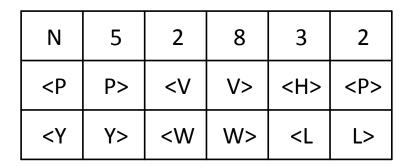


Figure 165: Package marking

52.2 Box labels

Here are the box labels used for the nRF52832.



Figure 166: Inner box label



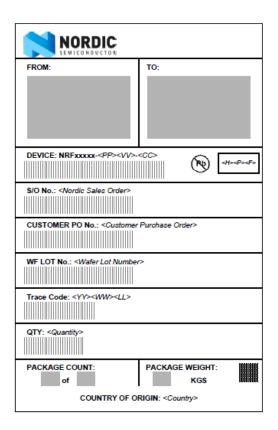


Figure 167: Outer box label

52.3 Order code

Here are the nRF52832 order codes and definitions.

Figure 168: Order code

Table 132: Abbreviations

Abbreviation	Definition and implemented codes
N52/nRF52	nRF52 Series product
832	Part code
<pp></pp>	Package variant code
<vv></vv>	Function variant code
<h><p><f></f></p></h>	Build code
	H - Hardware version code
	P - Production configuration code (production site, etc.)
<yy><ww><ll></ll></ww></yy>	F - Firmware version code (only visible on shipping container label) Tracking code
	YY - Year code
	WW - Assembly week number
<cc></cc>	LL - Wafer lot code Container code

52.4 Code ranges and values

Defined here are the nRF52832 code ranges and values.



Table 133: Package variant codes

<pp></pp>	Package	Size (mm)	Pin/Ball count	Pitch (mm)
QF	QFN	6 x 6	48	0.4
CI	WLCSP	3.0 x 3.2	50	0.4

Table 134: Function variant codes

<vv></vv>	Flash (kB)	RAM (kB)
AA	512	64
AB	256	32

Table 135: Hardware version codes

<h>></h>	Description
[A Z]	Hardware version/revision identifier (incremental)

Table 136: Production configuration codes

<p></p>	Description
[09]	Production device identifier (incremental)
[A Z]	Engineering device identifier (incremental)

Table 137: Production version codes

[AN, PZ] Version of preprogrammed firmware

Table 138: Year codes

<yy></yy>	Description
[1599]	Production year: 2015 to 2099

Table 139: Week codes

Table 140: Lot codes

<ll></ll>	Description	
[AA ZZ]	Wafer production lot identifier	

Table 141: Container codes

<cc></cc>	Description
R7	7" Reel
R	13" Reel
T	Tray

52.5 Product options

Defined here are the nRF52832 product options.

Table 142: nRF52832 order codes

Order code	Minimum ordering quantity (MOQ)	Comment
nRF52832-QFAA-R7	1000	Availability to be announced.
nRF52832-QFAA-R	3000	
nRF52832-QFAA-T	490	
nRF52832-CIAA-R7	1500	
nRF52832-CIAA-R	7000	
nRF52832-QFAB-R	3000	
nRF52832-QFAB-R7	1000	
nRF52832-QFAB-T	490	

Table 143: Development tools order code

Order code	Description
nRF52-DK	nRF52 Development Kit



53 Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from *Reference layout nRF52 Series*.

53.1 Schematic QFAA and QFAB QFN48 with internal LDO setup

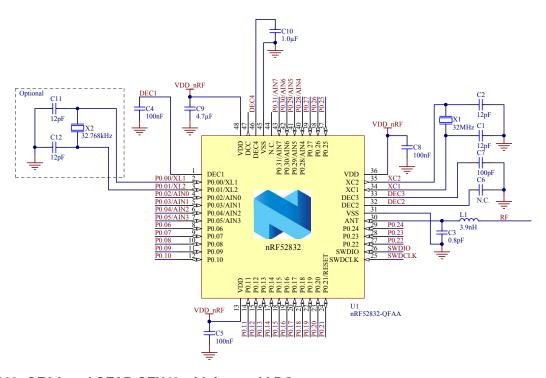


Figure 169: QFAA and QFAB QFN48 with internal LDO setup

Table 144: Bill of material for QFAA and QFAB QFN48 with internal LDO setup

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, ±5%	0402
C9	4.7 μF	Capacitor, X5R, ±10%	0603
C10	1.0 μF	Capacitor, X7R, ±10%	0603
L1	3.9 nH	High frequency chip inductor ±5%	0402
U1	nRF52832-QFAA	Multi-protocol Bluetooth low energy, ANT, and 2.4 GHz proprietary system on chip	QFN-48
	and nRF52832-QFAB		
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, total tol. ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, CI=9 pF, total tol. ±50 ppm	XTAL 3215



53.2 Schematic QFAA and QFAB QFN48 with DC/DC regulator setup

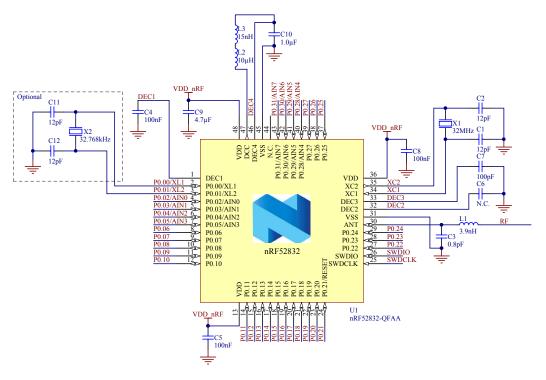


Figure 170: QFAA and QFAB QFN48 with DC/DC regulator setup

Table 145: Bill of material for QFAA and QFAB QFN48 with DC/DC regulator setup

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, ±5%	0402
C9	4.7 μF	Capacitor, X5R, ±10%	0603
C10	1.0 μF	Capacitor, X7R, ±10%	0603
L1	3.9 nH	High frequency chip inductor ±5%	0402
L2	10 μΗ	Chip inductor, IDC,min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52832-QFAA	Multi-protocol Bluetooth low energy, ANT, and 2.4 GHz proprietary system on chip	QFN-48
	and nRF52832-QFAB		
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, total tol. ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, CI=9 pF, total tol. ±50 ppm	XTAL_3215



53.3 Schematic QFAA and QFAB QFN48 with DC/DC regulator and NFC setup

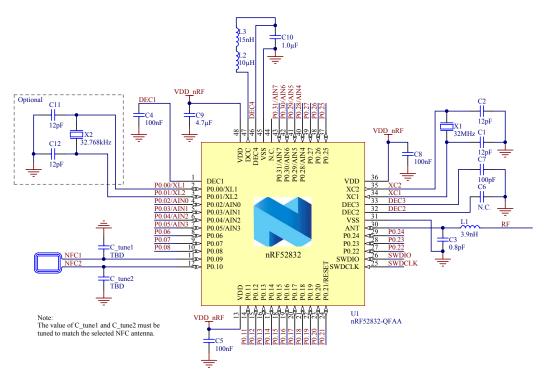


Figure 171: QFAA and QFAB QFN48 with DC/DC regulator and NFC setup

Table 146: Bill of material for QFAA and QFAB QFN48 with DC/DC converter and NFC setup

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, ±5%	0402
C9	4.7 μF	Capacitor, X5R, ±10%	0603
C10	1.0 μF	Capacitor, X7R, ±10%	0603
C _{tune1} , Ctune2	TBD pF	Capacitor, NPO, ±5%	0402
L1	3.9 nH	High frequency chip inductor ±5%	0402
L2	10 μΗ	Chip inductor, IDC,min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52832-QFAA	Multi-protocol Bluetooth low energy, ANT, and 2.4 GHz proprietary system on chip	QFN-48
	and nRF52832-QFAB		
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, CI=9 pF, ±50 ppm	XTAL_3215



53.4 Schematic CIAA WLCSP with internal LDO setup

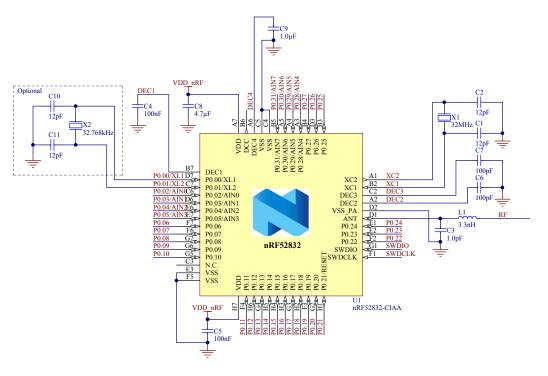


Figure 172: CIAA WLCSP with internal LDO setup

Table 147: Bill of material for CIAA WLCSP with internal LDO setup

Designator	Value	Description	Footprint
C1, C2, C10, C11	12 pF	Capacitor, NPO, ±2%	0201
C3	1.0 pF	Capacitor, NPO, ±5%	0201
C4, C5	100 nF	Capacitor, X7R, ±10%	0201
C6, C7	100 pF	Capacitor, NPO, ±5%	0201
C8	4.7 μF	Capacitor, X5R, ±10%	0603
C9	1.0 μF	Capacitor, X5R, ±5%	0402
L1	3.3 nH	High frequency chip inductor ±5%	0201
U1	nRF52832-CIAA	Multi-protocol Bluetooth low energy, ANT, and 2.4 GHz proprietary system on chip	WLCSP_C50
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, total tol. ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 2012, 32.768 kHz, CI=9 pF, ±50 ppm	XTAL_2012



53.5 Schematic CIAA WLCSP with DC/DC regulator setup

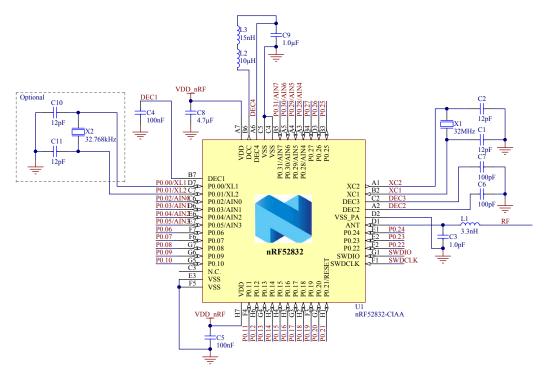


Figure 173: CIAA WLCSP with DC/DC regulator setup

Table 148: Bill of material for CIAA WLCSP with DC/DC regulator setup

Designator	Value	Description	Footprint
C1, C2, C10, C11	12 pF	Capacitor, NPO, ±2%	0201
C3	1.0 pF	Capacitor, NPO, ±5%	0201
C4, C5	100 nF	Capacitor, X7R, ±10%	0201
C6, C7	100 pF	Capacitor, NPO, ±5%	0201
C8	4.7 μF	Capacitor, X5R, ±10%	0603
C9	1.0 μF	Capacitor, X5R, ±5%	0402
L1	3.3 nH	High frequency chip inductor ±5%	0201
L2	10 μΗ	Chip inductor, IDC,min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52832-CIAA	Multi-protocol Bluetooth low energy, ANT, and 2.4 GHz proprietary system on chip	WLCSP_C50
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 2012, 32.768 kHz, CI=9 pF, ±50 ppm	XTAL 2012



53.6 Schematic CIAA WLCSP with DC/DC regulator and NFC setup

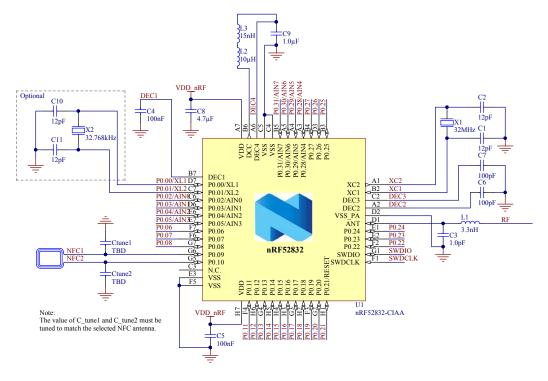


Figure 174: CIAA WLCSP with DC/DC regulator and NFC setup

For PCB reference layouts, see Reference layout nRF52 Series.

Table 149: Bill of material for CIAA WLCSP with DC/DC converter and NFC setup

Designator	Value	Description	Footprint
C1, C2, C10, C11	12 pF	Capacitor, NPO, ±2%	0201
C3	1.0 pF	Capacitor, NPO, ±5%	0201
C4, C5	100 nF	Capacitor, X7R, ±10%	0201
C6, C7	100 pF	Capacitor, NPO, ±5%	0201
C8	4.7 μF	Capacitor, X5R, ±10%	0603
C9	1.0 μF	Capacitor, X5R, ±5%	0402
C _{tune1} , C _{tune2}	TBD pF	Capacitor, NPO, ±5%	0201
L1	3.3 nH	High frequency chip inductor ±5%	0201
L2	10 μΗ	Chip inductor, IDC,min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52832-CIAA	Multi-protocol Bluetooth low energy, ANT, and 2.4 GHz proprietary system on chip	WLCSP_C50
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 2012, 32.768 kHz, CI=9 pF, ±50 ppm	XTAL_2012

53.7 PCB guidelines

A well-designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss in performance or functionality.

A qualified RF layout for the IC and its surrounding components, including matching networks, can be downloaded from *Reference layout nRF52 Series*.

To ensure optimal performance, it is essential that you follow the schematics and layout references closely. Especially in the case of the antenna matching circuitry (components between device pin ANT and the antenna), any changes to the layout can change the behavior, resulting in degradation of RF performance or a need to change component values. All the reference circuits are designed for use with a 50 ohm single end antenna.

A PCB with a minimum of two layers, including a ground plane, is recommended for optimal performance. On PCBs with more than two layers, put a keep-out area on the inner layers directly below the antenna



matching circuitry (components between device pin ANT and the antenna) to reduce the stray capacitances that influence RF performance.

A matching network is needed between the RF pin ANT and the antenna, to match the antenna impedance (normally 50 ohm) to the optimum RF load impedance for the chip. For optimum performance, the impedance for the matching network should be set as described in the recommended package reference circuitry in *Reference circuitry* on page 546 above.

The DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. See the schematics for recommended decoupling capacitor values. The supply voltage for the chip should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. A minimum of one via hole should be used for each VSS pin.

Fast switching digital signals should not be routed close to the crystal or the power supply lines. Capacitive loading of fast switching digital output lines should be minimized in order to avoid radio interference.

53.8 PCB layout example

The PCB layout shown below is a reference layout for the QFN package with internal LDO setup.

Important: Pay attention to how the capacitor C3 is grounded. It is not directly connected to the ground plane, but grounded via VSS pin 31. This is done to create additional filtering of harmonic components.

For all available reference layouts, see Reference layout nRF52 Series.

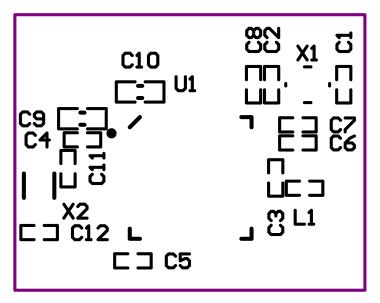


Figure 175: Top silk layer



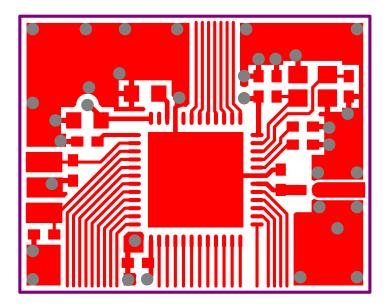


Figure 176: Top layer

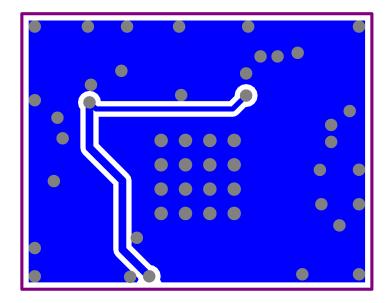


Figure 177: Bottom layer

Important: No components in bottom layer.



54 Liability disclaimer

Nordic Semiconductor ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic Semiconductor ASA does not assume any liability arising out of the application or use of any product or circuits described herein.

54.1 RoHS and REACH statement

Nordic Semiconductor products meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substances (RoHS) and the requirements of the REACH regulation (EC 1907/2006) on Registration, Evaluation, Authorization and Restriction of Chemicals.

The SVHC (Substances of Very High Concern) candidate list is continually being updated. Complete hazardous substance reports, material composition reports and latest version of Nordic's REACH statement can be found on our website.



54.2 Life support applications

Nordic Semiconductor products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury.

Nordic Semiconductor ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic Semiconductor ASA for any damages resulting from such improper use or sale.