nRF52832 Engineering B Errata

v1.3

Contents

Chapter 1
nRF52832 Engineering B Errata v1.3

This Errata document contains anomalies for the nRF52832 chip, revision Engineering B (QFAA-BA0, CHAA-AA0).

The document indicates which anomalies are fixed, inherited, or new compared to revision Engineering A.

Chapter 2
Change log

See the following list for an overview of changes from previous versions of this document.

Table 1: Change log

Version	Date	Change
nRF52832 Engineering B v1.3	28.09.2016	• Added: No. 108. "RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode"
nRF52832 Engineering B v1.2	05.07.2016	• Added: No. 84. "ISOURCE not functional" • Added: No. 86. "Triggering START task after offset calibration may write a sample to RAM" • Added: No. 87. "Unexpected wake from System ON Idle when using FPU" • Added: No. 88. "Increased current consumption when configured to pause in System ON idle" • Added: No. 89. "Static 400 µA current while using GPIOTE" • Added: No. 97. "High current consumption in System ON Idle mode"
nRF52832 Engineering B v1.1	17.02.2016	• Deleted: No. 53. "Using SCB.AIRCR.VECTRESET may get the chip into an undefined state" (not relevant) • Updated: No. 70. "Not able to wake CPU from System ON IDLE" • Updated: No. 73. "Event lost" • Updated: No. 78. "High current consumption when using timer STOP task only" • Added: No. 79. " A false EVENTS_FIELDDETECTED event occurs after the field is lost" • Added: No. 81. "PIN_CNF is not retained when in debug interface mode" • Added: No. 83. "STOPPED event occurs twice if the STOP task is triggered during a transaction"
nRF52832 Engineering B v1.0	21.01.2016	• Created separate document for IC revision Engineering B.
nRF52832-PAN v1.2	11.12.2015	• Added: No. 67. "Some events cannot be used with the PPI" • Added: No. 68. "EVENTS_HFCLKSTARTED can be generated before HFCLK is stable" • Added: No. 70. "Not able to wake CPU from System ON IDLE" • Added: No. 71. "RCOSC calibration" • Added: No. 72. "TASKS_ACTIVATE cannot be used with the PPI" • Added: No. 73. "Event lost" • Added: No. 74. "Started events fires prematurely" • Added: No. 75. "Increased current consumption" • Added: No. 76. "READY event is set sooner than it should" • Added: No. 77. "RC oscillator is not calibrated when first started"

Version	Date	Change
		• Added: No. 78. “High current consumption when using timer STOP task only”
nRF52832-PAN v1.1	09.10.2015	• Added: No. 12. “Reference ladder is not correctly calibrated” • Added: No. 15. “RAM[x].POWERSET/CLR read as zero” • Added: No. 20. “Register values are invalid” • Added: No. 30. “STOP Task and STOPPED Event are not functional” • Added: No. 36. “Some registers are not reset when expected” • Added: No. 31. “Calibration values are not correctly loaded from FICR at reset” • Added: No. 51. “Aligned stereo slave mode does not work” • Added: No. 53. “Using SCB.AIRCR.VECTRESET may get the chip into an undefined state” • Added: No. 54. “Wrong LRCK polarity in Aligned mode” • Added: No. 55. “RXPTRUPD and TXPTRUPD events asserted after STOP” • Added: No. 58. “SPIM clocks out an additional byte when RXD.MAXCNT = 1” • Added: No. 62. “Can draw current when not enabled” • Added: No. 63. “DC/DC does not automatically switch off in System ON IDLE” • Added: No. 64. “Only full bytes can be received or transmitted”

Chapter 3
New and inherited anomalies

The following anomalies are present in revision Engineering B of the nRF52832 chip.

Table 2: New and inherited anomalies

ID	Module	Description	New in Engineering B	Inherited from Engineering A
12	COMP	Reference ladder is not correctly calibrated		X
15	POWER	RAM[x].POWERSET/CLR read as zero		X
20	RTC	Register values are invalid		X
31	CLOCK	Calibration values are not correctly loaded from FICR at reset		X
36	CLOCK	Some registers are not reset when expected		X
51	I2S	Aligned stereo slave mode does not work	X	
54	I2S	Wrong LRCK polarity in Aligned mode	X	
55	I2S	RXPTRUPD and TXPTRUPD events asserted after STOP	X	
58	SPIM	An additional byte is clocked out when RXD.MAXCNT = 1		X
62	NFCT	Can draw current when not enabled	X	
63	POWER	DC/DC does not automatically switch off in System ON IDLE		X
64	NFCT	Only full bytes can be received or transmitted, but supports 4-bit frame transmit		X
67	NFCT,PPI	Some events cannot be used with the PPI		X
68	CLOCK	EVENTS_HFCLKSTARTED can be generated before HFCLK is stable		X
70	COMP	Not able to wake CPU from System ON IDLE		X
71	CLOCK	RCOSC calibration		X
72	NFCT,PPI	TASKS_ACTIVATE cannot be used with the PPI		X
73	TIMER	Event lost		X
74	SAADC	Started events fires prematurely		X
75	MWU	Increased current consumption	X	
76	LPCOMP	READY event is set sooner than it should	X	
77	CLOCK	RC oscillator is not calibrated when first started		X
78	TIMER	High current consumption when using timer STOP task only		X
79	NFCT	A false EVENTS_FIELDDETECTED event occurs after the field is lost	X	

ID	Module	Description	New in Engineering B	Inherited from Engineering A
81	GPIO	PIN_CNF is not retained when in debug interface mode	X	
83	TWIS	STOPPED event occurs twice if the STOP task is triggered during a transaction	X	
84	COMP	ISOURCE not functional		X
86	SAADC	Triggering START task after offset calibration may write a sample to RAM		X
87	CPU	Unexpected wake from System ON Idle when using FPU		X
88	WDT	Increased current consumption when configured to pause in System ON idle		X
89	TWI	Static 400 µA current while using GPIOTE	X	
97	GPIOTE	High current consumption in System ON Idle mode		X
108	RAM	RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode	X	

3.1 [12] COMP: Reference ladder is not correctly calibrated

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

COMP does not compare correctly.

Conditions

Always.

Consequences

COMP module is unusable.

Workaround

Execute the following code before enabling the COMP module:

```
*(volatile uint32_t *)0x40013540 = (*(volatile uint32_t *)0x10000324 &
 0x00001F00) >> 8;
```

3.2 [15] POWER: RAM[x].POWERSET/CLR read as zero

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

RAM[x].POWERSET and RAM[x].POWERCLR read as zero, even though the RAM is on.

Conditions

Always

Consequences

Not possible to read the RAM state using RAM[x].POWERSET and RAM[x].POWERCLR registers. Write works as it should.

Workaround

Use RAM[x].POWER to read the state of the RAM.

3.3 [20] RTC: Register values are invalid

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

RTC registers will not contain the correct/expected value if read.

Conditions

The RTC has been idle.

Consequences

RTC configuration cannot be determined by reading RTC registers.

Workaround

Execute the below code before you use RTC.

```
NRF_CLOCK->EVENTS_LFCLKSTARTED  = 0;
NRF_CLOCK->TASKS_LFCLKSTART     = 1;
while (NRF_CLOCK->EVENTS_LFCLKSTARTED == 0) {}
NRF_RTC0->TASKS_STOP = 0;
```

3.4 [31] CLOCK: Calibration values are not correctly loaded from FICR at reset

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

RCOSC32KICALLENGTH is initialized with the wrong FICR value.

Conditions

Always

Consequences

RCOSC32KICALLENGTH default value is wrong.

Workaround

Execute the following code after reset:

```
*(volatile uint32_t *)0x4000053C = ((*(volatile uint32_t *)0x10000244) &
0x0000E000) >> 13;
```

This code is already present in the latest system_nrf52.c file.

3.5 [36] CLOCK: Some registers are not reset when expected

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

After watchdog timeout reset, CPU lockup reset, soft reset, or pin reset, the following CLOCK peripheral registers are not reset: CLOCK->EVENTS_DONE, CLOCK->EVENTS_CTTO, CLOCK->CTIV

Conditions

After watchdog timeout reset, CPU Lockup reset, soft reset, and pin reset.

Consequences

Register reset values might be incorrect. It may cause undesired interrupts in case of enabling interrupts without clearing the DONE or CTTO events.

Workaround

Clear affected registers after reset. This workaround has already been added into system_nrf52.c file.

3.6 [51] I2S: Aligned stereo slave mode does not work

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

Symptoms

Sample values for the left channel are transmitted twice (for both channels within a frame), sample values for the right channel are lost.

Conditions

CONFIG.MODE = SLAVE, CONFIG.CHANNELS = STEREO, CONFIG.FORMAT = ALIGNED.

Consequences

Aligned format cannot be used for stereo transmission in Slave mode.

Workaround

None.

3.7 [54] I2S: Wrong LRCK polarity in Aligned mode

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

Symptoms

In Aligned mode, left and right samples are swapped.

Conditions

CONFIG.FORMAT = ALIGNED

Consequences

Left and right audio channels are swapped.

Workaround

Swap left and right samples in memory.

3.8 [55] I2S: RXPTRUPD and TXPTRUPD events asserted after STOP

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

Symptoms

The RXPTRUPD event is generated when the STOP task is triggered, even though reception (RX) is disabled. Similarly, the TXPTRUPD event is generated when the STOP task is triggered, even though transmission (TX) is disabled.

Conditions

A previous transfer has been performed with RX/TX enabled, respectively.

Consequences

The indication that RXTXD.MAXCNT words were received/transmitted is false.

Workaround

Ignore the RXPTRUPD and TXPTRUPD events after triggering the STOP task. Clear these events before starting the next transfer.

3.9 [58] SPIM: An additional byte is clocked out when RXD.MAXCNT = 1

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

SPIM clocks out additional byte.

Conditions

RXD.MAXCNT = 1

TXD.MAXCNT <= 1

Consequences

Additional byte is redundant.

Workaround

Use the SPI module (deprecated but still available) or use the following workaround with SPIM:

```
/**
 * @brief Work-around for transmitting 1 byte with SPIM.
 *
 * @param spim: The SPIM instance that is in use.
 * @param ppi_channel: An unused PPI channel that will be used by the
 workaround.
 * @param gpiote_channel: An unused GPIOTE channel that will be used by
 the workaround.
 *
 * @warning Must not be used when transmitting multiple bytes.
 * @warning After this workaround is used, the user must reset the PPI
 channel and the GPIOTE channel before attempting to transmit multiple
 bytes.
 */
void setup_workaround_for_ftpan_58(NRF_SPIM_Type * spim, uint32_t
 ppi_channel, uint32_t gpiote_channel)
{
    // Create an event when SCK toggles.
    NRF_GPIOTE->CONFIG[gpiote_channel] = (
        GPIOTE_CONFIG_MODE_Event <<
        GPIOTE_CONFIG_MODE_Pos
        ) | (
        spim->PSEL.SCK <<
        GPIOTE_CONFIG_PSEL_Pos
        ) | (
        GPIOTE_CONFIG_POLARITY_Toggle <<
        GPIOTE_CONFIG_POLARITY_Pos
        );

    // Stop the spim instance when SCK toggles.
    NRF_PPI->CH[ppi_channel].EEP = (uint32_t)&NRF_GPIOTE-
>EVENTS_IN[gpiote_channel];
    NRF_PPI->CH[ppi_channel].TEP = (uint32_t)&spim->TASKS_STOP;
    NRF_PPI->CHENSET = 1U << ppi_channel;

    // The spim instance cannot be stopped mid-byte, so it will finish
    // transmitting the first byte and then stop. Effectively ensuring
    // that only 1 byte is transmitted.
}
```

3.10 [62] NFCT: Can draw current when not enabled

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

Symptoms

Increased current consumption (>10 µA) in System OFF and System ON IDLE.

Conditions

NFCT is not enabled and supply voltage is above 2.5V.

Consequences

Current consumption in low power modes can be higher than specified.

Workaround

None

3.11 [63] POWER: DC/DC does not automatically switch off in System ON IDLE

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

The device will draw current periodically (in the mA range) when in System ON IDLE.

Conditions

DC/DC is enabled and in System ON IDLE.

Consequences

Average current consumption in idle mode is too high.

Workaround

None

3.12 [64] NFCT: Only full bytes can be received or transmitted, but supports 4-bit frame transmit

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

Data bits are not transmitted, or appear to not be received, if the Frame length is not a multiple of 8 bits (i.e. Frame includes data bits).

Conditions

Frame length is not a multiple of 8 bits (bytes only). Exception: 4-bit frame transmit supported.

Consequences

Partial bytes cannot be transferred:

- TXD.AMOUNT.TXDATABITS must be 0
- RXD.AMOUNT.RXDATABITS must be 0

Workaround

None

3.13 [67] NFCT,PPI: Some events cannot be used with the PPI

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

The following NFCT events do not trigger tasks when used with the PPI:

- EVENTS_AUTOCOLRESSTARTED
- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

Conditions

PPI is used to trigger peripheral tasks using the NFCT events.

Consequences

The PPI cannot be used to trigger tasks using the following NFCT events:

- EVENTS_AUTOCOLRESSTARTED
- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

Workaround

The EVENTS_AUTOCOLRESSTARTED cannot be used with the PPI.

Subtract an offset of 0x04 while configuring the PPI event end points for the following NFCT events:

- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

Examples:

```
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_COLLISION) - 0x04;
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_SELECTED) - 0x04;
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_STARTED) - 0x04;
```

3.14 [68] CLOCK: EVENTS_HFCLKSTARTED can be generated before HFCLK is stable

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

EVENTS_HFCLKSTARTED may come before HFXO is started.

Conditions

When using a 32 MHz crystal with start-up longer than 400 µs.

Consequences

Performance of radio and peripheral requiring HFXO will be degraded until the crystal is stable.

Workaround

32 MHz crystal oscillator startup time must be verified by the user. If the worst-case startup time is shorter than 400 µs, no workaround is required. If the startup time can be longer than 400 µs, the software must ensure, using a timer, that the crystal has had enough time to start up before using peripherals that require the HFXO. The Radio requires the HFXO to be stable before use. The ADC, TIMERs, and TEMP sensor for example can use the HFXO as a reference for improved accuracy.

3.15 [70] COMP: Not able to wake CPU from System ON IDLE

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

COMP event not able to wake CPU form System ON IDLE.

Conditions

Always

Consequences

CPU will not wake from System ON IDLE.

Workaround

Use the following workaround to prevent some core peripheral services from going to the lowest power mode. This will cause an increase of around 20 µA current in SYSTEM ON IDLE.

```
if (*(volatile uint32_t *)0x4006EC00 == 0)
{ *(volatile uint32_t *)0x4006EC00 = 0x9375; }
*(volatile unit32_t *) 0x4006EC14 = 0xC0;
```

To turn off this workaround (to save current):

```
if (*(volatile uint32_t *)0x4006EC00 == 0)
{ *(volatile uint32_t *)0x4006EC00 = 0x9375; }
*(volatile unit32_t *) 0x4006EC14 = 0x0;
```

3.16 [71] CLOCK: RCOSC calibration

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

RCOSC only calibrates on every second calibration request.

Conditions

Always

Consequences

RCOSC not properly calibrated.

Workaround

Trigger TASKS_CAL, wait for EVENTS_DONE. Trigger TASKS_CAL again, wait for EVENTS_DONE each time the RCOSC is to be calibrated.

3.17 [72] NFCT,PPI: TASKS_ACTIVATE cannot be used with the PPI

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

The NFCT peripheral does not get activated when the PPI is configured to trigger TASKS_ACTIVATE on any event.

Conditions

Always

Consequences

The TASKS_ACTIVATE cannot be used with the PPI.

Workaround

None

3.18 [73] TIMER: Event lost

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

If an event from the peripherals listed below comes within 125 ns of the CPU and all other peripherals going to IDLE, the event flag may not be set and the event would be lost. The effected peripherals are RTC, LPCOMP,

GPIO, and WDT. These peripherals are commonly used to wake the system from a low power IDLE state. Loss of events would prevent the wakeup from occurring.

Conditions

Always

Consequences

Lost events.

Workaround

Use the following workaround to prevent some core peripheral services from going to the lowest power mode. This will cause an increase of around 20 µA current in SYSTEM ON IDLE.

```
if (*(volatile uint32_t *)0x4006EC00 == 0)
{ *(volatile uint32_t *)0x4006EC00 = 0x9375; }
*(volatile unit32_t *) 0x4006EC14 = 0xC0;
```

To turn off this workaround (to save current):

```
if (*(volatile uint32_t *)0x4006EC00 == 0)
{ *(volatile uint32_t *)0x4006EC00 = 0x9375; }
*(volatile unit32_t *) 0x4006EC14 = 0x0;
```

3.19 [74] SAADC: Started events fires prematurely

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

False EVENTS_STARTED

Conditions

TACQ <= 5 µs

Consequences

The EVENTS_STARTED can come when not expected

Workaround

The module must be fully configured before it is enabled, and the TACQ configuration must be the last configuration set before ENABLE.

3.20 [75] MWU: Increased current consumption

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

Symptoms

Increased current consumption in System ON IDLE.

Conditions

When MWU is enabled.

Consequences

Increased current consumption in System ON IDLE.

Workaround

Do not use MWU or disable MWU before WFE/WFI, enable it on IRQ.

3.21 [76] LPCOMP: READY event is set sooner than it should

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

Symptoms

May receive unexpected events and wakeups from LPCOMP.

Conditions

LPCOMP is configured to send an event or to wake up the chip. LPCOMP.TASKS_START task is set and LPCOMP.EVENTS_READY event has been received.

Consequences

Unpredictable system behavior caused by falsely triggered events and wakeups.

Workaround

Use the following configuration sequence.

1. Configure the LPCOMP to send an event or wake up the chip, but do not enable any PPI channels or IRQ to be triggered from the LPCOMP events.
2. Trigger the LPCOMP.TASKS_START task and wait for the LPCOMP.EVENTS_READY event.
3. After receiving the LPCOMP.EVENTS_READY event wait for 115 µs.
4. After 115 µs, clear the LPCOMP.EVENTS_DOWN, LPCOMP.EVENTS_UP, and LPCOMP.EVENTS_CROSS events. LPCOMP is now ready to be used.

3.22 [77] CLOCK: RC oscillator is not calibrated when first started

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

The LFCLK RC oscillator frequency can have a frequency error of up to -25 to +40% after reset. A +/- 2% error is stated in the Product Specification.

Conditions

Always

Consequences

The LFCLK RC oscillator frequency is inaccurate.

Workaround

Calibrate the LFCLK RC oscillator before its first use after a reset.

3.23 [78] TIMER: High current consumption when using timer STOP task only

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

Increased current consumption when the timer has been running and the STOP task is used to stop it.

Conditions

The timer has been running (after triggering a START task) and then it is stopped using a STOP task only.

Consequences

Increased current consumption

Workaround

Use the SHUTDOWN task after the STOP task or instead of the STOP task.

3.24 [79] NFCT: A false EVENTS_FIELDDETECTED event occurs after the field is lost

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

Symptoms

A false EVENTS_FIELDDETECTED event occurs.

Conditions

The task TASK_SENSE is triggered within 150 µs of the event EVENTS_FIELDLOST.

Consequences

EVENTS_FIELDDETECTED will occur after a field is lost. (SHORT between eventfieldlost and taskSense should not be used since a false fieldDetected event will occur from using the task.)

Workaround

Wait 150 µs after an EVENTS_FIELDLOST event before triggering TASK_SENSE.

3.25 [81] GPIO: PIN_CNF is not retained when in debug interface mode

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

Symptoms

GPIO pin configuration is reset on wakeup from System OFF.

Conditions

The system is in debug interface mode.

Consequences

GPIO state unreliable until PIN_CNF is reconfigured..

3.26 [83] TWIS: STOPPED event occurs twice if the STOP task is triggered during a transaction

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

Symptoms

STOPPED event is set after clearing it.

Conditions

The STOP task is triggered during a transaction.

Consequences

STOPPED event occurs twice: When the STOP task is fired and when the master issues a stop condition on the bus. This could provoke an extra interrupt or a failure in the TWIS driver.

Workaround

The last STOPPED event must be accounted for in software.

3.27 [84] COMP: ISOURCE not functional

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

The programmable current source (ISOURCE) has too high varation. Variance over temp is >20 times specified nominal value

Conditions

Always.

Consequences

Inaccurate current source.

Workaround

None.

3.28 [86] SAADC: Triggering START task after offset calibration may write a sample to RAM

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

The first sample in the result buffer is incorrect, and will be present although the SAMPLE task has never been issued.

Conditions

The START task is triggered after performing calibration (through the CALIBRATEOFFSET task).

Consequences

Incorrect sample data in the result buffer.

Workaround

Calibration should follow the pattern STOP -> STOPPED -> CALIBRATEOFFSET -> CALIBRATEDONE -> STOP -> STOPPED -> START.

3.29 [87] CPU: Unexpected wake from System ON Idle when using FPU

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

The CPU is unexpectedly awoken from System ON Idle.

Conditions

The FPU has been used.

Consequences

The CPU is awoken from System ON Idle.

Workaround

The FPU can generate pending interrupts just like other peripherals, but unlike other peripherals there are no INTENSET, INTENCLR registers for enabling or disabling interrupts at the peripheral level. In order to prevent unexpected wake-up from System ON Idle, add this code before entering sleep:

```
#if (__FPU_USED == 1)
  _set_FPSCR(_get_FPSCR() & ~(0x0000009F));
  (void) __get_FPSCR();
  NVIC_ClearPendingIRQ(FPU_IRQn);
```

```
#endif
  __WFE();
```

3.30 [88] WDT: Increased current consumption when configured to pause in System ON idle

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

Using the mode where watchdog is paused in CPU Idle, the current consumption jumps from 3 µA to 400 µA.

Conditions

When we enable WDT with the CONFIG option to pause when CPU sleeps:

```
NRF_WDT->CONFIG = (WDT_CONFIG_SLEEP_Pause<<WDT_CONFIG_SLEEP_Pos);
```

Consequences

Reduced battery life

Workaround

Do not enter System ON IDLE within 125 µs after reloading the watchdog.

3.31 [89] TWI: Static 400 µA current while using GPIOTE

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

Symptoms

Static current consumption between 400 µA to 450 µA when using TWI in combination with GPIOTE.

Conditions

- GPIOTE is configured in event mode
- TWI utilizes EasyDMA

Consequences

Current consumption higher than specified

Workaround

Turn the TWI off and back on after it has been disabled. To do so: If TWI0 is used,

```
*(volatile uint32_t *)0x40003FFC = 0;
*(volatile uint32_t *)0x40003FFC;
*(volatile uint32_t *)0x40003FFC = 1;
```

If TWI1 is used,

```
*(volatile uint32_t *)0x40004FFC = 0;
*(volatile uint32_t *)0x40004FFC;
*(volatile uint32_t *)0x40004FFC = 1;
```

write 0 followed by a 1 to the POWER register (address 0xFFC) of the TWI that needs to be disabled. Reconfiguration of TWI is required before next usage.

3.32 [97] GPIOTE: High current consumption in System ON Idle mode

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

It was inherited from the previous IC revision Engineering A.

Symptoms

High current consumption (<20 µA) in System ON Idle mode

Conditions

GPIOTE used with one or more channels in input mode.

Consequences

Higher current consumption

Workaround

Use Port event to detect transitions on inputs instead of GPIOTE input mode.

3.33 [108] RAM: RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode

This anomaly applies to IC Rev. Engineering B, build codes QFAA-BA0, CHAA-AA0.

Symptoms

RAM not correctly retained.

Conditions

System ON Idle mode or System OFF is used with parts or all RAM retained.

Consequences

RAM not correctly retained.

Workaround

Apply the following code after any reset:

```
*(volatile uint32_t *)0x40000EE4 = (*(volatile uint32_t *)0x10000258 &
 0x0000004F);
```

This workaround is implemented in MDK version 8.9.0 and newer version. This workaround increases the I_RAM current per 4 KB section from 20nA to 30nA.

Chapter 4
Fixed anomalies

The anomalies listed in this table are no longer present in the current chip version.

For a detailed description of the fixed anomalies, see the Errata for revision Engineering A.

Table 3: Fixed anomalies

ID	Module	Description
1	I2S	I2S not functional
2	PWM	PWM not functional
3	PDM	PDM not functional
4	MWU	MWU not functional
7	NVMC,System	Cache is not functional
8	SAADC	Increased current consumption in system ON-IDLE
9	QDEC	Some features are not functional
10	RTC	RTC2 is not functional
11	System	Device is unable to stay in System OFF mode
16	System	RAM may be corrupt on wakeup from CPU IDLE
17	NFCT	The EVENTS_FIELDLOST is not generated
23	SPIM	END event is generated before ENDTX
24	NFCT	The FIELDPRESENT register read is not reliable
25	NFCT	Reset value of SENSRES register is incorrect
26	NFCT	NFC field does not wakeup the device from emulated system OFF
27	NFCT	Triggering NFCT ACTIVATE task also activates the Rx easyDMA
28	SAADC	Scan mode is not functional for some analog inputs
29	TWIS	Incorrect bits in ERRORSRC
30	TWIS	STOP Task is not functional
32	DIF	Debug session automatically enables TracePort pins
33	System	Code RAM is located at wrong address
34	System	Code and Data RAM are not mapped from the same physical RAM
35	CLOCK	HFCLK can draw current when not requested
37	RADIO	Encryption engine is slow by default.
38	PPI	Enable/disable tasks for channel group 4 and 5 cannot be triggered through PPI
39	NFCT	The automatic collision resolution does not handle CRC and parity errors

ID	Module	Description
40	NFCT	The FRAMEDELAYMODE = WindowGrid is not supported
41	GPIO	PIN_CNF[x] registers not reset after pin reset
42	PPI	FORK on the fixed channels is not functional
43	SPIS	SPIS0 is not functional
44	NVMC	Read after flash erase is unpredictable
46	SPIM,TWIM	EasyDMA list not functional
47	DIF	Trace is not functional
48	DIF	SWO only works if Trace is enabled.
49	RTC	RTC is not functional after LFCLK is restarted
57	NFCT	NFC Modulation amplitude
65	POWER	RAM[] registers mapping of RAM block and sections is wrong