nRF52832 Engineering A Errata v1.2

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Chapter 1
nRF52832 Engineering A Errata v1.2

This Errata document contains anomalies for the nRF52832 chip, revision Engineering A (QFAA-AA0, QFAA-AC0, CGAA-AA0).

Chapter 2
Change log

See the following list for an overview of changes from previous versions of this document.

Table 1: Change log

Version	Date	Change
nRF52832 Engineering A v1.2	05.07.2016	• Updated: No. 11. "Device is unable to stay in System OFF mode" • Added: No. 84. "ISOURCE not functional" • Added: No. 86. "Triggering START task after offset calibration may write a sample to RAM" • Added: No. 87. "Unexpected wake from System ON Idle when using FPU" • Added: No. 88. "Increased current consumption when configured to pause in System ON idle" • Added: No. 97. "High current consumption in System ON Idle mode"
nRF52832 Engineering A v1.1	17.02.2016	• Updated: No. 16. "RAM may be corrupt on wakeup from CPU IDLE" • Updated: No. 30. "STOP Task is not functional" • Updated: No. 57. "NFC Modulation amplitude" • Updated: No. 70. "Not able to wake CPU from System ON IDLE" • Updated: No. 73. "Event lost" • Updated: No. 78. "High current consumption when using timer STOP task only"
nRF52832 Engineering A v1.0	19.01.2016	• Created separate document for IC revision Engineering A. • Added: No. 57. "NFC Modulation amplitude"
nRF52832-PAN v1.2	11.12.2015	• Added: No. 67. "Some events cannot be used with the PPI" • Added: No. 68. "EVENTS_HFCLKSTARTED can be generated before HFCLK is stable" • Added: No. 70. "Not able to wake CPU from System ON IDLE" • Added: No. 71. "RCOSC calibration" • Added: No. 72. "TASKS_ACTIVATE cannot be used with the PPI" • Added: No. 73. "Event lost" • Added: No. 74. "Started events fires prematurely" • Added: No. 77. "RC oscillator is not calibrated when first started" • Added: No. 78. "High current consumption when using timer STOP task only"
nRF52832-PAN v1.1	09.10.2015	• Added: No. 31. "Calibration values are not correctly loaded from FICR at reset" • Added: No. 58. "SPIM clocks out an additional byte when RXD.MAXCNT = 1" • Added: No. 63. "DC/DC does not automatically switch off in System ON IDLE" • Added: No. 64. "Only full bytes can be received or transmitted"

Version	Date	Change
		• Added: No. 65. “RAM[] registers mapping of RAM block and sections is wrong”
nRF52832-PAN v1.0	15.06.2015	• Added: No. 1. “I2S not functional” • Added: No. 2. “PWM not functional” • Added: No. 3. “PDM not functional” • Added: No. 4. “MWU not functional” • Added: No. 7. “Cache is not functional” • Added: No. 8. “Increased current consumption in system ON-IDLE” • Added: No. 9. “Some features are not functional” • Added: No. 10. “RTC2 is not functional” • Added: No. 11. “Device is unable to stay in System-Off mode” • Added: No. 12. “Reference ladder is not correctly calibrated” • Added: No. 15. “RAM[x].POWERSET/CLR read as zero” • Added: No. 16. “RAM may be corrupt on wakeup from CPU IDLE” • Added: No. 17. “The EVENTS_FIELDLOST is not generated” • Added: No. 20. “Register values are invalid” • Added: No. 23. “END event is generated before ENDTX” • Added: No. 24. “The FIELDPRESENT register read is not reliable” • Added: No. 25. “Reset value of SENSRES register is incorrect” • Added: No. 26. “NFC field does not wakeup the device from emulated system OFF” • Added: No. 27. “Triggering NFCT ACTIVATE task also activates the Rx easyDMA” • Added: No. 28. “Scan mode is not functional for some analog inputs” • Added: No. 29. “Incorrect bits in ERRORSRC” • Added: No. 30. “STOP task is not functional” • Added: No. 32. “Debug session automatically enables TracePort pins” • Added: No. 33. “Code RAM is located at wrong address” • Added: No. 34. “Code and Data RAM are not mapped from the same physical RAM” • Added: No. 35. “HFCLK can draw current when not requested” • Added: No. 36. “Some registers are not reset when expected” • Added: No. 37. “Encryption engine is slow by default.” • Added: No. 38. “Enable/disable tasks for channel group 4 and 5 cannot be triggered through PPI” • Added: No. 39. “The automatic collision resolution does not handle CRC and parity errors” • Added: No. 40. “The FRAMEDELAYMODE = WindowGrid is not supported” • Added: No. 41. “PIN_CNF[x] registers not reset after pin reset” • Added: No. 42. “FORK on the fixed channels is not functional” • Added: No. 43. “SPIS0 is not functional” • Added: No. 44. “Read after flash erase is unpredictable” • Added: No. 46. “EasyDMA list not functional” • Added: No. 47. “Trace is not functional” • Added: No. 48. “SWO only works if Trace is enabled.” • Added: No. 49. “RTC is not functional after LFCLK is restarted”

Chapter 3
New and inherited anomalies

The following anomalies are present in revision Engineering A of the nRF52832 chip.

Table 2: New and inherited anomalies

ID	Module	Description	New in Engineering A
1	I2S	I2S not functional	X
2	PWM	PWM not functional	X
3	PDM	PDM not functional	X
4	MWU	MWU not functional	X
7	NVMC,System	Cache is not functional	X
8	SAADC	Increased current consumption in system ON-IDLE	X
9	QDEC	Some features are not functional	X
10	RTC	RTC2 is not functional	X
11	System	Device is unable to stay in System OFF mode	X
12	COMP	Reference ladder is not correctly calibrated	X
15	POWER	RAM[x].POWERSET/CLR read as zero	X
16	System	RAM may be corrupt on wakeup from CPU IDLE	X
17	NFCT	The EVENTS_FIELDLOST is not generated	X
20	RTC	Register values are invalid	X
23	SPIM	END event is generated before ENDTX	X
24	NFCT	The FIELDPRESENT register read is not reliable	X
25	NFCT	Reset value of SENSRES register is incorrect	X
26	NFCT	NFC field does not wakeup the device from emulated system OFF	X
27	NFCT	Triggering NFCT ACTIVATE task also activates the Rx easyDMA	X
28	SAADC	Scan mode is not functional for some analog inputs	X
29	TWIS	Incorrect bits in ERRORSRC	X
30	TWIS	STOP Task is not functional	X
31	CLOCK	Calibration values are not correctly loaded from FICR at reset	X
32	DIF	Debug session automatically enables TracePort pins	X
33	System	Code RAM is located at wrong address	X
34	System	Code and Data RAM are not mapped from the same physical RAM	X

ID	Module	Description	New in Engineering A
35	CLOCK	HFCLK can draw current when not requested	X
36	CLOCK	Some registers are not reset when expected	X
37	RADIO	Encryption engine is slow by default.	X
38	PPI	Enable/disable tasks for channel group 4 and 5 cannot be triggered through PPI	X
39	NFCT	The automatic collision resolution does not handle CRC and parity errors	X
40	NFCT	The FRAMEDELAYMODE = WindowGrid is not supported	X
41	GPIO	PIN_CNF[x] registers not reset after pin reset	X
42	PPI	FORK on the fixed channels is not functional	X
43	SPIS	SPIS0 is not functional	X
44	NVMC	Read after flash erase is unpredictable	X
46	SPIM,TWIM	EasyDMA list not functional	X
47	DIF	Trace is not functional	X
48	DIF	SWO only works if Trace is enabled.	X
49	RTC	RTC is not functional after LFCLK is restarted	X
57	NFCT	NFC Modulation amplitude	X
58	SPIM	An additional byte is clocked out when RXD.MAXCNT = 1	X
63	POWER	DC/DC does not automatically switch off in System ON IDLE	X
64	NFCT	Only full bytes can be received or transmitted, but supports 4-bit frame transmit	X
65	POWER	RAM[] registers mapping of RAM block and sections is wrong	X
67	NFCT,PPI	Some events cannot be used with the PPI	X
68	CLOCK	EVENTS_HFCLKSTARTED can be generated before HFCLK is stable	X
70	COMP	Not able to wake CPU from System ON IDLE	X
71	CLOCK	RCOSC calibration	X
72	NFCT,PPI	TASKS_ACTIVATE cannot be used with the PPI	X
73	TIMER	Event lost	X
74	SAADC	Started events fires prematurely	X
77	CLOCK	RC oscillator is not calibrated when first started	X
78	TIMER	High current consumption when using timer STOP task only	X
84	COMP	ISOURCE not functional	X
86	SAADC	Triggering START task after offset calibration may write a sample to RAM	X
87	CPU	Unexpected wake from System ON Idle when using FPU	X

ID	Module	Description	New in Engineering A
88	WDT	Increased current consumption when configured to pause in System ON idle	X
97	GPIOTE	High current consumption in System ON Idle mode	X

3.1 [1] I2S: I2S not functional

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.1 Symptoms

The I2S peripheral is not functional.

3.1 Conditions

Always.

3.1 Consequences

The I2S peripheral is not functional.

3.1 Workaround

None.

3.2 [2] PWM: PWM not functional

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.2 Symptoms

The PWM peripheral is not functional.

3.2 Conditions

Always.

3.2 Consequences

The PWM peripheral is not functional.

3.2 Workaround

None.

3.3 [3] PDM: PDM not functional

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.3 Symptoms

The PDM pheripheral is not functional.

3.3 Conditions

Always.

3.3 Consequences

The PDM pheripheral is not functional.

3.3 Workaround

None.

3.4 [4] MWU: MWU not functional

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.4 Symptoms

The MWU is not functional.

3.4 Conditions

Always.

3.4 Consequences

The MWU is not functional.

3.4 Workaround

None.

3.5 [7] NVMC,System: Cache is not functional

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.5 Symptoms

- CPU code execution is slower
- Coremark™ performance of the device is degraded

3.5 Conditions

CPU executing the firmware from flash memory.

3.5 Consequences

- Cache cannot be enabled
- Cannot profile the firmware using hit and miss counters.

3.5 Workaround

None.

3.6 [8] SAADC: Increased current consumption in system ON-IDLE

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.6 Symptoms

Increased current when SAADC is enabled but not sampling.

3.6 Conditions

SAADC enabled with TACQ < = 10µs.

3.6 Consequences

Increased current consumption.

3.6 Workaround

Disable SAADC when not in use or use SAADC with TACQ > 10µs.

3.7 [9] QDEC: Some features are not functional

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.7 Symptoms

The following features and settings are not functional in the QDEC:

Tasks:	RDCLRACC RDCLRDBL
Events:	DBLRDY STOPPED
Shortcuts:	from REPORTRDY to RDCLRACC from REPORTRDY to STOP from DBLRDY to RDCLRDBL from DBLRDY to STOP from SAMPLERDY to READCLRACC
Register settings:	SAMPLEPER setting of 32ms, 65ms and 131ms REPORTPER setting of 1Smpl (1 sample / report)

3.7 Conditions

Always.

3.7 Consequences

Listed features and settings are not functional.

3.7 Workaround

None.

3.8 [10] RTC: RTC2 is not functional

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.8 Symptoms

RTC2 is not functional.

3.8 Conditions

Always.

3.8 Consequences

RTC2 peripheral is not functional.

3.8 Workaround

None.

3.9 [11] System: Device is unable to stay in System OFF mode

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.9 Symptoms

Device wakes immediately from System OFF. Performing pin reset shows "wake-up from power off" as well as pin reset in POWER.RESETREAS.

3.9 Conditions

When PORT event is configured to wake from System OFF

3.9 Consequences

Device does not stay in System OFF.

3.9 Workaround

The wake on pin function needs to detect a valid wake-up condition before entering system OFF. This requires the temporary use of one GPIO pin in output mode. The workaround only needs to be executed when waking from POR or BOR reset, that is, when POWER.RESETREAS = 0x0000 0000 after wake up.

In the following example, GPIO P0.24 is used for the workaround, but any GPIO pin can be used by replacing "24" with another port pin number. The selected pin will momentarily be driven low by the workaround code.

Execute the following code after power on reset (POR) or brown out reset (BOR):

```
#define GPIO_SENSE_PIN      (24)

/* Configure a GPIO as input, detecting low level. */
NRF_P0->PIN_CNF[GPIO_SENSE_PIN] = (GPIO_PIN_CNF_DIR_Output    <<
 GPIO_PIN_CNF_DIR_Pos)    |

 (GPIO_PIN_CNF_INPUT_Connect << GPIO_PIN_CNF_INPUT_Pos)   |

 (GPIO_PIN_CNF_PULL_Disabled << GPIO_PIN_CNF_PULL_Pos)    |
```

```
 (GPIO_PIN_CNF_DRIVE_S0S1    << GPIO_PIN_CNF_DRIVE_Pos)   |

 (GPIO_PIN_CNF_SENSE_Low     << GPIO_PIN_CNF_SENSE_Pos);

/* Ensure that the level is low. */
NRF_P0->OUTCLR = 1UL << GPIO_SENSE_PIN;

/* Unconfigure the used GPIO. */
NRF_P0->PIN_CNF[GPIO_SENSE_PIN] = (GPIO_PIN_CNF_DIR_Input        <<
 GPIO_PIN_CNF_DIR_Pos)     |

 (GPIO_PIN_CNF_INPUT_Disconnect << GPIO_PIN_CNF_INPUT_Pos)   |

 (GPIO_PIN_CNF_PULL_Disabled    << GPIO_PIN_CNF_PULL_Pos)    |

 (GPIO_PIN_CNF_DRIVE_S0S1       << GPIO_PIN_CNF_DRIVE_Pos)   |

 (GPIO_PIN_CNF_SENSE_Disabled   << GPIO_PIN_CNF_SENSE_Pos);
```

3.10 [12] COMP: Reference ladder is not correctly calibrated

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.10 Symptoms

COMP does not compare correctly.

3.10 Conditions

Always.

3.10 Consequences

COMP module is unusable.

3.10 Workaround

Execute the following code before enabling the COMP module:

```
*(volatile uint32_t *)0x40013540 = (*(volatile uint32_t *)0x10000324 &
 0x00001F00) >> 8;
```

3.11 [15] POWER: RAM[x].POWERSET/CLR read as zero

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.11 Symptoms

RAM[x].POWERSET and RAM[x].POWERCLR read as zero, even though the RAM is on.

3.11 Conditions

Always

3.11 Consequences

Not possible to read the RAM state using RAM[x].POWERSET and RAM[x].POWERCLR registers. Write works as it should.

3.11 Workaround

Use RAM[x].POWER to read the state of the RAM.

3.12 [16] System: RAM may be corrupt on wakeup from CPU IDLE

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.12 Symptoms

On an event or interrupt where the CPU wakes up from IDLE state:

- The device hardfaults.
- Shows some unpredicted behavior consistent with RAM corruption.

3.12 Conditions

Always.

3.12 Consequences

Unpredicted behavior of the device.

3.12 Workaround

RAM blocks must be prevented from going to a low power state when the CPU goes to IDLE state (by executing the WFE or WFI instructions). Executing the following code before CPU sleep will ensure this:

```
*(volatile uint32_t *)0x4007C074 = 3131961357ul;
```

This code is already present in the latest system_nrf52.c file.

This configuration will also prevent RAM from going to low power (retention) state in system OFF and cause higher current consumption than documented in this mode. The following code can be executed before triggering the SYSTEMOFF.Enter to allow the RAM to go into retention state.

```
*(volatile uint32_t *)0x4007C074 = 2976579765ul;
```

3.13 [17] NFCT: The EVENTS_FIELDLOST is not generated

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.13 Symptoms

The EVENTS_FIELDLOST event is not generated. The SENSE task is not triggered if the shorts FIELDLOST_SENSE is used.

3.13 Conditions

Always.

3.13 Consequences

FIELDLOST event cannot be used reliably. The NFCT shortcut FIELDLOST_SENSE cannot be used reliably. Higher current consumption, since the NFCT cannot go into SENSE mode quickly and the device cannot go into sleep mode quickly based on FIELDLOST event.

3.13 Workaround

Do not use NFCT shortcut FIELDLOST_SENSE and FIELDLOST event.

Due to the software based work-around to handle the NFCT FIELDLOST event scenario, the NFCT shortcut FIELDDETECTED_ACTIVATE cannot be used either.

The FIELDLOST event is achieved using the following code in a busy loop.

```
            NRF_NFCT->AUTOCOLRESSTATUS = 0; /* Work-around for Errata 24.
 dummy write - no effect. */
            NRF_NFCT->AUTOCOLRESSTATUS = 0; /* Work-around for Errata 24.
 dummy write - no effect. */
            if  ((NRF_NFCT->FIELDPRESENT &
                  (NFCT_FIELDPRESENT_LOCKDETECT_Msk |
 NFCT_FIELDPRESENT_FIELDPRESENT_Msk)) ==
                 ((NFCT_FIELDPRESENT_FIELDPRESENT_NoField <<
 NFCT_FIELDPRESENT_FIELDPRESENT_Pos) |
                  (NFCT_FIELDPRESENT_LOCKDETECT_NotLocked <<
 NFCT_FIELDPRESENT_LOCKDETECT_Pos)))
            {
                /* Field is lost, handle the field lost event actions. */
            }
```

The FIELDDETECTED event is achieved using the following code in a busy loop.

```
            NRF_NFCT->AUTOCOLRESSTATUS = 0; /* Work-around for Errata 24.
 dummy write - no effect. */
            NRF_NFCT->AUTOCOLRESSTATUS = 0; /* Work-around for Errata 24.
 dummy write - no effect. */
            if  ((NRF_NFCT->FIELDPRESENT &
                  NFCT_FIELDPRESENT_FIELDPRESENT_Msk) !=
                 ((NFCT_FIELDPRESENT_FIELDPRESENT_NoField <<
 NFCT_FIELDPRESENT_FIELDPRESENT_Pos)))
            {
                /* Field is detected, handle the field detected event
 actions. */
            }
```

Example: Typical use case, go to SENSE mode when the field is lost and ACTIVATE when field is detected.

```
while (true)
{
    /* Wait for the field detection to happen */
    do
    {
        NRF_NFCT->AUTOCOLRESSTATUS = 0; /* dummy write - no effect. */
        NRF_NFCT->AUTOCOLRESSTATUS = 0; /* dummy write - no effect. */
    }while((NRF_NFCT->FIELDPRESENT &
    (NFCT_FIELDPRESENT_FIELDPRESENT_Msk)) ==
    (NFCT_FIELDPRESENT_FIELDPRESENT_NoField <<
 NFCT_FIELDPRESENT_FIELDPRESENT_Pos));
```

```
    NRF_NFCT->TASKS_ACTIVATE = 1;

    /* Wait for the field lost to happen */
    do
    {
        NRF_NFCT->AUTOCOLRESSTATUS = 0; /* dummy write - no effect. */
        NRF_NFCT->AUTOCOLRESSTATUS = 0; /* dummy write - no effect. */
    }while ((NRF_NFCT->FIELDPRESENT &
          (NFCT_FIELDPRESENT_LOCKDETECT_Msk |
 NFCT_FIELDPRESENT_FIELDPRESENT_Msk)) !=
         ((NFCT_FIELDPRESENT_FIELDPRESENT_NoField <<
 NFCT_FIELDPRESENT_FIELDPRESENT_Pos) |
          (NFCT_FIELDPRESENT_LOCKDETECT_NotLocked <<
 NFCT_FIELDPRESENT_LOCKDETECT_Pos)));

    NRF_NFCT->TASKS_SENSE = 1;

    /* Depending on the user application, the device can be put into
 system off here to save power while waiting for field. */
}
```

3.14 [20] RTC: Register values are invalid

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.14 Symptoms

RTC registers will not contain the correct/expected value if read.

3.14 Conditions

The RTC has been idle.

3.14 Consequences

RTC configuration cannot be determined by reading RTC registers.

3.14 Workaround

Execute the below code before you use RTC.

```
NRF_CLOCK->EVENTS_LFCLKSTARTED  = 0;
NRF_CLOCK->TASKS_LFCLKSTART     = 1;
while (NRF_CLOCK->EVENTS_LFCLKSTARTED == 0) {}
NRF_RTC0->TASKS_STOP = 0;
```

3.15 [23] SPIM: END event is generated before ENDTX

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.15 Symptoms

END event is generated before ENDTX.

3.15 Conditions

TXD.MAXCNT > RXD.MAXCNT

3.15 Consequences

END is unreliable in determining end of SPI transaction.

3.15 Workaround

Use ENDTX and/or ENDRX events instead of the END event.

3.16 [24] NFCT: The FIELDPRESENT register read is not reliable

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.16 Symptoms

The FIELDPRESENT register does not show the current field status.

3.16 Conditions

Always.

3.16 Consequences

The FIELDPRESENT status register cannot be used reliably.

3.16 Workaround

Write any register in NFCT twice before reading the FIELDPRESENT register.

3.17 [25] NFCT: Reset value of SENSRES register is incorrect

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.17 Symptoms

The device does not go through an automatic collision resolution successfully and does not generate a SELECTED event when automatic collision-resolution is enabled.

3.17 Conditions

Automatic collision resolution is enabled and the NFC peripheral is activated. The poller attempts a collision resolution sequence.

3.17 Consequences

The device does not go through an automatic collision resolution successfully.

3.17 Workaround

Write 0x00000001 to the SENSRES register before the NFC peripheral is enabled. The SENSRES can be modified based on user requirements later.

```
NRF_NFCT->SENSRES = (NFCT_SENSRES_BITFRAMESDD_SDD00001 <<
 NFCT_SENSRES_BITFRAMESDD_Pos);
```

3.18 [26] NFCT: NFC field does not wakeup the device from emulated system OFF

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.18 Symptoms

An NFC field does not wake up the device.

3.18 Conditions

When the Debugger Interface (DIF) is active.

3.18 Consequences

An NFC field cannot be used to wake up the device from the emulated system OFF while debugging the firmware using debugger.

3.18 Workaround

None.

3.19 [27] NFCT: Triggering NFCT ACTIVATE task also activates the Rx easyDMA

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.19 Symptoms

Memory corruption of the address pointed to by NFCT PACKETPTR register after triggering ACTIVATE task and during the collision resolution sequence. This happens even if the automatic collision resolution is enabled.

3.19 Conditions

- MAXLEN is non zero
- Trigger ACTIVATE task

3.19 Consequences

Memory corruption of the address pointed by the NFCT PACKETPTR register.

3.19 Workaround

Trigger the task TASKS_DISABLERXDATA immediately after triggering the TASKS_ACTIVATE task.

```
TASKS_ACTIVATE = 1;
TASKS_DISABLERXDATA = 1;
```

3.20 [28] SAADC: Scan mode is not functional for some analog inputs

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.20 Symptoms

SAADC result is the same for all channels in scan mode of AIN0-AIN7.

3.20 Conditions

More than one analog input is enabled.

3.20 Consequences

SAADC scan mode is not functional.

3.20 Workaround

None.

3.21 [29] TWIS: Incorrect bits in ERRORSRC

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.21 Symptoms

Incorrect mapping of OVERREAD and DNACK fields in ERRORSRC.

3.21 Conditions

Reading out ERRORSRC register.

3.21 Consequences

ERRORSRC will not read out as expected.

3.21 Workaround

Use the following bit indexes for ERRORSRC: OVERREAD=2, DNACK=1 ,OVERFLOW=0

3.22 [30] TWIS: STOP Task is not functional

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.22 Symptoms

In TX (READ command), SCL and SDA are pulled low and further communication is blocked. In RX (WRITE command), ERRORSRC shows 0x3.

3.22 Conditions

Always.

3.22 Consequences

It is not possible to use the TWIS STOP task for terminating ongoing transactions.

3.22 Workaround

Terminate ongoing transactions by disabling the TWIS, wait at least 1 µs for any ongoing transaction to complete, and then enable the TWIS.

3.23 [31] CLOCK: Calibration values are not correctly loaded from FICR at reset

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.23 Symptoms

RCOSC32KICALLENGTH is initialized with the wrong FICR value.

3.23 Conditions

Always

3.23 Consequences

RCOSC32KICALLENGTH default value is wrong.

3.23 Workaround

Execute the following code after reset:

```
*(volatile uint32_t *)0x4000053C = ((*(volatile uint32_t *)0x10000244) &
0x0000E000) >> 13;
```

This code is already present in the latest system_nrf52.c file.

3.24 [32] DIF: Debug session automatically enables TracePort pins

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.24 Symptoms

When a debug session is started, TracePort pins are automatically enabled. This may conflict with hardware connected to those pins (P0.18, P0.16, P0.15, P0.14 and P0.20).

3.24 Conditions

When a debug session is started.

3.24 Consequences

May conflict with hardware connected to pins P0.18, P0.16, P0.15, P0.14 and P0.20.

3.24 Workaround

Execute the following code:

```
CoreDebug->DEMCR &= ~CoreDebug_DEMCR_TRCENA_Msk;
```

This code is already present in the latest system_nrf52.c file.

The consequence of the workaround is that neither Trace, nor SWO nor Data Watchpoint and Trace are available during debugging.

3.25 [33] System: Code RAM is located at wrong address

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.25 Symptoms

The Code RAM reads as zero and can't be written.

3.25 Conditions

Always.

3.25 Consequences

The Code RAM will appear to be corrupted.

3.25 Workaround

Code RAM is located at address 0x0800_0000. Adjust your IDE project file/linkerscript/scatterfile so that the Code RAM is located at 0x0800_0000.

3.26 [34] System: Code and Data RAM are not mapped from the same physical RAM

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.26 Symptoms

Only the first 32 kB of Data RAM or Code RAM are functional. The contents of Data and Code RAM are independent; values written to one cannot be read from the other.

3.26 Conditions

Always.

3.26 Workaround

Adjust your IDE/linkerscript/scatterfile to fit this memory model. 64 kB of RAM is available by defining 2 RAM block locations with 32 kB length:

Block 1: Base address = 0x2000 0000, length = 0x8000
Block 2: Base address = 0x0800 0000, length = 0x8000

All RAM can be used for data variables without limitation. If Code is run from the SRAM segment of the System Address Map (Data RAM), execution will take longer because wait states will be introduced. EasyDMA transfers to and from RAM must be performed in the SRAM segment of the System Address Map (Data RAM).

See ERRATA#33 – Code RAM is located at the wrong address.

Important: This workaround must not be used for unaffected devices.

3.27 [35] CLOCK: HFCLK can draw current when not requested

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.27 Symptoms

Increased current consumption (> 100uA).

3.27 Conditions

HFCLK is not requested and supply voltage is above 2.0V.

3.27 Consequences

Current consumption in low power modes can be significantly higher than specified.

3.27 Workaround

None.

3.28 [36] CLOCK: Some registers are not reset when expected

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.28 Symptoms

After watchdog timeout reset, CPU lockup reset, soft reset, or pin reset, the following CLOCK peripheral registers are not reset: CLOCK->EVENTS_DONE, CLOCK->EVENTS_CTTO, CLOCK->CTIV

3.28 Conditions

After watchdog timeout reset, CPU Lockup reset, soft reset, and pin reset.

3.28 Consequences

Register reset values might be incorrect. It may cause undesired interrupts in case of enabling interrupts without clearing the DONE or CTTO events.

3.28 Workaround

Clear affected registers after reset. This workaround has already been added into system_nrf52.c file.

3.29 [37] RADIO: Encryption engine is slow by default.

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.29 Symptoms

When Radio encryption is enabled, TX or RX packets are sometimes corrupted. Encryption/decryption functions (ECB, AAR, and CCM) take longer than documented.

3.29 Conditions

Always.

3.29 Consequences

Radio packet error. Encryption takes longer time.

3.29 Workaround

Add the following code at the start of your program:

```
*(volatile uint32_t *)0x400005A0 = 0x3;
```

This code has already been added into system_nrf52.c.

3.30 [38] PPI: Enable/disable tasks for channel group 4 and 5 cannot be triggered through PPI

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.30 Symptoms

Triggering of the following tasks through PPI does not work:

TASKS_CHG[4].EN, Enable channel group 4
TASKS_CHG[4].DIS, Disable channel group 4
TASKS_CHG[5].EN, Enable channel group 5
TASKS_CHG[5].DIS, Disable channel group 5

3.30 Conditions

Always.

3.30 Consequences

Enable/disable tasks for channel group 4 and 5 cannot be triggered through PPI.

3.30 Workaround

Tasks have to be triggered through direct write to TASK address from CPU.

3.31 [39] NFCT: The automatic collision resolution does not handle CRC and parity errors

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.31 Symptoms

Frames with CRC and parity errors does not exit the automatic collision resolution activity.

3.31 Conditions

Always.

3.31 Consequences

For frames received with correct payload but the CRC and parity corrupted, the NFCT accepts these frames and goes to SELECTED state.

3.31 Workaround

None.

3.32 [40] NFCT: The FRAMEDELAYMODE = WindowGrid is not supported

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.32 Symptoms

The NFCT response frames are not aligned to the NFC-A bit grid, so the NFC poller device may not receive the frames.

3.32 Conditions

Always

3.32 Consequences

Some NFC poller devices may not receive the response frames from the NFCT.

3.32 Workaround

None.

3.33 [41] GPIO: PIN_CNF[x] registers not reset after pin reset

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.33 Symptoms

PIN_CNF registers are not reset after pin reset. Pins may be configured as an output and/or with pull enabled and/or with SENSE enabled.

3.33 Conditions

Always

3.33 Consequences

Possible higher than expected current consumption due to current flowing through pins, or spurious DETECT signals.

3.33 Workaround

Write default values to all PIN_CNF registers after a pin reset.

3.34 [42] PPI: FORK on the fixed channels is not functional

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.34 Symptoms

It is not possible to configure PPI.FORK[n].TEB register for fixed PPI channels (20-31).

3.34 Conditions

Always.

3.34 Consequences

Code using PPI.FORK on fixed PPI channels will not work.

3.34 Workaround

A programmable PPI channel has to be used to implement the connection.

3.35 [43] SPIS: SPIS0 is not functional

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.35 Symptoms

The SPIS0 is not functional.

3.35 Conditions

Always.

3.35 Consequences

The SPIS0 is not functional.

3.35 Workaround

None.

3.36 [44] NVMC: Read after flash erase is unpredictable

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.36 Symptoms

Reading flash after an erase operation returns invalid values.

3.36 Conditions

The flash page being read from was erased using NVMC.ERASEPAGE or NVMC.ERASEALL immediately before the read.

3.36 Consequences

Verifying a flash region is erased may fail. Writing to a flash page will never fail.

3.36 Workaround

Immediately after an erase operation, read from a page that was not erased in the operation, or write to any flash memory address. After one successful read or write, the symptom will not occur.

If ERASEALL was used, or it is not possible to identify which page was not erased in the operation, read from address 0x10000FFC after the erase operation as this is located in the FICR which is guaranteed to not be erased during the operation.

3.37 [46] SPIM,TWIM: EasyDMA list not functional

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.37 Symptoms

The EasyDMA list is not functional.

3.37 Conditions

Always.

3.37 Consequences

The EasyDMA list is not functional.

3.37 Workaround

None.

3.38 [47] DIF: Trace is not functional

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.38 Symptoms

Trace is not working, although the GPIO pins have been assigned to Trace.

3.38 Conditions

Always.

3.38 Consequences

Trace is not functional.

3.38 Workaround

None.

3.39 [48] DIF: SWO only works if Trace is enabled.

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.39 Symptoms

SWO is not working after enabling SWO.

3.39 Conditions

Always.

3.39 Consequences

SWO is not working.

3.39 Workaround

Instead of enabling SWO, enable Trace.

The only consequence is that 5 GPIOs will be captured, although only one is needed.

3.40 [49] RTC: RTC is not functional after LFCLK is restarted

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.40 Symptoms

RTC is not functional

3.40 Conditions

The LFCLK is stopped and then started again.

3.40 Consequences

Cannot restart the LFCLK.

3.40 Workaround

Do not stop the LFCLK.

3.41 [57] NFCT: NFC Modulation amplitude

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0.

3.41 Symptoms

The NFC poller is missing some frames from the NFCT device.

3.41 Conditions

Always

3.41 Consequences

The NFC poller might miss some frames from the NFCT device.

3.41 Workaround

Apply the following register setting during the device startup just after reset. *(volatile uint32_t *)0x40005610 = 0x00000005; *(volatile uint32_t *)0x40005688 = 0x00000001; *(volatile uint32_t *)0x40005618 = 0x00000000; *(volatile uint32_t *)0x40005614 = 0x0000003F; This code is already present in the latest system_nrf52.c file.

3.42 [58] SPIM: An additional byte is clocked out when RXD.MAXCNT = 1

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.42 Symptoms

SPIM clocks out additional byte.

3.42 Conditions

RXD.MAXCNT = 1

TXD.MAXCNT <= 1

3.42 Consequences

Additional byte is redundant.

3.42 Workaround

Use the SPI module (deprecated but still available) or use the following workaround with SPIM:

```
/**
 * @brief Work-around for transmitting 1 byte with SPIM.
 *
 * @param spim: The SPIM instance that is in use.
 * @param ppi_channel: An unused PPI channel that will be used by the
 workaround.
 * @param gpiote_channel: An unused GPIOTE channel that will be used by
 the workaround.
 *
 * @warning Must not be used when transmitting multiple bytes.
 * @warning After this workaround is used, the user must reset the PPI
 channel and the GPIOTE channel before attempting to transmit multiple
 bytes.
 */
void setup_workaround_for_ftpan_58(NRF_SPIM_Type * spim, uint32_t
 ppi_channel, uint32_t gpiote_channel)
{
    // Create an event when SCK toggles.
    NRF_GPIOTE->CONFIG[gpiote_channel] = (
        GPIOTE_CONFIG_MODE_Event <<
        GPIOTE_CONFIG_MODE_Pos
        ) | (
        spim->PSEL.SCK <<
        GPIOTE_CONFIG_PSEL_Pos
        ) | (
        GPIOTE_CONFIG_POLARITY_Toggle <<
        GPIOTE_CONFIG_POLARITY_Pos
        );

    // Stop the spim instance when SCK toggles.
    NRF_PPI->CH[ppi_channel].EEP = (uint32_t)&NRF_GPIOTE-
>EVENTS_IN[gpiote_channel];
    NRF_PPI->CH[ppi_channel].TEP = (uint32_t)&spim->TASKS_STOP;
    NRF_PPI->CHENSET = 1U << ppi_channel;

    // The spim instance cannot be stopped mid-byte, so it will finish
    // transmitting the first byte and then stop. Effectively ensuring
    // that only 1 byte is transmitted.
}
```

3.43 [63] POWER: DC/DC does not automatically switch off in System ON IDLE

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.43 Symptoms

The device will draw current periodically (in the mA range) when in System ON IDLE.

3.43 Conditions

DC/DC is enabled and in System ON IDLE.

3.43 Consequences

Average current consumption in idle mode is too high.

3.43 Workaround

None

3.44 [64] NFCT: Only full bytes can be received or transmitted, but supports 4-bit frame transmit

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.44 Symptoms

Data bits are not transmitted, or appear to not be received, if the Frame length is not a multiple of 8 bits (i.e. Frame includes data bits).

3.44 Conditions

Frame length is not a multiple of 8 bits (bytes only). Exception: 4-bit frame transmit supported.

3.44 Consequences

Partial bytes cannot be transferred:

- TXD.AMOUNT.TXDATABITS must be 0
- RXD.AMOUNT.RXDATABITS must be 0

3.44 Workaround

None

3.45 [65] POWER: RAM[] registers mapping of RAM block and sections is wrong

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.45 Symptoms

Using RAM[] registers to switch RAM retention on or off doesn't work as expected.

3.45 Conditions

Always.

3.45 Consequences

It is difficult to adjust the RAM retention to reduce power consumption.

3.45 Workaround

The easiest way to avoid problems is to switch on all RAM retention in all conditions, and do not micromanage the power consumption of the different RAM blocks and sections. The following code can be used:

```
NRF_POWER->RAM[0].POWER = 0xFFFFFFFF;
```

```
NRF_POWER->RAM[1].POWER = 0xFFFFFFFF;
NRF_POWER->RAM[2].POWER = 0xFFFFFFFF;
NRF_POWER->RAM[3].POWER = 0xFFFFFFFF;
NRF_POWER->RAM[4].POWER = 0xFFFFFFFF;
NRF_POWER->RAM[5].POWER = 0xFFFFFFFF;
NRF_POWER->RAM[6].POWER = 0xFFFFFFFF;
NRF_POWER->RAM[7].POWER = 0xFFFFFFFF;
```

3.46 [67] NFCT,PPI: Some events cannot be used with the PPI

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.46 Symptoms

The following NFCT events do not trigger tasks when used with the PPI:

- EVENTS_AUTOCOLRESSTARTED
- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

3.46 Conditions

PPI is used to trigger peripheral tasks using the NFCT events.

3.46 Consequences

The PPI cannot be used to trigger tasks using the following NFCT events:

- EVENTS_AUTOCOLRESSTARTED
- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

3.46 Workaround

The EVENTS_AUTOCOLRESSTARTED cannot be used with the PPI.

Subtract an offset of 0x04 while configuring the PPI event end points for the following NFCT events:

- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

Examples:

```
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_COLLISION) - 0x04;
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_SELECTED) - 0x04;
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_STARTED) - 0x04;
```

3.47 [68] CLOCK: EVENTS_HFCLKSTARTED can be generated before HFCLK is stable

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0.

3.47 Symptoms

EVENTS_HFCLKSTARTED may come before HFXO is started.

3.47 Conditions

When using a 32 MHz crystal with start-up longer than 400 µs.

3.47 Consequences

Performance of radio and peripheral requiring HFXO will be degraded until the crystal is stable.

3.47 Workaround

32 MHz crystal oscillator startup time must be verified by the user. If the worst-case startup time is shorter than 400 µs, no workaround is required. If the startup time can be longer than 400 µs, the software must ensure, using a timer, that the crystal has had enough time to start up before using peripherals that require the HFXO. The Radio requires the HFXO to be stable before use. The ADC, TIMERs, and TEMP sensor for example can use the HFXO as a reference for improved accuracy.

3.48 [70] COMP: Not able to wake CPU from System ON IDLE

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.48 Symptoms

COMP event not able to wake CPU form System ON IDLE.

3.48 Conditions

Always

3.48 Consequences

CPU will not wake from System ON IDLE.

3.48 Workaround

Use the following workaround to prevent some core peripheral services from going to the lowest power mode. This will cause an increase of around 20 µA current in SYSTEM ON IDLE.

```
if (*(volatile uint32_t *)0x4006EC00 == 0)
{ *(volatile uint32_t *)0x4006EC00 = 0x9375; }
*(volatile unit32_t *) 0x4006EC14 = 0xC0;
```

To turn off this workaround (to save current):

```
if (*(volatile uint32_t *)0x4006EC00 == 0)
{ *(volatile uint32_t *)0x4006EC00 = 0x9375; }
*(volatile unit32_t *) 0x4006EC14 = 0x0;
```

3.49 [71] CLOCK: RCOSC calibration

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0.

3.49 Symptoms

RCOSC only calibrates on every second calibration request.

3.49 Conditions

Always

3.49 Consequences

RCOSC not properly calibrated.

3.49 Workaround

Trigger TASKS_CAL, wait for EVENTS_DONE. Trigger TASKS_CAL again, wait for EVENTS_DONE each time the RCOSC is to be calibrated.

3.50 [72] NFCT,PPI: TASKS_ACTIVATE cannot be used with the PPI

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.50 Symptoms

The NFCT peripheral does not get activated when the PPI is configured to trigger TASKS_ACTIVATE on any event.

3.50 Conditions

Always

3.50 Consequences

The TASKS_ACTIVATE cannot be used with the PPI.

3.50 Workaround

None

3.51 [73] TIMER: Event lost

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.51 Symptoms

If an event from the peripherals listed below comes within 125 ns of the CPU and all other peripherals going to IDLE, the event flag may not be set and the event would be lost. The effected peripherals are RTC, LPCOMP, GPIO, and WDT. These peripherals are commonly used to wake the system from a low power IDLE state. Loss of events would prevent the wakeup from occurring.

3.51 Conditions

Always

3.51 Consequences

Lost events.

3.51 Workaround

Use the following workaround to prevent some core peripheral services from going to the lowest power mode. This will cause an increase of around 20 µA current in SYSTEM ON IDLE.

```
if (*(volatile uint32_t *)0x4006EC00 == 0)
{ *(volatile uint32_t *)0x4006EC00 = 0x9375; }
*(volatile unit32_t *) 0x4006EC14 = 0xC0;
```

To turn off this workaround (to save current):

```
if (*(volatile uint32_t *)0x4006EC00 == 0)
{ *(volatile uint32_t *)0x4006EC00 = 0x9375; }
*(volatile unit32_t *) 0x4006EC14 = 0x0;
```

3.52 [74] SAADC: Started events fires prematurely

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.52 Symptoms

False EVENTS_STARTED

3.52 Conditions

TACQ <= 5 µs

3.52 Consequences

The EVENTS_STARTED can come when not expected

3.52 Workaround

The module must be fully configured before it is enabled, and the TACQ configuration must be the last configuration set before ENABLE.

3.53 [77] CLOCK: RC oscillator is not calibrated when first started

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.53 Symptoms

The LFCLK RC oscillator frequency can have a frequency error of up to -25 to +40% after reset. A +/- 2% error is stated in the Product Specification.

3.53 Conditions

Always

3.53 Consequences

The LFCLK RC oscillator frequency is inaccurate.

3.53 Workaround

Calibrate the LFCLK RC oscillator before its first use after a reset.

3.54 [78] TIMER: High current consumption when using timer STOP task only

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.54 Symptoms

Increased current consumption when the timer has been running and the STOP task is used to stop it.

3.54 Conditions

The timer has been running (after triggering a START task) and then it is stopped using a STOP task only.

3.54 Consequences

Increased current consumption

3.54 Workaround

Use the SHUTDOWN task after the STOP task or instead of the STOP task.

3.55 [84] COMP: ISOURCE not functional

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.55 Symptoms

The programmable current source (ISOURCE) has too high varation. Variance over temp is >20 times specified nominal value

3.55 Conditions

Always.

3.55 Consequences

Inaccurate current source.

3.55 Workaround

None.

3.56 [86] SAADC: Triggering START task after offset calibration may write a sample to RAM

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0.

3.56 Symptoms

The first sample in the result buffer is incorrect, and will be present although the SAMPLE task has never been issued.

3.56 Conditions

The START task is triggered after performing calibration (through the CALIBRATEOFFSET task).

3.56 Consequences

Incorrect sample data in the result buffer.

3.56 Workaround

Calibration should follow the pattern STOP -> STOPPED -> CALIBRATEOFFSET -> CALIBRATEDONE -> STOP -> STOPPED -> START.

3.57 [87] CPU: Unexpected wake from System ON Idle when using FPU

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.57 Symptoms

The CPU is unexpectedly awoken from System ON Idle.

3.57 Conditions

The FPU has been used.

3.57 Consequences

The CPU is awoken from System ON Idle.

3.57 Workaround

The FPU can generate pending interrupts just like other peripherals, but unlike other peripherals there are no INTENSET, INTENCLR registers for enabling or disabling interrupts at the peripheral level. In order to prevent unexpected wake-up from System ON Idle, add this code before entering sleep:

```
#define FPU_EXCEPTION_MASK 0x0000009F
 __set_FPSCR(__get_FPSCR() & ~(FPU_EXCEPTION_MASK));
 (void) __get_FPSCR();
 NVIC_ClearPendingIRQ(FPU_IRQn);
 __WFE();
```

3.58 [88] WDT: Increased current consumption when configured to pause in System ON idle

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0, CGAA-AA0.

3.58 Symptoms

Using the mode where watchdog is paused in CPU Idle, the current consumption jumps from 3 µA to 400 µA.

3.58 Conditions

When we enable WDT with the CONFIG option to pause when CPU sleeps:

```
NRF_WDT->CONFIG = (WDT_CONFIG_SLEEP_Pause<<WDT_CONFIG_SLEEP_Pos);
```

3.58 Consequences

Reduced battery life

3.58 Workaround

Do not use mode where WDT is paused when CPU sleeps

3.59 [97] GPIOTE: High current consumption in System ON Idle mode

This anomaly applies to IC Rev. Engineering A, build codes QFAA-AA0, QFAA-AC0.

3.59 Symptoms

High current consumption (<20 µA) in System ON Idle mode

3.59 Conditions

GPIOTE used with one or more channels in input mode.

3.59 Consequences

Higher current consumption

3.59 Workaround

Use Port event to detect transitions on inputs instead of GPIOTE input mode.