nRF52820

Revision 2

Errata

v1.3

NORDIC® SEMICONDUCTOR

Contents

1 nRF52820 Revision 2 Errata

This Errata document contains anomalies and configurations for the nRF52820 chip, Revision 2 (QDAA-C00).

The document indicates which anomalies are fixed, inherited, or new compared to Engineering B.

2 Revision history

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nRF52820 Revision 2 v1.3	05.06.2023	• Added: No. 263. “On-the-fly decryption fails for direction finding packets” • Added: No. 265. “Pin mapping is not functional in PSELRESET” • Updated: No. 246. “Intermittent extra current consumption when going to sleep”
nRF52820 Revision 2 v1.2	09.02.2022	• Added: No. 243. “T_IFS is inaccurate with Bluetooth Long Range” • Added: No. 251. “NVMC ERASEALL is blocked when access port protection is enabled” • Added: No. 258. “PHYEND event is delayed for some AoA and AoD configurations” • Removed: No. 87. “Unexpected wake from System ON Idle when using FPU”
nRF52820 Revision 2 v1.1	09.11.2020	• Added: No. 233. “NVMC READYNEXT not generated” • Added: No. 245. “CRC is wrong when data whitening is enabled and address field is included in CRC calculation” • Added: No. 246. “Intermittent extra current consumption when going to sleep” • Added: No. 248. “Reading DTX in MODECNF0 gives incorrect value”
nRF52820 Revision 2 v1.0	29.06.2020	• Added: No. 20. “Register values are invalid” • Added: No. 36. “Some registers are not reset when expected” • Added: No. 66. “Linearity specification not met with default settings” • Added: No. 78. “High current consumption when using timer STOP task only” • Added: No. 87. “Unexpected wake from System ON Idle when using FPU” • Added: No. 136. “Bits in RESETREAS are set when they should not be” • Added: No. 173. “Writes to LATCH register take several CPU cycles to take effect” • Added: No. 176. “Flash erase through CTRL-AP fails due to watchdog time-out” • Added: No. 184. “Erase or write operations from the external debugger fail when CPU is not halted” • Added: No. 187. “USB cannot be enabled” • Added: No. 210. “Bits in GPIO LATCH register are incorrectly set to 1” • Added: No. 219. “I2C timing spec is violated at 400 kHz” • Added: No. 223. “ Unexpected behavior after reset” • Added: No. 225. “RSSI parameter adjustment” • Added: No. 228. “No interrupt is generated for SYNC event”

3 New and inherited anomalies

The following anomalies are present in Revision 2 of the nRF52820 chip.

ID	Module	Description	Inherited from Engineering B
20	RTC	Register values are invalid	X
36	CLOCK	Some registers are not reset when expected	X
66	TEMP	Linearity specification not met with default settings	X
78	TIMER	High current consumption when using timer STOP task only	X
136	System	Bits in RESETREAS are set when they should not be	X
173	GPIO	Writes to LATCH register take several CPU cycles to take effect	X
176	System	Flash erase through CTRL-AP fails due to watchdog time-out	X
184	NVMC	Erase or write operations from the external debugger fail when CPU is not halted	X
187	USBD	USB cannot be enabled	X
210	GPIO	Bits in GPIO LATCH register are incorrectly set to 1	X
219	TWIM	I2C timing spec is violated at 400 kHz	X
223	USBD	Unexpected behavior after reset	X
225	RADIO	RSSI parameter adjustment	X
228	RADIO	No interrupt is generated for SYNC event	X
233	NVMC	NVMC READYNEXT not generated	X
243	RADIO	T_IFS is inaccurate with Bluetooth Long Range	X
245	RADIO	CRC is wrong when data whitening is enabled and address field is included in CRC calculation	X
246	System	Intermittent extra current consumption when going to sleep	X
248	RADIO	Reading DTX in MODECNF0 gives incorrect value	X
251	NVMC	NVMC ERASEALL is blocked when access port protection is enabled	X
258	RADIO	PHYEND event is delayed for some AoA and AoD configurations	X
263	CCM	On-the-fly decryption fails for direction finding packets	X
265	UICR	Pin mapping is not functional in PSELRESET	X

Table 1: New and inherited anomalies

3.1 [20] RTC: Register values are invalid

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

RTC registers will not contain the correct/expected value if read.

Conditions

The RTC has been idle.

Consequences

RTC configuration cannot be determined by reading RTC registers.

Workaround

Execute the below code before you use RTC.

```
NRF_CLOCK->EVENTS_LFCLKSTARTED  = 0;
NRF_CLOCK->TASKS_LFCLKSTART     = 1;
while (NRF_CLOCK->EVENTS_LFCLKSTARTED == 0) {}
NRF_RTC0->TASKS_STOP = 0;
```

3.2 [36] CLOCK: Some registers are not reset when expected

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

After watchdog timeout reset, CPU lockup reset, soft reset, or pin reset, the following CLOCK peripheral registers are not reset:

- CLOCK->EVENTS_DONE
- CLOCK->EVENTS_CTTO
- CLOCK->CTIV

Conditions

After watchdog timeout reset, CPU Lockup reset, soft reset, and pin reset.

Consequences

Register reset values might be incorrect. It may cause undesired interrupts in case of enabling interrupts without clearing the DONE or CTTO events.

Workaround

Clear affected registers after reset. This workaround has already been added into system_nrf52.c file. This workaround has already been added into system_nrf52840.c file present in MDK 8.11.0 or later.

3.3 [66] TEMP: Linearity specification not met with default settings

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

TEMP module provides non-linear temperature readings over the specified temperature range.

Conditions

Always.

Consequences

TEMP module returns out of spec temperature readings.

Workaround

Execute the following code after reset:

```
NRF_TEMP->A0 = NRF_FICR->TEMP.A0;
NRF_TEMP->A1 = NRF_FICR->TEMP.A1;
NRF_TEMP->A2 = NRF_FICR->TEMP.A2;
NRF_TEMP->A3 = NRF_FICR->TEMP.A3;
NRF_TEMP->A4 = NRF_FICR->TEMP.A4;
NRF_TEMP->A5 = NRF_FICR->TEMP.A5;
NRF_TEMP->B0 = NRF_FICR->TEMP.B0;
NRF_TEMP->B1 = NRF_FICR->TEMP.B1;
NRF_TEMP->B2 = NRF_FICR->TEMP.B2;
NRF_TEMP->B3 = NRF_FICR->TEMP.B3;
NRF_TEMP->B4 = NRF_FICR->TEMP.B4;
NRF_TEMP->B5 = NRF_FICR->TEMP.B5;
NRF_TEMP->T0 = NRF_FICR->TEMP.T0;
NRF_TEMP->T1 = NRF_FICR->TEMP.T1;
NRF_TEMP->T2 = NRF_FICR->TEMP.T2;
NRF_TEMP->T3 = NRF_FICR->TEMP.T3;
NRF_TEMP->T4 = NRF_FICR->TEMP.T4;
```

This code is already present in the latest system_nrf52.c file and in the system_nrf52840.c file released in MDK 8.12.0.

3.4 [78] TIMER: High current consumption when using timer STOP task only

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

Increased current consumption when the timer has been running and the STOP task is used to stop it.

Conditions

The timer has been running (after triggering a START task) and then it is stopped using a STOP task only.

Consequences

Increased current consumption.

Workaround

Use the SHUTDOWN task after the STOP task or instead of the STOP task.

3.5 [136] System: Bits in RESETREAS are set when they should not be

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

After pin reset, RESETREAS bits other than RESETPIN might also be set.

Conditions

A pin reset has triggered.

Consequences

If the firmware evaluates RESETREAS, it might take the wrong action.

Workaround

When RESETREAS shows a pin reset (RESETPIN), ignore other reset reason bits.

Important: RESETREAS bits must be cleared between resets.

Apply the following code after any reset:

```
if (NRF_POWER->RESETREAS & POWER_RESETREAS_RESETPIN_Msk){
    NRF_POWER->RESETREAS =  ~POWER_RESETREAS_RESETPIN_Msk;
}
```

This workaround is implemented in MDK version 8.13.0 and later.

3.6 [173] GPIO: Writes to LATCH register take several CPU cycles to take effect

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

A bit in the LATCH register reads '1' even after clearing it by writing '1'.

Conditions

Reading the LATCH register right after writing to it.

Consequences

Old value of the LATCH register is read.

Workaround

Have at least 3 CPU cycles of delay between the write and the subsequent read to the LATCH register. This can be achieved by having 3 dummy reads to the LATCH register.

3.7 [176] System: Flash erase through CTRL-AP fails due to watchdog time-out

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

Full flash erase through CTRL-AP is not successful.

Conditions

WDT is enabled.

Consequences

Flash is not erased. If the device has a WDT time-out less than 1 ms and is readback-protected through UICR.APPROTECT, there is a risk of permanently preventing the erasing of the flash.

Workaround

Try again.

3.8 [184] NVMC: Erase or write operations from the external debugger fail when CPU is not halted

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

The erase or write operation fails or takes longer time than specified.

Conditions

NVMC erase or write operation initiated using an external debugger. CPU is not halted.

Consequences

The NVMC erase or write operation fails or takes longer time than specified.

Workaround

Halt the CPU by writing to DHCSR (Debug Halting Control and Status Register) before starting NVMC erase or write operation from the external debugger. See the ARM infocenter to get the details of the DHCSR register.

Programming tools provided by Nordic Semiconductor comply with this.

3.9 [187] USBD: USB cannot be enabled

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

After writing to NRF_USBD->ENABLE, no EVENTS_USBEVENT is triggered, and USB->EVENTCAUSE is not updated.

Conditions

Most recent reset type is soft reset or CPU lockup reset, or after a new firmware update to flash.

Consequences

USB is not working.

Workaround

Implement code similar to the following around the USB enabling:

```
*(volatile uint32_t *)0x4006EC00 = 0x00009375;
*(volatile uint32_t *)0x4006ED14 = 0x00000003;
*(volatile uint32_t *)0x4006EC00 = 0x00009375;

/* Enable the peripheral */
NRF_USBD->ENABLE = USBD_ENABLE_ENABLE_Enabled<< USBD_ENABLE_ENABLE_Pos;

/* Waiting for peripheral to enable, this should take a few µs */
while (0 == (NRF_USBD->EVENTCAUSE & USBD_EVENTCAUSE_READY_Msk))
{
    /* Empty loop */
}
NRF_USBD->EVENTCAUSE &= ~USBD_EVENTCAUSE_READY_Msk;

*(volatile uint32_t *)0x4006EC00 = 0x00009375;
*(volatile uint32_t *)0x4006ED14 = 0x00000000;
*(volatile uint32_t *)0x4006EC00 = 0x00009375;
```

nRF5 SDK version 15 will include this workaround.

3.10 [210] GPIO: Bits in GPIO LATCH register are incorrectly set to 1

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

The GPIO.LATCH[n] register is unexpectedly set to 1 (Latched).

Conditions

Set GPIO.PIN_CNF[n].SENSE at low level (3) at the same time as PIN_CNF[n].INPUT is set to Connect (0).

Consequences

The GPIO.LATCH[n] register is set to 1 (Latched). This could have side effects, depending on how the chip is configured to use this LATCH register.

Workaround

Always configure PIN_CNF[n].INPUT before PIN_CNF[n].SENSE.

3.11 [219] TWIM: I2C timing spec is violated at 400 kHz

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

The low period of the SCL clock is too short to meet the I2C specification at 400 kHz. The actual low period of the SCL clock is 1.25 µs while the I2C specification requires the SCL clock to have a minimum low period of 1.3 µs.

Conditions

Using TWIM at 400 kHz.

Consequences

TWI communication might not work at 400 kHz with I2C compatible devices.

Workaround

If communication does not work at 400 kHz with an I2C compatible device that requires the SCL clock to have a minimum low period of 1.3 µs, use 390 kHz instead of 400kHz by writing 0x06200000 to the FREQUENCY register. With this setting, the SCL low period is greater than 1.3 µs.

3.12 [223] USBD: Unexpected behavior after reset

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

The USBD might behave unexpectedly.

Conditions

USBD is enabled for the first time after a reset (USBD.ENABLE=1).

Consequences

The USBD internal state might not be reset correctly,

Note: This failure has not been reported or reproduced under test at the time of publication.

Workaround

When enabling the USBD for the first time after a reset, disable and re-enable. Wait for the status signal NRF_USBD->EVENTCAUSE set to USBD_EVENTCAUSE_READY after enabling, then disable and re-enable.

3.13 [225] RADIO: RSSI parameter adjustment

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

RSSI changes over temperature.

Conditions

Temperature ≤ +10°C or > +30°C.

Consequences

RSSI parameter not within specified accuracy.

Workaround

Add the following compensation to the RSSI sample value based on temperature measurement (the on-chip TEMP peripheral can be used to measure temperature):

- For TEMP ≤ -30°C, RSSISAMPLE = RSSISAMPLE +3
- For TEMP > -30°C and TEMP ≤ -10°C, RSSISAMPLE = RSSISAMPLE +2
- For TEMP > -10°C and TEMP ≤ +10°C, RSSISAMPLE = RSSISAMPLE +1
- For TEMP > +10°C and TEMP ≤ +30°C, RSSISAMPLE = RSSISAMPLE + 0
- For TEMP > +30°C and TEMP ≤ +50°C, RSSISAMPLE = RSSISAMPLE - 1
- For TEMP > +50°C and TEMP ≤ +70°C, RSSISAMPLE = RSSISAMPLE - 2
- For TEMP > +70°C and TEMP ≤ +85°C, RSSISAMPLE = RSSISAMPLE - 3
- For TEMP > +85°C, RSSISAMPLE = RSSISAMPLE - 4

3.14 [228] RADIO: No interrupt is generated for SYNC event

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

Interrupt Service Routine (ISR) for the SYNC event does not run.

Conditions

Always.

Consequences

ISR for the SYNC event does not run.

Workaround

Connect the SYNC event to an EGU task through a PPI channel. Handle the interrupt in the corresponding EGU ISR.

3.15 [233] NVMC: NVMC READYNEXT not generated

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

When executing from NVM and performing an NVM operation, READYNEXT might not be asserted. If the program is waiting for READYNEXT, the program stops executing.

Conditions

When executing from NVM. Using READYNEXT when executing from RAM is not affected.

Consequences

READYNEXT should not be used when executing from NVM.

Workaround

Use READY instead. Using READY instead of READYNEXT has no penalty when executing from NVM.

3.16 [243] RADIO: T_IFS is inaccurate with Bluetooth Long Range

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

The measured T_IFS is inaccurate for LE Coded PHY.

Conditions

Using default values of the TIFS register.

Consequences

T_IFS does not meet the accuracy required by the Bluetooth specification.

Workaround

Depending on the mode of the received packet and the mode selected for the next transmission, update the TIFS register with the following values:

- RX: mode 6 (S=2), TX: mode 6 (S=2) : 144
- RX: mode 5 (S=8), TX: mode 5 (S=8) : 149
- RX: mode 5 (S=8), TX: mode 6 (S=2) : 139
- RX: mode 6 (S=2), TX: mode 5 (S=8) : 154

The TIFS register must be updated before the DISABLED event from the receive packet. Otherwise, the new value is not taken into account for the next transmission. The rate of the last received packet can be found in the CISTAT field of the PDUSTAT register. The CISTAT field is updated approximately 1 µs after the ADDRESS event. The SoftDevice, Zephyr Controller subsystem (Zephyr and nRF Connect SDK), and SoftDevice Controller subsystem (nRF Connect SDK) are not affected by this errata.

3.17 [245] RADIO: CRC is wrong when data whitening is enabled and address field is included in CRC calculation

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

CRC failures are reported.

Conditions

In RX, if data whitening is enabled and the CRC checker is configured to take the address field into CRC calculations.

Consequences

CRC failures are reported though received packet contents are good.

3.18 [246] System: Intermittent extra current consumption when going to sleep

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

Extra current consumption in the range of 350 µA when in System On Idle.

Conditions

A high-speed peripheral (CPU, CRYPTOCELL, USB, or CTRL-AP) accesses a RAM block which is being accessed by a low-speed peripheral through the DMA bus with a specific timing, and the high-speed peripheral has higher priority than the low-speed peripheral.

Consequences

Extra current consumption in System On Idle.

Workaround

Apply the following code after any reset:

```
*(volatile uint32_t *)0x4007AC84ul = 0x00000002ul;
```

Workaround consequences: Up to 40 µA current increase when the 16 MHz clock is used.

3.19 [248] RADIO: Reading DTX in MODECNF0 gives incorrect value

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

Reading DTX in MODECNF0 gives incorrect value.

Conditions

Always.

Consequences

Reading MODECNF0.DTX field returns wrong value.

Workaround

Treat MODECNF0.DTX field as write only.

3.20 [251] NVMC: NVMC ERASEALL is blocked when access port protection is enabled

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

NVMC ERASEALL is blocked when access port protection is enabled.

Conditions

Always

Consequences

ERASEALL cannot be triggered by the CPU once access port protection is enabled.

Workaround

Use page erase if the content of the NVM needs to be erased by the CPU once access port protection has been enabled.

3.21 [258] RADIO: PHYEND event is delayed for some AoA and AoD configurations

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

The PHYEND event is generated 16 µs too late when compared to the actual end of frame on air.

Conditions

The RADIO peripheral enables the parsing of CTEInfo from the received packets in Bluetooth Low Energy modes using the CTEINLINECONF register and the received PDU does not contain CTEInfo.

Consequences

If protocol timing, for example T_IFS, is based on the PHYEND event, the device is not compliant.

Workaround

Checking the CTEPRESENT event allows software to detect this case. It must then compensate any timing based on the PHYEND event by 16 µs.

3.22 [263] CCM: On-the-fly decryption fails for direction finding packets

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

MICSTATUS reports CheckFail, and decrypted data is wrong.

Conditions

The header of the received Bluetooth packets has the CP bit set and contains the CTEInfo byte.

Consequences

Direction finding packets are incorrectly rejected.

Workaround

Replace the PPI connection from RADIO EVENTS_ADDRESS event to CCM TASKS_CRYPT with a PPI connection from RADIO EVENTS_BCMATCH to CCM TASKS_CRYPT and configure the RADIO register BCC with the value 3.

3.23 [265] UICR: Pin mapping is not functional in PSELRESET

This anomaly applies to Revision 2, build codes QDAA-C00.

It was inherited from the previous IC revision Engineering B.

Symptoms

Pin mapping is not functional for PSELRESET.

Consequences

When mapping GPIOs to nRESET according to nRF52820 Product Specification, nRESET is not connected to the GPIO as configured in UICR.PSELRESET[n].PIN.

Workaround

When configuring PIN in UICR.PSELRESET[n] registers, clear bit 5 to 0.