nRF21540

Product Specification

v1.1.1

Key features

Key features:	Applications:
• Front-end module with RF PA and LNA	• Smart Home applications
• Supports *Bluetooth*® Low Energy, IEEE 802.15.4, and proprietary applications	• Industrial and factory automation
• Max output power 22 dBm	• Asset tracking
• Adjustable output gain from 5 ±1 dB to 21 ±1 dB	• Advanced CE remote controls
• User programmable modes for TX gain	• Sports and fitness
• Non-volatile memory storage for gain settings	• Toys
• Dual antenna port with antenna diversity support	• Medical
• RX gain +13 dB	• Beacons
• Single-ended 50 Ω matched input and output	
• 110 mA at +20 dBm output power	
• 38 mA at +10 dBm output power	
• Control interface via I/O, SPI, or a combination of both	
• Supply voltage 1.7 V to 3.6 V, suitable for 1.8 V ±5% systems	
• Operating temperature -40°C to 105°C	
• Package variant QFN16 4 x 4 mm	

Contents

1 Revision history

Date	Version	Description
September 2021	1.1.1	The following content has been added or updated: • Reference circuitry corrected R1
July 2021	1.1	The following content has been added or updated: • Reference circuitry updated for nRF21540 QDAA-G00 and later • Updated electrical specifications
August 2020	1.0	First release

2 About this document

This document is organized into chapters that are based on the modules and peripherals available in the IC.

2.1 Document status

The document status reflects the level of maturity of the document.

Document name	Description
Objective Product Specification (OPS)	Applies to document versions up to 1.0. This document contains target specifications for product development.
Product Specification (PS)	Applies to document versions 1.0 and higher. This document contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Table 1: Defined document names

2.2 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

2.2.1 Fields and values

The **Id (Field Id)** row specifies the bits that belong to the different fields in the register. If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column.

A blank space means that the field is reserved and read as undefined, and it also must be written as `0` to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column. The **Value Id** may be omitted in the single-bit bit fields when values can be substituted with a Boolean type enumerator range, e.g. true/false, disable(d)/enable(d), on/off, and so on.

Values are usually provided as decimal or hexadecimal. Hexadecimal values have a `0x` prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example 1, 3, 9.
- Range of values, e.g. [0..4], indicating all values from and including 0 and 4.
- Implicit values. If no values are indicated in the **Value** column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value Id**, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with '..'.

A feature marked **Deprecated** should not be used for new designs.

2.2.2 Permissions

Different fields in a register might have different access permissions enforced by hardware.

The access permission for each register field is documented in the **Access** column in the following ways:

Access	Description	Hardware behavior
RO	Read-only	Field can only be read. A write will be ignored.
WO	Write-only	Field can only be written. A read will return an undefined value.
RW	Read-write	Field can be read and written multiple times.
W1	Write-once	Field can only be written once per reset. Any subsequent write will be ignored. A read will return an undefined value.
RW1	Read-write-once	Field can be read multiple times, but only written once per reset. Any subsequent write will be ignored.

Table 2: Register field permission schemes

2.3 Registers

Register overview

Register	Offset	Description
DUMMY	0x514	Example of a register controlling a dummy feature

2.3.1 DUMMY

Address offset: 0x514

Example of a register controlling a dummy feature

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID					D	D	D	D						C	C	C								B							A	A
Reset 0x00050002	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	FIELD_A			Example of a read-write field with several enumerated values
			Disabled	0	The example feature is disabled
			NormalMode	1	The example feature is enabled in normal mode
			ExtendedMode	2	The example feature is enabled along with extra functionality
B	RW	FIELD_B			Example of a deprecated read-write field This field is deprecated.
			Disabled	0	The override feature is disabled
			Enabled	1	The override feature is enabled
C	RW	FIELD_C			Example of a read-write field with a valid range of values
			ValidRange	[2..7]	Example of allowed values for this field
D	RW	FIELD_D			Example of a read-write field with no restriction on the values

3 Product overview

nRF21540 is an RF front-end module suitable for Bluetooth Low Energy and IEEE 802.15.4 range extension.

Device features include a configurable gain power amplifier (PA) in the transmit path (TX) and a low noise amplifier (LNA) in the receive path (RX). Single-ended operation on both **TRX** and **ANT1/2** ports is supported and requires four external components (for single antenna operation) for the RF path, plus antenna termination for the unused antenna port.

The device is controlled through a set of input pins. Alternatively, the device can be controlled by writing to internal control registers through the SPI interface. The two antenna ports enable applications using antenna diversity and can be selected using pin **ANT_SEL**.

Highly configurable gain in Transmit state enables the application to implement adaptive gain control algorithms.

Gain settings can be stored for factory device calibration to user configurable output power through on-board non-volatile memory.

4 Block diagram

The block diagram illustrates the overall system.

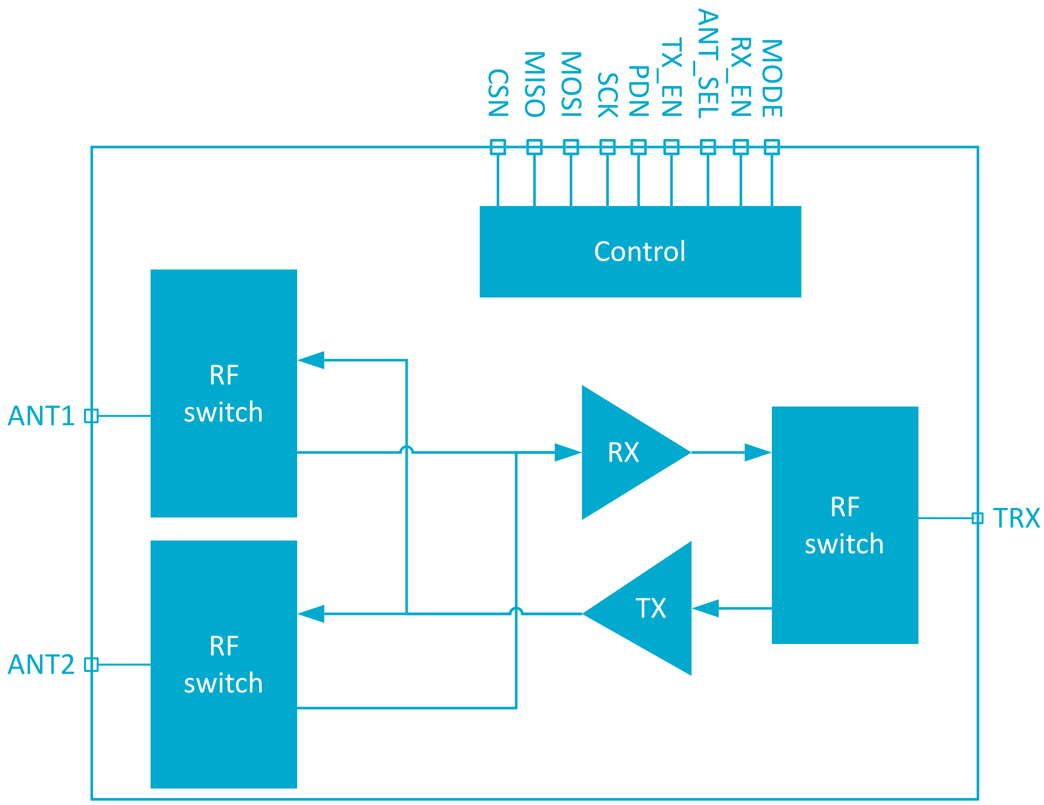

Figure 1: nRF21540 Block diagram

5 Device control

nRF21540 uses an internal state machine to control the operation of the device. The state machine can be controlled through direct pin control or through the built-in SPI slave interface.

5.1 Operational states

This section describes how nRF21540 is put in different operational states.

When **PDN** is set to 0, the device is in Power-down state. When **PDN** is set to 1, the device is activated and enters Program state. All registers will contain reset values when the device enters Program state. It can be set to any other state (Receive, Transmit, and UICR Program) using pin control or the SPI interface.

State transitions are controlled by pins **PDN**, **RX_EN**, and **TX_EN**, or bit fields in SPI registers CONFREG0 and CONFREG1. For timings required when switching between operating states, see State transition timing on page 12.

When the device is in Receive state, the receive path is active and the transmit path is disabled. In the Receive state, the LNA is enabled. When the device is in the Receive state, **CSN** needs to be driven low as shown in Figure 3: Pin control RX state on page 12.

When the device is in Transmit state, the transmit path is enabled and the receive path is disabled. In Transmit state, the PA is enabled. The device features a configurable TX output power, see TX power control on page 13 for details.

Note: Enabling multiple states simultaneously is not supported.

UICR Program state enables programming of default settings for TX power control to UICR EFUSE (one time programmable memory). UICR Program state is accessed from Program state by writing specific values to register CONFREG1. Registers CONFREG2 and CONFREG3 are where bit programming definition and triggering of UICR EFUSE programming happen. See UICR programming on page 14 for more details about UICR programming.

The SPI register interface is described in detail in SPI interface on page 15.

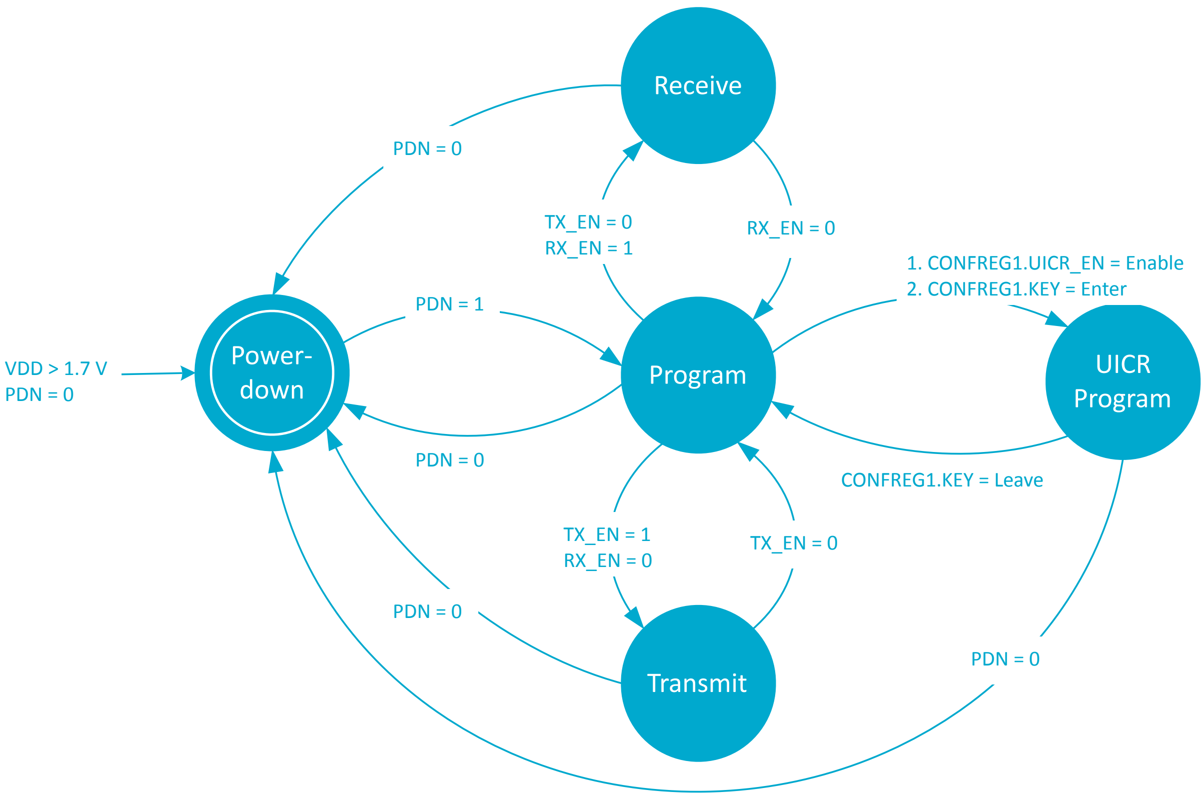

Figure 2: State diagram

State	Symbol	Description
Power-down	PD	The device is in Power-down state.
Program	PG	The device can be configured and set to other states.
UICR program	UICR	User defined initialization values for POUTA_SEL, POUTA_UICR, POUTB_SEL, and POUTB_UICR can be configured to UICR.
Receive	RX	The RX path is enabled. .
Transmit	TX	The TX path is enabled.

Table 3: Operating states description

5.2 Antenna control

ANT_SEL selects the antenna interface used during RX or TX. Antenna interface control is specified in the following table.

State	ANT_SEL	Description
Power-down	X	Antenna switches disabled (i.e. isolating)
Program	X	Antenna switches disabled (i.e. isolating)
UICR program	X	Antenna switches disabled (i.e. isolating)
Receive	0	ANT1 enabled, ANT2 disabled
	1	ANT1 disabled, ANT2 enabled
Transmit	0	ANT1 enabled, ANT2 disabled
	1	ANT1 disabled, ANT2 enabled

Table 4: Antenna switch control with ANT_SEL in different states

5.3 State transition timing

Settling time requirements when switching between operational states are defined in the following table.

When using SPI control, the maximum settling time is defined from the falling edge of SPI clock cycle 16. For more details on SPI, see SPI interface on page 15.

Note: GPIO control is faster than SPI control.

Symbol	Parameter	Note	Max.	Unit
$T_{TRX \rightarrow PD}$	Settling time from states TX or RX to PD	Triggered by PDN	10	µs
$T_{PD \rightarrow PG}$	Settling time from state PD to PG	Triggered by PDN	17.5	µs
$T_{PG \rightarrow TRX}$	Settling time from state PG to TX or RX	Triggered by RX_EN, TX_EN, or through SPI register control	10.5	µs
$T_{TRX \rightarrow PG}$	Power-off time when changing from RX or TX to PG	Triggered by RX_EN, TX_EN, or through SPI register control	3	µs
$T_{PG \rightarrow PD}$	Settling time from state PG to PD	Triggered by PDN	10	µs

Table 5: Settling times

An example of RX timing using an **RX_EN** pin-based configuration is shown in the following figure.

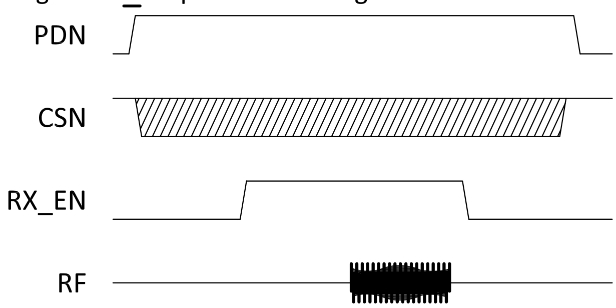

Figure 3: Pin control RX state

The following figure shows the Receive state configured using SPI.

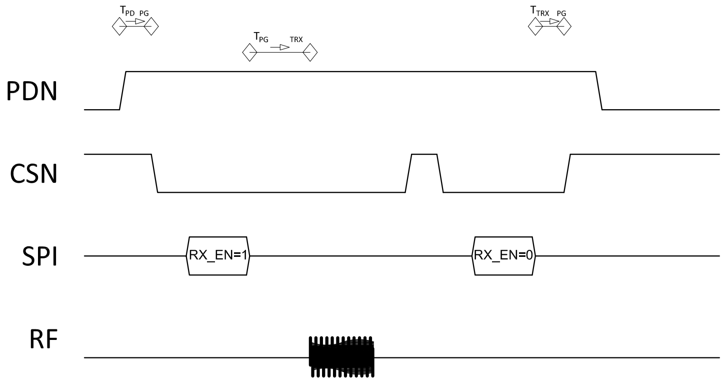

Figure 4: SPI control RX state

The following figure shows the Transmit state configured through pin.

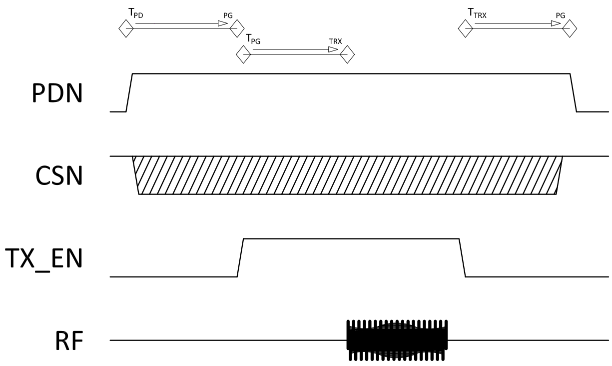

Figure 5: Pin control TX state

The following figure shows the Transmit state configured using SPI.

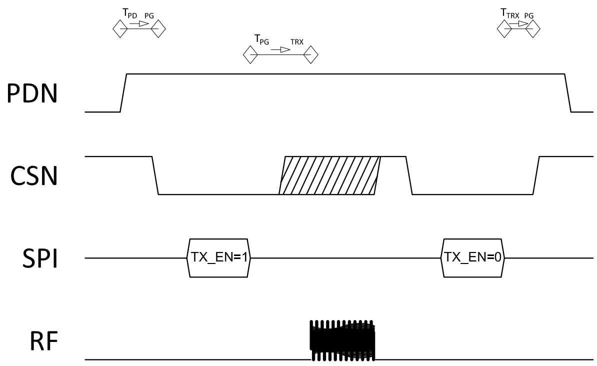

Figure 6: SPI control TX state

5.4 TX power control

The output power for the Transmit state is configured through pin control or the SPI interface.

> **Note:** Gain should not be changed while the device is in the Transmit state.

When output power is configured through pins, **MODE** is used to set one of two preset values to the TX power control. Preset values update the TX_Gain value when **MODE** control changes in the Program state. The same functionality is enabled by writing to the MODE bit in CONFREG0. Custom preset values are stored in UICR and selected as default.

The SPI interface can also control the output power. From Program state, and before entering the Transmit state, TX_Gain is configured by writing the gain value over SPI to the TX_GAIN field in the CONFREG0 register. SPI write overwrites the initialization TX_Gain value. The Transmit state can then be entered by writing CONFREG0.TX_EN in the same SPI write cycle, or later by using **TX_EN** pin.

Changing **MODE** or the MODE bit in CONFREG0 triggers a reload of a default value to TX_Gain. Setting **MODE** or the MODE bit loads POUTB, while clearing them loads POUTA. The default value is used when a new value is loaded to TX_Gain during the SPI write cycle. This changes the MODE bit. When a new value is loaded to TX_Gain during the SPI write cycle, the default value is used, changing the MODE bit.

The following table shows TX power control with MODE control and corresponding preset values of TX_Gain in Program state.

MODE	POUTA_SEL	POUTB_SEL	TX_Gain	Description
0	0	X	POUTA_PROD	Chip production default value used
1	X	0	POUTB_PROD	Chip production default value used
0	1	X	POUTA_UICR	End-user default value used
1	X	1	POUTB_UICR	End-user default value used

Table 6: TX power control

5.5 UICR programming

The UICR Program state enables the automated programming sequence for UICR EFUSE cell.

The automated programming sequence can be utilized in the following way.

1. Apply VDD supply voltage using these EFUSE programming specifications.

Parameter	**Allowed range**
V_{DD}	3.45 V to 3.60 V
T_{OP}	0°C to 85°C

2. Write `Enable` to field UICR_EN in register CONFREG1 to enable UICR Program state.
3. Write `Enter` to field KEY in register CONFREG1 to enter UICR Program state.
4. Write desired configuration values for POUTB_SEL and POUTB_UICR to register CONFREG3.
5. Write desired configuration values for POUTA_SEL and POUTA_UICR to register CONFREG2.
6. Write a `1` to WR_UICR in register CONFREG2. Wait for 0.5 ms to guarantee successful programming.
7. Reset the circuit by setting **PDN** to `0` and then back to `1`.

The values are now programmed to registers CONFREG2 and CONFREG3. To verify, set the device to UICR mode and read registers CONFREG2 and CONFREG3.

6 SPI interface

The data transitions for slave in and out (MOSI and MISO) happen on the falling edge of the serial clock (SCK). All SPI transfers are 2 bytes long.

Input data is sampled on the rising edge of SCK, starting with the first rising edge. Therefore, it is required that the first bit is stable on the first rising clock edge of SCK. Common definitions for SPI bus are CPOL = 0 and CPHA = 0. In other words, SPI mode 0. The serial data frame is 16 bits long and consists of three parts in the following transmission order: command (Cmd), address, and data. All fields are sent on MOSI line MSB first. In the event of a write operation, a command is 2 bits long, an address is 6 bits long, followed by 8 bits of data. CSN is active low and it is assumed that it is set to `0` at least half an SCK cycle before the first rising edge of SCK, and then again to logical `1` earliest after half a cycle of 16th SCK falling edge.

The following commands are used:

- READ, **`b10`** – This command allows reading of registers. The register address to read from is sent after the command. The read data will be clocked out to the MISO line during the data part of the SPI frame.
- WRITE, **`b11`** – This command allows writing to registers. The last 8 bits sent on the MOSI line will be written to a register pointed with 6-bit address field. The write command has writeback property. When a register is accessed by the write command to update its value, the previous register value will be written to the MISO line in serial format MSB first.

SPI timing specification presents the required timings between CSN signal and SCK edge.

The following figure shows a configuration example for SPI when writing to register CONFREG0. The WRITE command **`b11`** is written to the command field. The first bit on the MOSI line must be set to its value (in this case to `1`) before the first rising edge of SCK occurs. This is because Cmd is read on the rising edge of the first and second SCK cycle. SCK rising edges 3 to 8 are used to read the address field, and 9 to 16 read the data field. Register CONFREG0 writeback data is written on the MISO line starting on the falling edge of cycle 8 so that the rising edges of cycle 9 to 16 can be used to read in MISO data on the Master side. Guaranteed settling time for the first read bit before the cycle 9 falling edge can be found in SPI timing specification.

Functionality of the read operation is similar to writeback, meaning that read data is written to the MISO line starting on the cycle 8 falling edge when the read command is given in the Cmd field.

An overview of register address space and accessibility of registers in different operation states is found in SPI timing.

The detailed register map is given in the Register interface on page 25.

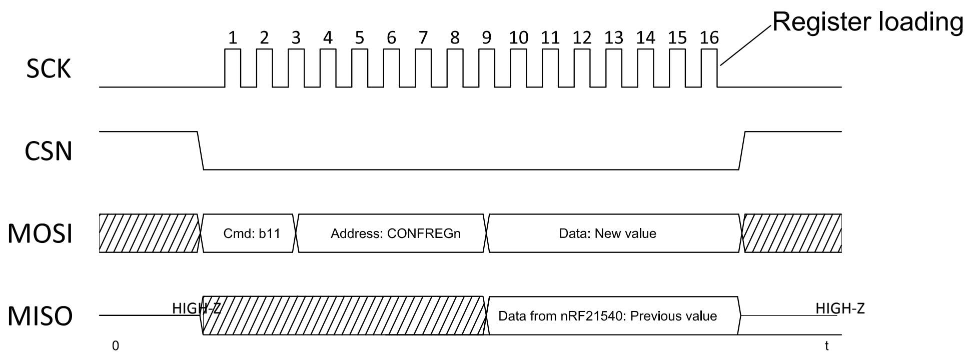

Figure 7: SPI write configuration example

Register	Function	Accessible via SPI in the following states
CONFREG0	TX state control and TX gain control in Program state	PG, RX, TX, UICR
CONFREG1	RX state control and RX gain control in Program state	PG, RX, TX, UICR
CONFREG2, CONFREG3	UICR programming interface registers	UICR
PARTNUMBER, HW_REVISION[7:4]	Part number, hardware revision	PG
HW_ID0, HW_ID1	Hardware ID	PG

Table 7: Register overview and accessibility in different operation states

7 Electrical specification

The device is calibrated at 25°C to VDD=3.0 V. For other conditions, see Typical characteristics on page 18.

Condition	Value
VDD	3 V
Temperature	25°C
Frequency	2440 MHz
Z_L	50 Ω
P_{IN_TRX}	0 dBm

Table 8: Current consumption scenarios, common conditions

7.1 Electrical specification

7.1.1 Current consumption

Symbol	Description	Min.	Typ.	Max.	Units
I_{PD}	State: PD		45		nA
I_{PG}	State: PG		1.1		mA
I_{RX}	State: RX		2.9		mA
I_{TX_10dBm}	State: TX P_{OUT} = 10 dBm		38		mA
I_{TX_20dBm}	State: TX P_{OUT} = 20 dBm		110		mA

7.1.2 RX

Symbol	Description	Min.	Typ.	Max.	Units
f	Operating frequency range	2360		2500	MHz
G_{RX}	Gain		13		dB
NF_{RX}	Noise figure		2.7		dB
$IMD3_{-50dBm}$	Two tone IMD at -50 dBm Two tone CW, f0: 2440 MHz, f1: +/- 3 MHz, f2: +/- 6 MHz		-109		dBm
$IMD3_{-30dBm}$	Two tone IMD at -30 dBm Two tone CW, f0: 2440 MHz, f1: +/- 3 MHz, f2: +/- 6 MHz		-75		dBm
$H2_{RX}$	Harmonic 2nd (CW, -10 dBm)		-20		dBm
$H3_{RX}$	Harmonic 3rd (CW, -10 dBm)		-17		dBm
S_{11_ANTdB}	ANT port input reflection (over input frequency, 50 Ω)		-7		dB
S_{22_TRXdB}	TRX port output reflection (over input frequency, 50 Ω)		-12.0		dB
$P_{MAX,RX}$	Maximum output power (at TRX, P_{IN} = 0 dBm)		2.5	5.0	dBm

7.1.3 TX

Symbol	Description	Min.	Typ.	Max.	Units
f	Operating frequency range	2360		2500	MHz
P_{SAT}	Saturated output power; GFSK/OQPSK modulation		21.5		dBm
G_{TX}	Power Gain		20		dB
$T_{carrier}$	Carrier switching time P_{OUT} from -30 dBm to +20 dBm			1	µs
$P_{SPUR2MHz}$	In-band spurious emissions 2 MHz (GFSK/OQPSK)			-26	dBm
$P_{SPUR3MHz}$	In-band spurious emissions 3 MHz (GFSK/OQPSK)			-36	dBm
H2, H3	Harmonic, 2nd, 3rd; RBW = 1.0 MHz			-42	dBm
S_{11_TRXdB}	Input reflection at TRX pin (over input frequency range, 50 Ω)		-10		dB
$VSWR_{STB}$	Unconditionally stable				-
$VSWR_{RGN}$	No permanent damage (load 10:1, all phase angles)				-
PAE	Power Added Efficiency		32		%

7.1.4 SPI timing specification

Symbol	Description	Min.	Typ.	Max.	Units
$T_{SPI,START}$	Minimum time from PDN high to SPI is ready to receive data	17.5			µs
T_{SCK}	SCK clock period (50% duty cycle)	112	125		ns
$T_{CSN\text{-}SCK1}$	CSN lead time Time from CSN set to 0 to first rising edge at SCK	62.5			ns
$T_{SCK16\text{-}CSN}$	CSN trail time Time from 16th falling edge at SCK to CSN set to 1	62.5			ns
T_{CSN}	CSN idle time Time required between consecutive transmissions	125			ns
T_{S_MISO}	MISO settling time Guaranteed settling margin for MISO before 9th rising edge at SCK	30			ns

7.2 Typical characteristics

The following figure shows the TX output power control behavior for typical conditions.

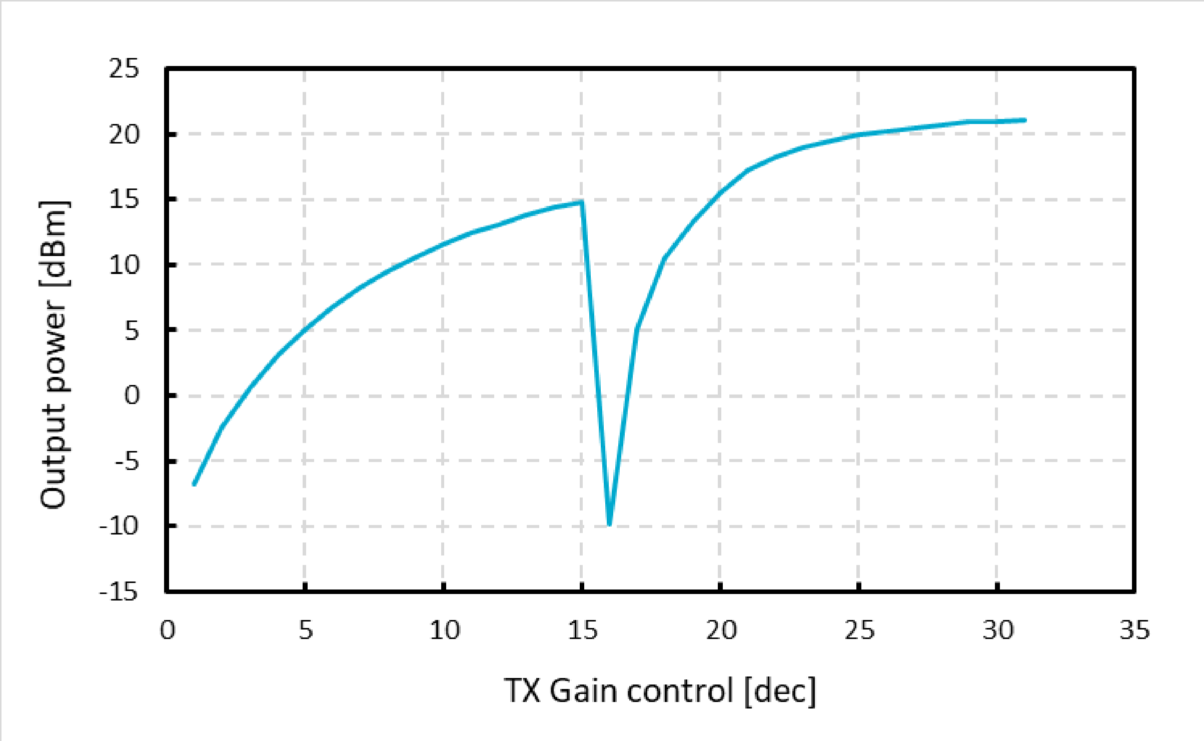

Figure 8: TX gain control behavior

The following figure shows the relationship between TX gain and current consumption.

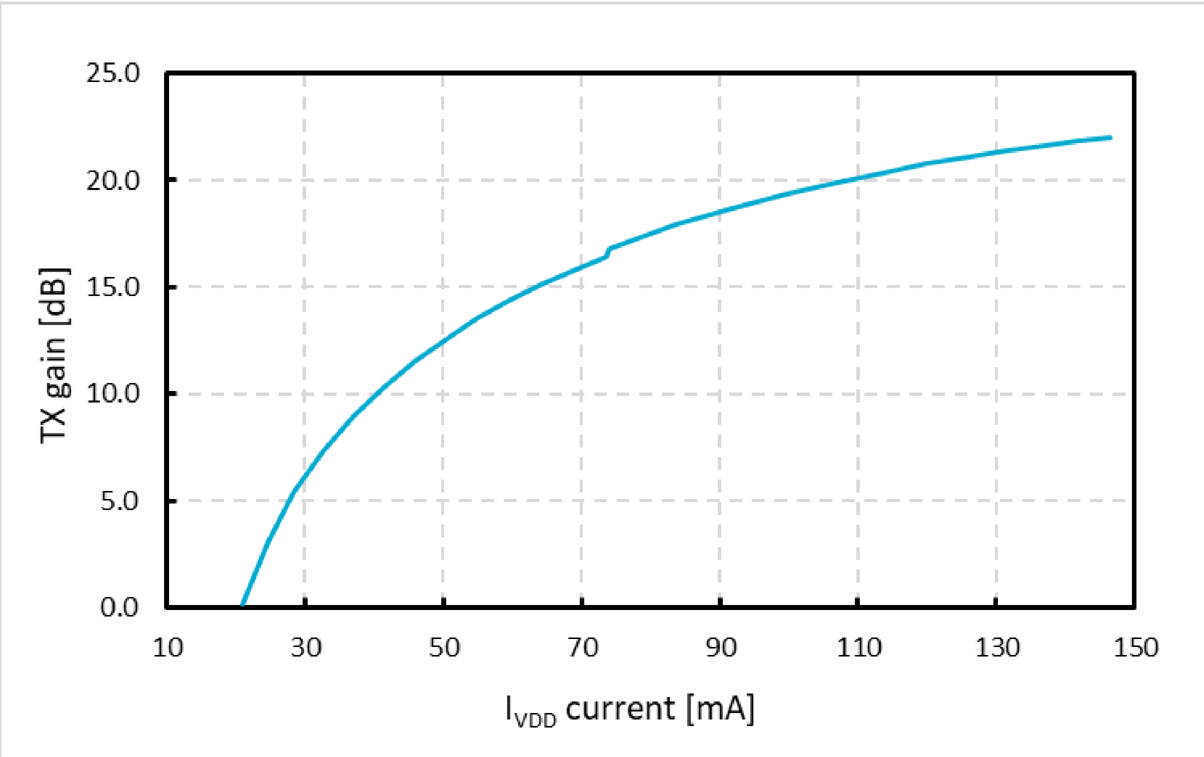

Figure 9: TX gain and current consumption

The following figure shows the TX gain over operating frequency for typical conditions, with register CONFREG0.TX_GAIN=`POUTA_PROD` (20 dB).

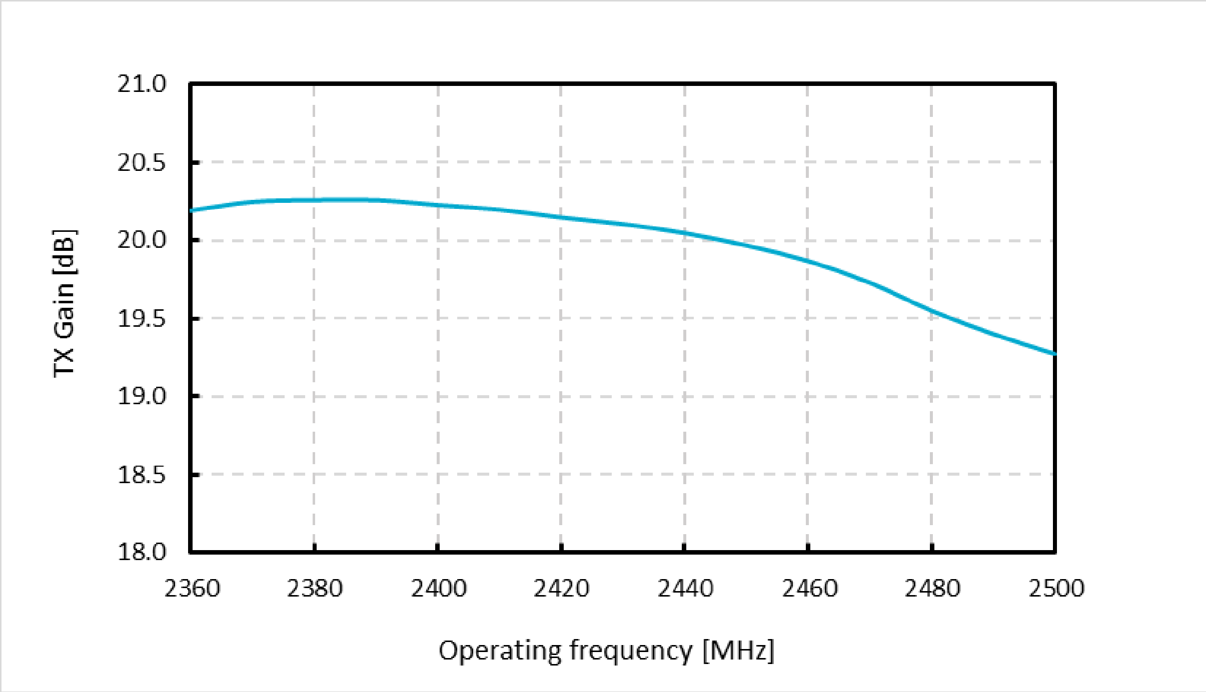

Figure 10: TX gain over operating frequency 20 dB

The following figure shows the TX gain over operating frequency for typical conditions, with register CONFREG0.TX_GAIN=`POUTB_PROD` (10 dB).

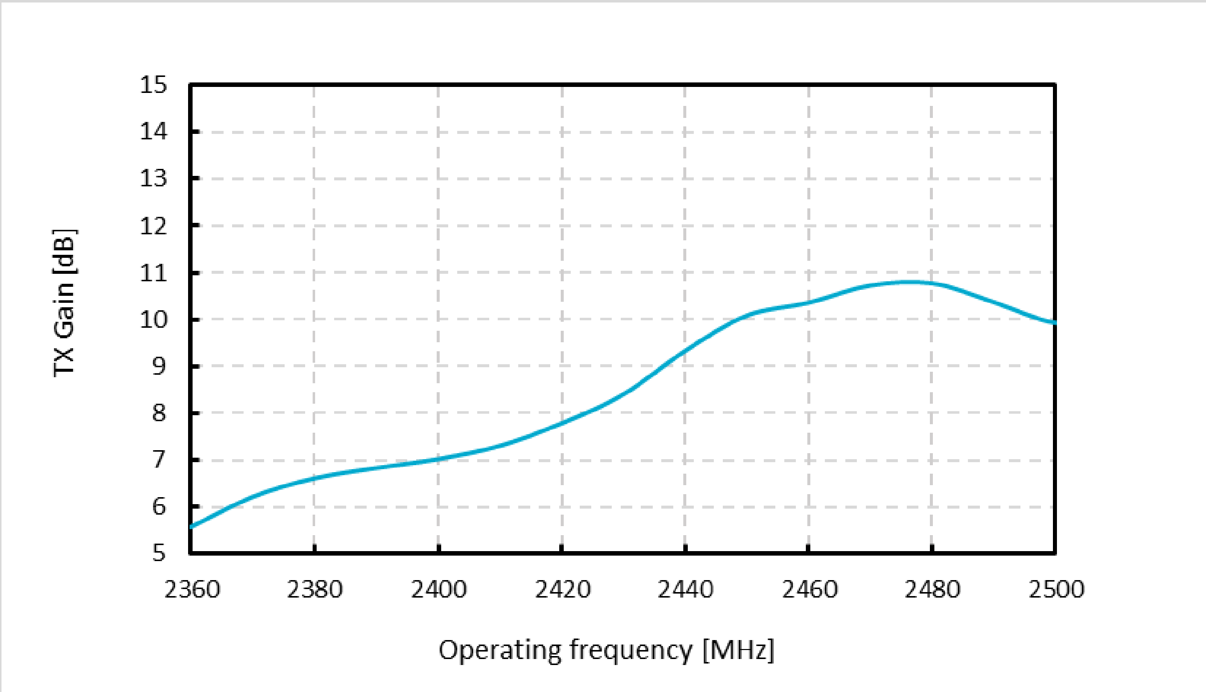

Figure 11: TX gain over operating frequency 10 dB

The following figure shows the TX gain over operating temperature, with register CONFREG0.TX_GAIN=`POUTA_PROD` (20 dB).

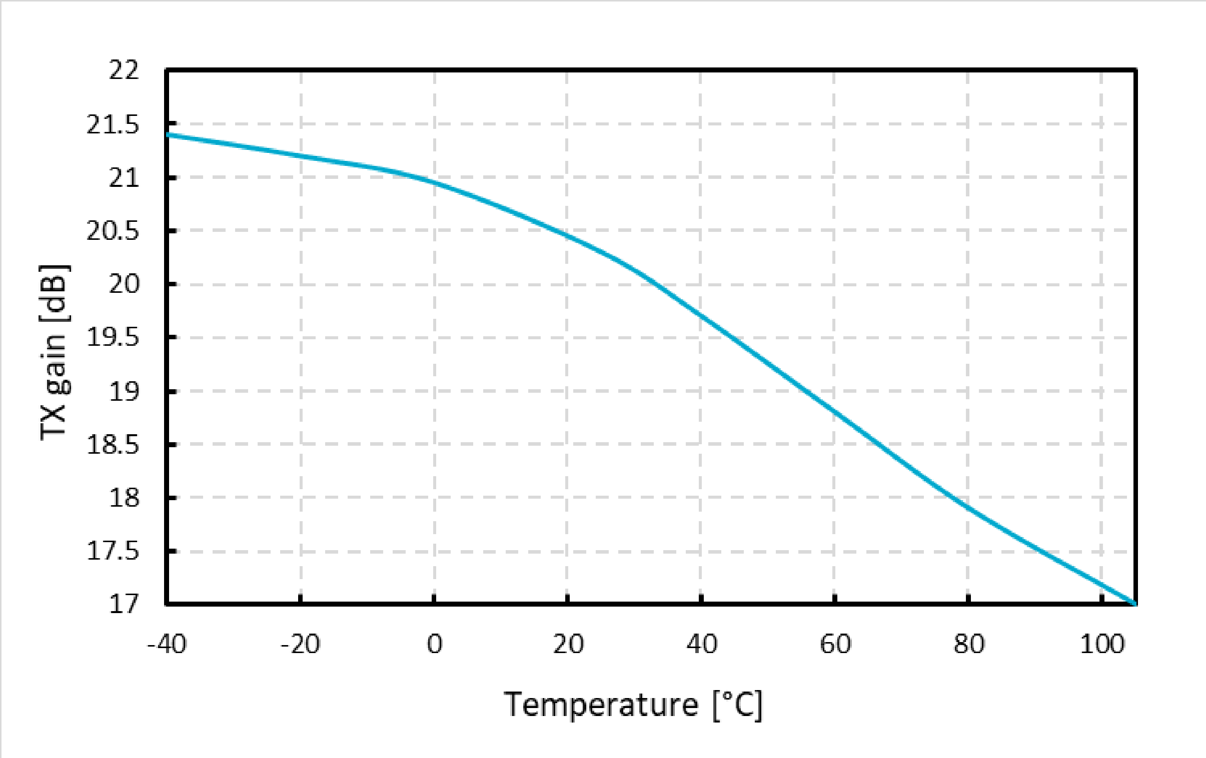

Figure 12: TX gain over temperature 20 dB

The following figure shows the TX gain over operating temperature, with register CONFREG0.TX_GAIN=`POUTB_PROD` (10 dB).

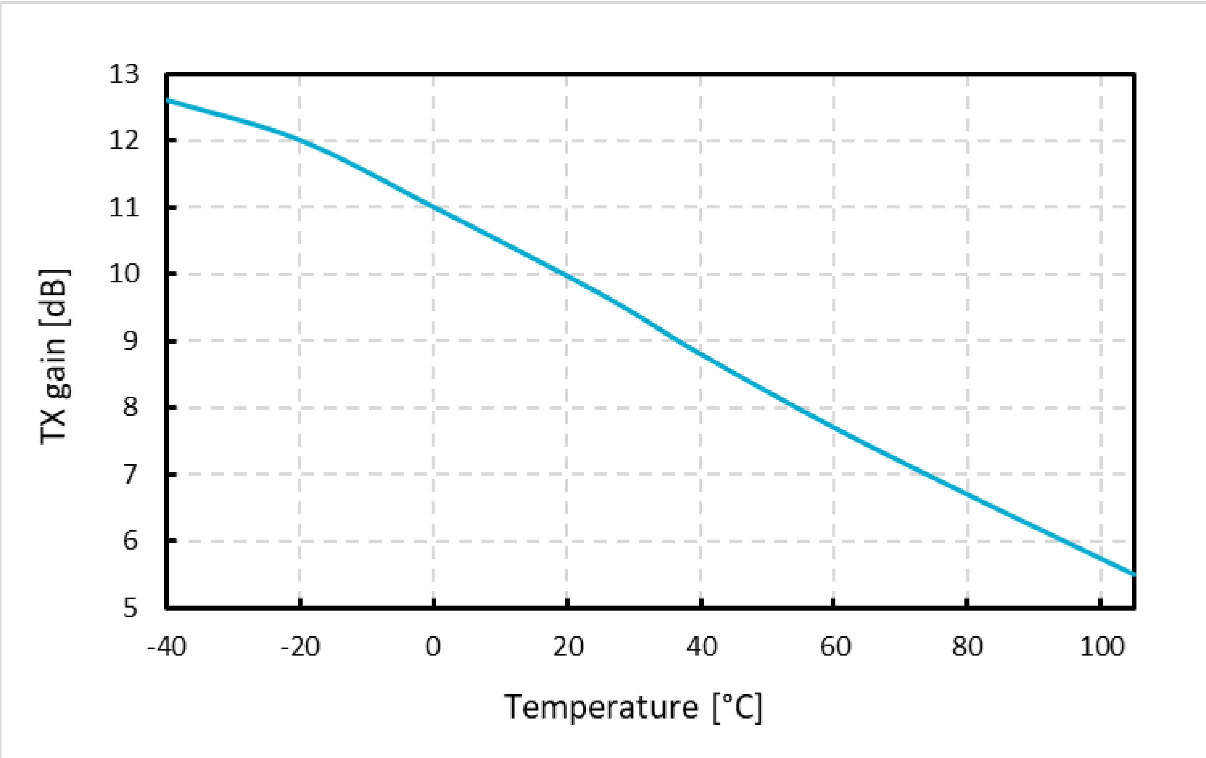

Figure 13: TX gain over temperature 10 dB

The following figure shows the TX gain over VDD, with register CONFREG0.TX_GAIN=`POUTA_PROD` (20 dB).

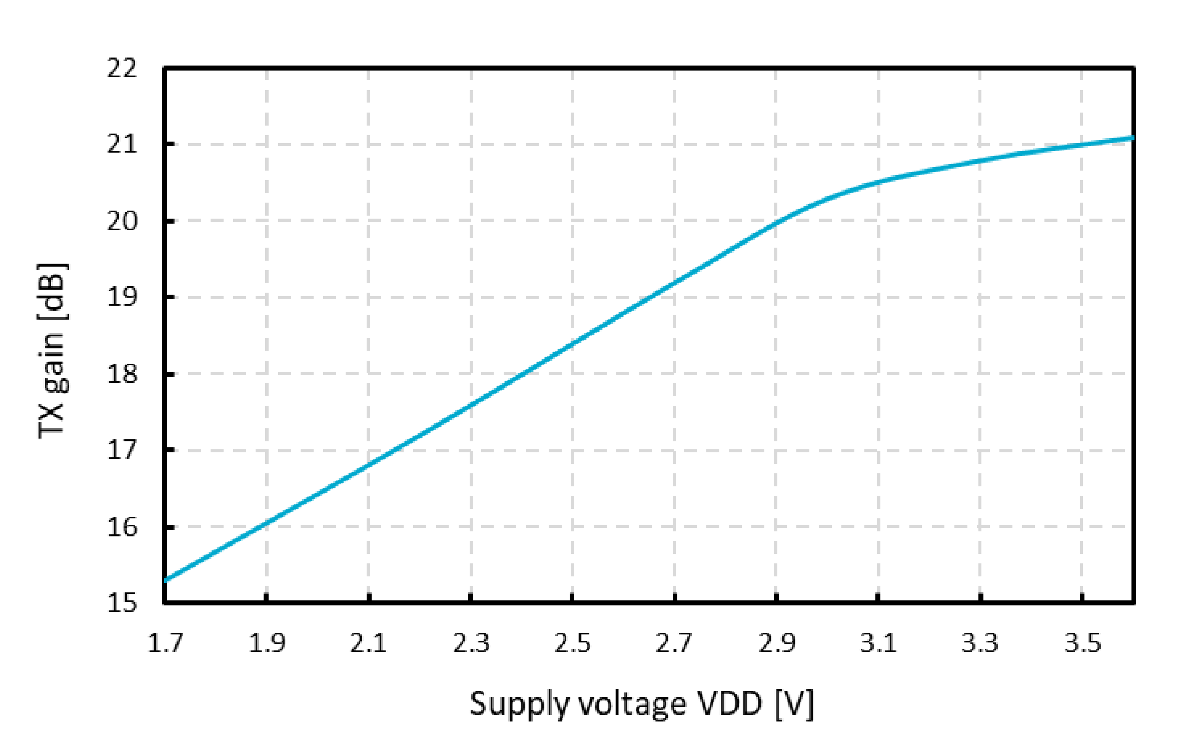

Figure 14: TX gain over VDD 20 dB

The following figure shows the TX gain over VDD, with register CONFREG0.TX_GAIN=`POUTB_PROD` (10 dB).

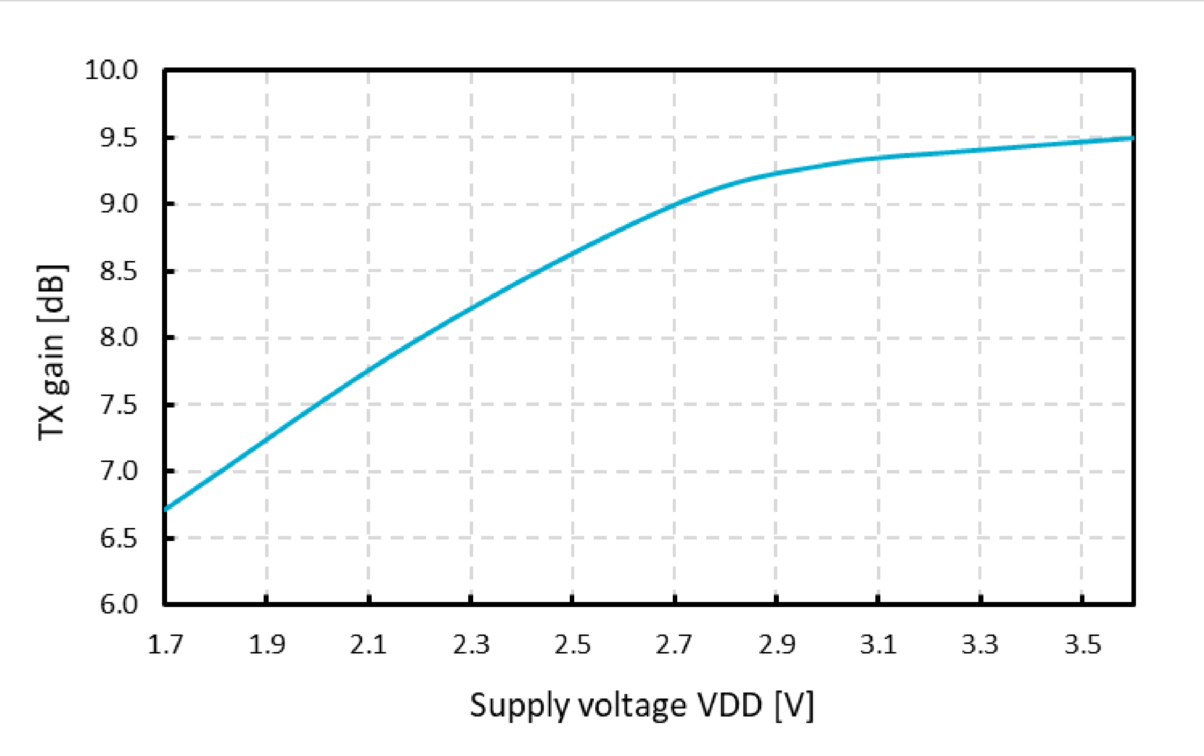

Figure 15: TX gain over VDD 10 dB

The following figure shows the RX gain over the operating frequency.

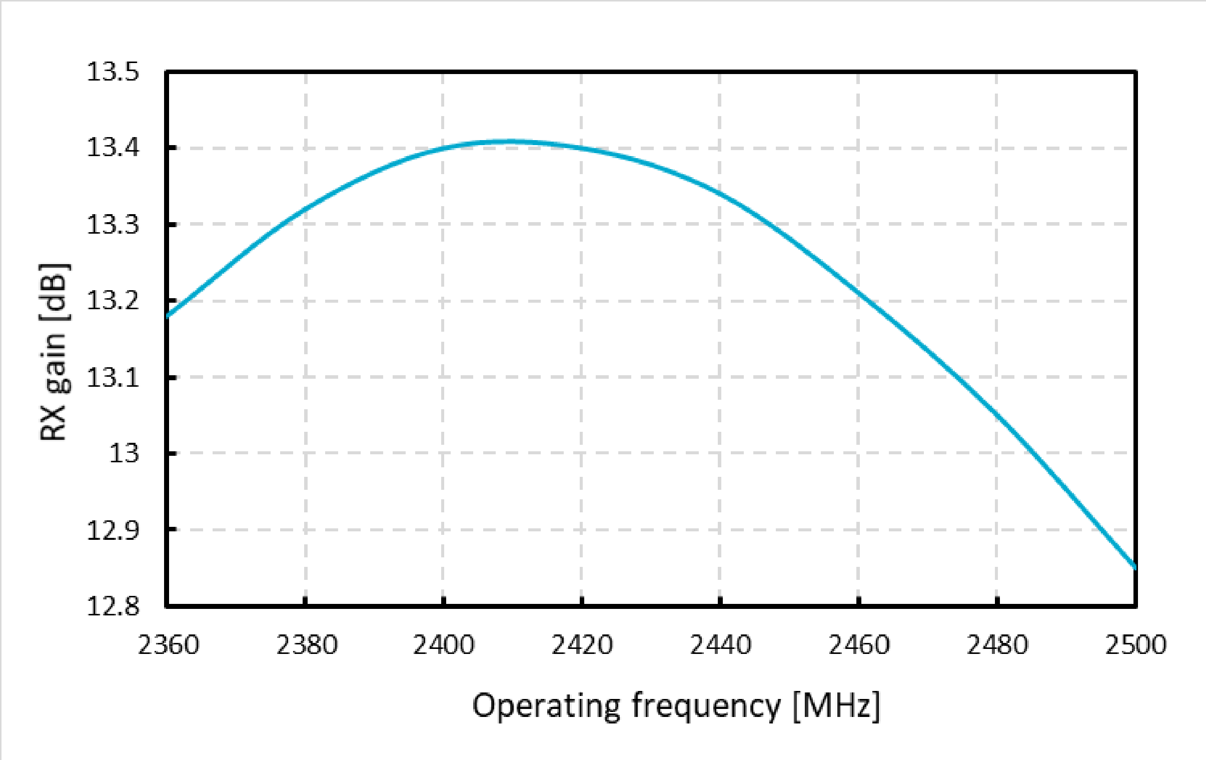

Figure 16: RX gain over operating frequency

The following figure shows the RX gain over temperature.

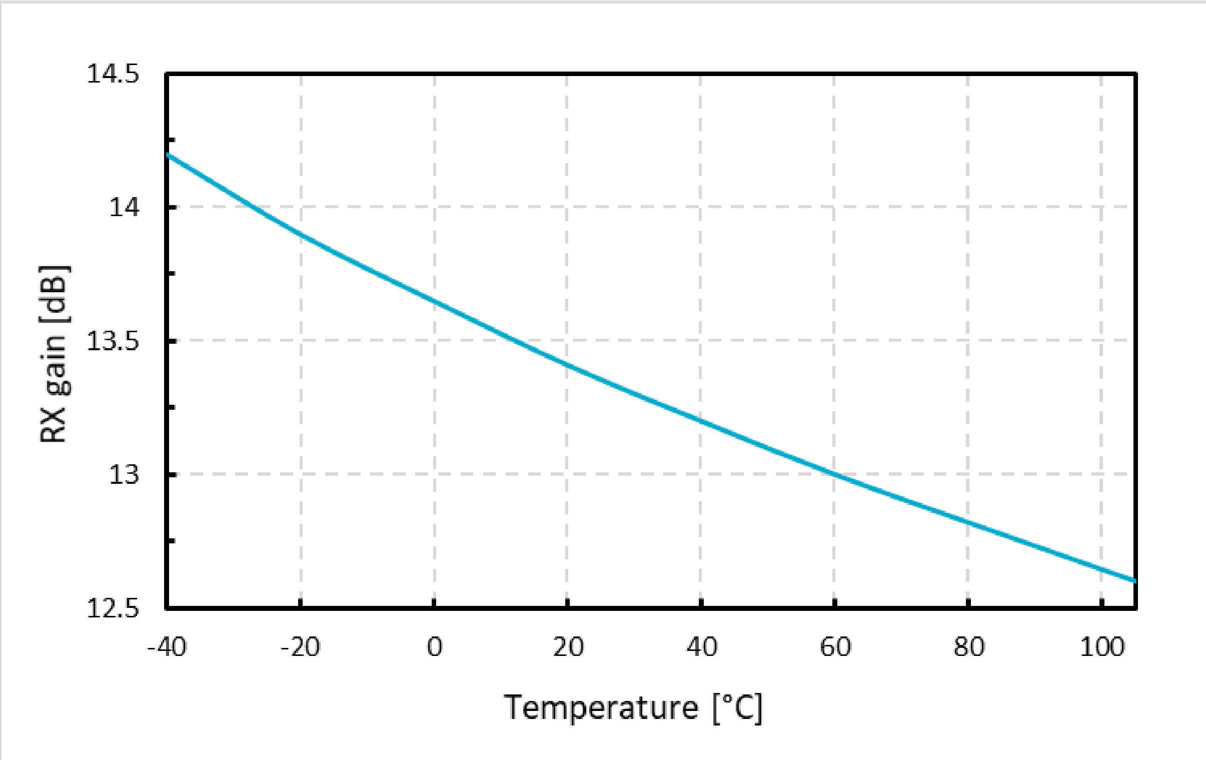

Figure 17: RX gain over temperature

The following figure shows the RX gain over VDD.

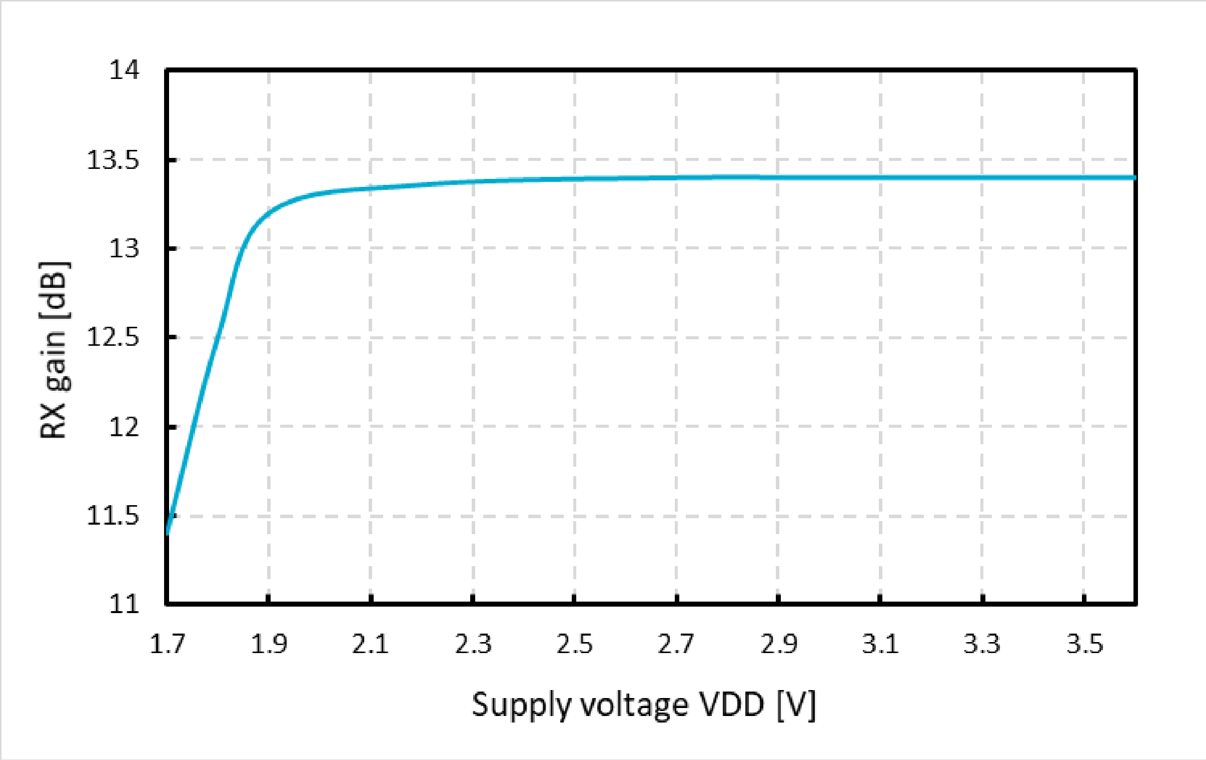

Figure 18: RX gain over VDD

8 Register interface

8.1 Registers

Instances

Instance	Base address	Description
REGIF	0x00000000	Register interface

Register overview

Register	Offset	Description
CONFREG0	0x0	Configuration register 0
CONFREG1	0x1	Configuration register 1
CONFREG2	0x2	Configuration register 2
CONFREG3	0x3	Configuration register 3
PARTNUMBER	0x14	
HW_REVISION	0x15	
HW_ID0	0x16	
HW_ID1	0x17	

8.1.1 CONFREG0

Address offset: 0x0

Configuration register 0

Bit number					7	6	5	4	3	2	1	0
ID						C	C	C	C	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	TX_EN			TX enable
			Disable	0	TX mode disabled
			Enable	1	TX mode enabled
B	RW	MODE			Select preset value of TX output power.
			0	0	TX_Gain = POUTA
			1	1	TX_Gain = POUTB
C	RW	TX_GAIN			TX gain control (0: minimum, 31: maximum) EFUSE value loaded at reset. Initialized with value from POUTA or POUTB. See CONFREG2 and CONFREG3.

8.1.2 CONFREG1

Address offset: 0x1

Configuration register 1

Bit number	7	6	5	4	3	2	1	0
ID	E	E	E	E		C		A
Reset 0x00	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	RX_EN			RX enable
			Disable	0	RX mode disabled
			Enable	1	RX mode enabled
C	RW	UICR_EN			UICR program mode enable
			Disable	0	
			Enable	1	
E	RW	KEY			UICR program mode enter/leave key
			Enter	15	Set to 0xF when enabling UICR program mode
			Leave	0	Set to 0x0 when leaving UICR program mode

8.1.3 CONFREG2

Address offset: 0x2

Configuration register 2

Bit number	7	6	5	4	3	2	1	0
ID	D		B	A	A	A	A	A
Reset 0x00	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	POUTA_UICR			User defined initialization value for POUTA (0: minimum - PA disabled, 31: maximum)
B	RW	POUTA_SEL			
			0	0	TX_Gain initialized with POUTA_PROD (20 dBm +/- 0.5 dB)
			1	1	TX_Gain initialized with POUTA_UICR
D	RW	WR_UICR			Write UICR memory
			0	0	EFUSE idle
			1	1	EFUSE write

8.1.4 CONFREG3

Address offset: 0x3

Configuration register 3

Bit number	7	6	5	4	3	2	1	0
ID			B	A	A	A	A	A
Reset 0x00	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	POUTB_UICR			User defined initialization value for POUTB (0: minimum - PA disabled, 31: maximum)
B	RW	POUTB_SEL			
			0	0	TX_Gain initialized with POUTB_PROD (10 dBm +/- 1.5 dB)
			1	1	TX_Gain initialized with POUTB_UICR

8.1.5 PARTNUMBER

Address offset: 0x14

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0xFF						**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	R	PARTNUMBER			Part identification number								
			21540	0x0C	nRF21540								

8.1.6 HW_REVISION

Address offset: 0x15

Bit number						7	6	5	4	3	2	1	0
ID						B	B	B	B				
Reset 0xFF						**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description								
B	R	HW_REVISION			HW revision code								
			QD	0x2	QFN16								

8.1.7 HW_ID0

Address offset: 0x16

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0xFF						**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	R	HW_ID0			Hardware ID, MSB								
			AAG0	0x02									

8.1.8 HW_ID1

Address offset: 0x17

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0xFF						**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	R	HW_ID1			Hardware ID, LSB								
			AAG0	0x1C									

9 Hardware and layout

9.1 Pin assignments

The pin assignment figure and tables describe the pinouts for the device. There are also recommendations for how the GPIO pins should be configured, in addition to any usage restrictions.

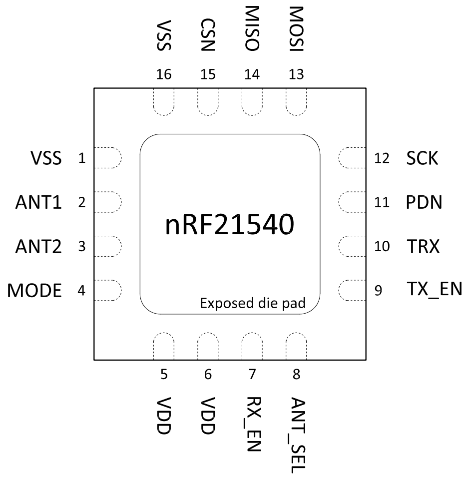

Figure 19: QFN16 pin assignments, top view

Pin number	Pin name	Type	Description
1	**VSS**	Power	Ground
2	**ANT1**	RF I/O	First antenna interface
3	**ANT2**	RF I/O	Second antenna interface
4	**MODE**	Digital IN	TX power mode control
5	**VDD**	Power	Supply voltage
6	**VDD**	Power	Supply voltage
7	**RX_EN**	Digital IN	RX mode enable
8	**ANT_SEL**	Digital IN	Antenna select
9	**TX_EN**	Digital IN	TX mode enable
10	**TRX**	RF IO	Transceiver interface
11	**PDN**	Digital IN	Power-down, active low
12	**SCK**	Digital IN	SPI clock Connect to VSS if SPI interface is not used
13	**MOSI**	Digital IN	SPI data in Connect to VSS if SPI interface is not used
14	**MISO**	Digital OUT	SPI data out Leave unconnected if SPI interfaces is not used
15	**CSN**	Digital IN	SPI chip select, active low Connect to VDD if SPI interface is not used
16	**VSS**	Power	Ground
DAP	**VSS**	Power	Ground

Table 9: Pin assignments

9.2 Mechanical specifications

The mechanical specifications for the package shows the dimensions in millimeters.

9.2.1 QFN 4 x 4 mm package

Dimensions in millimeters for the QFN 4 x 4 mm package.

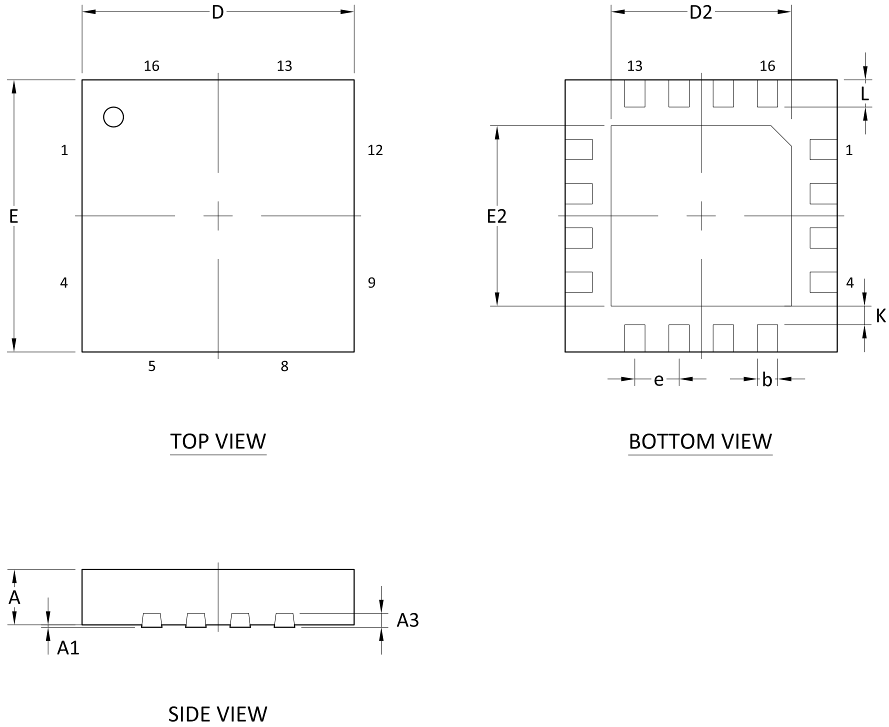

Figure 20: QFN 4 x 4 mm package

	A	A1	A3	b	D	E	D2	E2	e	K	L
Min.	0.8	0		0.25			2.55	2.55			0.35
Nom.	0.85	0.035	0.203	0.3	4	4	2.65	2.65	0.65		0.4
Max.	0.9	0.05		0.35			2.75	2.75			0.45

Table 10: QFN dimensions in millimeters

9.3 Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from the product page for the nRF21540 on www.nordicsemi.com.

9.3.1 Schematic with single antenna

The reference circuitry schematic shows the single antenna application schematic.

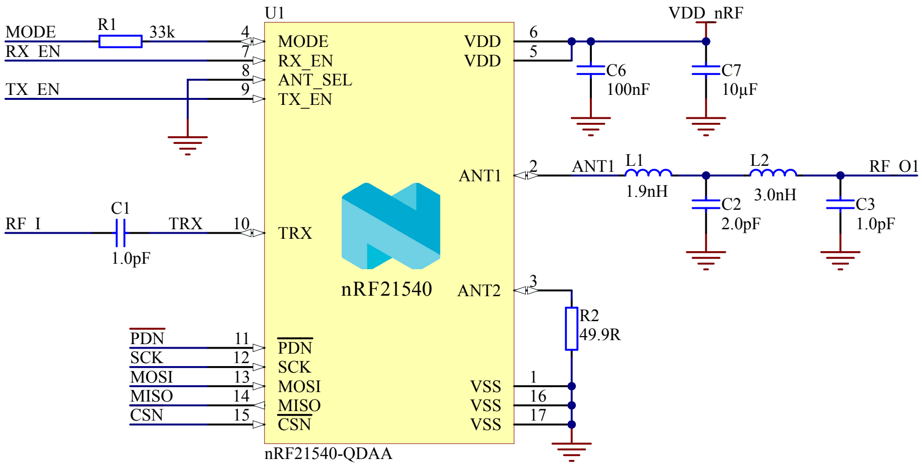

Figure 21: Reference circuitry schematic for single antenna

The following table lists the recommended and tested component types and values.

Designator	Value	Description	Footprint
C1, C3	1.0 pF	Capacitor, NP0, ±0.05 pF	0201
C2	2.0 pF	Capacitor, NP0, ±0.05 pF	0201
C6	100 nF	Capacitor, X5R, ±10%	0201
C7	10 µF	Capacitor, X5R, ±20%	0603
L1	1.9 nH	High frequency chip inductor, ±0.1 nH, 120 mΩ	0201
L2	3.0 nH	High frequency chip inductor, ±0.1 nH, 120 mΩ	0201
R1	33 kΩ	Resistor, ±1%	0201
R2	49.9 Ω	Resistor, ±1%	0201
U1	nRF21540-QDAA	Radio front-end/range extender for 2.4 GHz	QFN-16

Table 11: Bill of material for QFN16

9.3.2 Schematic with dual antenna

The reference circuitry schematic shows the dual antenna application schematic.

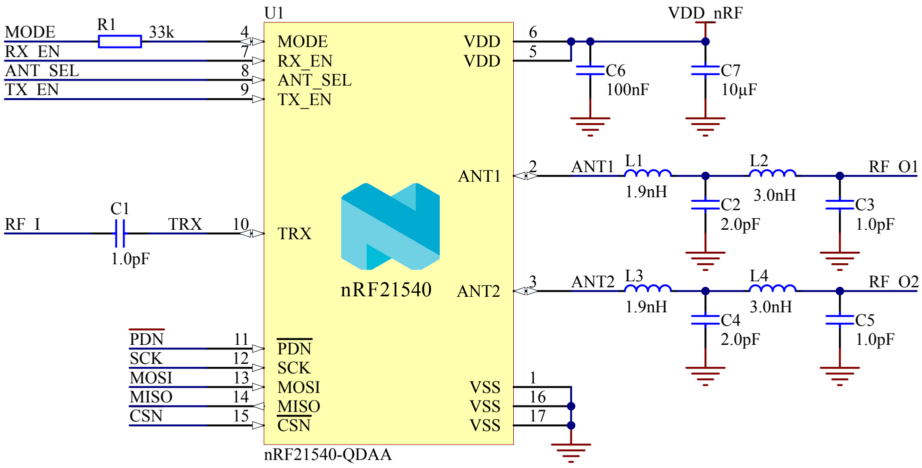

Figure 22: Reference circuitry schematic for dual antenna

The following table lists the recommended and tested component types and values.

Designator	Value	Description	Footprint
C1, C3, C5	1.0 pF	Capacitor, NP0, ±0.05 pF	0201
C2, C4	2.0 pF	Capacitor, NP0, ±0.05 pF	0201
C6	100 nF	Capacitor, X5R, ±10%	0201
C7	10 µF	Capacitor, X5R, ±20%	0603
L1, L3	1.9 nH	High frequency chip inductor, ±0.1 nH, 120 mΩ	0201
L2, L4	3.0 nH	High frequency chip inductor, ±0.1 nH, 120 mΩ	0201
R1	33 kΩ	Resistor, ±1%	0201
U1	nRF21540-QDAA	Radio front-end/range extender for 2.4 GHz	QFN-16

Table 12: Bill of material for QFN16

10 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	Main supply voltage/battery	Functional range	1.7	3.0	3.6	V
V_{IH}	Digital input high	SPI, PDN, ANT_SEL	0.7 V_{VDD}		V_{VDD}	V
V_{IL}	Digital input low	SPI, PDN, ANT_SEL	V_{VSS}		0.3 V_{VDD}	V
F_{SCK}	SPI clock frequency	Exceeding may cause SPI malfunction		8	8.9	MHz
C_{MISO}	MISO load capacitance	Exceeding may cause SPI read malfunction			50	pF
T_{OP}	Operating temperature range	Board temperature, 1 mm from the package	-40	+25	+105	°C
Z_L	Load impedance			50		Ω

Table 13: Recommended operating conditions

11 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed to for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Pin	Note	Min.	Max.	Unit
VDD	Supply voltage	0	3.6	V
VSS	Supply voltage		0	V
$V_{I/O}$	Digital I/O pin voltage VDD ≤ 3.6 V	-0.3	VDD + 0.3	V
P_{IN_TRX}	RF I/O pin input power CW, Transmit mode		+5	dBm
P_{IN_ANT}	RF I/O pin input power CW, Receive/Program mode		+15	dBm

Table 14: Pin voltage

	Note	Min.	Max.	Unit
Storage temperature		-40	125	°C
Reflow soldering temperature	IPC/JEDEC J-STD-020		260	°C
MSL	Moisture sensitivity level 2			
ESD HBM	Human Body Model		1	kV
ESD CDM	Charged Device Model		2	kV

Table 15: Environmental

12 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

12.1 Package marking

The nRF21540 package is marked as shown in the following figure.

N	2	1	5	4	0
<P	P>	<V	V>	<H>	<P>
<Y	Y>	<W	W>	<L	L>

Figure 23: Package marking

12.2 Box labels

The following figures show the box labels used for nRF21540.

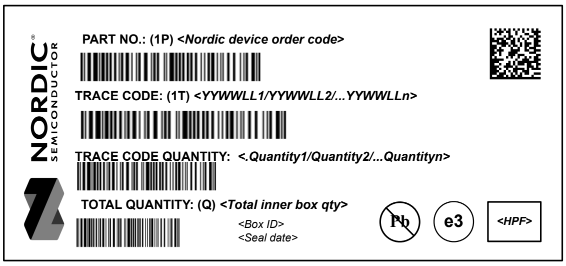

Figure 24: Inner box label

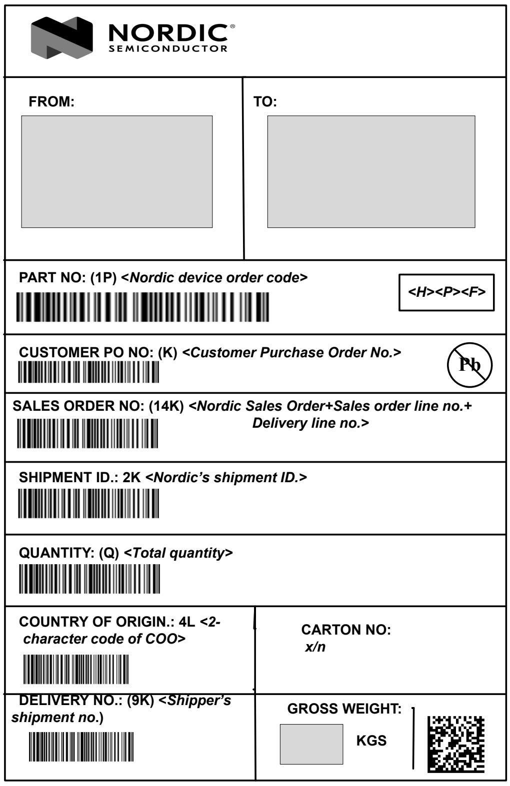

Figure 25: Outer box label

12.3 Order code

The following are the order codes and definitions for nRF21540.

n	R	F	2	1	5	4	0	-	<P	P>	<V	V>	-	<C	C>

Figure 26: Order code

Abbreviation	Definition and implemented codes
N21/nRF21	nRF21 series product
540	Part code
<PP>	Package variant code
<VV>	Function variant code
<H><P><F>	Build code H - Hardware version code P - Production configuration code (production site, etc.) F - Firmware version code (only visible on shipping container label)
<YY><WW><LL>	Tracking code YY - Year code WW - Assembly week number LL - Wafer lot code
<CC>	Container code

Table 16: Abbreviations

12.4 Code ranges and values

Defined here are the nRF21540 code ranges and values.

<PP>	Package	Size (mm)	Pin/Ball count	Pitch (mm)
QD	QFN	4 x 4	16	0.65

Table 17: Package variant codes

<VV>	Description
AA	Production variant

Table 18: Function variant codes

<H>	Description
[A . . Z]	Hardware version/revision identifier (incremental)

Table 19: Hardware version codes

<P>	Description
[0 . . 9]	Production device identifier (incremental)
[A . . Z]	Engineering device identifier (incremental)

Table 20: Production configuration codes

<F>	Description
[A . . N, P . . Z]	Version of preprogrammed firmware
[0]	Delivered without preprogrammed firmware

Table 21: Production version codes

<YY>	Description
[16 . . 99]	Production year: 2016 to 2099

Table 22: Year codes

<WW>	Description
[1 . . 52]	Week of production

Table 23: Week codes

<LL>	Description
[AA . . ZZ]	Wafer production lot identifier

Table 24: Lot codes

<CC>	Description
R7	7" Reel
R	13" Reel

Table 25: Container codes

12.5 Product options

Defined here are the nRF21540 product options.

Order code	MOQ[1]
nRF21540-QDAA-R	4000 pcs
nRF21540-QDAA-R7	1500 pcs

Table 26: nRF21540 order codes

Order code	Description
nRF21540-DB	nRF21540 Development Bundle

Table 27: Development tools order code

1 Minimum Ordering Quantity

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