nPM1300 Revision 1

Errata v1.0



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1 nPM1300 Revision 1 Errata

This Errata document contains anomalies and configurations for the nPM1300 chip, Revision 1 (QEAA-C00, CAAA-C00).

The document indicates which anomalies are fixed, inherited, or new compared to Engineering C.



2 Revision history

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nPM1300 Revision 1 v1.0	25.10.2023	 Added: No. 27. "Programming BUCK voltage increases current consumption" Added: No. 28. "BUCK mode transition is outside of specification" Added: No. 30. "BUCK output voltage accuracy is outside specification" Added: No. 31. "Increased BUCK Hysteretic quiescent current" Added: No. 32. "Reduced BUCK Hysteretic efficiency "



3 New and inherited anomalies

The following anomalies are present in Revision 1 of the nPM1300 chip.

ID	Module	Description	New in Revision 1	Inherited from Engineering C
27	BUCK	Programming BUCK voltage increases current consumption		х
28	BUCK	BUCK mode transition is outside of specification		Х
30	BUCK	BUCK output voltage accuracy is outside specification		Х
31	BUCK	Increased BUCK Hysteretic quiescent current	Х	
32	BUCK	Reduced BUCK Hysteretic efficiency		Х

Table 1: New and inherited anomalies

3.1 [27] BUCK: Programming BUCK voltage increases current consumption

This anomaly applies to Revision 1, build codes QEAA-C00, CAAA-C00.

It was inherited from the previous IC revision Engineering C.

Symptoms

Quiescent current of BUCK is higher than expected.

Conditions

Host software sets BUCK voltage for the first time after a power-up event, and the value is the same as the voltage already set by VSET resistor. This is done by setting BUCKnSWCTRLSEL to SWCTRL while BUCKnNORMVOUT and BUCKnVOUTSTATUS are equal.

Consequences

BUCK quiescent current increases by 1 mA.

Workaround

Host software must initially ensure BUCKnNORMVOUT and BUCKnVOUTSTATUS are not equal when BUCKnSWCTRLSEL is set. Host software can set BUCKnNORMVOUT equal to BUCKnVOUTSTATUS once an alternate BUCKnNORMVOUT has been set.



3.2 [28] BUCK: BUCK mode transition is outside of specification

This anomaly applies to Revision 1, build codes QEAA-C00, CAAA-C00.

It was inherited from the previous IC revision Engineering C.

Symptoms

BUCK changes mode from Hysteretic to PWM or from PWM to hysteretic at a load current that deviates from typical specification. Increased output voltage ripple or increased quiescent current might be seen as a result of this.

Conditions

BUCK is enabled in AUTO mode. When input voltage is above 4.2 V and output voltage is set below 1.4 V, PWM to Hysteretic transition level has an increased spread. For high input voltages and high output voltages, Hysteretic to PWM transition can happen at a lower load current than expected.

Consequences

When BUCK is in PWM instead of being in Hysteretic mode, BUCK quiescent current can increase by approximately 4 mA causing lower efficiency at light load currents. When BUCK is toggling between PWM and Hysteretic modes, increased output voltage ripple might be observed.

Workaround

Force hysteretic or PWM mode through TWI or through a configured GPIO from host software. Choose mode to maximize efficiency.

3.3 [30] BUCK: BUCK output voltage accuracy is outside specification

This anomaly applies to Revision 1, build codes QEAA-C00, CAAA-C00.

It was inherited from the previous IC revision Engineering C.

Symptoms

BUCK output voltage exhibits a negative transient.

Conditions

One or both of the following conditions are present:

- Data is transmitted on TWI lines.
- BUCK is transitioning mode from PWM to Hysteretic when BUCKS are in auto mode and nPM1300 supplied only by VBAT. Resulting transient duration depends on load. Lower loads exhibit a longer transient.



Consequences

BUCK output voltage transient exceeds specification of $\pm 5\%$. BUCK output voltage reduces by approximately 8%.

Workaround

If data is being transmitted on TWI lines, avoid TWI activity when output voltage accuracy is critical. Reducing driver strength of TWI reduces inaccuracy.

If BUCK is transitioning mode from PWM to Hysteretic when BUCKS are in auto mode and nPM1300 supplied only by VBAT, use forced PWM or Hysteric mode when output voltage accuracy is critical.

3.4 [31] BUCK: Increased BUCK Hysteretic quiescent current

This anomaly applies to Revision 1, build codes QEAA-C00, CAAA-C00.

Symptoms

BUCK quiescent current increases during Hysteretic load currents below typically 5 mA.

Conditions

BUCK load current has decreased to below 20 mA while in Hysteretic mode.

Consequences

BUCK quiescent current increases by approximately 300 µA.

Workaround

Prompt read or write over TWI from host below a load current of 5 mA.

3.5 [32] BUCK: Reduced BUCK Hysteretic efficiency

This anomaly applies to Revision 1, build codes QEAA-C00, CAAA-C00.

It was inherited from the previous IC revision Engineering C.

Symptoms

BUCK Hysteretic efficiency is 10% points lower than typically specified.

Conditions

BUCK is in Hysteretic mode.

Consequences

BUCK efficiency is reduced. Power draw is increased while in Hysteretic mode.



Workaround

None.



4 Fixed anomalies

The anomalies listed in this table are no longer present in the current chip version.

For a detailed description of the fixed anomalies, see the Errata for Engineering C.

ID	Module	Description
24	BUCK, CONTROL	Restart fails after reset with VBUS and VBAT connected
26	SYSREG	nPM1300 is not USB compliant
29	BUCK	Increased BUCK Hysteretic quiescent current

Table 2: Fixed anomalies

