

## Product Anomaly Notification (PAN)

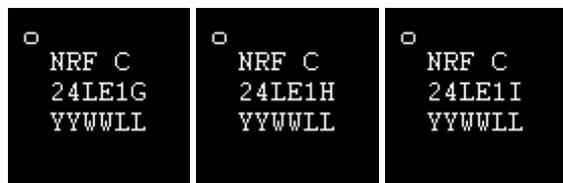
<b>Device affected</b> (product name): nRF24LE1-O17Q24/Q32/Q48	<b>Device version(s) affected:</b> A, C, M
<b>Date (YYYY-MM-DD):</b> 2011-01-26	<b>PAN no.:</b> PAN-018
<b>Nordic Semiconductor reference:</b> Thomas Embla Bonnerud, Product Manager	<b>Document version:</b> 4.1

### Summary

#### Anomalies:

1. Wakeup from Register Retention power-down mode fails under the conditions that XOSC16M is ON in power-down and XOSC16M is the only 16 MHz clock source
2. The chip fails to wakeup from power down mode: Deep Sleep, Memory Retention timers on and Memory Retention timers off.

#### Marking / tracing:



Build: C

Build: C

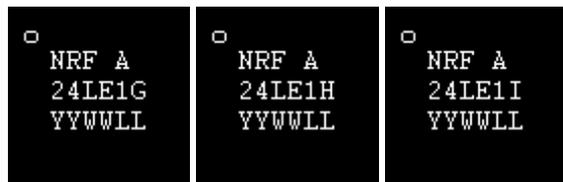
Build: C



Build: M

Build: M

Build: M



Build: A

Build: A

Build: A

Please refer to nRF24LE1 OTP Product Specification for package marking details.  
 Any package type, year, week and lot number does have this anomaly.

#### Authorization for Nordic Semiconductor

Product Manager

Date: 2011-01-26

Sign:

Thomas Embla Bonnerud



## Detailed Description

<b>1.</b>
<b>Symptoms:</b> Code execution after wakeup from Register Retention will behave unpredictably
<b>Conditions:</b> The following firmware settings for clock to the microcontroller system are made before entering power-down: - CLKCTRL[7] = '1' (Keep XOSC16M on in Register Retention mode) - CLKCTRL[5:4] = '10' (Start XOSC16M only)
<b>Consequences:</b> The device will not wake up from Register Retention
<b>Workaround:</b> In nRF24LE1-O firmware, preset start of both 16 MHz oscillators before entering Register Retention:  CLKCTRL[5:4] = '00'  Clock will be sourced from RCOSC16M initially and automatically switched to XOSC16M. At this point in time RCOSC16M will be stopped by hardware

<b>2.</b>
<b>Symptoms:</b> The chip fails to wakeup from power down mode: Deep Sleep, Memory Retention timers on and Memory Retention timers off.
<b>Conditions:</b> Not all devices are affected by this anomaly. Testing indicates that between 10 to 30% are affected and if it is affected the anomaly have no dependence on external conditions like supply voltage or temperature. Even if the device is affected it may wake-up from power down mode, but sooner or later it will fail to wake-up.
<b>Consequences:</b> The chips that fail to wakeup will remain in the power down mode until reset by reset pin or power on reset.
<b>Workaround:</b> Use power down mode Register Retention instead of power down mode Deep Sleep, Memory Retention timers on and Memory Retention timers off.  The consequence of this workaround is an increase in power consumption of 0,5uA – 1,5uA depending of the initial power down mode used. Please refer to nRF24LE1 OTP Product Specification for differences between the power down modes.