nRF52840
Engineering A

Errata

v1.6

NORDIC®
SEMICONDUCTOR

Contents

1 nRF52840 Engineering A Errata

This Errata document contains anomalies for the nRF52840 chip, revision Engineering A (QIAA-AA0).

NORDIC
SEMICONDUCTOR

2 Change log

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nRF52840 Engineering A v1.6	30.05.2018	• Added: No. 200. "Cannot write to SIZE.EPOUT register"
nRF52840 Engineering A v1.5	23.03.2018	• Updated: No. 89. "Static 400 μA current while using GPIOTE" • Updated: No. 122. "QSPI uses current after being disabled" • Updated: No. 171. "USB might not power up" • Added: No. 192. "LFRC frequency offset after calibration" • Added: No. 194. "STOP task does not switch off all resources" • Added: No. 196. "PSEL acquires GPIOs regardless of ENABLE" • Added: No. 201. "EVENTS_HFCLKSTARTED might be generated twice"
nRF52840 Engineering A v1.4	09.02.2018	• Updated: No. 143. "False CRC failures on specific addresses" • Updated: No. 164. "Low selectivity in long range mode" • Added: No. 154. "USBD acknowledges setup stage without STATUS task" • Added: No. 162. "Writing to registers with offset address 0x52C causes USB to halt" • Added: No. 171. "USB might not power up"
nRF52840 Engineering A v1.3	13.11.2017	• Added: No. 78. "High current consumption when using timer STOP task only" • Added: No. 158. "High power consumption in DISABLED state" • Added: No. 166. "ISO double buffering not functional" • Added: No. 170. "NRF_I2S->PSEL CONNECT fields are not readable" • Added: No. 173. "Writes to LATCH register take several CPU cycles to take effect" • Added: No. 176. "Flash erase through CTRL-AP fails due to watchdog time-out" • Added: No. 179. "COMPARE event is generated twice from a single RTC compare match" • Added: No. 180. "Wrong PLL calibration in production" • Added: No. 181. "Invalid value in FICR for double-size NFCID1 " • Added: No. 183. "False SEQEND[0] and SEQEND[1] events" • Added: No. 184. "Erase or write operations from the external debugger fail when CPU is not halted"

NORDIC
SEMICONDUCTOR

Version	Date	Change
nRF52840 Engineering A v1.2	12.07.2017	• Updated: No. 66. "Linearity specification not met with default settings" • Updated: No. 142. "Sensitivity not according to specification" • Added: No. 143. "False CRC failures on specific addresses" • Added: No. 153. "RSSI parameter adjustment" • Added: No. 155. "IN event may occur more than once on input edge" • Added: No. 156. "Some CLR tasks give unintentional behavior" • Added: No. 160. "VDDHDIV5 not functional" • Added: No. 164. "Low sensitivity in long range mode"
nRF52840 Engineering A v1.1	21.04.2017	• Revoked (invalid): No. 51. "Aligned stereo slave mode does not work" • Added: No. 97. "High current consumption in System ON Idle mode" • Revoked (invalid): No. 101. "Sleep current increases after soft reset" • Updated: No. 115. "RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode" • Revoked (invalid): No. 129. "Reading EPSTALL register causes undefined behavior" • Revoked (invalid): No. 130. "Writing to certain read-only registers causes undefined behavior" • Updated: No. 136. "Bits in RESETREAS are set when they should not be" • Added: No. 144. "Not optimal NFC performance " • Added: No. 145. "SPIM3 not functional" • Added: No. 147. "LFRC ULP mode not calibrated in production" • Added: No. 150. "EVENT_STARTED does not fire" • Added: No. 151. "Access to protected memory through Cache"

NORDIC
SEMICONDUCTOR

Version	Date	Change
nRF52840 Engineering A v1.0	06.12.2016	- Added: No. 15. "RAM[x].POWERSET/CLR read as zero" - Added: No. 20. "Register values are invalid" - Added: No. 36. "Some registers are not reset when expected" - Added: No. 51. "Aligned stereo slave mode does not work" - Added: No. 54. "Wrong LRCK polarity in Aligned mode" - Added: No. 55. "RXPTRUPD and TXPTRUPD events asserted after STOP" - Added: No. 58. "An additional byte is clocked out when RXD.MAXCNT = 1" - Added: No. 66. "Linearity specification not met with default settings" - Added: No. 68. "EVENTS_HFCLKSTARTED can be generated before HFCLK is stable" - Added: No. 81. "PIN_CNF is not retained when in debug interface mode" - Added: No. 83. "STOPPED event occurs twice if the STOP task is triggered during a transaction" - Added: No. 87. "Unexpected wake from System ON Idle when using FPU" - Added: No. 89. "Static 400 µA current while using GPIOTE" - Added: No. 94. "BUSSTATE register is not functional" - Added: No. 96. "DMA buffers can only be located in the first 64 kB of data RAM" - Added: No. 98. "Not able to communicate with the peer" - Added: No. 101. "Sleep current increases after soft reset" - Added: No. 103. "Reset value of CCM.MAXPACKETSIZE causes encryption, decryption, and MIC failures" - Added: No. 104. "EPDATA event is not always generated" - Added: No. 110. "Packet loss or degraded sensitivity" - Added: No. 111. "Retention in OFF mode is not controlled by RAM[n].POWER->SxRETENTION, but by RAM[n].POWER->SxPOWER " - Added: No. 112. "False SFD field matches in IEEE 802.15.4 mode RX" - Added: No. 113. "Single-ended mode with external reference is not functional" - Added: No. 115. "RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode" - Added: No. 116. "HFCLK not stopped when entering into SENSE_FIELD state" - Added: No. 117. "Reading address 0x40029618 blocks the device" - Added: No. 118. "Reading halfwords or bytes from the XIP region is not supported" - Added: No. 119. "Wake up from System OFF on V_{BUS} detect is not functional" - Added: No. 121. "Second read and long read commands fail" - Added: No. 122. "QSPI uses current after being disabled" - Added: No. 127. "Two stop bit setting is not functional" - Added: No. 128. "RATIO register is not functional" - Added: No. 129. "Reading EPSTALL register causes undefined behavior"

Version	Date	Change
		• Added: No. 130. "Writing to certain read-only registers causes undefined behavior"
		• Added: No. 131. "EasyDMA transfer size is limited to 255 bytes"
		• Added: No. 133. "NRF_RADIO->EVENTS_BCMATCH event might trigger twice"
		• Added: No. 134. "ISOINCONFIG register is not functional"
		• Added: No. 135. "SIZE.ISOOUT register does not report empty incoming packets"
		• Added: No. 136. "Bits in RESETREAS are set when they should not be"
		• Added: No. 140. "REG0 External circuitry supply in LDO mode is not functional in System ON IDLE "
		• Added: No. 142. "Sensitivity not according to specification"

NORDIC
SEMICONDUCTOR

3 New and inherited anomalies

The following anomalies are present in revision Engineering A of the nRF52840 chip.

ID	Module	Description	New in Engineering A
15	POWER	RAM[x].POWERSET/CLR read as zero	X
20	RTC	Register values are invalid	X
36	CLOCK	Some registers are not reset when expected	X
54	I2S	Wrong LRCK polarity in Aligned mode	X
55	I2S	RXPTRUPD and TXPTRUPD events asserted after STOP	X
58	SPIM	An additional byte is clocked out when RXD.MAXCNT = 1	X
66	TEMP	Linearity specification not met with default settings	X
68	CLOCK	EVENTS_HFCLKSTARTED can be generated before HFCLK is stable	X
78	TIMER	High current consumption when using timer STOP task only	X
81	GPIO	PIN_CNF is not retained when in debug interface mode	X
83	TWIS	STOPPED event occurs twice if the STOP task is triggered during a transaction	X
87	CPU	Unexpected wake from System ON Idle when using FPU	X
89	GPIOTE	Static 400 µA current while using GPIOTE	X
94	USBD	BUSSTATE register is not functional	X
96	I2S	DMA buffers can only be located in the first 64 kB of data RAM	X
97	GPIOTE	High current consumption in System ON Idle mode	X
98	NFCT	Not able to communicate with the peer	X
103	CCM	Reset value of CCM.MAXPACKETSIZE causes encryption, decryption, and MIC failures	X
104	USBD	EPDATA event is not always generated	X
110	RADIO	Packet loss or degraded sensitivity	X
111	RAM	Retention in OFF mode is not controlled by RAM[n].POWER->SxRETENTION, but by RAM[n].POWER->SxPOWER	X
112	RADIO	False SFD field matches in IEEE 802.15.4 mode RX	X
113	COMP	Single-ended mode with external reference is not functional	X
115	RAM	RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode	X
116	NFCT	HFCLK not stopped when entering into SENSE_FIELD state	X

NORDIC®
SEMICONDUCTOR

ID	Module	Description	New in Engineering A
117	System	Reading address 0x40029618 blocks the device	X
118	QSPI	Reading halfwords or bytes from the XIP region is not supported	X
119	POWER	Wake up from System OFF on V_{BUS} detect is not functional	X
121	QSPI	Second read and long read commands fail	X
122	QSPI	QSPI uses current after being disabled	X
127	UARTE	Two stop bit setting is not functional	X
128	PDM	RATIO register is not functional	X
131	UARTE	EasyDMA transfer size is limited to 255 bytes	X
133	CLOCK,RADIO	NRF_RADIO->EVENTS_BCMATCH event might trigger twice	X
134	USBD	ISOINCONFIG register is not functional	X
135	USBD	SIZE.ISOOUT register does not report empty incoming packets	X
136	System	Bits in RESETREAS are set when they should not be	X
140	POWER	REG0 External circuitry supply in LDO mode is not functional in System ON IDLE	X
142	RADIO	Sensitivity not according to specification	X
143	RADIO	False CRC failures on specific addresses	X
144	NFCT	Not optimal NFC performance	X
145	SPIM	SPIM3 not functional	X
147	CLOCK	LFRC ULP mode not calibrated in production	X
150	SAADC	EVENT_STARTED does not fire	X
151	NVMC	Access to protected memory through Cache	X
153	RADIO	RSSI parameter adjustment	X
154	USBD	USBD acknowledges setup stage without STATUS task	X
155	GPIOTE	IN event may occur more than once on input edge	X
156	GPIOTE	Some CLR tasks give unintentional behavior	X
158	RADIO	High power consumption in DISABLED state	X
160	SAADC	VDDHDIV5 not functional	X
162	USBD	Writing to registers with offset address 0x52C causes USB to halt	X
164	RADIO	Low selectivity in long range mode	X
166	USBD	ISO double buffering not functional	X
170	I2S	NRF_I2S->PSEL CONNECT fields are not readable	X
171	USB,USBD	USB might not power up	X
173	GPIO	Writes to LATCH register take several CPU cycles to take effect	X

NORDIC
SEMICONDUCTOR

ID	Module	Description	New in Engineering A
176	System	Flash erase through CTRL-AP fails due to watchdog time-out	X
179	RTC	COMPARE event is generated twice from a single RTC compare match	X
180	USBD	Wrong PLL calibration in production	X
181	NFCT	Invalid value in FICR for double-size NFCID1	X
183	PWM	False SEQEND[0] and SEQEND[1] events	X
184	NVMC	Erase or write operations from the external debugger fail when CPU is not halted	X
192	CLOCK	LFRC frequency offset after calibration	X
194	I2S	STOP task does not switch off all resources	X
196	I2S	PSEL acquires GPIOs regardless of ENABLE	X
200	USBD	Cannot write to SIZE.EPOUT register	X
201	CLOCK	EVENTS_HFCLKSTARTED might be generated twice	X

Table 1: New and inherited anomalies

3.1 [15] POWER: RAM[x].POWERSET/CLR read as zero

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

RAM[x].POWERSET and RAM[x].POWERCLR read as zero, even though the RAM is on.

Conditions

Always.

Consequences

Not possible to read the RAM state using RAM[x].POWERSET and RAM[x].POWERCLR registers. Write works as it should.

Workaround

Use RAM[x].POWER to read the state of the RAM.

3.2 [20] RTC: Register values are invalid

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

RTC registers will not contain the correct/expected value if read.

Conditions

The RTC has been idle.

Consequences

RTC configuration cannot be determined by reading RTC registers.

Workaround

Execute the below code before you use RTC.

```
NRF_CLOCK->EVENTS_LFCLKSTARTED  = 0;
NRF_CLOCK->TASKS_LFCLKSTART     = 1;
while (NRF_CLOCK->EVENTS_LFCLKSTARTED == 0) {}
NRF_RTC0->TASKS_STOP = 0;
```

3.3 [36] CLOCK: Some registers are not reset when expected

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

After watchdog timeout reset, CPU lockup reset, soft reset, or pin reset, the following CLOCK peripheral registers are not reset:

- CLOCK->EVENTS_DONE
- CLOCK->EVENTS_CTTO
- CLOCK->CTIV

Conditions

After watchdog timeout reset, CPU Lockup reset, soft reset, and pin reset.

Consequences

Register reset values might be incorrect. It may cause undesired interrupts in case of enabling interrupts without clearing the DONE or CTTO events.

Workaround

Clear affected registers after reset. This workaround has already been added into system_nrf52.c file. This workaround has already been added into system_nrf52840.c file present in MDK 8.11.0 or later.

3.4 [54] I2S: Wrong LRCK polarity in Aligned mode

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

In Aligned mode, left and right samples are swapped.

Conditions

CONFIG.FORMAT = ALIGNED

Consequences

Left and right audio channels are swapped.

Workaround

Swap left and right samples in memory.

3.5 [55] I2S: RXPTRUPD and TXPTRUPD events asserted after STOP

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The RXPTRUPD event is generated when the STOP task is triggered, even though reception (RX) is disabled. Similarly, the TXPTRUPD event is generated when the STOP task is triggered, even though transmission (TX) is disabled.

Conditions

A previous transfer has been performed with RX/TX enabled, respectively.

Consequences

The indication that RXTXD.MAXCNT words were received/transmitted is false.

Workaround

Ignore the RXPTRUPD and TXPTRUPD events after triggering the STOP task. Clear these events before starting the next transfer.

3.6 [58] SPIM: An additional byte is clocked out when RXD.MAXCNT = 1

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

SPIM clocks out additional byte.

Conditions

RXD.MAXCNT = 1

TXD.MAXCNT <= 1

Consequences

Additional byte is redundant.

Workaround

Use the SPI module (deprecated but still available) or use the following workaround with SPIM:

```c
/**
 * @brief Work-around for transmitting 1 byte with SPIM.
 *
 * @param spim: The SPIM instance that is in use.
 * @param ppi_channel: An unused PPI channel that will be used by the workaround.
 * @param gpiote_channel: An unused GPIOTE channel that will be used by the workaround.
 *
 * @warning Must not be used when transmitting multiple bytes.
 * @warning After this workaround is used, the user must reset the PPI channel and the
 GPIOTE channel before attempting to transmit multiple bytes.
 */
void setup_workaround_for_ftpan_58(NRF_SPIM_Type * spim, uint32_t ppi_channel, uint32_t
 gpiote_channel)
{
    // Create an event when SCK toggles.
    NRF_GPIOTE->CONFIG[gpiote_channel] = (
        GPIOTE_CONFIG_MODE_Event <<
        GPIOTE_CONFIG_MODE_Pos
        ) | (
        spim->PSEL.SCK <<
        GPIOTE_CONFIG_PSEL_Pos
        ) | (
        GPIOTE_CONFIG_POLARITY_Toggle <<
        GPIOTE_CONFIG_POLARITY_Pos
        );

    // Stop the spim instance when SCK toggles.
    NRF_PPI->CH[ppi_channel].EEP = (uint32_t)&NRF_GPIOTE->EVENTS_IN[gpiote_channel];
    NRF_PPI->CH[ppi_channel].TEP = (uint32_t)&spim->TASKS_STOP;
    NRF_PPI->CHENSET = 1U << ppi_channel;

    // The spim instance cannot be stopped mid-byte, so it will finish
    // transmitting the first byte and then stop. Effectively ensuring
    // that only 1 byte is transmitted.
}
```

3.7 [66] TEMP: Linearity specification not met with default settings

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

TEMP module provides non-linear temperature readings over the specified temperature range.

Conditions

Always.

Consequences

TEMP module returns out of spec temperature readings.

Workaround

Execute the following code after reset:

```
        NRF_TEMP->A0 = NRF_FICR->TEMP.A0;
        NRF_TEMP->A1 = NRF_FICR->TEMP.A1;
        NRF_TEMP->A2 = NRF_FICR->TEMP.A2;
        NRF_TEMP->A3 = NRF_FICR->TEMP.A3;
        NRF_TEMP->A4 = NRF_FICR->TEMP.A4;
        NRF_TEMP->A5 = NRF_FICR->TEMP.A5;
        NRF_TEMP->B0 = NRF_FICR->TEMP.B0;
        NRF_TEMP->B1 = NRF_FICR->TEMP.B1;
        NRF_TEMP->B2 = NRF_FICR->TEMP.B2;
        NRF_TEMP->B3 = NRF_FICR->TEMP.B3;
        NRF_TEMP->B4 = NRF_FICR->TEMP.B4;
        NRF_TEMP->B5 = NRF_FICR->TEMP.B5;
        NRF_TEMP->T0 = NRF_FICR->TEMP.T0;
        NRF_TEMP->T1 = NRF_FICR->TEMP.T1;
        NRF_TEMP->T2 = NRF_FICR->TEMP.T2;
        NRF_TEMP->T3 = NRF_FICR->TEMP.T3;
        NRF_TEMP->T4 = NRF_FICR->TEMP.T4;
```

This code is already present in the latest system_nrf52.c file and in the system_nrf52840.c file released in MDK 8.12.0.

3.8 [68] CLOCK: EVENTS_HFCLKSTARTED can be generated before HFCLK is stable

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

EVENTS_HFCLKSTARTED may come before HFXO is started.

Conditions

When using a 32 MHz crystal with start-up longer than 400 µs.

Consequences

Performance of radio and peripheral requiring HFXO will be degraded until the crystal is stable.

Workaround

32 MHz crystal oscillator startup time must be verified by the user. If the worst-case startup time is shorter than 400 μs, no workaround is required. If the startup time can be longer than 400 μs, the software must ensure, using a timer, that the crystal has had enough time to start up before using peripherals that require the HFXO. The Radio requires the HFXO to be stable before use. The ADC, TIMERs, and TEMP sensor for example can use the HFXO as a reference for improved accuracy.

3.9 [78] TIMER: High current consumption when using timer STOP task only

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Increased current consumption when the timer has been running and the STOP task is used to stop it.

Conditions

The timer has been running (after triggering a START task) and then it is stopped using a STOP task only.

Consequences

Increased current consumption.

Workaround

Use the SHUTDOWN task after the STOP task or instead of the STOP task.

3.10 [81] GPIO: PIN_CNF is not retained when in debug interface mode

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

GPIO pin configuration is reset on wakeup from System OFF.

Conditions

The system is in debug interface mode.

Consequences

GPIO state unreliable until PIN_CNF is reconfigured.

3.11 [83] TWIS: STOPPED event occurs twice if the STOP task is triggered during a transaction

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

NORDIC
SEMICONDUCTOR

Symptoms

STOPPED event is set after clearing it.

Conditions

The STOP task is triggered during a transaction.

Consequences

STOPPED event occurs twice: When the STOP task is fired and when the master issues a stop condition on the bus. This could provoke an extra interrupt or a failure in the TWIS driver.

Workaround

The last STOPPED event must be accounted for in software.

3.12 [87] CPU: Unexpected wake from System ON Idle when using FPU

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The CPU is unexpectedly awoken from System ON Idle.

Conditions

The FPU has been used.

Consequences

The CPU is awoken from System ON Idle.

Workaround

The FPU can generate pending interrupts just like other peripherals, but unlike other peripherals there are no INTENSET, INTENCLR registers for enabling or disabling interrupts at the peripheral level. In order to prevent unexpected wake-up from System ON Idle, add this code before entering sleep:

```
#if (__FPU_USED == 1)
  __set_FPSCR(__get_FPSCR() & ~(0x0000009F));
  (void) __get_FPSCR();
  NVIC_ClearPendingIRQ(FPU_IRQn);
#endif
  __WFE();
```

3.13 [89] GPIOTE: Static 400 µA current while using GPIOTE

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

NORDIC
SEMICONDUCTOR

Symptoms

Static current consumption between 400 µA and 450 µA when using SPIM or TWIM in combination with GPIOTE.

Conditions

- GPIOTE is configured in event mode
- TWIM/SPIM utilizes EasyDMA

Consequences

Current consumption higher than specified.

Workaround

Turn the TWIM/SPIM off and back on after it has been disabled. To do so, write 0 followed by 1 to the POWER register (address 0xFFC) of the TWIM/SPIM that must be disabled:

- If TWIM0 or SPIM0 is used:

```
*(volatile uint32_t *)0x40003FFC = 0;
*(volatile uint32_t *)0x40003FFC;
*(volatile uint32_t *)0x40003FFC = 1;
```

- If TWIM1 or SPIM1 is used:

```
*(volatile uint32_t *)0x40004FFC = 0;
*(volatile uint32_t *)0x40004FFC;
*(volatile uint32_t *)0x40004FFC = 1;
```

- If SPIM2 is used:

```
*(volatile uint32_t *)0x40023FFC = 0;
*(volatile uint32_t *)0x40023FFC;
*(volatile uint32_t *)0x40023FFC = 1;
```

Reconfiguration of TWIM/SPIM is required before next usage.

3.14 [94] USBD: BUSSTATE register is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

BUSSTATE register is not functional.

Conditions

Always.

NORDIC
SEMICONDUCTOR

Consequences

Reading BUSSTATE will not show the state of the bus as documented. No impact on USB 2.0 compliance.

Workaround

None.

3.15 [96] I2S: DMA buffers can only be located in the first 64 kB of data RAM

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The I2S will not read and write the RAM location specified by the data pointer.

Conditions

DMA buffers are located entirely or in part above address 0x2000 FFFF.

Consequences

Data or memory corruption

Workaround

Set DMA buffers to use memory range 0x2000 0000 to 0x2000 FFFF.

3.16 [97] GPIOTE: High current consumption in System ON Idle mode

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

High current consumption (<20 µA) in System ON Idle mode.

Conditions

GPIOTE used with one or more channels in input mode.

Consequences

Higher current consumption.

Workaround

Use Port event to detect transitions on inputs instead of GPIOTE input mode.

NORDIC
SEMICONDUCTOR

3.17 [98] NFCT: Not able to communicate with the peer

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The NFCT is not able to receive or transmit messages to the peer.

Conditions

Always

Consequences

The NFCT cannot communicate with the peer.

Workaround

Write 0x00038148 to 0x4000568C before the NFC peripheral is enabled:

```
  *(volatile uint32_t *)0x4000568Cul = 0x00038148ul;
```

The workaround is included in the system_nrf52840.c file present in MDK 8.11.0 or later.

3.18 [103] CCM: Reset value of CCM.MAXPACKETSIZE causes encryption, decryption, and MIC failures

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Failing encryption, decryption, and MIC on extended length packets.

Conditions

Always for extended length packets.

Consequences

Failing encryption, decryption, and MIC on extended length packets.

Workaround

Set CCM.MAXPACKETSIZE to 0xFB.

This workaround has already been added into the system_nrf52840.c file present in MDK 8.11.1 or later.

3.19 [104] USBD: EPDATA event is not always generated

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The EPDATA event might not be generated, and the related update of EPDATASTATUS does not occur.

Conditions

Sometimes.

Consequences

It is not possible to develop a custom USB stack.

Workaround

Use the USB stack provided in Nordic's SDK.

3.20 [110] RADIO: Packet loss or degraded sensitivity

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

In BLE Long Range or 802.15.4 modes, subsequent packets after the first packet might not be received. In BLE and proprietary modes, the sensitivity might be degraded.

Conditions

Always.

Consequences

Might lose packets in BLE LR or 802.15.4 mode. Might lose some sensitivity in BLE and proprietary mode.

Workaround

Always disable the radio after having received a packet (using TASK_DISABLE). The workaround is included in the S132 and S140 SoftDevice.

3.21 [111] RAM: Retention in OFF mode is not controlled by RAM[n].POWER->SxRETENTION, but by RAM[n].POWER->SxPOWER

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Current consumption in OFF mode is higher than expected. RAM contents are retained in OFF mode when they should not be.

Conditions

Always.

Consequences

Cannot independently control RAM retention in OFF mode and power in ON mode.

Workaround

Use RAM[n].POWER->SxPOWER to control the retention in OFF mode and power in ON mode. Exercise caution when using this workaround, becausee the firmware requires a certain amount of RAM to be powered when waking from OFF mode (such as the RAM where the call stack is located), and RAM[n].POWER registers are retained registers.

3.22 [112] RADIO: False SFD field matches in IEEE 802.15.4 mode RX

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

False FRAMESTART, ADDRESS, PAYLOAD, and END events are triggered and a corrupted packet with a failing CRC is received.

Conditions

The SFD octet of the packet on air does not match the value configured in the SFD register.

Consequences

Packet with CRC error is received, when it should have been discarded based on SFD field.

Workaround

Check for CRC failure after the END event triggers.

3.23 [113] COMP: Single-ended mode with external reference is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

COMP output is not correct.

Conditions

COMP is used in single-ended mode with external reference.

Consequences

COMP cannot be used in this mode.

NORDIC
SEMICONDUCTOR

Workaround

None.

3.24 [115] RAM: RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

RAM not correctly retained.

Conditions

System ON Idle mode or System OFF is used with parts or all RAM retained.

Consequences

RAM not correctly retained.

Workaround

Apply the following code after any reset:

```
*(volatile uint32_t *)0x40000EE4 = ( (*(volatile uint32_t *)0x40000EE4 & 0x00000070) | //
 Keep bit 6:4
                                    (*(uint32_t *)0x10000258 & 0x0000000F) ); // Replace
 bit 3:0
```

This workaround has already been added into system_nrf52840.c file present in MDK 8.11.0 or later. This workaround increases the I_RAM current per 4 KB section from 20 nA to 30 nA.

3.25 [116] NFCT: HFCLK not stopped when entering into SENSE_FIELD state

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Higher current consumption than specified in SENSE_FIELD state.

Conditions

The NFCT is going from ACTIVATED state to SENSE_FIELD state.

Consequences

Higher current consumption in SENSE_FIELD state.

NORDIC
SEMICONDUCTOR

Workaround

- Do not use the FIELDLOST_SENSE shortcut in NFCT.
- Do not use a PPI channel to short FIELDLOST event and SENSE task in NFCT.
- When the FIELDLOST event is triggered in NFCT, write 0x01 to address 0x40005010. Then trigger the SENSE task in NFCT to go into SENSE_FIELD state.

3.26 [117] System: Reading address 0x40029618 blocks the device

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The debugger interface is lost. The device halts or seems to stop executing.

Conditions

Reading address 0x40029618ul, either directly from firmware or with the debugger (for example, using a memory window in the IDE).

Consequences

Crash. Need to power cycle the device and restart the debugging session.

Workaround

Do not read address 0x40029618ul.

3.27 [118] QSPI: Reading halfwords or bytes from the XIP region is not supported

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The CPU is interrupted with a bus fault.

Conditions

The CPU reads a halfword or a byte from the XIP region. The following instructions could cause a byte or halfword load:

- LDRB
- LDRBT
- LDREXB
- LDRSB
- LDRSBT
- LDRH
- LDRHT
- LDREXH

NORDIC
SEMICONDUCTOR

- LDRSH
- LDRSHT
- TBB
- TBH

Consequences

Cannot run code from external memory.

Workaround

Link the firmware such that the run-time location of the read-only data section is in internal flash or RAM. Also, do not write assembly or C code that reads byte or halfword sized data from external flash.

ARM[®] Compiler armcc

To prevent the generation of TBB and TBH instructions, use the compiler command line option `-- execute_only`. This option will also prevent the generation of instructions that read literals from code sections.

GNU ARM Embedded Toolchain

Using version Q3 2016 or later, you can prevent the generation of TBB and TBH instructions by using the compiler option `-mpure-code`. This option will also prevent the generation of instructions that read literals from the .text section.

3.28 [119] POWER: Wake up from System OFF on V$_{BUS}$ detect is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

In System OFF mode, the device will not wake up when V$_{BUS}$ supply is connected.

Conditions

Always.

Consequences

The device remains is System OFF mode.

Workaround

External circuitry can be used to translate V$_{BUS}$ voltage levels to GPIO voltage levels that can be used to trigger a GPIO DETECT signal (configured using the GPIOTE peripheral) to wake from System OFF.

3.29 [121] QSPI: Second read and long read commands fail

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

NORDIC
SEMICONDUCTOR

Symptoms

- QSPI read command never gets sent.
- QSPI read command of more than 0x20 characters fails.

Conditions

QSPI.IFCONFIG1 is different than 0xYY0404YY, where Y is any value.

Consequences

QSPI is not functional.

Workaround

When writing IFCONFIG1, make sure to write 0x0404 to IFCONFIG1[23:8].

3.30 [122] QSPI: QSPI uses current after being disabled

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Current consumption is too high.

Conditions

After QSPI has been activated by the use of TASKS_ACTIVATE task.

Consequences

Current consumption is too high.

Workaround

Execute the following code before disabling QSPI:

```
*(volatile uint32_t *)0x40029010ul = 1ul;
*(volatile uint32_t *)0x40029054ul = 1ul
```

3.31 [127] UARTE: Two stop bit setting is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Setting CONFIG.STOP=Two (2 stop bits) has no effect.

Conditions

Always.

Consequences

UARTE traffic with 2 stop bit setting is not supported.

Workaround

None.

3.32 [128] PDM: RATIO register is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The RATIO register is not functional.

Conditions

Always.

Consequences

The only supported ratio between PDM_CLK and output audio sample rate is 64.

Workaround

None.

3.33 [131] UARTE: EasyDMA transfer size is limited to 255 bytes

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

DMA transfer is not as long as configured. Only the 8 least significant bits of RXD.MAXCNT and TXD.MAXCNT registers are functional.

Conditions

RXD.MAXCNT and/or TXD.MAXCNT are configured for DMA transfers > 255 bytes.

Consequences

EasyDMA transfer sizes longer than 255 bytes are not supported. Larger size values are treated modulo 256.

Workaround

Split long transfers into chunks of 255 bytes or less.

NORDIC
SEMICONDUCTOR

3.34 [133] CLOCK,RADIO: NRF_RADIO->EVENTS_BCMATCH event might trigger twice

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

A task might be triggered twice by the NRF_RADIO->EVENTS_BCMATCH event.

Conditions

- The NRF_RADIO->EVENTS_BCMATCH event is used to trigger tasks through PPI or SHORTS.
- BCC is set to match after one more bit than the packet size during TX.

Consequences

Tasks connected through PPI or SHORTS to this event might be triggered twice.

Workaround

None.

3.35 [134] USBD: ISOINCONFIG register is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The ISOINCONFIG register is not functional

Conditions

Always.

Consequences

Not possible to change the behavior of the ISO IN endpoint response to an IN token when no data is to be sent. The USBD will not respond to the IN token in this situation.

Workaround

None.

3.36 [135] USBD: SIZE.ISOOUT register does not report empty incoming packets

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The SIZE.ISOOUT register does not report empty incoming packets in the ZERO field.

NORDIC
SEMICONDUCTOR

Conditions

Always.

Consequences

The firmware cannot rely on the ZERO field to know if a zero-length ISO OUT packet has been received.

Workaround

None.

3.37 [136] System: Bits in RESETREAS are set when they should not be

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

After pin reset, RESETREAS bits other than RESETPIN might also be set.

Conditions

A pin reset has triggered.

Consequences

If the firmware evaluates RESETREAS, it might take the wrong action.

Workaround

When RESETREAS shows a pin reset (RESETPIN), ignore other reset reason bits.

> **Important:** RESETREAS bits must be cleared between resets.

Apply the following code after any reset:

```
if (NRF_POWER->RESETREAS & POWER_RESETREAS_RESETPIN_Msk){
    NRF_POWER->RESETREAS =  ~POWER_RESETREAS_RESETPIN_Msk;
}
```

This workaround is implemented in MDK version 8.13.0 and later.

3.38 [140] POWER: REG0 External circuitry supply in LDO mode is not functional in System ON IDLE

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

External circuitry supply does not work. A BOR might occur.

NORDIC
SEMICONDUCTOR

Conditions

Using REG0 in LDO mode in System ON IDLE.

Consequences

External circuitry supply cannot be used to supply current >1 mA in System ON IDLE.

Workaround

Use REG0 in DCDC mode.

3.39 [142] RADIO: Sensitivity not according to specification

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Radio receiver sensitivity is 1 dB lower than specified.

Conditions

All radio modes.

Consequences

Reduction in receiver sensitivity.

Workaround

None.

3.40 [143] RADIO: False CRC failures on specific addresses

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

100% CRC failure rate even if the payload is received correctly.

Conditions

1 Mbit/s and 2 Mbit/s Nordic proprietary radio mode and Bluetooth Low Energy. `CRCCNF.SKIPADDR = 0`. CRC calculation includes the address field.

NORDIC
SEMICONDUCTOR

Logical address 0 and logical address 1 to 7 have the same BASE address MSBs configured.

```
ADDRLEN=5
BASE0 = 0xAAAAXXXX
BASE1 = 0xAAAAXXXX
ADDRLENLEN=4
BASE0 = 0xAAXXXXXX
BASE1 = 0xAAXXXXXX
```

AND logical address 0 and one of the logical addresses 1 to 7 have the same PREFIX value configured.

The issue is present regardless of which logical address is enabled in RXADDRESSES.

Consequences

If receiving on logical address 0, the address is reconstructed incorrectly for CRC calculation, resulting in CRCSTATUS.CRCError being returned. However, the received payload bytes are correct. Packet error rate 100 percent. RXMATCH shows the wrong logical address.

Workaround

Use one of the following workarounds:

- Use the ESB and Gazell libraries of SDK v14.0.0 or later.

  This implementation applies the following workaround.
- Set bit 16 in RXADDRESSES to 1.
- Apply the following code before triggering the RXEN task:

  ```
    *(volatile uint32_t *) 0x40001774 = ((*(volatile uint32_t *) 0x40001774) & 0xfffffffe)
  | 0x01000000;
  ```

  This code will reduce sensitivity with 3 dB.

3.41 [144] NFCT: Not optimal NFC performance

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Short NFC read distance or failing NFC connection with peer device.

Conditions

Always.

Consequences

No connection or short read distance to peer device.

NORDIC®
SEMICONDUCTOR

Workaround

Execute the following code before using the NFCT peripheral:

```
*(volatile uint32_t *)0x4000561c = 0x1ul;
*(volatile uint32_t *)0x4000562c = 0x3Ful;
*(volatile uint32_t *)0x4000563c = 0x0ul;
*(volatile uint32_t *)0x40005528 = 0xCul;
```

3.42 [145] SPIM: SPIM3 not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The SPIM3 peripheral is not functional.

Conditions

Always.

Consequences

The SPIM3 peripheral is not functional.

Workaround

None.

3.43 [147] CLOCK: LFRC ULP mode not calibrated in production

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The LFRC oscillator non-calibrated frequency tolerance (ftol_uncal_lfulp) in ULP mode is not according to specification.

Conditions

LFRC in ULP mode.

Consequences

The LFRC ULP oscillator non-calibrated frequency is unreliable.

Workaround

Do calibration after each power-up, after changing mode between normal mode and ULP mode, and if the temperature changes more than 40°C.

NORDIC
SEMICONDUCTOR

3.44 [150] SAADC: EVENT_STARTED does not fire

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

EVENT_STARTED does not fire.

Conditions

ADC started (TASKS_START) with PPI task. Any channel configured to TACQ <= 5 µs.

Consequences

ADC cannot be started (TASKS_START) with PPI if TACQ <= 5 µs.

Workaround

Use TAQC > 5 µs when starting ADC from PPI.

3.45 [151] NVMC: Access to protected memory through Cache

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

CPU stalls.

Conditions

Instruction cache enabled. Parts of Flash protected by ACL against reads. Reading or instruction fetching from a read protected area.

Consequences

CPU stalls and not hardfaults. Only recoverable by an external reset (pin reset or power reset, and watchdog timer if enabled)

Workaround

None.

3.46 [153] RADIO: RSSI parameter adjustment

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

RSSI changes over temperature.

Conditions

Temperature ≤ +10°C or > +30°C.

Consequences

RSSI parameter not within specified accuracy.

Workaround

Add the following compensation to the RSSI sample value based on temperature measurement (the on-chip TEMP peripheral can be used to measure temperature):

- For TEMP ≤ -30°C, RSSISAMPLE = RSSISAMPLE +3
- For TEMP > -30°C and TEMP ≤ -10°C, RSSISAMPLE = RSSISAMPLE +2
- For TEMP > -10°C and TEMP ≤ +10°C, RSSISAMPLE = RSSISAMPLE +1
- For TEMP > +10°C and TEMP ≤ +30°C, RSSISAMPLE = RSSISAMPLE + 0
- For TEMP > +30°C and TEMP ≤ +50°C, RSSISAMPLE = RSSISAMPLE - 1
- For TEMP > +50°C and TEMP ≤ +70°C, RSSISAMPLE = RSSISAMPLE - 2
- For TEMP > +70°C, RSSISAMPLE = RSSISAMPLE - 3

3.47 [154] USBD: USBD acknowledges setup stage without STATUS task

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Unexpected control endpoint stall during enumeration and/or loss of data.

Conditions

USB protocol is in "Status stage", and the optional "Data stage" preceding the "Status stage" was included. USBD is waiting for the STATUS task to be triggered from software to allow ACK to be sent to Host.

Consequences

USBD sends ACK to Host during "Status stage", regardless of whether the STATUS task has been triggered. New data may be received by USBD before old data has been processed. Stalling may occur if STATUS task is triggered too late, for example, during the next SETUP transaction.

Workaround

For OUT transfers: Do not use the STATUS task if the SETUP transaction contains data. For IN transfers: Trigger STATUS task using the PPI or SHORT register. There is no possibility to properly STALL any SETUP transfer that consists of data based on the analyzed data.

3.48 [155] GPIOTE: IN event may occur more than once on input edge

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

IN event occurs more than once on an input edge.

Conditions

Input signal edges are closer together than 1.3 µs or >= 750 kHz for a periodic signal.

Consequences

Tasks connected through PPI or SHORTS to this event might be triggered twice.

Workaround

Apply the following code when any GPIOTE channel is configured to generate an IN event on edges that can occur within 1.3 µs of each other:

```
*(volatile uint32_t *)(NRF_GPIOTE_BASE + 0x600 + (4 * GPIOTE_CH_USED)) = 1;
```

> **Important:** A clock is kept on by the workaround and must be reverted to avoid higher current consumption when GPIOTE is not in use, using the following code:
>
> ```
> *(volatile uint32_t *)(NRF_GPIOTE_BASE + 0x600 + (4 * GPIOTE_CH_USED)) = 0;
> ```

3.49 [156] GPIOTE: Some CLR tasks give unintentional behavior

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

One of the following:

- Current consumption is high when entering IDLE.
- Latency for detection changes on inputs connected to GPIOTE channels becoming longer that expected.

Conditions

Using the following tasks:

Address	GPIOTE task
0x060	TASK_CLR[0]
0x064	TASK_CLR[1]
0x068	TASK_CLR[2]
0x06C	TASK_CLR[3]
0x070	TASK_CLR[4]
0x074	TASK_CLR[5]
0x078	TASK_CLR[6]
0x07C	TASK_CLR[7]

Consequences

High current consumption or too long time from external event to internal triggering of PPI event and/or IRQ from GPIOTE.

Using TASK_CLR[n] for even values of n has the side effect of setting the system in constant latency mode (see POWER->TASKS_CONSTLAT). Using TASK_CLR[n] for odd values of n has the side effect of setting the system in low power mode (see POWER->TASKS_LOWPOWER).

Workaround

To set the system back in the mode it was before using the TASK_CLR[n], triggering of tasks with even n must be followed by triggering any of the TASK_CLR with odd n and vice versa.

3.50 [158] RADIO: High power consumption in DISABLED state

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Power consumption is 500 µA when the radio is disabled (should be 40 - 50 µA).

Conditions

RXEN Radio, wait for READY (ramping up), START, and immediately followed by DISABLE.

Consequences

Increased current consumption.

Workaround

Do not trigger DISABLE immediately after START.

3.51 [160] SAADC: VDDHDIV5 not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

NORDIC
SEMICONDUCTOR

Symptoms

VDDHDIV5 setting on CH[x].PSELP and CH[x].PSELN is not functional.

Conditions

Always.

Consequences

VDDHDIV5 setting on CH[x].PSELP and CH[x].PSELN is not functional.

Workaround

None.

3.52 [162] USBD: Writing to registers with offset address 0x52C causes USB to halt

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

USB halts.

Conditions

USBD is enabled and runs in NORMAL mode. Writing data with LSB set to '1' to any IP register with ID 0x52C (i.e., address set to any value in the range of 0x4000_0000 to 0x4007_FFFF with the last 12 bits equal to 52C). This affects the following registers:

- GPIOTE->CONFIG[7]
- PPI->CH[3].TEP
- RADIO->TXADDRESS
- TEMP->A3
- SAADC->CH[1].LIMIT
- PDM->FILTER.HPDISABLE
- PWM->SEQ[0].ENDDELAY

Consequences

USBD stops working until reset.

Workaround

None.

3.53 [164] RADIO: Low selectivity in long range mode

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

NORDIC
SEMICONDUCTOR

Symptoms

Lower than specified selectivity in BLE long range mode.

Conditions

Receiving in long range mode.

Consequences

Reduced selectivity.

Workaround

Add the following code after reset or before enabling the radio, when using BLE long range mode:

```
*(volatile uint32_t *)0x4000173C |= 0x80000000;
*(volatile uint32_t *)0x4000173C = ((*(volatile uint32_t *)0x4000173C & 0xFFFFFF00) |
 0x5C);
```

When using other Radio modes, use the below code to return to original settings before enabling the Radio:

```
*(volatile uint32_t *)0x4000173C &= ~0x80000000;
```

3.54 [166] USBD: ISO double buffering not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The double buffering of the ISO EPs of the USBD is not functional.

Conditions

Always. With default settings, the buffers overlap.

Consequences

During ISO transition, received or transmitted data is likely to be corrupted.

Workaround

Reconfigure ISO buffers during initialization of USBD. After each time the USBD peripheral is enabled, apply the following code:

```
*((volatile uint32_t *)(NRF_USBD_BASE + 0x800)) = 0x7E3;
*((volatile uint32_t *)(NRF_USBD_BASE + 0x804)) = 0x40;
```

NORDIC
SEMICONDUCTOR

3.55 [170] I2S: NRF_I2S->PSEL CONNECT fields are not readable

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

- CONNECT field of NRF_I2S->PSEL.MCK is not readable.
- CONNECT field of NRF_I2S->PSEL.SCK is not readable.
- CONNECT field of NRF_I2S->PSEL.LRCK is not readable.
- CONNECT field of NRF_I2S->PSEL.SDIN is not readable.
- CONNECT field of NRF_I2S->PSEL.SDOUT is not readable.

Conditions

Always.

Consequences

When reading the value of NRF_I2S->PSEL registers, the CONNECT field might not return the same value that has been written to it.

Workaround

None.

3.56 [171] USB,USBD: USB might not power up

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The USBD might not reach its active state. It is also possible that the USBD reaches its active state, but with an increased delay.

Conditions

Firmware enables USBD or exits USBD low power mode (clears USBD->LOWPOWER) and enters System ON IDLE before the USBD module is fully powered up.

Consequences

The USBD sometimes does not function.

Workaround

To enable the USBD (USBD.ENABLE = 1) or to wake the USBD during SUSPEND (USBD.LOWPOWER = 0), apply the following code:

```
if(*(volatile uint32_t *)0x4006EC00 == 0x00000000)
{
  *(volatile uint32_t *)0x4006EC00 = 0x00009375;
}
*(volatile uint32_t *)0x4006EC14 = 0x000000C0;
*(volatile uint32_t *)0x4006EC00 = 0x00009375;


NRF_USBD->ENABLE = 0x00000001; // or NRF_USBD->LOWPOWER = 0x00000000;
```

After receiving the corresponding acknowledgment event (i.e. USBD.EVENTS_USBEVENT with USBD.EVENTCAUSE.READY=1 in case of enabling or USBD->EVENTCAUSE.USBWUALLOWED=1 in case of wakeup), apply the following code:

```
if(*(volatile uint32_t *)0x4006EC00 == 0x00000000)
{
  *(volatile uint32_t *)0x4006EC00 = 0x00009375;
}
*(volatile uint32_t *)0x4006EC14 = 0x00000000;
*(volatile uint32_t *)0x4006EC00 = 0x00009375;
```

3.57 [173] GPIO: Writes to LATCH register take several CPU cycles to take effect

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

A bit in the LATCH register reads '1' even after clearing it by writing '1'.

Conditions

Reading the LATCH register right after writing to it.

Consequences

Old value of the LATCH register is read.

Workaround

Have at least 3 CPU cycles of delay between the write and the subsequent read to the LATCH register. This can be achieved by having 3 dummy reads to the LATCH register.

3.58 [176] System: Flash erase through CTRL-AP fails due to watchdog time-out

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Full flash erase through CTRL-AP is not successful.

Conditions

WDT is enabled.

Consequences

Flash is not erased. If the device has a WDT time-out less than 1 ms and is readback-protected through UICR.APPROTECT, there is a risk of permanently preventing the erasing of the flash.

Workaround

Try again.

3.59 [179] RTC: COMPARE event is generated twice from a single RTC compare match

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Tasks connected to RTC COMPARE event through PPI are triggered twice per compare match.

Conditions

RTC registers are being accessed by CPU while RTC is running.

Consequences

Tasks connected to RTC COMPARE event through PPI are triggered more often than expected.

Workaround

Do not access the RTC registers, including the COMPARE event register, from CPU while waiting for the RTC COMPARE event. Note that CPU interrupt from this event can still be enabled.

3.60 [180] USBD: Wrong PLL calibration in production

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

USB PLL frequency is not according to specification.

NORDIC
SEMICONDUCTOR

Conditions

Some engineering devices with date code 1716 and later.

Consequences

USB not functional.

Workaround

None.

3.61 [181] NFCT: Invalid value in FICR for double-size NFCID1

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

NFC not communicating with the peer device.

Conditions

Using NFCID1 values from FICR and using double-size ID. FICR address 0x454 NFC.TAGHEADER1.UD4 is equal to 0x88.

Consequences

NFC does not communicate reliably with the peer device.

Workaround

Do not use 0x88 value in NFCID1.

3.62 [183] PWM: False SEQEND[0] and SEQEND[1] events

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

False SEQEND[0] and SEQEND[1] events are being generated.

Conditions

Any of the LOOPSDONE_SEQSTARTn shortcuts are enabled. LOOP register is non-zero and sequence 1 is one value long.

Consequences

SEQEND[0] and SEQEND[1] events might falsely trigger other tasks if these are routed through the PPI.

NORDIC
SEMICONDUCTOR

Workaround

Avoid using the LOOPSDONE_SEQSTARTn shortcuts, when LOOP register is non-zero and sequence 1 is one value long.

3.63 [184] NVMC: Erase or write operations from the external debugger fail when CPU is not halted

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The erase or write operation fails or takes longer time than specified.

Conditions

NVMC erase or write operation initiated using an external debugger. CPU is not halted.

Consequences

The NVMC erase or write operation fails or takes longer time than specified.

Workaround

Halt the CPU by writing to DHCSR (Debug Halting Control and Status Register) before starting NVMC erase or write operation from the external debugger. See the ARM infocenter to get the details of the DHCSR register.

Programming tools provided by Nordic Semiconductor comply with this.

3.64 [192] CLOCK: LFRC frequency offset after calibration

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

LFRC oscillator frequency is wrong after calibration, exceeding 500 ppm.

Conditions

On some devices, when entering System ON Idle while calibration is ongoing.

Consequences

After calibration, LFRC has a frequency offset that is outside specification.

Workaround

Apply the following code before starting the RCOSC32K calibration:

```
*(volatile uint32_t *)0x40000C34 = 0x00000002;
```

Apply the following code after the RCOSC32K calibration is finished:

```
*(volatile uint32_t *)0x40000C34 = 0x00000000;
```

This workaround is included in SDK v15.0.0 and SoftDevices S140, S132, and S112 v6.0.0.

3.65 [194] I2S: STOP task does not switch off all resources

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Current consumption too high (~900 µA) after using the STOP task.

Conditions

I2S was running and was stopped by triggering the STOP task.

Consequences

Current consumption higher than specified.

Workaround

Apply the following code after the STOP task:

```
*((volatile uint32_t *)0x40025038) = 1;
*((volatile uint32_t *)0x4002503C) = 1;
```

3.66 [196] I2S: PSEL acquires GPIOs regardless of ENABLE

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

I2S controls GPIO even when I2S is not enabled.

Conditions

When using I2S->PSEL to configure GPIO.

NORDIC
SEMICONDUCTOR

Consequences

GPIO selected for I2S cannot be used for any other peripheral.

Workaround

Do not rely on the pins selected in I2S->PSEL registers being free when I2S->ENABLE is set to DISABLE.

Only set the CONNECT bit in the I2S->PSEL registers to CONNECTED immediately before enabling I2S. When disabling I2S, set the CONNECT bit in the I2S->PSEL registers to DISCONNECTED.

3.67 [200] USBD: Cannot write to SIZE.EPOUT register

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

SIZE.EPOUT[n] registers are not writable.

Conditions

When a user tries to write SIZE.EPOUT[n] register to accept further OUT traffic ignoring current endpoint data and state.

Consequences

Cannot use SIZE.EPOUT[n] register write to allow traffic on the endpoint.

Workaround

1. Trigger a dummy EasyDMA transfer on the endpoint (hard to make it 100% stable).
2. Use the following code to clear EPOUTn:

```
void epout_drop(uint8_t n)
{
    *((volatile uint32_t *)(0x40027800)) = 0x7C5 + (2u * n);
    *((volatile uint32_t *)(0x40027804)) = 0;
    (void)(*((volatile uint32_t *)(0x40027804)));
}
```

The code should be executed from critical region to make sure that nothing interrupts the above registers access sequence.

3.68 [201] CLOCK: EVENTS_HFCLKSTARTED might be generated twice

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

EVENTS_HFCLKSTARTED might occur twice, and HFCLKSTAT might be wrong.

NORDIC
SEMICONDUCTOR

Conditions

When running HFCLK with crystal.

Consequences

HFCLKSTAT might be wrong when reading it after HFCLK is started.

Workaround

Disregard HFCLKSTAT and EVENT_HFCLKSTARTED after first EVENT_HFCLKSTARTED.

This workaround is included in nRF5 SDK v15.0.0 and SoftDevices S140, S132, and S112 v6.0.0.

NORDIC
SEMICONDUCTOR