nRF52832 Errata v1.1

2015-10-09

Contents

Chapter 1
nRF52832 Errata v1.1

This Errata document contains anomalies for the nRF52832 chip, revision Engineering A (QFAA-AA0, QFAA-AC0, CGAA-AA0), Engineering B (QFAA-BA0, QFAA-BB0, CHAA-AA0, CHAA-AB0), Rev 1 (QFAA-B00, CHAA-A00).

Chapter 2
Change log

See the following list for an overview of changes from previous versions of this document.

Table 1: Change log

Version	Date	Change
nRF52832-PAN v1.1	09.10.2015	• Added: No. 16. "RAM may be corrupt on wakeup from CPU IDLE" • Added: No. 31. "Calibration values are not correctly loaded from FICR at reset" • Added: No. 51. "Aligned stereo slave mode does not work" • Added: No. 53. "Using SCB.AIRCR.VECTRESET may get the chip into an undefined state" • Added: No. 54. "Wrong LRCK polarity in Aligned mode" • Added: No. 55. "RXPTRUPD and TXPTRUPD events asserted after STOP" • Added: No. 58. "SPIM clocks out an additional byte when RXD.MAXCNT = 1" • Added: No. 62. "Can draw current when not enabled" • Added: No. 63. "DC/DC does not automatically switch off in System ON IDLE" • Added: No. 64. "Only full bytes can be received or transmitted" • Added: No. 65. "RAM[] registers mapping of RAM block and sections is wrong"

Chapter 3
New and inherited anomalies

The following anomalies are present in the nRF52832 chip.

Table 2: New and inherited anomalies

ID	Module	Description	Revision		
			Engineering A	Engineering B	Rev 1
8	SAADC	Increased current consumption in system ON-IDLE	X		
12	COMP	Reference ladder is not correctly calibrated	X	X	X
15	POWER	RAM[x].POWERSET/CLR read as zero	X	X	X
16	System	RAM may be corrupt on wakeup from CPU IDLE	X		
20	RTC	Register values are invalid	X	X	X
30	TWIS	STOP Task and STOPPED Event are not functional	X	X	X
31	CLOCK	Calibration values are not correctly loaded from FICR at reset	X	X	X
36	CLOCK	Some registers are not reset when expected	X	X	X
51	I2S	Aligned stereo slave mode does not work		X	X
53	CPU	Using SCB.AIRCR.VECTRESET may get the chip into an undefined state		X	X
54	I2S	Wrong LRCK polarity in Aligned mode		X	X
55	I2S	RXPTRUPD and TXPTRUPD events asserted after STOP		X	X
58	SPIM	SPIM clocks out an additional byte when RXD.MAXCNT = 1	X	X	X
62	NFCT	Can draw current when not enabled		X	
63	POWER	DC/DC does not automatically switch off in System ON IDLE	X	X	
64	NFCT	Only full bytes can be received or transmitted	X	X	X
65	POWER	RAM[] registers mapping of RAM block and sections is wrong	X		

3.1 [8] SAADC: Increased current consumption in system ON-IDLE

This anomaly applies to IC rev. Engineering A (QFAA-AA0, QFAA-AC0, CGAA-AA0).

3.1 Symptoms

Increased current when SAADC is enabled but not sampling.

3.1 Conditions

SAADC enabled with TACQ < = 10µs.

3.1 Consequences

Increased current consumption.

3.1 Workaround

Disable SAADC when not in use or use SAADC with TACQ > 10µs.

3.2 [12] COMP: Reference ladder is not correctly calibrated

This anomaly applies to IC rev. Engineering A (QFAA-AA0, QFAA-AC0, CGAA-AA0), IC rev. Engineering B (QFAA-BA0, QFAA-BB0, CHAA-AA0, CHAA-AB0), IC rev. Rev 1 (QFAA-B00, CHAA-A00).

3.2 Symptoms

COMP does not compare correctly.

3.2 Conditions

Always.

3.2 Consequences

COMP module is unusable.

3.2 Workaround

Execute the following code before enabling the COMP module:

```
*(volatile uint32_t *)0x40013540 = (*(volatile uint32_t *)0x10000324 &
 0x00001F00) >> 8;
```

3.3 [15] POWER: RAM[x].POWERSET/CLR read as zero

This anomaly applies to IC rev. Engineering A (QFAA-AA0, QFAA-AC0, CGAA-AA0), IC rev. Engineering B (QFAA-BA0, QFAA-BB0, CHAA-AA0, CHAA-AB0), IC rev. Rev 1 (QFAA-B00, CHAA-A00).

3.3 Symptoms

RAM[x].POWERSET and RAM[x].POWERCLR read as zero, even though the RAM is on.

3.3 Conditions

Always

3.3 Consequences

Not possible to read the RAM state using RAM[x].POWERSET and RAM[x].POWERCLR registers. Write works as it should.

3.3 Workaround

Use RAM[x].POWER to read the state of the RAM.

3.4 [16] System: RAM may be corrupt on wakeup from CPU IDLE

This anomaly applies to IC rev. Engineering A (QFAA-AA0, QFAA-AC0, CGAA-AA0).

3.4 Symptoms

On an event or interrupt where the CPU wakes up from IDLE state:

- The device hardfaults.
- Shows some unpredicted behavior consistent with RAM corruption.

3.4 Conditions

Always.

3.4 Consequences

Unpredicted behavior of the device.

3.4 Workaround

RAM blocks must be prevented from going to a low power state when the CPU goes to IDLE state (by executing the WFE or WFI instructions). Executing the following code before CPU sleep will ensure this:

```
*(uint32_t *)0x4007C074 = 3131961357;
```

The workaround should be applied after any kind of reset, so it would be ideal to add this code in the system startup code.

This configuration will also prevent RAM from going to low power (retention) state in system OFF and cause higher current consumption than documented in this mode. The following code can be executed before triggering the SYSTEMOFF.Enter to allow the RAM to go into retention state.

```
*(uint32_t *)0x4007C074 = 2976579765;
```

3.5 [20] RTC: Register values are invalid

This anomaly applies to IC rev. Engineering A (QFAA-AA0, QFAA-AC0, CGAA-AA0), IC rev. Engineering B (QFAA-BA0, QFAA-BB0, CHAA-AA0, CHAA-AB0), IC rev. Rev 1 (QFAA-B00, CHAA-A00).

3.5 Symptoms

RTC registers will not contain the correct/expected value if read.

3.5 Conditions

The RTC has been idle.

3.5 Consequences

RTC configuration cannot be determined by reading RTC registers.

3.5 Workaround

Execute the below code before you use RTC.

```
NRF_CLOCK->EVENTS_LFCLKSTARTED  = 0;
NRF_CLOCK->TASKS_LFCLKSTART     = 1;
while (NRF_CLOCK->EVENTS_LFCLKSTARTED == 0) {}
NRF_RTC0->TASKS_STOP = 0;
```

3.6 [30] TWIS: STOP Task and STOPPED Event are not functional

This anomaly applies to IC rev. Engineering A (QFAA-AA0, QFAA-AC0, CGAA-AA0), IC rev. Engineering B (QFAA-BA0, QFAA-BB0, CHAA-AA0, CHAA-AB0), IC rev. Rev 1 (QFAA-B00, CHAA-A00).

3.6 Symptoms

In TX (READ command), SCL and SDA are pulled low and further communication is blocked. In RX (WRITE command), ERRORSRC shows 0x3.

3.6 Conditions

Always.

3.6 Consequences

It is not possible to use the TWIS STOP task for terminating ongoing transactions.

3.6 Workaround

Terminate ongoing transactions by disabling the TWIS, wait at least 1 µs for any ongoing transaction to complete, and then enable the TWIS.

3.7 [31] CLOCK: Calibration values are not correctly loaded from FICR at reset

This anomaly applies to IC rev. Engineering A (QFAA-AA0, QFAA-AC0, CGAA-AA0), IC rev. Engineering B (QFAA-BA0, QFAA-BB0, CHAA-AA0, CHAA-AB0), IC rev. Rev 1 (QFAA-B00, CHAA-A00).

3.7 Symptoms

RCOSC32KICALLENGTH is initialized with the wrong FICR value.

3.7 Conditions

Always

3.7 Consequences

RCOSC32KICALLENGTH default value is wrong.

3.7 Workaround

Execute the following code after reset:

```
*(volatile uint32_t *)0x4000053C = ((*(volatile uint32_t *)0x10000244) &
0x0000E000) >> 13;
```

This code is already present in the latest system_nrf52.c file.

3.8 [36] CLOCK: Some registers are not reset when expected

This anomaly applies to IC rev. Engineering A (QFAA-AA0, QFAA-AC0, CGAA-AA0), IC rev. Engineering B (QFAA-BA0, QFAA-BB0, CHAA-AA0, CHAA-AB0), IC rev. Rev 1 (QFAA-B00, CHAA-A00).

3.8 Symptoms

After watchdog timeout reset, CPU lockup reset, soft reset, or pin reset, the following CLOCK peripheral registers are not reset: CLOCK->EVENTS_DONE, CLOCK->EVENTS_CTTO, CLOCK->CTIV

3.8 Conditions

After watchdog timeout reset, CPU Lockup reset, soft reset, and pin reset.

3.8 Consequences

Register reset values might be incorrect. It may cause undesired interrupts in case of enabling interrupts without clearing the DONE or CTTO events.

3.8 Workaround

Clear affected registers after reset. This workaround has already been added into system_nrf52.c file.

3.9 [51] I2S: Aligned stereo slave mode does not work

This anomaly applies to IC rev. Engineering B (QFAA-BA0, QFAA-BB0, CHAA-AA0, CHAA-AB0), IC rev. Rev 1 (QFAA-B00, CHAA-A00).

3.9 Symptoms

Sample values for the left channel are transmitted twice (for both channels within a frame), sample values for the right channel are lost.

3.9 Conditions

CONFIG.MODE = SLAVE, CONFIG.CHANNELS = STEREO, CONFIG.FORMAT = ALIGNED.

3.9 Consequences

Aligned format cannot be used for stereo transmission in Slave mode.

3.9 Workaround

None.

3.10 [53] CPU: Using SCB.AIRCR.VECTRESET may get the chip into an undefined state

This anomaly applies to IC rev. Engineering B (QFAA-BA0, QFAA-BB0, CHAA-AA0, CHAA-AB0), IC rev. Rev 1 (QFAA-B00, CHAA-A00).

3.10 Symptoms

Undefined behavior.

3.10 Conditions

SCB.AIRCR.VECTRESET is set to 1

3.10 Consequences

Unknown

3.10 Workaround

Do not use SCB.AIRCR.VECTRESET

3.11 [54] I2S: Wrong LRCK polarity in Aligned mode

This anomaly applies to IC rev. Engineering B (QFAA-BA0, QFAA-BB0, CHAA-AA0, CHAA-AB0), IC rev. Rev 1 (QFAA-B00, CHAA-A00).

3.11 Symptoms

In Aligned mode, left and right samples are swapped.

3.11 Conditions

CONFIG.FORMAT = ALIGNED

3.11 Consequences

Left and right audio channels are swapped.

3.11 Workaround

Swap left and right samples in memory.

3.12 [55] I2S: RXPTRUPD and TXPTRUPD events asserted after STOP

This anomaly applies to IC rev. Engineering B (QFAA-BA0, QFAA-BB0, CHAA-AA0, CHAA-AB0), IC rev. Rev 1 (QFAA-B00, CHAA-A00).

3.12 Symptoms

The RXPTRUPD event is generated when the STOP task is triggered, even though reception (RX) is disabled. Similarly, the TXPTRUPD event is generated when the STOP task is triggered, even though transmission (TX) is disabled.

3.12 Conditions

A previous transfer has been performed with RX/TX enabled, respectively.

3.12 Consequences

The indication that RXTXD.MAXCNT words were received/transmitted is false.

3.12 Workaround

Ignore the RXPTRUPD and TXPTRUPD events after triggering the STOP task. Clear these events before starting the next transfer.

3.13 [58] SPIM: SPIM clocks out an additional byte when RXD.MAXCNT = 1

This anomaly applies to IC rev. Engineering A (QFAA-AA0, QFAA-AC0), IC rev. Engineering B (QFAA-BA0, QFAA-BB0, CHAA-AA0, CHAA-AB0), IC rev. Rev 1 (QFAA-B00, CHAA-A00).

3.13 Symptoms

SPIM clocks out additional byte.

3.13 Conditions

RXD.MAXCNT = 1 TXD.MAXCNT <= 1

3.13 Consequences

Additional byte is redundant.

3.13 Workaround

Use the SPI module (deprecated but still available) or use the following workaround with SPIM:

```
/**
 * @brief Work-around for transmitting 1 byte with SPIM.
 *
 * @param spim: The SPIM instance that is in use.
 * @param ppi_channel: An unused PPI channel that will be used by the
 workaround.
 * @param gpiote_channel: An unused GPIOTE channel that will be used by
 the workaround.
 *
 * @warning Must not be used when transmitting multiple bytes.
 * @warning After this workaround is used, the user must reset the PPI
 channel and the GPIOTE channel before attempting to transmit multiple
 bytes.
 */
void setup_workaround_for_ftpan_58(NRF_SPIM_Type * spim, uint32_t
 ppi_channel, uint32_t gpiote_channel)
{
    // Create an event when SCK toggles.
    NRF_GPIOTE->CONFIG[gpiote_channel] = (
        GPIOTE_CONFIG_MODE_Event <<
        GPIOTE_CONFIG_MODE_Pos
        ) | (
        spim->PSEL.SCK <<
        GPIOTE_CONFIG_PSEL_Pos
        ) | (
        GPIOTE_CONFIG_POLARITY_Toggle <<
        GPIOTE_CONFIG_POLARITY_Pos
        );

    // Stop the spim instance when SCK toggles.
    NRF_PPI->CH[ppi_channel].EEP = (uint32_t)&NRF_GPIOTE-
>EVENTS_IN[gpiote_channel];
    NRF_PPI->CH[ppi_channel].TEP = (uint32_t)&spim->TASKS_STOP;
    NRF_PPI->CHENSET = 1U << ppi_channel;
```

```
    // The spim instance cannot be stopped mid-byte, so it will finish
    // transmitting the first byte and then stop. Effectively ensuring
    // that only 1 byte is transmitted.
}
```

3.14 [62] NFCT: Can draw current when not enabled

This anomaly applies to IC rev. Engineering B (QFAA-BA0, CHAA-AA0).

3.14 Symptoms

Increased current consumption (>10µA) in System OFF and System ON IDLE.

3.14 Conditions

NFCT is not enabled and supply voltage is above 2.5V.

3.14 Consequences

Current consumption in low power modes can be higher than specified.

3.14 Workaround

None

3.15 [63] POWER: DC/DC does not automatically switch off in System ON IDLE

This anomaly applies to IC rev. Engineering A (QFAA-AA0, QFAA-AC0, CGAA-AA0), IC rev. Engineering B (QFAA-BA0, CHAA-AA0).

3.15 Symptoms

The device will draw current periodically (in the mA range) when in System ON IDLE.

3.15 Conditions

DC/DC is enabled and in System ON IDLE.

3.15 Consequences

Average current consumption in idle mode is too high.

3.15 Workaround

None

3.16 [64] NFCT: Only full bytes can be received or transmitted

This anomaly applies to IC rev. Engineering A (QFAA-AA0, QFAA-AC0, CGAA-AA0), IC rev. Engineering B (QFAA-BA0, QFAA-BB0, CHAA-AA0, CHAA-AB0), IC rev. Rev 1 (QFAA-B00, CHAA-A00).

3.16 Symptoms

Data bits are not transmitted, or appear to not be received, if the Frame length is not a multiple of 8 bits (i.e. Frame includes data bits).

3.16 Conditions

Frame length is not a multiple of 8 bits (bytes only).

3.16 Consequences

Partial bytes cannot be transferred:

- TXD.AMOUNT.TXDATABITS must be 0
- RXD.AMOUNT.RXDATABITS must be 0

3.16 Workaround

None

3.17 [65] POWER: RAM[] registers mapping of RAM block and sections is wrong

This anomaly applies to IC rev. Engineering A (QFAA-AA0, QFAA-AC0, CGAA-AA0).

3.17 Symptoms

Using RAM[] registers to switch RAM retention on or off doesn't work as expected.

3.17 Conditions

Always.

3.17 Consequences

It is difficult to adjust the RAM retention to reduce power consumption.

3.17 Workaround

The easiest way to avoid problems is to switch on all RAM retention in all conditions, and do not micromanage the power consumption of the different RAM blocks and sections. The following code can be used:

```
NRF_POWER->RAM[0].POWER = 0xFFFFFFFF;
NRF_POWER->RAM[1].POWER = 0xFFFFFFFF;
NRF_POWER->RAM[2].POWER = 0xFFFFFFFF;
NRF_POWER->RAM[3].POWER = 0xFFFFFFFF;
NRF_POWER->RAM[4].POWER = 0xFFFFFFFF;
NRF_POWER->RAM[5].POWER = 0xFFFFFFFF;
NRF_POWER->RAM[6].POWER = 0xFFFFFFFF;
NRF_POWER->RAM[7].POWER = 0xFFFFFFFF;
```

Chapter 4
Fixed anomalies

The anomalies listed in this table are no longer present in the current chip versions.

For a detailed description of the fixed anomalies, see the previous version of the Errata.

Table 3: Fixed anomalies

ID	Module	Description
1	I2S	I2S not functional
2	PWM	PWM not functional
3	PDM	PDM not functional
4	MWU	MWU not functional
7	NVMC,System	Cache is not functional
9	QDEC	Some features are not functional
10	RTC	RTC2 is not functional
11	System	Device is unable to stay in System-Off mode
17	NFCT	The EVENTS_FIELDLOST is not generated
23	SPIM	END event is generated before ENDTX
24	NFCT	The FIELDPRESENT register read is not reliable
25	NFCT	Reset value of SENSRES register is incorrect
26	NFCT	NFC field does not wakeup the device from emulated system OFF
27	NFCT	Triggering NFCT ACTIVATE task also activates the Rx easyDMA
28	SAADC	Scan mode is not functional for some analog inputs
29	TWIS	Incorrect bits in ERRORSRC
32	DIF	Debug session automatically enables TracePort pins
33	System	Code RAM is located at wrong address
34	System	Code and Data RAM are not mapped from the same physical RAM
35	CLOCK	HFCLK can draw current when not requested
37	RADIO	Encryption engine is slow by default.
38	PPI	Enable/disable tasks for channel group 4 and 5 cannot be triggered through PPI
39	NFCT	The automatic collision resolution does not handle CRC and parity errors
40	NFCT	The FRAMEDELAYMODE = WindowGrid is not supported
41	GPIO	PIN_CNF[x] registers not reset after pin reset
42	PPI	FORK on the fixed channels is not functional

ID	Module	Description
43	SPIS	SPIS0 is not functional
44	NVMC	Read after flash erase is unpredictable
46	SPIM,TWIM	EasyDMA list not functional
47	DIF	Trace is not functional
48	DIF	SWO only works if Trace is enabled.
49	RTC	RTC is not functional after LFCLK is restarted
57	NFCT	NFC Modulation amplitude