

nRF51824

Product Anomaly Notice v1.0

This Product Anomaly Notice contains anomalies for the following package variants and builds of the nRF51824 chip:

Package and Variant	Build code
QFAA	A00

Table 1 Package, Variants, and Build codes covered in this document

Authorization for Nordic Semiconductor

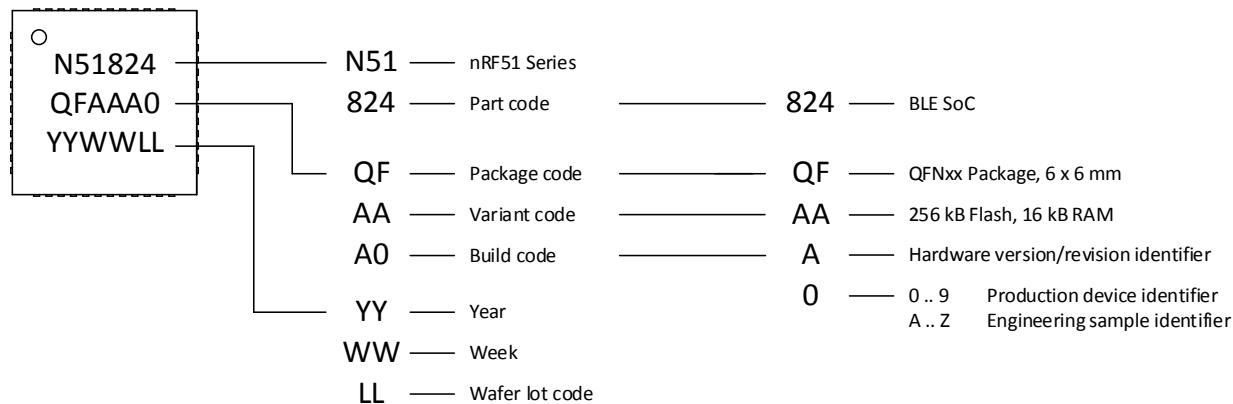
Product Manager: Date: Signed:
Thomas Embla Bonnerud 2016-09-29



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1. Chip Marking



2. Change log

Version	Date	Change
nRF51824-PAN v1.0	2016-09-29	First release.

3. Overview

3.1 New and inherited anomalies

PAN ID	Module	Description	QFAA	New/ Inherited ¹
75.	LFCLK	RC oscillator is not calibrated when first started.	X	New
70.	LPCOMP	READY event is sent before LPCOMP is ready.	X	New
71.	MPU	The register MPU.RLENR0 will not give runtime protection of RAM locations above 8 kB.	X	New
69.	MPU	MPU Protect All (PALL) does not protect RAM above 8 kB from debugger access.	X	New
61.	RADIO	Designs based on nRF51822 QFN packets using balun BAL-NRF01D3 are likely to fail Korean teleregulatory requirements.	X	New
72.	RTC	Writing to RTC registers without starting the LFCLK could lead to increased current consumption.	X	New
74.	SPIS	ORC character is not clocked out on MISO when MAXTX = 0.	X	New
67.	SYSTEM	Emulated system OFF mode makes POWER.RESET register inaccessible.	X	New
73.	TIMER	Use of an EVENT from any TIMER module to trigger a TASK in GPIOTE or RTC using the PPI could fail under certain conditions.	X	New
38.	WDT	The watchdog config option "RUN while paused by the debugger" does not work.	X	New

¹ 'New' is anomalies introduced in the current chip version listed in **Table 1**, while 'Inherited' is anomalies already present in the previous chip version.

4. New and inherited anomalies

75. LFCLK: RC oscillator is not calibrated when first started.

Symptoms:

Timings measured using the LFCLK RC oscillator are off.

Conditions:

The LFCLK RC oscillator has not been calibrated after the last reset.

Consequences:

The LFCLK RC oscillator frequency can show -25% to +40 % offset.

Workaround:

Calibrate the LFCLK RC oscillator before its first use after reset.

70. LPCOMP: READY event is sent before LPCOMP is ready.

Symptoms:

May receive unexpected events and wakeups from LPCOMP.

Conditions:

LPCOMP is configured to send an event or to wake up the chip. LPCOMP.TASKS_START task is set and LPCOMP.EVENTS_READY event has been received.

Consequences:

Unpredictable system behavior caused by false triggered events and wakeups.

Workaround:

Use the following configuration sequence:

1. Configure the LPCOMP to send an event or wake up the chip, but do not enable any PPI channels or IRQ to be triggered from the LPCOMP events.
2. Trigger the LPCOMP.TASKS_START task and wait for the LPCOMP.EVENTS_READY event.
3. After receiving the LPCOMP.EVENTS_READY event wait for 36 µs.
4. After 36 µs, clear the LPCOMP.EVENTS_DOWN, LPCOMP.EVENTS_UP and LPCOMP.EVENTS_CROSS events.

LPCOMP is now ready to be used.

71. MPU: The register MPU.RLENR0 will not give runtime protection of RAM locations above 8 kB.**Symptoms:**

Code running from region 1 accessing RAM in region 0 that is located above the first 8 kB does not give a hard fault exception as specified in the nRF51 Series Reference manual.

Conditions:

Always when the RAM is divided into two regions.

Consequences:

Missing runtime protection of addresses above 8 kB will make it harder to detect unintended write operations to RAM region 0 from code region 1.

Such unintended write operations could lead to malfunction of the firmware.

Workaround:

None. (Debugging of the code could be done using the xxAC version of nRF51822/nRF51422 where this PAN is fixed).

69. MPU: MPU Protect All (PALL) does not protect RAM above 8 kB from debugger access.**Symptoms:**

Reading RAM using Serial Wire Debug (SWD) returns the actual RAM content, and not 0x00 as specified in the nRF51 Series Reference manual.

Conditions:

Always when UICR.RBPCONF.PALL is set to 0x00.

Consequences:

RAM addresses above 8 kB will be accessible using the SWD interface.

Workaround:

None.

61. RADIO: Designs based on nRF51822 QFN packets using balun BAL-NRF01D3 are likely to fail Korean teleregulatory requirements.**Symptoms:**

LO leakage is too high.

Conditions:

Designs based on the QFN packets nRF51822-QFAA/nRF51822-QFAB combined with ST Microelectronics balun, BAL-NRF01D3 (as described in the reference layout nRF51822-DF-ST v1.0).

Consequences:

The designs are likely to fail Korean teleregulatory spurious emission limits due to LO leakage.

Workaround:

There are several alternative baluns to BAL-NRF01D3, please refer to www.nordicsemi.com for details.

72. RTC: Writing to RTC registers without starting the LFCLK could lead to increased current consumption.**Symptoms:**

Increased current consumption.

Conditions:

Setting up the RTC by writing to its registers without starting the LFCLK.

Consequences:

The user will experience an increase in the current consumption of ~1 mA.

Workaround:

Always run the LFCLK for a minimum of one LFCLK clock cycle after writing to the RTC registers.

74. SPIS: ORC character is not clocked out on MISO when MAXTX = 0.**Symptoms:**

The SPIS does not send the ORC character as expected.

Conditions:

SPIS is configured with MAXTX = 0.

Consequences:

Data sent on the MISO line is not the ORC character but the data pointed to by the TXDPTR.

Workaround:

In the case where the SPI slave does not have any data to be sent (MAXTX = 0). Set MAXTX = 1, with the first byte in the TX buffer set equal to the ORC character.

67. System: Emulated system OFF mode makes POWER.RESET register inaccessible.**Symptoms:**

Pin reset using the debugger does not work.

Conditions:

Device is in emulated System OFF mode.

Consequences:

Pin reset using the debugger does not work.

Workaround:

Before pin reset, halt the core and generate a soft reset. This will take the device out of Emulated System Off, making the POWER.RESET register accessible.

Note: Latest Nordic Semiconductor tools already perform this action automatically.

73. TIMER: Use of an EVENT from any TIMER module to trigger a TASK in GPIOTE or RTC using the PPI could fail under certain conditions.**Symptoms:**

One or more EVENTS from the TIMER module are lost.

Conditions:

Routing TASK's from the TIMERx module to GPIOTE or RTCx using the PPI and at the same time going into sleep mode.

Consequences:

One or more TASKS triggering are lost.

Workaround:

Use the following code when using any Timer in those conditions:

```
*(uint32_t *)0x40008C0C = 1; //for Timer 0
*(uint32_t *)0x40009C0C = 1; //for Timer 1
*(uint32_t *)0x4000AC0C = 1; //for Timer 2
```

When the conditions are no longer met, use the following code:

```
*(uint32_t *)0x40008C0C = 0; //for Timer 0
*(uint32_t *)0x40009C0C = 0; //for Timer 1
*(uint32_t *)0x4000AC0C = 0; //for Timer 2
```

A typical code workaround for an application that use TIMER2 to route TASKS to a GPIOTE can be:

```
/* Add workaround when starting timer2 */
*(uint32_t *)0x4000AC0C = 1; //for Timer 2
NRF_TIMER2->TASKS_START = 1;

/* Add workaround when stopping timer2 */
NRF_TIMER2->TASKS_STOP = 1;
*(uint32_t *)0x4000AC0C = 0; //for Timer 2
```

38. WDT: The watchdog config option "RUN while paused by the debugger" does not work.**Symptoms:**

The debugger and microcontroller do not communicate. The microcontroller does not run any code.

Conditions:

The watchdog is configured to "run while halted by the debugger", and the watchdog timer expires with the debugger connected.

Consequences:

The debugger and microcontroller do not communicate. The microcontroller does not run any code.

Workaround:

Do not configure the watchdog timer to run while paused by the debugger.